FS26

Safety System Basis Chip with low power for ASIL D/ASIL B

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Product data sheet

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Document information

Information	Content
Keywords	Safety, SBC, automotive, low power, ASIL B, ASIL D
Abstract	Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series.

1 General description

Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series. FS26 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS26 applications include power train, chassis, safety, and low-end gateway technology.

This family of devices consists of several versions that are pin-to-pin and software compatible. These versions support a wide range of applications with Automotive Safety Integrity Levels (ASIL) B or D, offering choices in number of output rails, output voltage settings, operating frequencies, power-up sequencing, and integrated system-level features.

The FS26 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. It offers a high-precision reference voltage supply for the system, and for two independent tracking regulators. The FS26 also offers various functionalities for system control and diagnostics, including an analog multiplexer, general-purpose input/outputs (GPIOs), and selectable wake-up events from I/O, long duration timer, or serial peripheral interface (SPI) communication.

The FS26 is developed in compliance with the ISO 26262 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on-demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.

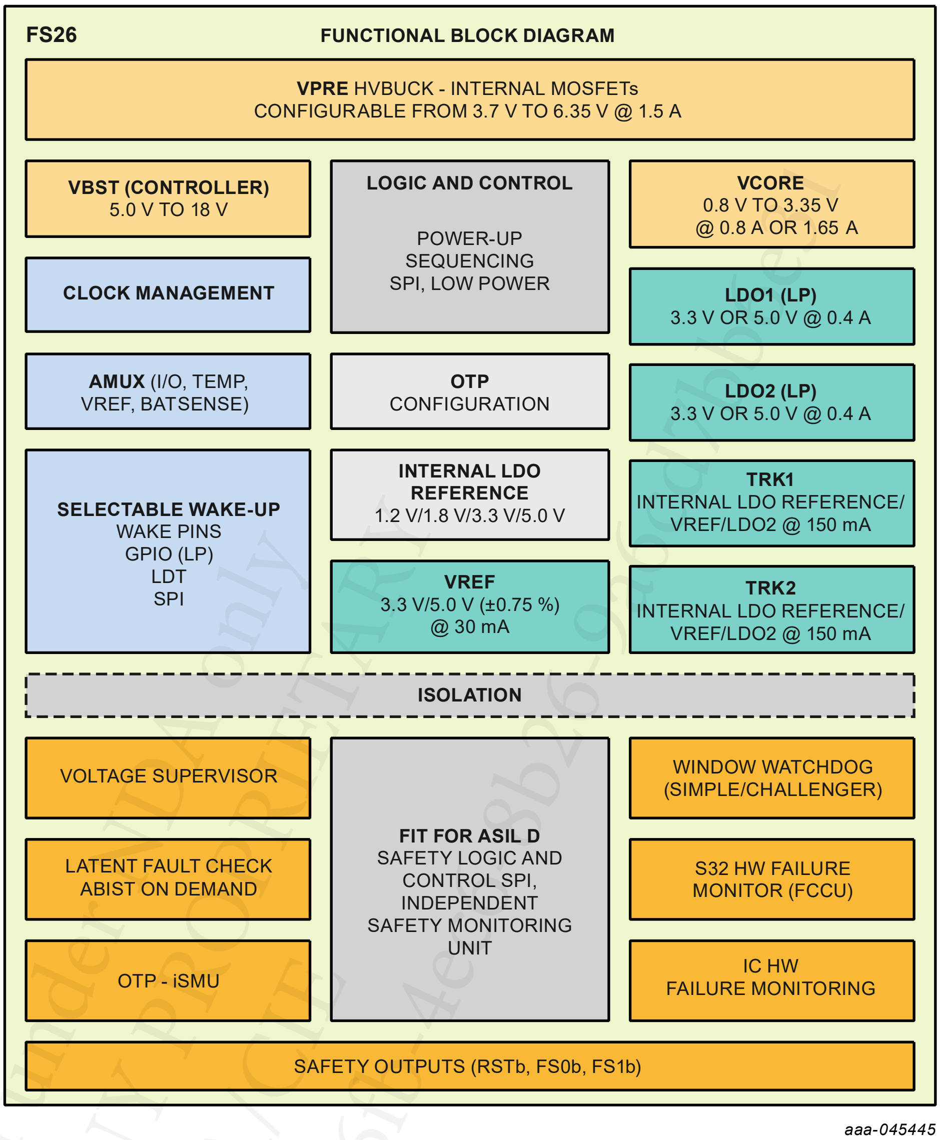
FS26
FUNCTIONAL BLOCK DIAGRAM
VPRE HVBUCK - INTERNAL MOSFETs
CONFIGURABLE FROM 3.7 V TO 6.35 V @ 1.5 A
VBST (CONTROLLER)
5.0 V TO 18 V
LOGIC AND CONTROL
POWER-UP
SEQUENCING
SPI, LOW POWER
VCORE
0.8 V TO 3.35 V
@ 0.8 A OR 1.65 A
CLOCK MANAGEMENT
LDO1 (LP)
3.3 V OR 5.0 V @ 0.4 A
AMUX (I/O, TEMP,
VREF, BATSENSE)
OTP
CONFIGURATION
LDO2 (LP)
3.3 V OR 5.0 V @ 0.4 A
SELECTABLE WAKE-UP
WAKE PINS
GPIO (LP)
LDT
SPI
INTERNAL LDO
REFERENCE
1.2 V/1.8 V/3.3 V/5.0 V
TRK1
INTERNAL LDO REFERENCE/
VREF/LDO2 @ 150 mA
VREF
3.3 V/5.0 V (±0.75 %)
@ 30 mA
TRK2
INTERNAL LDO REFERENCE/
VREF/LDO2 @ 150 mA
ISOLATION
VOLTAGE SUPERVISOR
FIT FOR ASIL D
SAFETY LOGIC AND
CONTROL SPI,
INDEPENDENT
SAFETY MONITORING
UNIT
WINDOW WATCHDOG
(SIMPLE/CHALLENGER)
LATENT FAULT CHECK
ABIST ON DEMAND
S32 HW FAILURE
MONITOR (FCCU)
OTP - iSMU
IC HW
FAILURE MONITORING
SAFETY OUTPUTS (RSTb, FS0b, FS1b)
aaa-045445

Figure 1. Functional block diagram

2 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Support operating voltage range down to battery 3.2 V with VBST
- Support operating voltage range down to battery 6 V without VBST
- Low Power OFF mode with 30 µA quiescent current
- Low Power Standby mode with 25 µA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI communication.

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for Low Power Standby mode operation.
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V.
- VBST: Asynchronous boost controller with external low-side switch, diode, and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: High-precision reference voltage with 0.75 % accuracy for External ADC reference and internal tracking reference.
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Support high-voltage protection for ECU off board operation. Each Tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIO with wake-up capability or HS/LS driver
- Programmable long duration timer (LDT) for system shutdown and wake-up control
- Monitoring of system voltages (Including Battery voltage monitoring) through the analog multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI activity
- Device control via 32-bit SPI interface with cyclic redundancy checks (CRC)

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards.

Functional safety

- Scalable portfolio from Automotive Safety Integrity Levels (ASIL) B to D

- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple or challenger watchdog function
- Analog built-in self-test (ABIST) and Logical Built-In Self-Test (LBIST) at start up
- Analog built-in self-test (ABIST) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP Emulation mode for hardware development and evaluation
- Debug mode for software development, MCU programming, and debugging

3 Simplified application diagram

Figure 2 shows a simplified block diagram for a typical system with an FS26, using the boost controller to support battery cold-crank events.

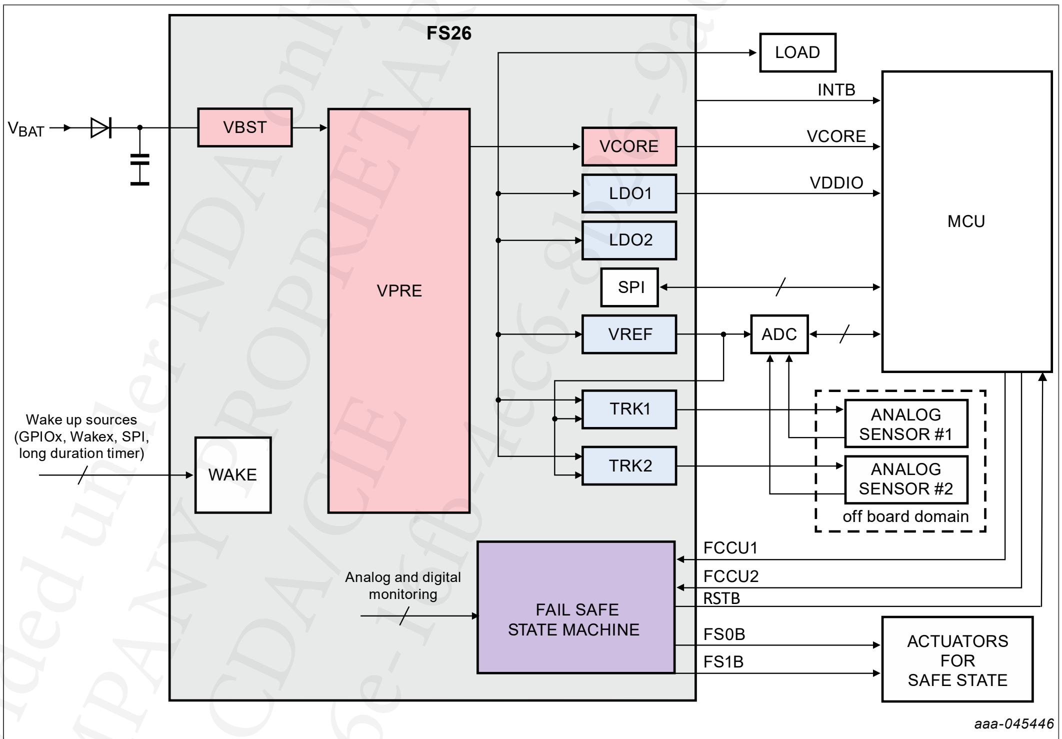

Figure 2. Example of application diagram (with VBST as a front-end regulator)

Figure 3 shows a simplified block diagram for a typical system with an FS26, using the boost controller to generate a voltage above the high-voltage buck output voltage.

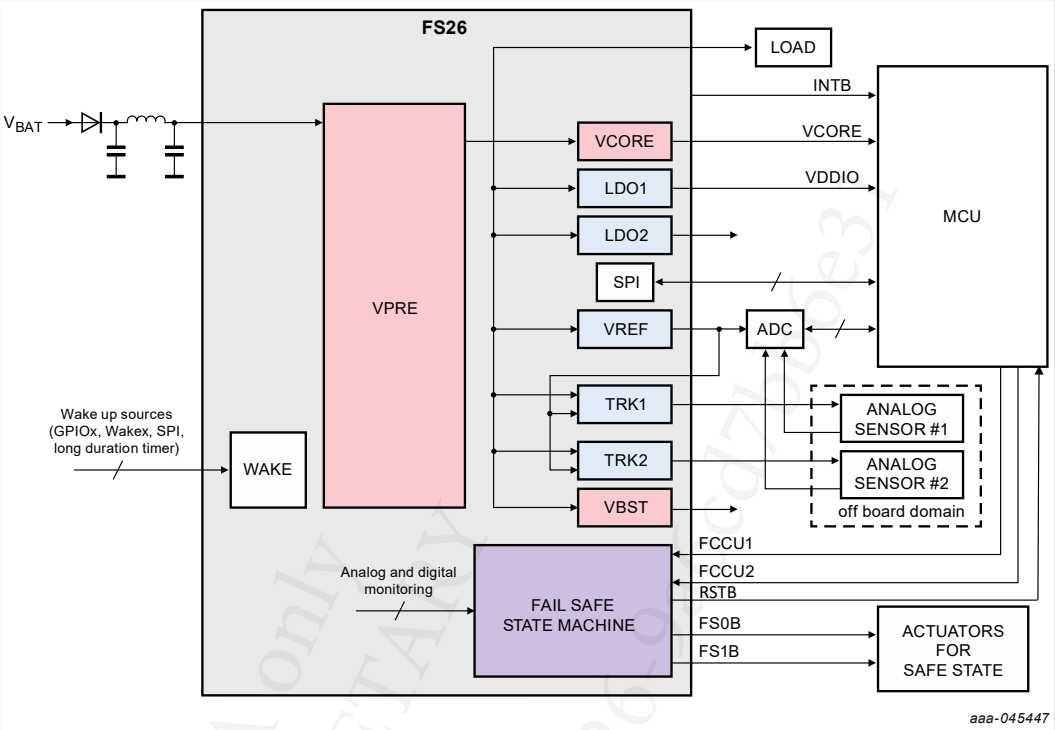

Figure 3. Example of application diagram (with VBST as a back-end regulator)

4 Ordering information

This section describes the part numbers available for purchase, with their main differences. It also depicts how the part number reference is built.

4.1 Part number definition

Figure 4 shows how the FS26xyz part number is used to describe the available feature set of each device.

FS26xx
Product Numbering Scheme

P	FS	26 X Y	A	M	Zzz	AD
Release Type	Family	Product Core	Release Version	Temperature	Funct. or Param. variant	Package
M Production	FS High Voltage Power Management	2600-2633 Core	A Initial Release	M -40 to 125 °C	A0 No OTP	AD LQFP48
P Pre-release			B-Z as required		A1-ZZ Unique part identification	
S Customer special						

FS 2 6 X Y Z

Z	ASIL
B	Fit for ASIL B (Simple W/D, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

Y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b and LDT

X	PMIC Solution
0	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
1	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers
2	Vcore 1.65 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
3	Vcore 1.65 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers

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Figure 4. Part number breakdown

Figure 5 maps FS26 part numbers vs. product feature sets.

Vcore	0.8 A core				1.65 A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D

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Figure 5. Part number mapping versus features set

4.2 Part number list

Table 1. Device segmentation

Part Number	DEV_ID[5:0]	Tracker 2	Core Current Capability	Long Duration Timer	Tracker 2 Monitoring	FS1B	ABIST on demand	Watchdog Type	Fault Recovery	FCCU Monitoring	LBIST
FS2600B	0x01	NO	0.8 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2601B	0x02	NO	0.8 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2602B	0x03	NO	0.8 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2603B	0x04	NO	0.8 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2600D	0x05	NO	0.8 A	NO	NO	NO	YES	Challenger	YES	YES	YES

Table 1. Device segmentation...*continued*

Part Number	DEV_ID[5:0]	Tracker 2	Core Current Capability	Long Duration Timer	Tracker 2 Monitoring	FS1B	ABIST on demand	Watchdog Type	Fault Recovery	FCCU Monitoring	LBIST
FS2601D	0x06	NO	0.8 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2602D	0x07	NO	0.8 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2603D	0x08	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2610B	0x09	YES	0.8 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2611B	0x0A	YES	0.8 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2612B	0x0B	YES	0.8 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2613B	0x0C	YES	0.8 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2610D	0x0D	YES	0.8 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2611D	0x0E	YES	0.8 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2612D	0x0F	YES	0.8 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2613D	0x10	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
FS2620B	0x11	NO	1.65 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2621B	0x12	NO	1.65 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2622B	0x13	NO	1.65 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2623B	0x14	NO	1.65 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2620D	0x15	NO	1.65 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2621D	0x16	NO	1.65 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2622D	0x17	NO	1.65 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2623D	0x18	NO	1.65 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2630B	0x19	YES	1.65 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2631B	0x1A	YES	1.65 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2632B	0x1B	YES	1.65 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2633B	0x1C	YES	1.65 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2630D	0x1D	YES	1.65 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2631D	0x1E	YES	1.65 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2632D	0x1F	YES	1.65 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2633D	0x20	YES	1.65 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Additional part numbers will exist with different features and parametric settings. Table 1 is an example of a part number list.

Table 2. Orderable part numbers

Part number	Description	Package
MFS2613AMDA2AD	S32K344+ FS26 EVB ASIL D S32K3X4EVB-x257	
MFS2613AMDA3AD	S32K344 HVBMS Reference design	
MFS2613AMDA4AD	S32K344 Body Control Module Reference design (white board)	
MFS2613AMDA6AD	S32K344 48 V MC Development platform	
MFS2621AMDABAD	Aurix TC38, TC29	**LQPF48**
MFS2613AMDDCAD	S32K324 5G T-BOX + Gateway	
MFS2600AMBA0AD	Superset covering FS2600B devices	
MFS2600AMDA0AD	Superset covering FS2600D devices	
MFS2601AMBA0AD	Superset covering FS2601B devices	

Table 2. Orderable part numbers*...continued*

Part number	Description	Package
MFS2601AMDA0AD	Superset covering FS2601D devices	
MFS2602AMBA0AD	Superset covering FS2602B devices	
MFS2602AMDA0AD	Superset covering FS2602D devices	
MFS2603AMBA0AD	Superset covering FS2603B devices	
MFS2603AMDA0AD	Superset covering FS2603D devices	
MFS2610AMBA0AD	Superset covering FS2610B devices	
MFS2610AMDA0AD	Superset covering FS2610D devices	
MFS2611AMBA0AD	Superset covering FS2611B devices	
MFS2611AMDA0AD	Superset covering FS2611D devices	
MFS2612AMBA0AD	Superset covering FS2612B devices	
MFS2612AMDA0AD	Superset covering FS2612D devices	
MFS2613AMBA0AD	Superset covering FS2613B devices	
MFS2613AMDA0AD	Superset covering FS2613D devices	
MFS2620AMBA0AD	Superset covering FS2620B devices	
MFS2620AMDA0AD	Superset covering FS2620D devices	
MFS2621AMBA0AD	Superset covering FS2621B devices	
MFS2621AMDA0AD	Superset covering FS2621D devices	
MFS2622AMBA0AD	Superset covering FS2622B devices	
MFS2622AMDA0AD	Superset covering FS2622D devices	
MFS2623AMBA0AD	Superset covering FS2623B devices	
MFS2623AMDA0AD	Superset covering FS2623D devices	
MFS2630AMDA0AD	Superset covering FS2630D devices	
MFS2630AMBA0AD	Superset covering FS2630B devices	
MFS2631AMBA0AD	Superset covering FS2631B devices	
MFS2631AMDA0AD	Superset covering FS2631D devices	
MFS2632AMBA0AD	Superset covering FS2632B devices	
MFS2632AMDA0AD	Superset covering FS2632D devices	
MFS2633AMBA0AD	Superset covering FS2633B devices	
MFS2633AMDA0AD	Superset covering FS2633D devices	

Empty OTP samples can be ordered for engineering purposes using part number **PFS2630AMDA0AD**. See Table 215 for the complete OTP content description.

5 Applications

xEV and powertrain market

- Inverter
- Onboard charger (OBC), DCDC
- Battery management system (BMS)
- Belt starter generator (BSG)

Body market

- Gateway
- Zonal control
- Body controller
- Smart junction box

Safety and chassis

- Suspension
- Power steering

MCU attach

- NXP S32K3 family
- Infineon AURIX family (TC2xx and TC3xx)
- Renesas RH850 family
- Cypress Traveo family

6 Block diagram

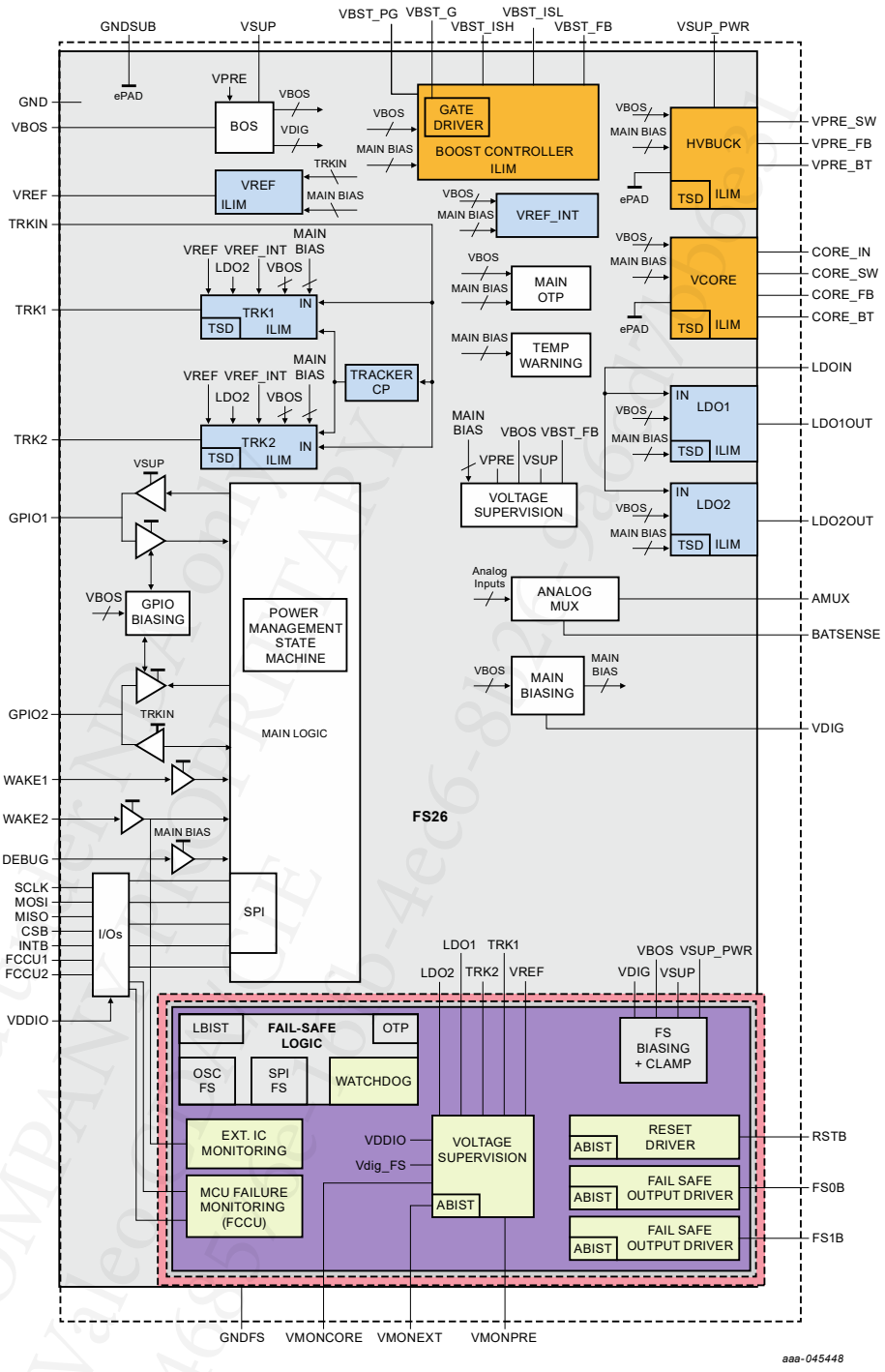


Figure 6. Block diagram of the FS26

7 Pinning information

7.1 Pinning

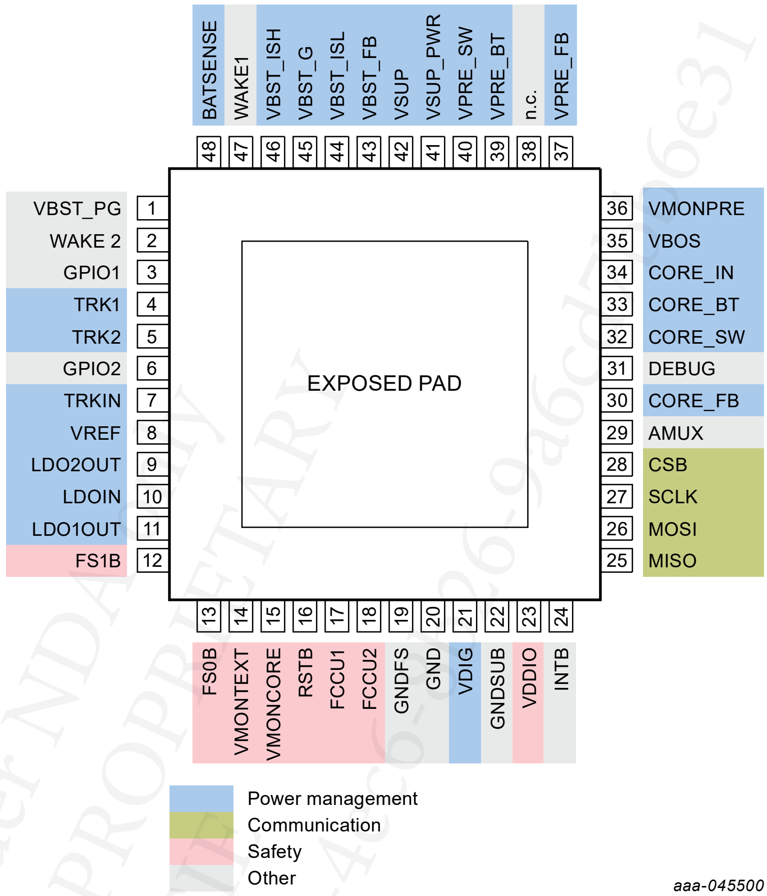

BATSENSE 48
WAKE1 47
VBST_ISH 46
VBST_G 45
VBST_ISL 44
VBST_FB 43
VSUP 42
VSUP_PWR 41
VPRE_SW 40
VPRE_BT 39
n.c. 38
VPRE_FB 37
VBST_PG 1
WAKE 2 2
GPIO1 3
TRK1 4
TRK2 5
GPIO2 6
TRKIN 7
VREF 8
LDO2OUT 9
LDOIN 10
LDO1OUT 11
FS1B 12
36 VMONPRE
35 VBOS
34 CORE_IN
33 CORE_BT
32 CORE_SW
31 DEBUG
30 CORE_FB
29 AMUX
28 CSB
27 SCLK
26 MOSI
25 MISO
EXPOSED PAD
13 FS0B
14 VMONTEXT
15 VMONCORE
16 RSTB
17 FCCU1
18 FCCU2
19 GNDFS
20 GND
21 VDIG
22 GNDSUB
23 VDDIO
24 INTB
Power management
Communication
Safety
Other
aaa-045500

Figure 7. Pin assignment in LQFP48 package with exposed pad

7.2 Pin descriptions

Table 3. Pin descriptions

Symbol	Pin Number	Type	Description
VBST_PG	1	Digital output	Power Good signal for boost controller
WAKE2	2	Analog input	WAKE2 input pin or ERROR monitoring input
GPIO1	3	Analog output / Digital Input	General Purpose I/O 1
TRK1	4	Analog output	TRK1 output
TRK2	5	Analog output	TRK2 output
GPIO2	6	Analog output / Digital Input	General Purpose I/O 2
TRKIN	7	Analog input	Tracker Input
VREF	8	Analog output	Voltage reference output
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO input voltage supply
LDO1OUT	11	Analog output	LDO1 output
FS1B	12	Digital output	Safety output #1

Table 3. Pin descriptions*...continued*

Symbol	Pin Number	Type	Description
FS0B	13	Digital output	Safety output #0
VMONEXT	14	Analog input	External voltage monitoring input
VMONCORE	15	Analog input	VCORE voltage monitoring input
RSTB	16	Digital input/output	Reset input/output
FCCU1	17	Digital input	Fault Control Collection Unit 1
FCCU2	18	Digital input	Fault Control Collection Unit 2
GNDFS	19	Ground connection	GND for fail-safe circuitry
GND	20	Ground connection	GND for main circuitry
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI Primary In Secondary out
MOSI	26	Digital input	SPI Primary Out Secondary input
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog Multiplexer output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best Of Supply decoupling output
VMONPRE	36	Analog input	VPRE monitoring pin
VPRE_FB	37	Analog input	VPRE feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to GND)

8 Connection of unused pins

Table 4. Connection of unused pins

Symbol	Pin Number	Type	Connection if not used
VBST_PG	1	Digital output	Grounded
WAKE2	2	Analog input	Open - Internal pulldown can be activated by OTP (with WK2PD_OTP = 1)
GPIO1	3	Analog output / Digital Input	Open - Internal pulldown can be activated by OTP (with IO1PD_OTP = 1)
TRK1	4	Analog output	Open - TRK1 to be configured OFF for power up sequence TRK1_SLOT_OTP[2:0] = 111
TRK2	5	Analog output	Open - TRK2 to be configured OFF for power up sequence TRK2_SLOT_OTP[2:0] = 111
GPIO2	6	Analog output / Digital Input	Open - Internal pulldown can be activated by OTP (with IO2PD_OTP = 1)
TRKIN	7	Analog input	**Connection mandatory** when using VREF, TRK1, TRK2, or GPIO2 as High-side driver. Otherwise Open when not used.
VREF	8	Analog output	Open
LDO2OUT	9	Analog output	Open - LDO2 to be configured OFF for power up sequence (with LDO2_SLOT_OTP[2:0] = 111)
LDOIN	10	Analog input	Open
LDO1OUT	11	Analog output	Open - LDO1 to be configured OFF for power up sequence (with LDO1_SLOT_OTP[2:0] = 111)
FS1B	12	Digital output	Open - 2 MΩ internal pulldown
FS0B	13	Digital output	Open - 2 MΩ internal pulldown
VMONEXT	14	Analog input	Open - VMONEXT to be disabled by OTP
VMONCORE	15	Analog input	Open
RSTB	16	Digital input/output	**Connection mandatory**
FCCU1	17	Digital input	Open - 800 kΩ internal pulldown
FCCU2	18	Digital input	Open - 200 kΩ internal pullup to VDDIO
GNDFS	19	Ground connection	**Connection mandatory**
GND	20	Ground connection	**Connection mandatory**
VDIG	21	Analog output	**Connection mandatory with external decoupling capacitor (normalized value 1 µF)**
GNDSUB	22	Ground connection	**Connection mandatory**
VDDIO	23	Analog input	**Connection mandatory**
INTB	24	Digital output	Open - 10 kΩ internal pullup to VDDIO
MISO	25	Digital output	Open - push pull structure
MOSI	26	Digital input	Open - 450 kΩ internal pullup to VDDIO
SCLK	27	Digital input	External pulldown to GND
CSB	28	Digital input	Open - 450 kΩ internal pullup to VDDIO
AMUX	29	Analog output	Open
CORE_FB	30	Analog input	Open
DEBUG	31	Digital input	**Connection mandatory**
CORE_SW	32	Analog output	Open
CORE_BT	33	Analog input	Open
CORE_IN	34	Analog input	Open
VBOS	35	Analog output	**Connection mandatory**
VMONPRE	36	Analog input	**Connection mandatory**
VPRE_FB	37	Analog input	**Connection mandatory**
NC	38	non connected pin	Not applicable
VPRE_BT	39	Analog output	**Connection mandatory**
VPRE_SW	40	Analog output	**Connection mandatory**
VSUP_PWR	41	Analog input	**Connection mandatory**
VSUP	42	Analog input	**Connection mandatory**

Table 4. Connection of unused pins*...continued*

Symbol	Pin Number	Type	Connection if not used
VBST_FB	43	Analog input	**Connection mandatory when VBST is used in front-end.** Grounded when VBST is not used.
VBST_ISL	44	Analog input	**Connection mandatory when VBST is used in front-end.** Grounded when VBST is not used.
VBST_G	45	Analog output	Open when VBST is not used.
VBST_ISH	46	Analog input	**Connection mandatory when VBST is used in front-end.** Grounded when VBST is not used.
WAKE 1	47	Analog input	Open - Internal pulldown can be activated by OTP (with WK1PD_OTP = 1)
BATSENSE	48	Analog input	**Connection mandatory**
EP	49	Ground connection	**Connection mandatory**

9 Maximum ratings

Table 5. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	-0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB	DC voltage at GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB pins	-0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with -10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	-18.0	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	-1.2	40	V
CORE_BT	DC voltage at CORE_BT pin	-0.3	12.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW pins	-0.3	8.5	V
VBOS	DC voltage at VBOS pin	-0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G and VBST_PG pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, GNDSUB, EP	DC voltage at GNDFS, GND, GNDSUB pins, and exposed pad (EP)	-0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	—	mA

10 Electrostatic discharge

Table 6. ESD

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H.				
V_{ESD_HBM}	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	-500	500	V
V_{ESD_CDM2}	Corner pins	-750	750	V
Gun Test				
V_{ESD_CDT1}	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT2}	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT3}	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT4}	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT5}	Operating ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	-8	8	kV

11 Thermal ratings

Table 7. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{STG}	Storage temperature	-55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S SPI bit	145	155	170	°C

Table 8. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance Junction to Ambient[1]	25	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance Junction to Case Bottom[2][3] (with uniform power dissipation on the silicon die)	1.7	°C/W
$R_{\theta JCTOP}$	Thermal resistance Junction to Case Top[1][3]	13.5	°C/W
Ψ_{JT}	Thermal characterization parameter Junction to Top[4]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

12 EMC compliance

The FS26 EMC performance is verified against BISS generic IC EMC Test Specification version 2.0 from 07.2012 and FMC1278 Rev3 Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems from 2018. For performance results and specific conditions, refer to the FS26 webpage.

13 Supply voltage and operating range

13.1 Supply voltage

Depending on the chosen front-end voltage regulator (VPRE or VBST), the FS26 can support two different supply voltage ranges.

If VBST is chosen to be the front-end DCDC converter (directly connected to the battery), the supply voltage of the FS26 can go down to voltage levels typical of a cold-crank event. Because of this, the FS26 can still provide all available regulated voltages, even when the battery line drops below the VPRE output voltage. In this case, the supply voltage operating range is extended to V_{BST_IN} range.

When VPRE is chosen to be the first DCDC converter connected to the battery, the FS26 is unable to provide power rails when the supply voltage is below the V_{PREIN} minimum limit. This topology is chosen for applications that do not need to support cold-crank events.

If an application requires voltages above the VPRE output voltage, the boost controller can be used to generate these voltages. In this case, the supply voltage operating range is narrowed down to the V_{PREIN} voltage range.

The VSUP pin is monitored to avoid erratic startups and shutdowns of the FS26. Specific voltage thresholds are implemented with hysteresis. When the VSUP pin voltage is rising, the FS26 will not start until the VSUP pin voltage crosses the V_{SUP_UVH} threshold. If V_{SUP} goes below V_{SUP_UVL} before the end of the power up sequence, the device will restart. Once the power up sequence is finished and the device is in Normal mode, V_{SUP_UVL} has no effect.

The VSUPUV6_I SPI bit can notify the system that the input voltage of the FS26 is decreasing, indicating that the VSUP pin voltage has crossed the V_{SUPUV6} voltage threshold.

Table 9. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{SUP}	Device input supply voltage (on VSUP pin)	V_{SUP_UVL}	12	36	V
V_{SUP_UVH}	V_{SUP} undervoltage threshold (rising edge on VSUP pin) VSUP_UVTH_OTP = 0 (recommended for VBST in front-end configuration) VSUP_UVTH_OTP = 1 (mandatory for VBST in back-end configuration or not used)	 4.6 5.95	 4.8 6.1	 5.0 6.25	V
V_{SUP_OV}	Threshold voltage to latch the interrupt VSUPOV_I (on VSUP pin)	19.3	20	20.7	V
V_{SUP_UVL}	V_{SUP} undervoltage threshold (falling edge on V_{SUP} pin) VSUP_UVTH_OTP = 0 (recommended for VBST in front-end configuration) VSUP_UVTH_OTP = 1 (mandatory for VBST in back-end configuration or not used)	 4.1 5.5	 4.3 5.65	 4.5 5.8	V
V_{SUP_UV6}	Threshold voltage to latch the interrupt VSUPUV6_I (on VSUP pin)	5.8	6.0	6.2	V
V_{PRE_UVH}	V_{PRE} undervoltage threshold high (rising edge on V_{PRE} pin)	2.9	3.0	3.1	V
V_{PRE_UVL}	V_{PRE} undervoltage threshold low (falling edge on V_{PRE} pin)	2.5	2.6	2.7	V
V_{PRE_UVBOS}	V_{PRE} undervoltage threshold to switch VBOS from VPRE to VSUP when BOS_IN_OTP[1:0] = 00	3.4	3.55	3.7	V

13.2 Operating range

13.2.1 Operating range in Normal mode

The FS26 device supports two distinct topologies for boost converter configuration, giving two distinct operating ranges for the input voltage. When the boost is used as a front-end regulator, a wider input supply range is supported. When the boost is used as a back-end regulator or is not used, the supply voltage needs to be V_{PRE_HDR} higher than the VPRE output voltage to ensure full parametric operation.

Figure 8 describes the supply range of the FS26 with or without the boost used as a front-end or back-end regulator. Front-end topology should be used to support cold-crank events on the battery input. In the back-end configuration, full operation is guaranteed when V_{SUP} is higher than V_{PRE} output voltage + V_{PRE_HDR}. (See Section 20.2 for V_{PRE_HDR}).

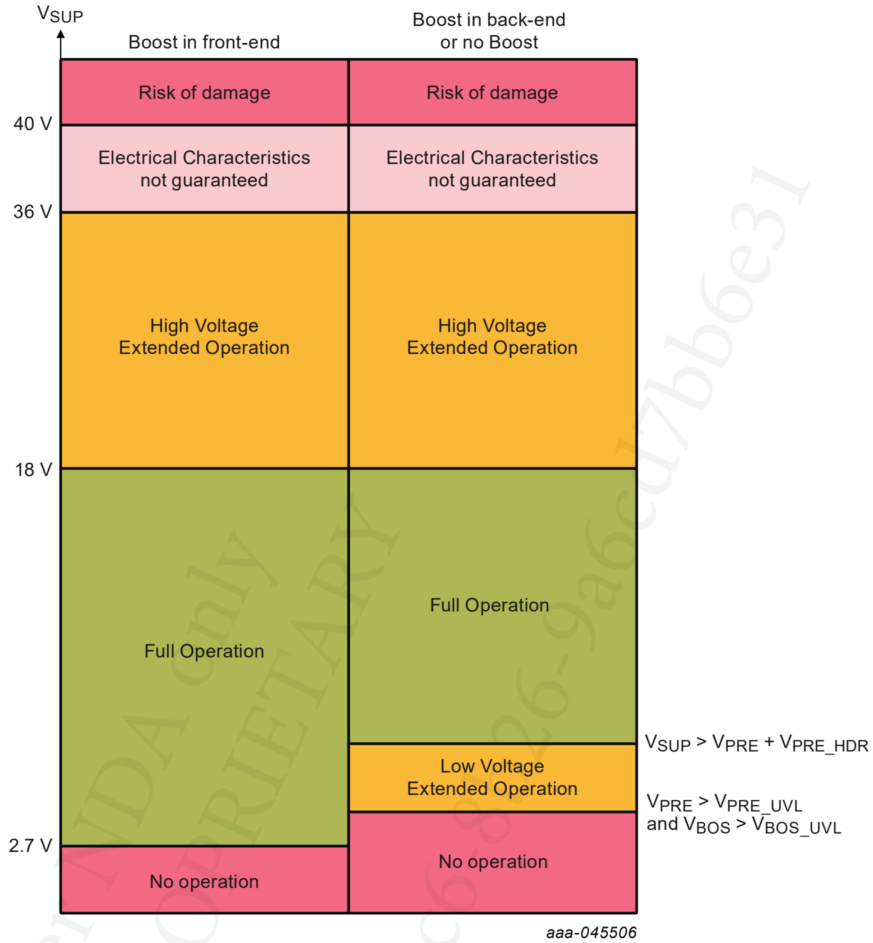


Figure 8. Input voltage range in Normal mode

13.2.2 Operating range in Low Power modes

In Standby and LPOFF modes, monitors are disabled to ensure lowest current consumption. The minimum operating condition is V_{BOS_POR}.

Figure 9 describes the supply range of the FS26 in Standby and LPOFF modes. When transitioning to Standby mode, the boost regulator will be turned off and VPRE will switch from VPRE_OTP[5:0] to VPRE_LP_OTP[5:0].

When the device is in LPOFF mode, all the regulators are turned off.

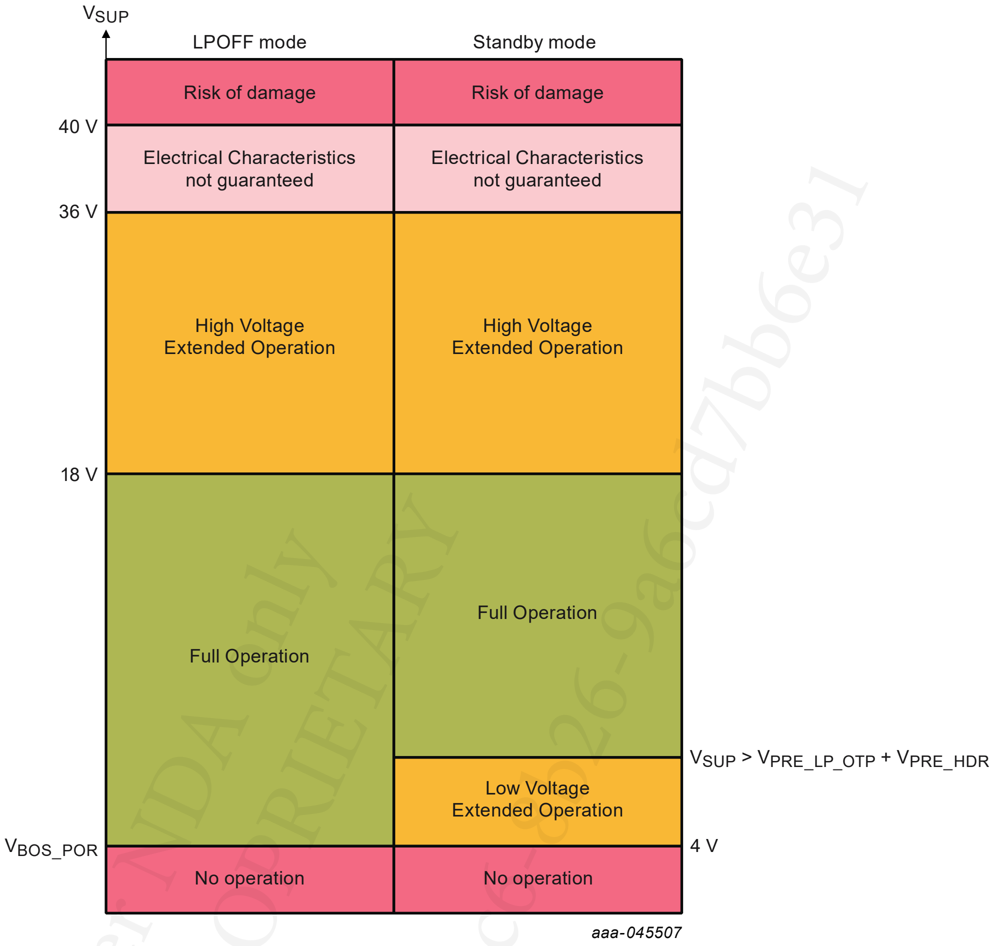


Figure 9. Input voltage range in Standby and LPOFF modes

Figure 8 and Figure 9 legend:

- **No Operation** means the device is not providing the expected functionality or is shut down.
- **Low Voltage Extended Operation** means the device remains functional but with reduced electrical performance.
  - VPRE may be in drop out mode. VPRE output voltage may decrease below its nominal value and the transient load will be degraded.
- **Full Operation** means the device is providing the expected functionality with full electrical performance within the limits of the data sheet and within the operating mission profile of the safety manual.
- **High Voltage Extended Operation** means the device is providing the expected functionality with full electrical performance within the limits of the data sheet but for a limited period of time:
  - This could occur during load dump or double-battery jump-start events, for example.
  - In case the application requires operation above 18 V continuously (for example, for 24 V applications), contact your NXP sales representative to assess the reliability impact.
- **Electrical Characteristics not guaranteed** means the device remains functional, but with reduced electrical performance.
  - In Low Power mode, the quiescent current will increase.

– In normal operation, the VPRE thermal limitation may trigger the thermal shutdown. VPRE transient load will be degraded.

- **Risk of damage** means the device is overstressed, with a risk of damage to the device.

14 Current consumption

Table 10. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Quiescent current					
I_{Q_NORMAL}	Current consumption in Normal mode on the battery: • V_{SUP} = V_{SUP_PWR} = 13.5 V (including current from BATSENSE pin) • VBST enabled but not switching. • VPRE output voltage set at 5.5 V • L_{VPRE} = 10 µH • VCORE enabled and output voltage set at 1.5 V • LDO1 enabled and output voltage set at 5.0 V • LDO2 enabled and output voltage set at 3.3 V • TRK1 and TRK2 enabled and output voltage set at 5 V • VREF enabled and output voltage set at 5 V • Long Duration Timer enabled • All regulators output current = 0 A		15	25	mA
I_{Q_STBY} [1]	Current consumption in Standby mode on the battery • T_A = 25 °C • T_A = 40 °C[2] • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 12 V, 18 V (including current from BATSENSE pin) • VPRE output voltage set at 3.7 V (PFM mode) • L_{VPRE} = 10 µH • LDO1 enabled, V_{LDO1} = 3.3 V • LDO2 disabled. Typ 3 µA additional on V_{SUP} when enabled at 3.3 V • Long Duration Timer disabled, < 1 µA when enabled. • GPIOx disabled in standby • RSTB released, pulled up to V_{PRE} • FS0B = 0 and FS1B = 0 pulled up to a disabled supply in Standby mode.		32 36 40	— — 60	µA
I_{Q_STBY}	Current consumption in Standby mode on the battery • T_A = 25 °C • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 5.4 V (including current from BATSENSE pin) • VPRE output voltage set at 3.7 V and 5.05 V (PFM mode) • L_{VPRE} = 10 µH • LDO1 enabled, V_{LDO1} = 3.3 V when V_{PRE} = 3.7 V, V_{LDO1} = 5.0 V when V_{PRE} = 5.05 V. • LDO2 disabled. Typ 3 µA additional on V_{SUP} when enabled at 3.3 V • Long Duration Timer disabled. < 1 µA when enabled. • GPIOx disabled in standby • RSTB released, pulled up to V_{PRE} • FS0B = 0 and FS1B = 0 pulled up to a disabled supply in Standby mode.		90 110	— 130	µA
I_{Q_LPOFF}	Current consumption in LPOFF mode on the battery • T_A = 25 °C • T_A = 40 °C[2] • T_A = 85 °C[2] • V_{SUP} = V_{SUP_PWR} = 5.4 V, 12 V, 18 V • (Including current from BATSENSE pin) • All regulators are disabled. • Long Duration Timer disabled. < 1 µA when enabled. • GPIOx disabled in LPOFF		30 32 40	— — 60	µA

[1] In Standby mode VBAT current is reduced, due to the ratio between VBAT and VPRE voltages.
[2] Guaranteed by characterization. Tested in production at 25°C only.

14.1 Total battery current consumption estimation in Standby mode

The Standby mode current consumption can be estimated using Figure 10 and Figure 11 at T_A = 25 °C and T_A = 85 °C, depending on the use case. The measurements were made with the following assumptions:

- V_{SUP} = V_{SUP_PWR} = 12 V.
- L_{VPRE} = 10 µH
- Long Duration Timer disabled.
- GPIOx disabled in standby.
- RSTB released and pulled up to VPRE.
- FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode.
- All regulators unloaded.

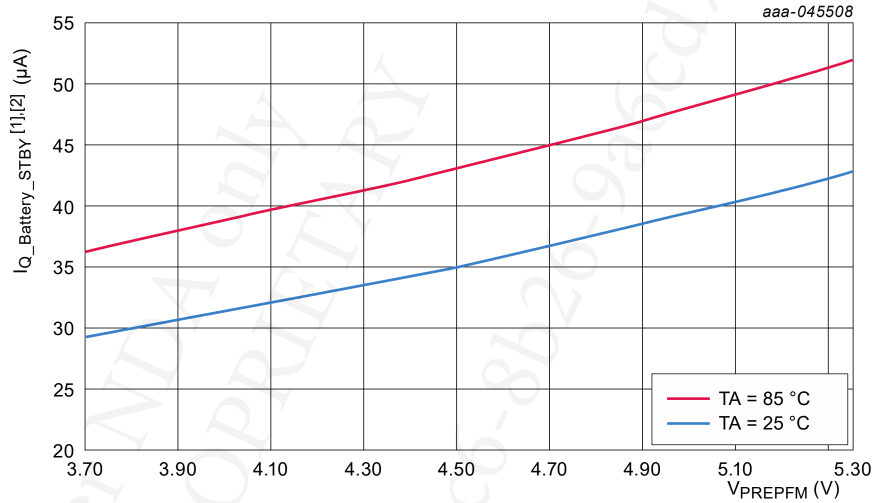


Figure 10. Battery current consumption in Standby mode (LDO1 and LDO2 disabled)

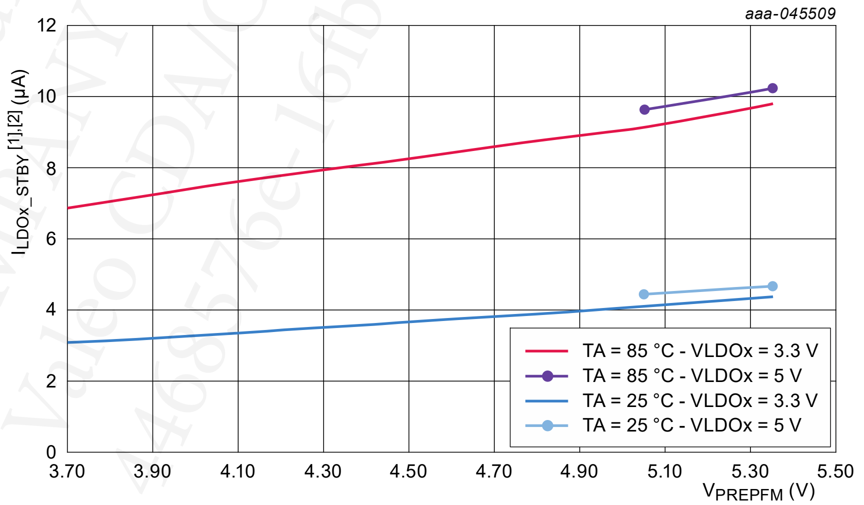


Figure 11. LDOx current consumption in Standby mode

When LDOx is used at 5 V, VPRE output voltage in Standby mode must be 5.35 V to comply with the LDOx minimum dropout voltage. [1] [2]

The total Standby mode current consumption can be estimated at either T_A = 25 °C or T_A = 85 °C using the following formula:

$$I_{Q\_Total\_Battery\_STBY}\ (\mu A) = I_{Q\_Battery\_STBY} + I_{LDOx\_STBY} \times N$$

Where N is the number of LDOx used.

14.2 Standby mode current consumption

In most cases, LDO1 or LDO2 regulators are used in Standby mode to supply light loads.

The total battery current consumption can be estimated using Figure 12 at T_A = 25 °C and T_A = 85 °C, depending on the LDO1 or LDO2 load. The measurements have been done with the following assumptions:

- V_{SUP} = V_{SUP_PWR} = 12 V.
- L_{VPRE} = 10 µH
- Long Duration Timer disabled.
- GPIOx disabled in standby.
- RSTB released and pulled up to VPRE.
- FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode.
- LDO1 and LDO2 enabled.
- V_{LDO1} = 3.3 V, V_{LDO2} = 5 V and V_{PRE} = 5.35 V.
- No external load on VPRE.

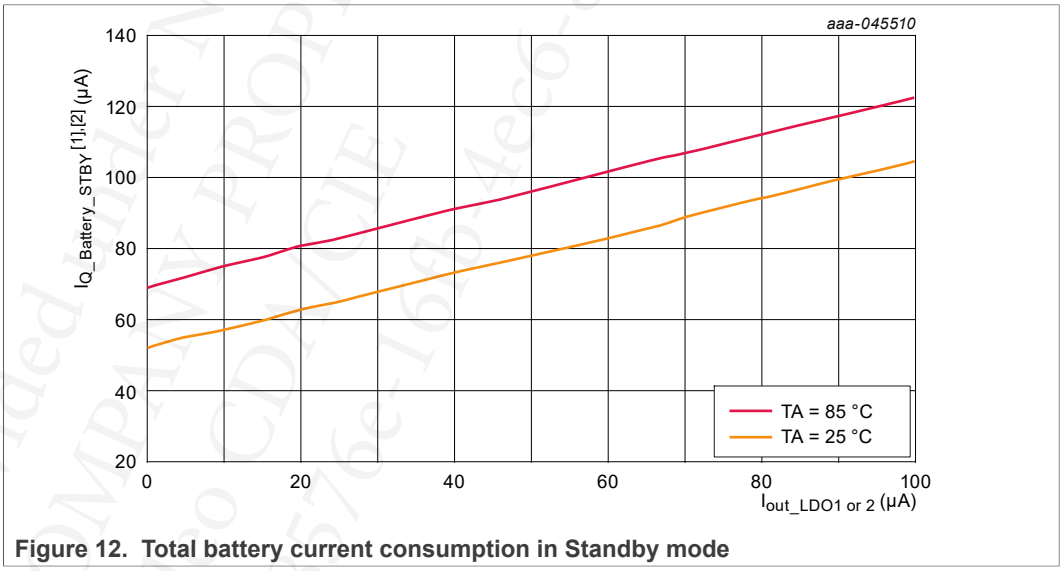


Figure 12. Total battery current consumption in Standby mode

The total battery current consumption can also vary depending on the chosen inductor for L_{VPRE}. Below additional measurements have been done with the following assumptions:

- Long Duration Timer disabled.
- GPIOx disabled in standby.

1 In Standby mode VBAT current is reduced, due to the ratio between VBAT and VPRE voltages.
2 Guaranteed by characterization. Tested in production at 25°C only.

- RSTB released and pulled up to VPRE.
- $V_{SUP} = V_{SUP\_PWR} = 12$ V.
- FS0B asserted, FS1B pulled up to a disabled supply in Standby mode.
- LDO1 and LDO2 disabled.
- $V_{PRE} = 5.35$ V or 3.7 V.
- No external load on VPRE.

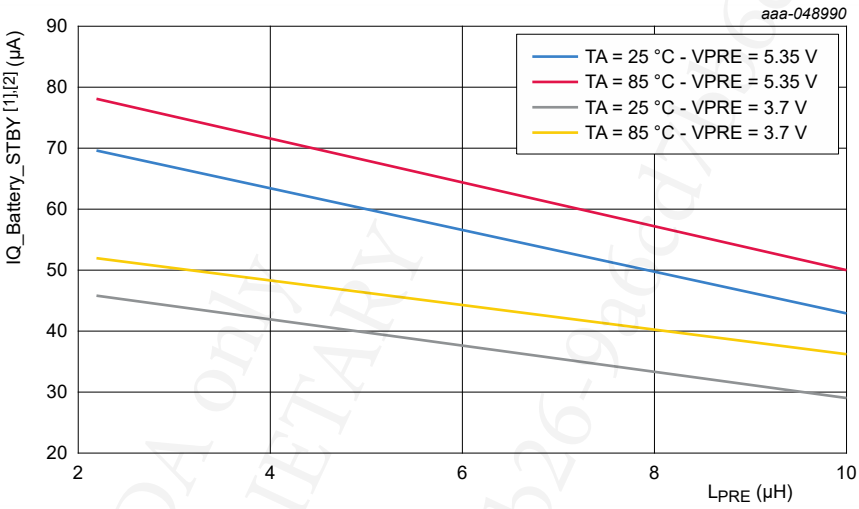


Figure 13. Battery current consumption in STBY mode with V_{PRE} = 3.70 V or 5.35 V and LDOx disabled

15 General device operation

15.1 Simplified functional state diagram

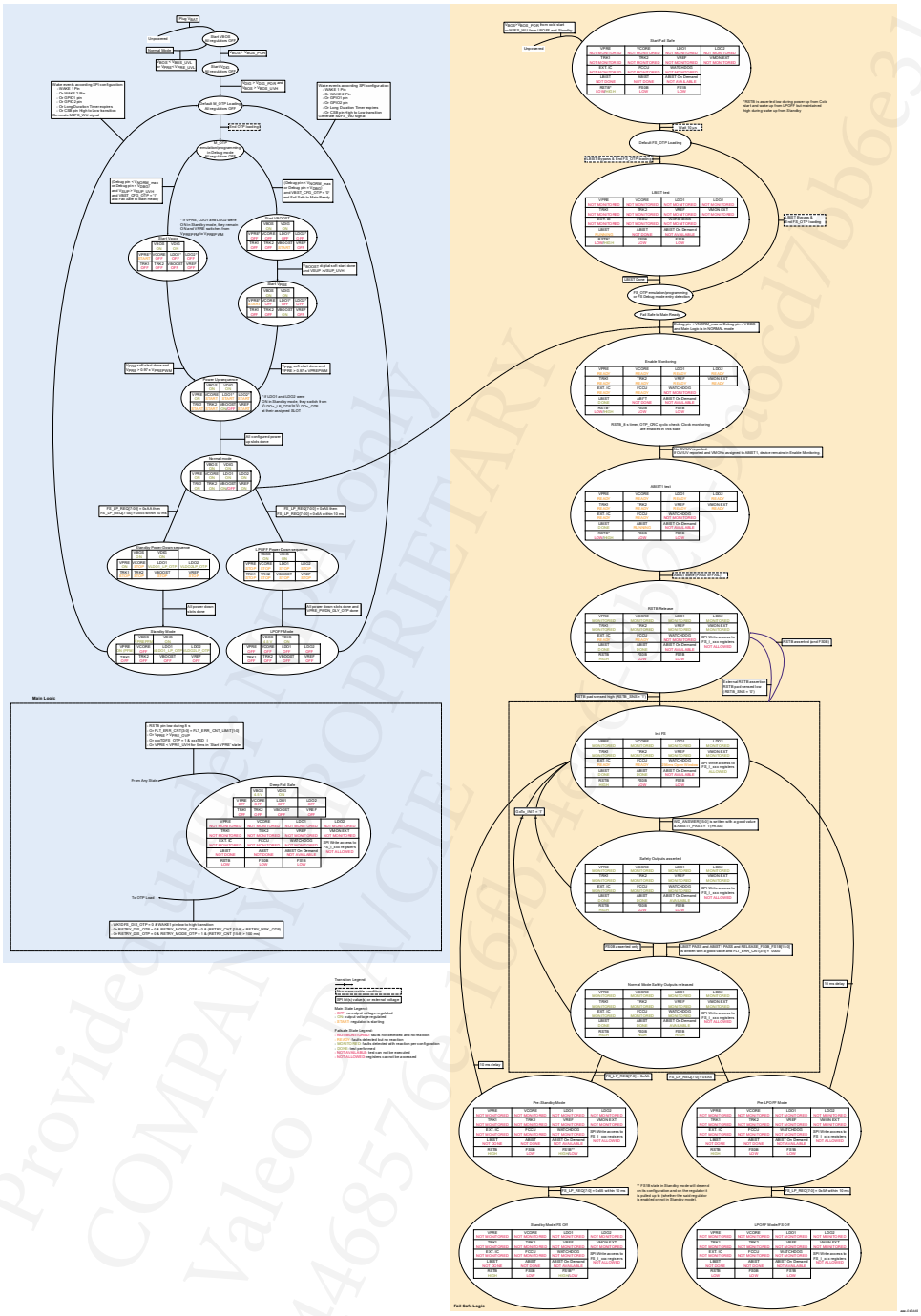


Figure 14. Simplified functional state diagram

15.2 Functional device operation and power modes

FS26 operation is divided in two independent logic blocks to achieve best in class functional safety coverage. The main state machine manages the power management, the Low Power modes, and the wake-up sources while the fail-safe state machine manages the monitoring of the power management, the monitoring of the microcontroller and the monitoring of an external IC.

The FS26 provides three main operating modes:

- ***Normal mode*** is intended to be the fully functional mode. All power supplies are enabled as required by the system, and all system functionality provided by the FS26 is available. During Normal mode, the fail-safe state machine is available and providing full monitoring and operation of all the safety features in the device.
- ***Standby mode*** is intended to be the Low Power ON mode, providing support to the minimum system requirements with low current consumption from the battery. During the *Standby mode*, only the VPRE remains enabled to supply the microcontroller I/O rails. LDO1 and LDO2 can be enabled in this mode depending on the OTP configuration. GPIO1 and GPIO2 can remain at the same state as in *Normal mode*, depending on the SPI configuration. *Standby mode* is assumed to be a safe state with no critical activity, and therefore the fail-safe state machine is disabled to achieve minimum current consumption by the system.
- ***LPOFF mode*** is intended to be the Low Power OFF mode, with no active system supplies except GPIO1, which can remain enabled. Logic circuitry is internally supplied to allow proper wake up from any of the available wake-up mechanisms, with the minimum current consumption possible.

The system can wake up from any of the Low Power modes via any of the following selectable wake-up mechanisms available in the device (availability is dependent on part number):

- WAKE1 and WAKE2 pins
- GPIO1 and GPIO2 pins
- Long Duration Timer (LDT) expiration
- SPI activity via edge detection of the CSB pin

Table 11 summarizes the operating modes and available features:

Table 11. Operating modes summary

Operating Mode	Power supply state			Wake-up sources and capabilities		
	VPRE	LDOx GPIOx	VBST, VCORE TRK1, TRK2, VREF	WAKEx, GPIOx	LDT	MCU
NORMAL	PWM, ON	ON (Optional)	ON (Optional)	N/A	N/A	N/A
LPOFF	OFF	OFF (GPIO1 optional)	OFF	YES	YES (Optional)	NO
STANDBY	PFM, ON	ON (Optional)	OFF	YES	YES (Optional)	YES

For specific faults or when too many faults occur, the device can enter ***Deep Fail Safe*** state (DFS). In this state, all regulators are OFF, safety outputs are asserted, the SPI interface is not accessible and the device waits for specific events to move to ***Fuses Load*** state again.

Exhaustive list of conditions that put the FS26 in ***Deep Fail Safe*** state:

- RSTB pin is sensed to low level (when it's driven high by the FS26) for a time longer than 8 seconds.
- Too many faults occur: fault error counter reaches its programmed limit (FLT_ERR_CNT[3:0] = FLT_ERR_CNT_LIMIT[1:0]).
- When FAULT_DFS_EN_OTP = 1 device enters ***Deep Fail Safe*** state as soon as RSTB or FS0B is asserted.
- VPRE output voltage crosses V_{PRE_OVP} threshold for a time longer than t_{VPRE_OVP}.
- A thermal shutdown (TSD) occurs, and this TSD is configured by the SPI to cause entry into ***Deep Fail Safe*** state (that is, VPRETDFS = '1' and VPRETSD_I = '1'). If the DFS is disabled, the device will not transition to DFS mode but the regulator will be disabled.

Exhaustive list of conditions that make the device leave the ***Deep Fail Safe*** state to ***Fuses Load*** state:

- WAKE 1 pin is toggled from low to high level by the system and the OTP configuration allows WAKE 1 to resume from ***Deep Fail Safe*** state (WK1DFS_DIS_OTP = '0')
- Auto-retry mode is enabled by OTP (RETRY_DIS_OTP = '0') and 'Infinite retry' is selected (RETRY_MODE_OTP = '1'): the FS26 is making an attempt to exit from the ***Deep Fail Safe*** state and to go to the ***Fuses Load*** state every 100 ms and RETRY_CNT increments every 16 counts. Once RETRY_CNT reaches the RETRY_MSK_OTP value, the RETRY_CNT time value is clamped and retries occur infinitely to the last clamped retry frequency until a valid condition to exit ***Deep Fail Safe*** is detected.
- Auto-retry mode is enabled by OTP (RETRY_DIS_OTP = '0') and 'Limited retry' is selected by (RETRY_MODE_OTP = '0'): the FS26 is making an attempt to exit from the ***Deep Fail Safe*** state and to go to ***Fuses Load*** state while the retry counter value (RETRY_CNT) is below the limit configured by OTP (RETRY_MSK_OTP). When the retry counter is equal to the configured limit, the FS26 stays in the ***Deep Fail Safe*** state.

Example: the first time the device enters ***Deep Fail Safe,*** it will make an attempt to retry every 100 ms, and after 16 retries the counter increases to (RETRY_CNT) + 1 and then uses the next value of 200 ms, and so on, until (RETRY_CNT) = (RETRY_MSK_OTP).

Deep Fail Safe entry can be bypassed by setting MDFS_OTP = '1' and DFS_DIS_OTP = '1'. This means that any request coming from the ***Deep Fail Safe*** sources list will be ignored. RSTB and safety outputs will still be asserted in case of fault.

15.3 Fail-safe state machine

The fail-safe state machine is designed to run independently from the main state machine. However, all necessary handshaking signals are provided to ensure seamless operation as a single device. These signals are protected up to 40 V to ensure the integrity of the fail-safe circuitry, keeping maximum isolation between both blocks.

During the power up of the fail-safe state machine (from a cold boot or a wake-up event), the system performs logic built-in self-test (LBIST) on all the gates related to the functional safety operation, as well as analog built-in self-test (ABIST) on all the analog blocks dedicated to safety monitoring and notification.

An ABIST on demand can be requested through a SPI command, to allow the system to check the integrity of the safety mechanisms at any point during the Normal mode and to detect potential latent faults when the application is running.

The RSTB pin is provided to inform the microcontroller that system power supplies are up and in regulation regardless of the results of the ABIST. A configurable watchdog counter is included to ensure the microcontroller is able to communicate with the FS26, which can react to any failure condition and place the system in a safe state.

Two safety outputs, FS0B and FS1B, are provided to keep the system in a safe state until the microcontroller acknowledges it is safe to start normal operation, or when a fault is present. When a fault is present, these outputs prevent the system from entering an unsafe state.

When the microcontroller is properly initialized, it can request to release FSxB through a SPI command to set the application to Normal mode, with all the selected monitoring activated. The FS26 will react by asserting the safety pins (RSTB and FSxB), according to its configuration, when a fault is detected.

15.4 Application flowchart

In an application, the debug pin is connected to GND and a watchdog refresh is required as soon as the INIT_FS window is closed. The system enters Normal mode once the safety outputs are released. Figure 15 is a high-level flowchart illustrating entry into Normal mode in the application.

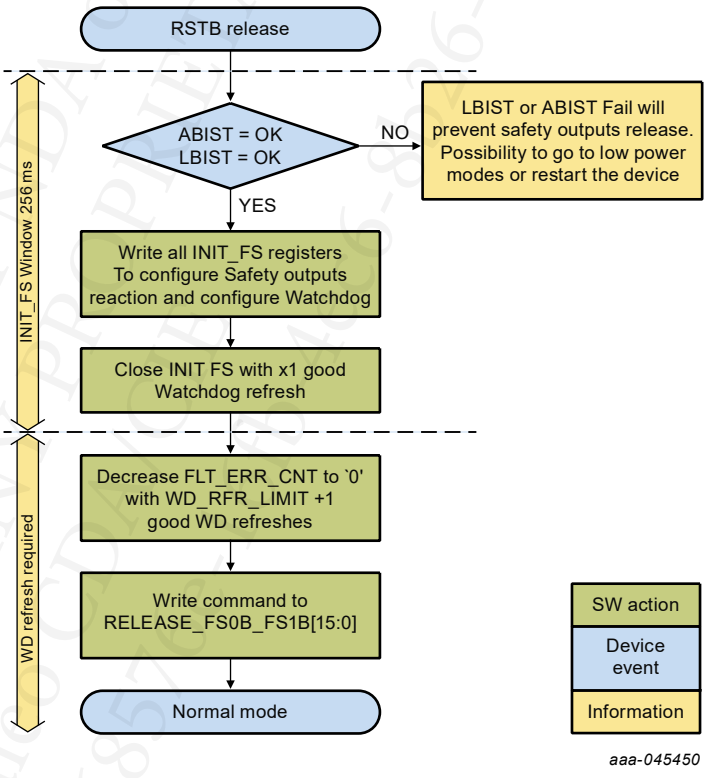


Figure 15. Application flowchart

15.5 Input power topology

The FS26 provides two input topologies to address various system needs. A reverse protection Schottky diode (D_{BAT}) between battery voltage (V_{BAT}) and the FS26 is required. Depending on the system configuration, the FS26 can obtain V_{SUP} in two main configurations:

1. The switching boost controller (VBST) can be used as the front-end supply to support system cranking events with voltage drops down to 2.7 V at the V_{BST_IN} input. When VBST is used as the front-end supply, the battery voltage (V_{BAT}) is applied at the input of the boost controller. During normal operation when V_{SUP} > VBST_OTP, the boost controller stops switching and operates in Pass-Through mode.

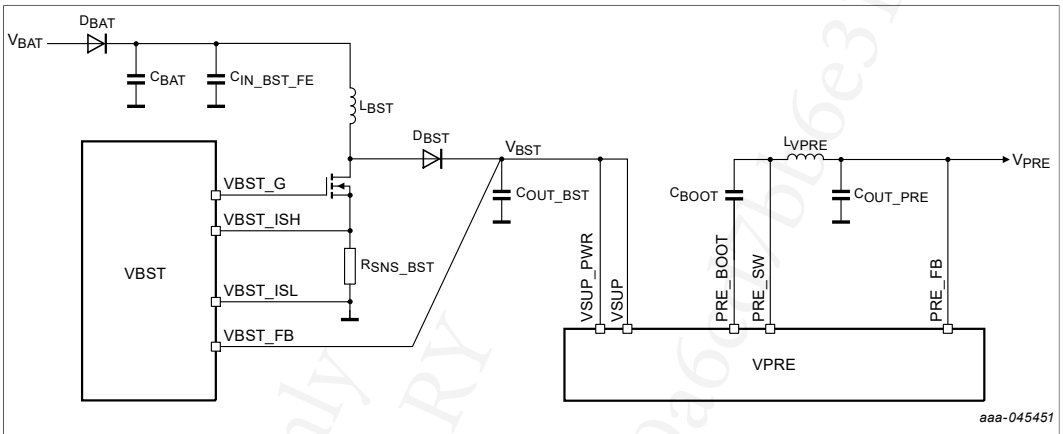


Figure 16. Input topology: front-end boost controller

When V_{SUP} < VBST_OTP, the boost controller starts switching to maintain V_{SUP} above the V_{SUP_UVH} threshold, thus ensuring system operation during crank profiles.

2. For systems with less severe or no cranking events, the input power can be applied directly to the VSUP pin. In this scenario, the FS26 can ensure functionality if V_{SUP} > V_{PRE} + V_{PRE_HDR} (Section 20.2 for V_{PRE_HDR}). The device will shut down if V_{PRE} < V_{PRE_UVL}. The reverse voltage protection diode and a PI-filter are needed to guarantee optimal EMI performance.

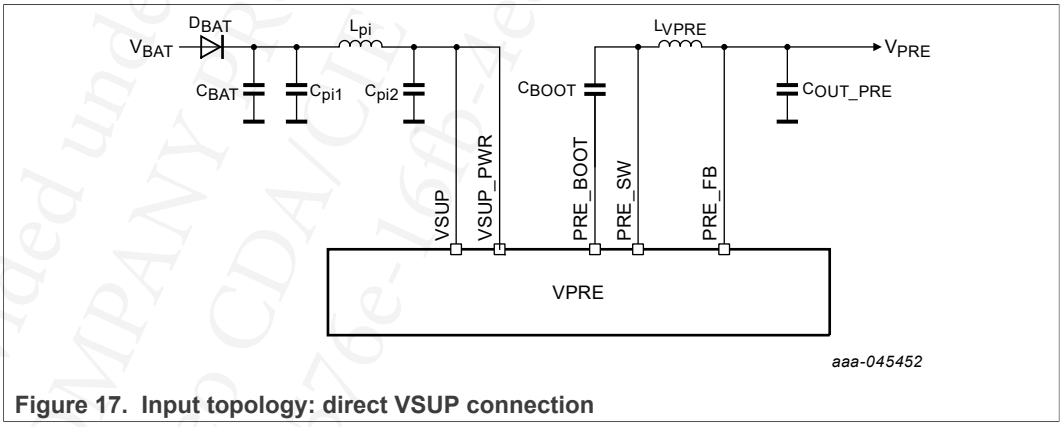


Figure 17. Input topology: direct VSUP connection

At the chip level, the power-up sequencing and operating thresholds are referenced to VSUP input. However, proper considerations should be made to ensure the system level requirements are met with respect to V_{BAT} voltage.

15.6 System power up and power down

When a voltage is applied to the VSUP pin, the FS26 starts its internal power-up biasing. As the internal best of supply (BOS) reaches regulation and the default OTP configuration is loaded, the system proceeds to turn on the output regulators based on

the OTP configuration of the device. The regulators' power-up sequence is dependent on the input power topology used in the system:

With VBST used as the front-end supply

- VBST is enabled first and will ensure $V_{SUP} > V_{SUP\_UVH}$.
- Once V_{SUP} has crossed the V_{SUP_UVH} threshold, VPRE is enabled automatically.
- The remaining regulators will start as set in the OTP power-up sequence configuration.

Direct connection to VSUP

- Once V_{SUP} has crossed the V_{SUP_UVH} threshold, VPRE is enabled automatically.
- The remaining regulators will start in their corresponding power up slot as set in the OTP power-up sequence configuration.

15.6.1 Regulator power-up sequence

Seven slots are available to program the startup sequence of VCORE, LDO1, LDO2, VREF, VTRK1, and VTRK2, as well as the GPIO1 and GPIO2 signals for external control.

The power-up sequence starts from SLOT_0 to SLOT_6, with a TSLOT_OTP delay between each slot. RSTB is released after SLOT_6. Regulators assigned to “SLOT_7/OFF” are not started during the power-up sequence and can be enabled later in Normal mode via a SPI command. When VBST is used in back-end supply, it can only be enabled via a SPI command once the device is in Normal mode.

Each regulator is assigned to a slot by OTP configuration using the dedicated OTP bits. Each slot is executed regardless of whether a regulator is assigned to a slot or not. Slots can be bypassed with SLOT_BYP_OTP. A regulator assigned to a bypassed slot will not start in the power-up sequence.

When the last power-up slot is complete, monitoring of the voltages is enabled. If the soft start of a regulator is not complete and the output voltage is still below the UV monitoring, the UV is detected and reported in the corresponding flag. Therefore, NXP recommends clearing all the UV flags at each startup during INIT_FS.

When VCORE is enabled, the bootstrap capacitor must be charged. Therefore, the VCORE regulator output starts to ramp-up with a delay of 100 μs from the beginning of the slot.

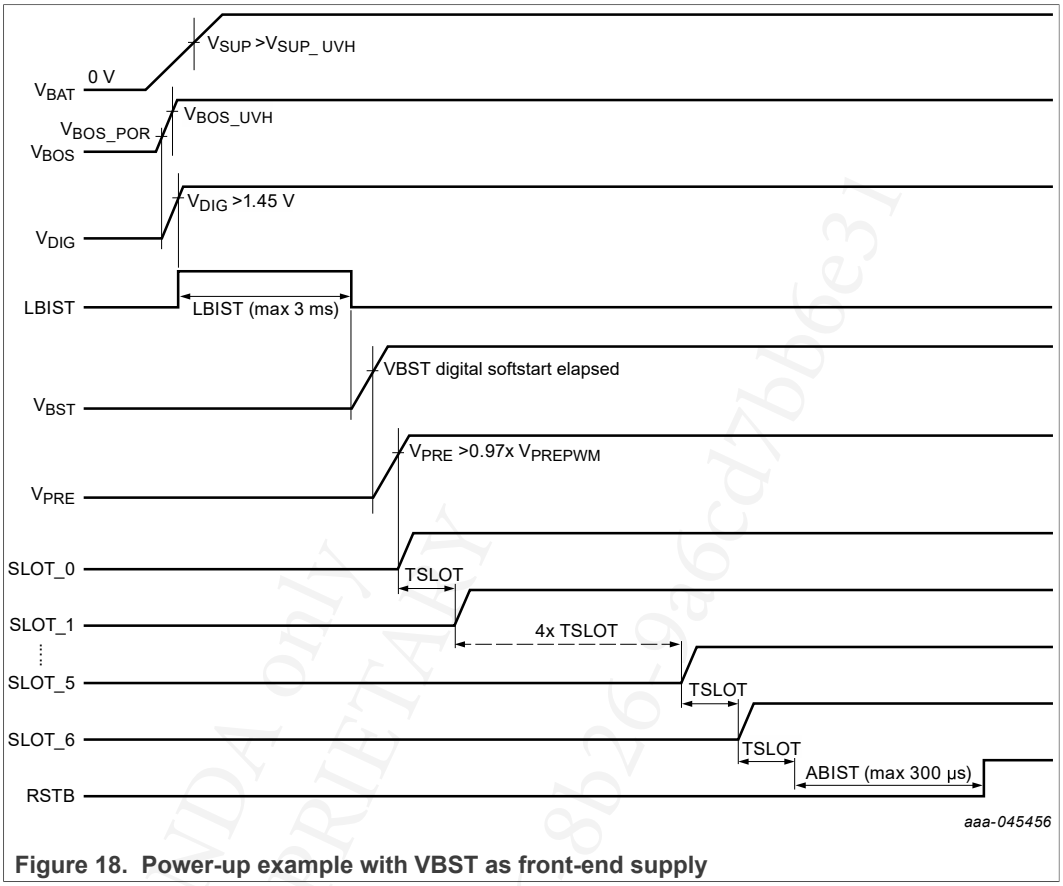


Figure 18. Power-up example with VBST as front-end supply

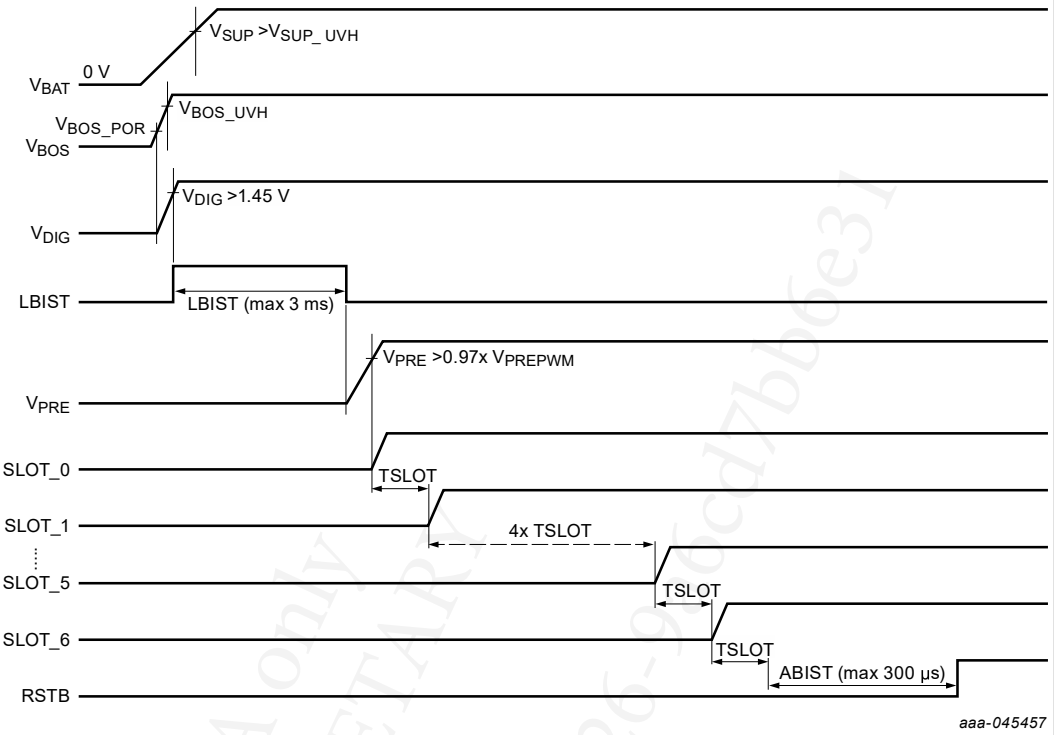


Figure 19. Power-up example with direct battery supply

To reduce the power-up timing, an OTP configuration is provided to bypass the unused slots (that is, bypass Slot X to Slot 6).

Once the power-up sequence is complete, the Main state machine is in Normal mode, which is the application running mode with all the regulators ON.

15.6.2 System power-down sequence

During a power-down event, the device uses the same slot bits to turn off the voltage regulators, in reverse order from the power-up sequence.

If a slot bypass configuration is enabled, the device will start the power-down sequence from the selected slot in the OTP configuration.

When powering down to the Standby mode, VPRE remains enabled. LDO1 and LDO2 can be programmed to also remain enabled during the Standby mode. GPIO1 and GPIO2 can also remain in the same state that they were in, in Normal mode. All other regulators are disabled as defined by the slot bits.

When powering down into the LPOFF mode, all voltage regulators are disabled as described in the power-down sequence. Once the voltage regulators in the sequencer are disabled, the VPRE will start powering off, followed by the VBST if it is used as the front-end supply.

If VBST is used in back-end mode, the regulator will be turned off in the first power-down slot.

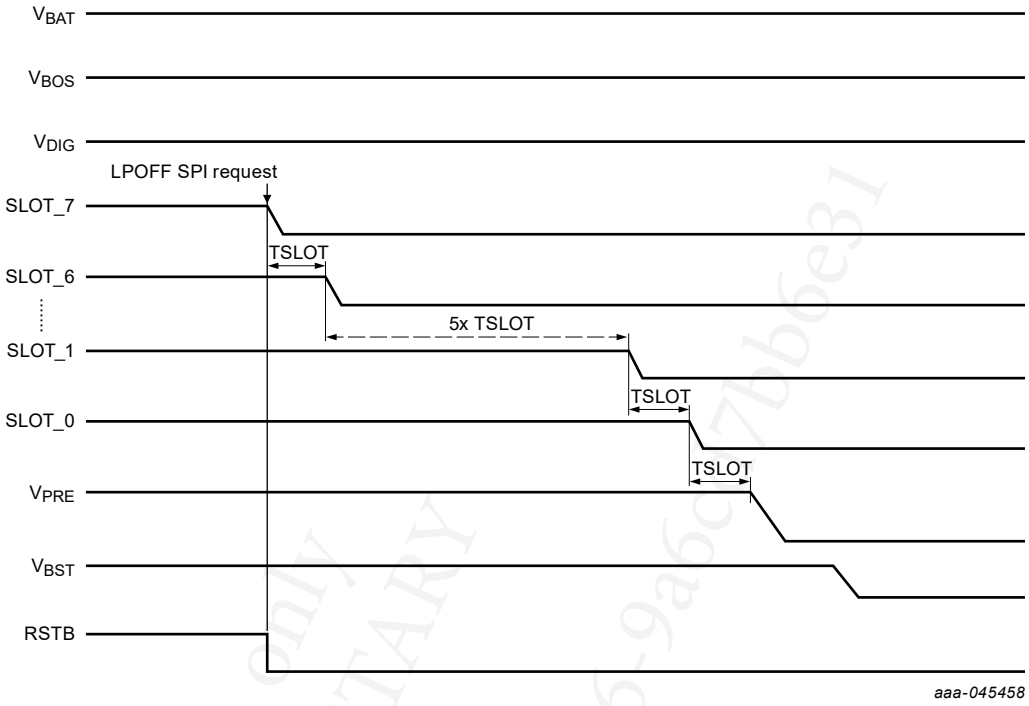


Figure 20. Power down example with VBST as front-end supply

15.7 Wake-up sources

The FS26 has several selectable wake-up sources from the Low Power modes:

- WAKEx pin:
  - The WAKEx pins can be configured to detect wake-up events internal or external to the ECU.
  - The WAKEx pins can detect wake-up event on high level or low level.
- GPIOx pin:
  - The GPIOx pins can be configured as inputs to detect wake-up events internal to the ECU.
  - The GPIOx pins can detect wake-up event on high level or low level.
- SPI chip select wake-up:
  - When the SPI wake up is enabled, the device wakes up with any activity on the SPI bus (transition from high to low of CSB pin).
  - In case of a SPI wake up, the first SPI command is ignored, and the FS26 will be able to respond to the subsequent SPI commands after 1.5 ms.
- Long Duration Timer (LDT) expired:
  - Wake up from the LDT is available (part number dependent).
  - When the LDT is enabled, it can be configured to generate a wake-up event when the timer expires. This feature allows the system to perform cyclic system verifications while it is in the Low Power mode.

15.8 SPI communication

The FS26 uses a 32-bit SPI, with the following arrangement:

MOSI (primary out, secondary in) bits:

- Bit 31: Main or fail-safe registers selection
- Bit 30 to 25: Register address
- Bit 24: Read/Write (For reading Bit 24 = ‘0’; For writing Bit 24 = ‘1’)
- Bit 23 to 8: Control bits
- Bit 7 to 0: Cyclic redundant check (CRC)

MISO (primary in, secondary out) bits:

- Bit 31-24: General device status
- Bits 23 to 8: Extended device status, or device internal control register content or device flags (see Table 12)
- Bit 7 to 0: Cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

The MCU is the primary driving MOSI and FS26 is the secondary driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge, MSB first. In a write command, MISO [23:8] bits are the previous register bits and MISO [7:0] is the CRC of the message sent by the FS26. In a read command, MOSI [23:8] bits are all 0 and MOSI [7:0] is the CRC of the message sent by the MCU. Figures 20 and 21 describe the SPI communication protocol for writing data into the FS26 or reading data from the FS26.

The FS_EN bit is set high as soon as the fail-safe state machine enters Enable monitoring state. The bit remains enabled during the normal operation until the system has successfully moved into any of the low-power states.

In all other states, FS_EN bit is set at 0.

The M_AVAL bit is set high as soon as the main state machine is in Normal mode state. In all other states, this bit is set to 0.

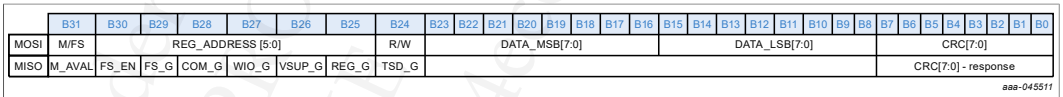


Figure 21. SPI Write operation protocol

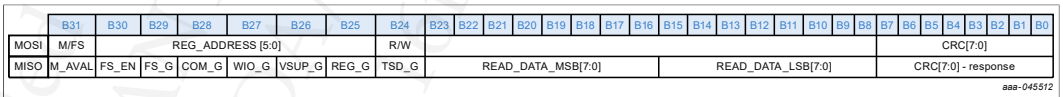


Figure 22. SPI read operation protocol

Table 12. MISO general device status bits descriptions

Bit	Symbol	Description
31	M_AVAL	**Main state machine availability**
		0 Main state machine is not available (the main state machine is not in Normal mode)
		1 Main state machine is available and able to respond (the main state machine is in Normal mode)
		Reset on power-on reset (POR)
30	FS_EN	**Fail-safe state machine status**
		0 Fail-safe state machine is not available.

Table 12. MISO general device status bits descriptions *...continued*

Bit	Symbol	Description
		1 Fail-safe state machine is available and able to respond
		Reset on power-on reset (POR)
29	FS_G	**Interrupt notification from the Fail-Safe Domain**
		0 No event present reported into the Fail-Safe Domain
		1 An interrupt or flag is present in the Fail-Safe Domain
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Flags Reporting: VPRE_OV, VPRE_UV, CORE_OV, CORE_UV, LDO1_OV, LDO1_UV, LDO2_OV, LDO2_UV, TRK1_OV, TRK1_UV, TRK2_OV, TRK2_UV, REF_OV, REF_UV, EXT_OV, EXT_UV, BAD_WD_DATA, BAD_WD_TIMING, FCCU12, FCCU1, FCCU2, ERRMON, ABIST1_PASS, ABIST2_PASS, LBIST_STATUS[1:0]
28	COM_G	**Interrupt notification from the M_COM_FLG or FS_DIAG_SAFETY1 registers**
		0 No event reported into M_COM_FLG or FS_DIAG_SAFETY1 registers
		1 An interrupt or Flag is present in the M_COM_FLG or FS_DIAG_SAFETY1 registers
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Source Register: M_COM_FLG, FS_DIAG_SAFETY1
		Flags Reporting: MSPI_CRC_I, MSPI_CLK_I, MSPI_REQ_I, SPI_FS_CLK, SPI_FS_CRC, SPI_FS_REQ
27	WIO_G	**Interrupt notification from the M_WIO_FLG register**
		0 No event reported into M_WIO_FLG register
		1 An interrupt or Flag is present in the M_WIO_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Source Register: M_WIO_FLG
		Flags Reporting: WUEVENT, LDT_I, GPIO2_I, GPIO1_I, WK2_I, WK1_I
26	VSUP_G	**Interrupt notification from the M_VSUP_FLG register**
		0 No event reported into M_VSUP_FLG register
		1 An interrupt or Flag is present in the M_VSUP_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Source Register: M_VSUP_FLG
		Flags Reporting: VBOSUVH_I, VSUPOV_I, VSUPUV6_I, VSUPUVH_I
25	REG_G	**Interrupt notification from the M_REG_FLG register**
		0 No event reported into M_REG_FLG register
		1 An interrupt or Flag is present in the M_REG_FLG register

Table 12. MISO general device status bits descriptions *...continued*

Bit	Symbol	Description
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Source Register: M_REG_FLG
		Flags Reporting: VBSTOV_I, VPREUVH_I, VPREOC_I, TRK2OC_I, TRK1OC_I, COREOC_I, LDO2OC_I, LDO1OC_I, VBSTOC_I
24	TSD_G	**Interrupt notification from the M_TSD_FLG register**
		0 No event reported into M_TSD_FLG register
		1 An interrupt or Flag is present in the M_TSD_FLG register
		Reset on power-on reset (POR), cleared when all individual bits are cleared
		Source Register: M_TSD_FLG
		Flags Reporting: TWARN_I, GPIO1TSD_I, VPRETSD_I, TRK2TSD_I, TRK1TSD_I, CORETSD_I, LDO2TSD_I, LDO1TSD_I

15.8.1 Cyclic redundancy check

An 8-bit cyclic redundancy check (CRC) is required for each Write and Read SPI command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

Figure 23 is an example of CRC encoding HW implementation:

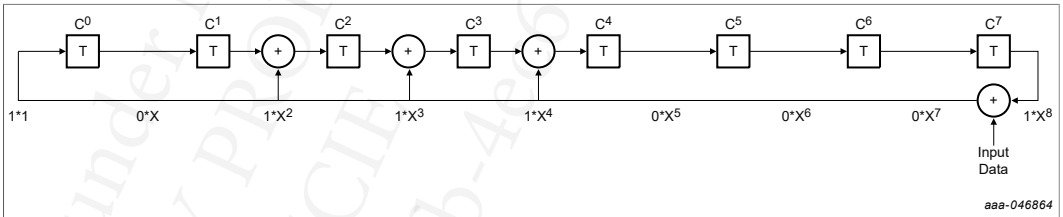


Figure 23. CRC encoder example

The effect of the CRC encoding procedure is shown in Table 13. The seed value is appended into the most significant bits of the shift register.

Table 13. Data preparation for CRC encoding

Seed	M/FS	Register Address	Read/Write	Data_MSB	Data_LSB
0xFF	Bit[31]	Bits[30:25]	Bit[24]	Bits[23:16]	Bits[15:8]

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 32-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, the initial CRC byte composed of zeros is replaced and the CRC is transmitted.

Procedure for CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.

- If the shift register contains all zeros, the CRC is correct.
- If the shift register contains a value other than zero, the CRC is incorrect.

15.8.2 SPI electrical characteristics and timing diagram

Table 14. SPI Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Interface I/O input supply					
V_{DDIO}	VDDIO supply voltage range	3.0	—	5.5	V
Static Electrical Characteristics					
SPI_{VIL}	CSB, SCLK, MOSI low level input voltage	0.3 x V_{DDIO}	—	—	V
SPI_{VIH}	CSB, SCLK, MOSI high level input voltage	—	—	0.7 x V_{DDIO}	V
$SCLK_{IPD}$	SCLK internal pulldown current source	7	10	13	µA
$MISO_{VOH}$	MISO high output voltage (I = 2.0 mA)	V_{DDIO} - 0.4	—	—	V
$MISO_{VOL}$	MISO low output voltage (I = 2.0 mA)	—	—	0.4	V
I_{MISO}	3-state leakage current (VDDIO = 5.0 V)	- 5.0	—	5.0	µA
$SPI_{PULL-up}$	CSB, MOSI internal pullup (pullup to VDDIO)	190	450	800	kΩ
C_{SPI}	Input capacitor at CSB, SCLK, MOSI	—	—	10	pF

Table 14. SPI Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Dynamic Electrical Characteristics					
F_{SPI}	SPI operation frequency (50% DC)	0.5	—	10	MHz
t_{CLH}	Minimum time SCLK = HIGH	50	—	—	ns
t_{CLL}	Minimum time SCLK = LOW	50	—	—	ns
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge)	—	—	30	ns
t_{CSDV}	CSB = low to data at MISO active	—	—	70	ns
t_{SCLCH}	SCLK low before CSB low (setup time SCLK to CSB change H/L)	70	—	—	ns
t_{HCLCL}	SCLK change L/H after CSB = low	70	—	—	ns
t_{SCLD}	SDI input setup time (SCLK change H/L after MOSI data valid)	35	—	—	ns
t_{HCLD}	SDI input hold time (MOSI data hold after SCLK change H/L)	35	—	—	ns
t_{SCLCL}	SCLK low before CSB high	90	—	—	ns
t_{HCLCH}	SCLK high after CSB high	90	—	—	ns
t_{PCHD}	CSB L/H to MISO at high-impedance	—	—	75	ns
t_{ONCSB}	CSB min. high time	500	—	—	ns
t_{CBS_MIN}	CSB filter time	10	—	40	ns

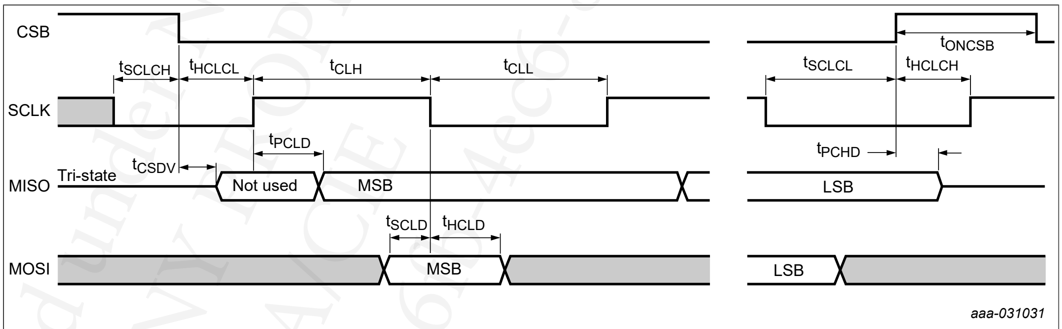


Figure 24. SPI timing diagram

16 Register mapping

Table 15. Main SPI register map

Register	Address								Read/Write	Reference
	M/FS	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0	Hex		
M_DEVICEID	0	0	0	0	0	0	0	#0 (00h)	Read Only	Section 17.1
M_PROGID	0	0	0	0	0	0	1	#1 (01h)	Read Only	Section 17.2
M_STATUS	0	0	0	0	0	1	0	#2 (02h)	Read Only	Section 17.3
M_TSD_FLG	0	0	0	0	0	1	1	#3 (03h)	Read and Write	Section 17.4
M_TSD_MSK	0	0	0	0	1	0	0	#4 (04h)	Read and Write	Section 17.5
M_REG_FLG	0	0	0	0	1	0	1	#5 (05h)	Read and Write	Section 17.6
M_REG_MSK	0	0	0	0	1	1	0	#6 (06h)	Read and Write	Section 17.7
M_VSUP_FLG	0	0	0	0	1	1	1	#7 (07h)	Read and Write	Section 17.8
M_VSUP_MSK	0	0	0	1	0	0	0	#8 (08h)	Read and Write	Section 17.9
M_WIO_FLG	0	0	0	1	0	0	1	#9 (09h)	Read and Write	Section 17.17
M_WIO_MSK	0	0	0	1	0	1	0	#10 (0Ah)	Read and Write	Section 17.11
M_COM_FLG	0	0	0	1	0	1	1	#11 (0Bh)	Read and Write	Section 17.12
M_COM_MSK	0	0	0	1	1	0	0	#12 (0Ch)	Read and Write	Section 17.13
M_SYS_CFG	0	0	0	1	1	0	1	#13 (0Dh)	Read and Write	Section 17.14
M_TSD_CFG	0	0	0	1	1	1	0	#14 (0Eh)	Read and Write	Section 17.15
M_REG_CFG	0	0	0	1	1	1	1	#15 (0Fh)	Read and Write	Section 17.16
M_WIO_CFG	0	0	1	0	0	0	0	#16 (10h)	Read and Write	Section 17.17
M_REG_CTRL1	0	0	1	0	0	0	1	#17 (11h)	Read and write	Section 17.18
M_REG_CTRL2	0	0	1	0	0	1	0	#18 (12h)	Write Only	Section 17.19
M_AMUX_CTRL	0	0	1	0	0	1	1	#19 (13h)	Read and Write	Section 17.20
M_LDT_CFG1	0	0	1	0	1	0	0	#20 (14h)	Read and Write	Section 17.21
M_LDT_CFG2	0	0	1	0	1	0	1	#21 (15h)	Read and Write	Section 17.22
M_LDT_CFG3	0	0	1	0	1	1	0	#22 (16h)	Read and Write	Section 17.23
M_LDT_CTRL	0	0	1	0	1	1	1	#23 (17h)	Read and Write	Section 17.24
M_MEMORY0	0	0	1	1	0	0	0	#24 (18h)	Read and Write	Section 17.25
M_MEMORY1	0	0	1	1	0	0	1	#25 (19h)	Read and Write	Section 17.26

Table 16. Fail-safe SPI register map

Register	Address								Read/Write	Reference
	M/FS	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0	Hex		
FS_GRL_FLAGS	1	0	0	0	0	0	0	#26 (40h)	Read Only	Section 18.1
FS_I_OVUV_SAFE_ REACTION1	1	0	0	0	0	0	1	#27 (41h)	Write during Init phase, then Read only	Section 18.1
FS_I_NOT_OVUV_SAFE_ REACTION1	1	0	0	0	0	1	0	#28 (42h)	Write during Init phase, then Read only	
FS_I_OVUV_SAFE_ REACTION2	1	0	0	0	0	1	1	#29 (43h)	Write during Init phase, then Read only	Section 18.3
FS_I_NOT_OVUV_SAFE_ REACTION2	1	0	0	0	1	0	0	#30 (44h)	Write during Init phase, then Read only	
FS_I_WD_CFG	1	0	0	0	1	0	1	#31 (45h)	Write during Init phase, then Read only	Section 18.4
FS_I_NOT_WD_CFG	1	0	0	0	1	1	0	#32 (46h)	Write during Init phase, then Read only	
FS_I_SAFE_INPUTS	1	0	0	0	1	1	1	#33 (47h)	Write during Init phase, then Read only	Section 18.5
FS_I_NOT_SAFE_INPUTS	1	0	0	1	0	0	0	#34 (48h)	Write during Init phase, then Read only	
FS_I_FSSM	1	0	0	1	0	0	1	#35 (49h)	Write during Init phase, then Read only	Section 18.6

Table 16. Fail-safe SPI register map*...continued*

Register	Address								Read/Write	Reference
	M/FS	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0	Hex		
FS_I_NOT_FSSM	1	0	0	1	0	1	0	#36 (4Ah)	Write during Init phase, then Read only	
FS_WDW_DURATION	1	0	0	1	0	1	1	#37 (4Bh)	Read and Write	Section 18.7
FS_NOT_WDW_DURATION	1	0	0	1	1	0	0	#38 (4Ch)	Read and Write	
FS_WD_ANSWER	1	0	0	1	1	0	1	#39 (4Dh)	Write Only	Section 18.8
FS_WD_TOKEN	1	0	0	1	1	1	0	#40 (4Eh)	Read and Write	Section 18.9
FS_ABIST_ON_DEMAND	1	0	0	1	1	1	1	#41 (4Fh)	Read and Write	Section 18.10
FS_OVUV_REG_STATUS	1	0	1	0	0	0	0	#42 (50h)	Read and Write	Section 18.11
FS_RELEASE_FS0B_FS1B	1	0	1	0	0	0	1	#43 (51h)	Write Only	Section 18.12
FS_SAFE_IOS_1	1	0	1	0	0	1	0	#44 (52h)	Read and Write	Section 18.13
FS_SAFE_IOS_2	1	0	1	0	0	1	1	#45 (53h)	Read and Write	Section 18.14
FS_DIAG_SAFETY1	1	0	1	0	1	0	0	#46 (54h)	Read and Write	Section 18.15
FS_DIAG_SAFETY2	1	0	1	0	1	0	1	#47 (55h)	Read and Write	Section 18.16
FS_INTB_MASK	1	0	1	0	1	1	0	#48 (56h)	Read and Write	Section 18.17
FS_STATES	1	0	1	0	1	1	1	#49 (57h)	Read and Write	Section 18.18
FS_LP_REQ	1	0	1	1	0	0	0	#50 (58h)	Read and Write	Section 18.19
FS_LDT_LPSEL	1	0	1	1	0	0	1	#51 (59h)	Read and Write	Section 18.20

17 Main register mapping

17.1 M_DEVICEID (0x00)

Table 17. M_DEVICEID register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	FULL_LAYER_REV[2:0]			METAL_LAYER_REV[2:0]			FAM_ID[3:2]	
Reset	0	1	1	0	0	1	0	1

Bit	7	6	5	4	3	2	1	0
Read	FAM_ID[1:0]		DEV_ID[5:0]					
Reset	1	1	OTP	OTP	OTP	OTP	OTP	OTP

Table 18. M_DEVICEID register bit description

Bit	Symbol	Description
15 to 13	FULL_LAYER_REV[2:0]	Full Layer Mask revision
		000 Unused
		001 Pass A silicon
		010 Pass B silicon
		011 Pass C silicon
		100 Pass D silicon
		101 Pass E silicon
		110 Pass F silicon
		111 Pass G silicon
		Reset Condition: N/A
12 to 10	METAL_LAYER_REV[2:0]	Metal Mask revision
		000 Rev X.0 (Default full Layer revision)
		001 Rev X.1

Table 18. M_DEVICEID register bit description*...continued*

Bit	Symbol	Description
		010 Rev X.2
		011 Rev X.3
		100 Rev X.4
		101 Rev X.5
		110 Rev X.6
		111 Rev X.7
		Reset Condition: N/A
9 to 6	FAM_ID[3:0]	Device Family Identification
		0111 FS26 family Fixed on metal.
		Reset Condition: N/A
5 to 0	DEV_ID[5:0]	Device ID
		FS26 Version dependent
		OTP Fuse load

17.2 M_PROGID (0x01)

Table 19. M_PROGID register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	PROG_IDH[8:0]							
Reset	OTP							

Bit	7	6	5	4	3	2	1	0
Read	PROG_IDL[8:0]							
Reset	OTP							

Table 20. M_PROGID register bit description

Bit	Symbol	Description
15 to 8	PROG_IDH[8:0]	Higher byte to set the first letter for the OTP ID code (A-Z)
		Program ID dependent
		OTP Fuse load
7 to 0	PROG_IDL[8:0]	Lower byte to set the second letter for OTP ID code (A-Z)
		Program ID dependent
		OTP Fuse load

17.3 M_STATUS (0x02)

Table 21. M_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	TWARN_S	VDBG_ VOLT_S	VBSTFB_ ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	GPIO2_S	GPIO1_S
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	VREF_S	VBST_S	VPRE_S	TRK2_S	TRK1_S	CORE_S	LDO2_S	LDO1_S
Reset	0	0	0	0	0	0	0	0

Table 22. M_STATUS register bit description

Bit	Symbol	Description
15	TWARN_S	Real-time status of Thermal Warning flag
		0 T_J is below T_{WARN} threshold
		1 T_J is above T_{WARN} threshold
		Real-time information
14	VDBG_VOLT_S	Real-time status of MCU FLASH MODE
		0 Debug pin voltage < V_{NORM_MAX} (1.8 V)
		1 Debug pin voltage > V_{DBG_MIN} (2.5 V)
		Real-time information
13	VBSTFB_ ACTIVE_S	Real-time status of VBST switching status
		0 VBST LX node is not switching
		1 VBST LX node is switching
		Real-time information
12	VBSTFB_UV_S	Real-time status of VBST_FB pin
		0 VSBT_FB below $V_{BST\_UV\_TH}$
		1 VSBT_FB above $V_{BST\_UV\_TH}$
		Real-time information
11	WK2_S	Real-time status of WAKE2 pin
		0 WAKE2 is low
		1 WAKE2 is high
		Real-time information
10	WK1_S	Real-time status of WAKE1 pin
		0 WAKE1 is low
		1 WAKE1 is high
		Real-time information
9	GPIO2_S	GPIO2 pin status
		0 GPIO2 is low
		1 GPIO2 is high
		Real-time information
8	GPIO1_S	GPIO1 pin status
		0 GPIO1 is low
		1 GPIO1 is high
		Real-time information
7	VREF_S	Real time status of VREF Regulator
		0 VREF is Disabled
		1 VREF is Enabled
		Real-time information
6	VBST_S	Real time status of VBST Regulator
		0 VBST is Disabled
		1 VBST is Enabled
		Real-time information
5	VPRE_S	Real time status of VPRE Regulator
		0 VPRE is Disabled
		1 VPRE is Enabled
		Real-time information
4	TRK2_S	Real time status of TRK2 Regulator

Table 22. M_STATUS register bit description*...continued*

Bit	Symbol	Description
		0 TRK2 is Disabled
		1 TRK2 is Enabled
		Real-time information
3	TRK1_S	Real time status of TRK1 Regulator
		0 TRK1 is Disabled
		1 TRK1 is Enabled
		Real-time information
2	CORE_S	Real time status of VCORE Regulator
		0 VCORE is Disabled
		1 VCORE is Enabled
		Real-time information
1	LDO2_S	Real time status of LDO2 Regulator
		0 LDO2 is Disabled
		1 LDO2 is Enabled
		Real-time information
0	LDO1_S	Real time Status of LDO1 Regulator
		0 LDO1 is Disabled
		1 LDO1 is Enabled
		Real-time information

17.4 M_TSD_FLG (0x03)

Table 23. M_TSD_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	TWARN_I	0	0	0	0	0	0	0
Read	TWARN_I	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Read	0	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
Reset	0	0	0	0	0	0	0	0

Table 24. M_TSD_FLG register bit description

Bit	Symbol	Description
15	TWARN_I	Central Temp sensor has crossed the Thermal warning threshold on the rising edge
		0 No Thermal warning detected
		1 Thermal warning occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
6	GPIO1TSD_I	Interrupt flag when GPIO1 Thermal shutdown event occurs
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
5	VPRETSD_I	Interrupt flag when VPRE Thermal shutdown event occurs

Table 24. M_TSD_FLG register bit description*...continued*

Bit	Symbol	Description
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
4	TRK2TSD_I	Interrupt flag when TRK2 Thermal shutdown event occurs
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
3	TRK1TSD_I	Interrupt flag when TRK1 Thermal shutdown event occurs
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
2	CORETSD_I	Interrupt flag when VCORE Thermal shutdown event occurs
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
1	LDO2TSD_I	Interrupt flag when LDO2 Thermal shutdown event occurs
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write write '1')
0	LDO1TSD_I	Interrupt flag when LDO1 Thermal shutdown event occurs
		0 No Thermal Shutdown event detected
		1 Thermal Shutdown event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')

17.5 M_TSD_MSK (0x04)

Table 25. M_TSD_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	TWARN_M	0	0	0	0	0	0	0
Read	TWARN_M	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
Read	0	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
Reset	0	0	0	0	0	0	0	0

Table 26. M_TSD_MSK register bit description (default value in bold)

Bit	Symbol	Description
15	TWARN_M	Inhibit Interrupt when a Thermal warning occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
6	GPIO1TSD_M	Inhibit Interrupt when GPIO1 Thermal Shutdown occurs

Table 26. M_TSD_MSK register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
5	VPRETSD_M	Inhibit Interrupt when VPRE Thermal Shutdown occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
4	TRK2TSD_M	Inhibit Interrupt when TRK2 Thermal Shutdown occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
3	TRK1TSD_M	Inhibit Interrupt when TRK1 Thermal Shutdown occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
2	CORETSD_M	Inhibit Interrupt when VCORE Thermal Shutdown occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
1	LDO2TSD_M	Inhibit Interrupt when LDO2 Thermal Shutdown occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
0	LDO1TSD_M	Inhibit Interrupt when LDO1 Thermal Shutdown occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)

17.6 M_REG_FLG (0x05)

Table 27. M_REG_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	VBSTOV_I
Read	0	0	0	0	0	0	0	VBSTOV_I
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I
Read	VPREUVH_I	VBSTOC_I	VPREOC_I	TRK2OC_I	TRK1OC_I	COREOC_I	LDO2OC_I	LDO1OC_I
Reset	0	0	0	0	0	0	0	0

Table 28. M_REG_FLG register bit description

Bit	Symbol	Description
8	VBSTOV_I	Interrupt flag when VBST_FB has crossed overvoltage threshold
		0 V_{BST} has not crossed $V_{BST\_OV\_TH}$ threshold
		1 V_{BST} crossed $V_{BST\_OV\_TH}$ threshold

Table 28. M_REG_FLG register bit description*...continued*

Bit	Symbol	Description
		Reset on Power on Reset (POR) or Clear on Write (write '1')
7	VPREUVH_I	Interrupt flag when VPRE crosses UVH threshold on the falling edge
		0 VPRE has not crossed V_{PRE_UVH} threshold
		1 VPRE crossed V_{PRE_UVH} threshold
		Reset on Power on Reset (POR) or Clear on Write (write '1')
6	VBSTOC_I	Interrupt flag when VBST overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')
5	VPREOC_I	Interrupt flag when VPRE overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')
4	TRK2OC_I	Interrupt flag when TRK2 overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')
3	TRK1OC_I	Interrupt flag when TRK1 Overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')
2	COREOC_I	Interrupt flag when VCORE Overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')
1	LDO2OC_I	Interrupt flag when LDO2 Overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')
0	LDO1OC_I	Interrupt flag when LDO1 Overcurrent event occurs
		0 No Overcurrent event detected
		1 Overcurrent event occurred
		Reset on Power on Reset (POR) or Clear on Write (write '1')

17.7 M_REG_MSK (0x06)

Table 29. M_REG_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	VBSTOV_M
Read	0	0	0	0	0	0	0	VBSTOV_M
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Read	VPREUVH_M	VBSTOC_M	VPREOC_M	TRK2OC_M	TRK1OC_M	COREOC_M	LDO2OC_M	LDO1OC_M
Reset	0	0	0	0	0	0	0	0

Table 30. M_REG_MSK register bit description (default value in bold)

Bit	Symbol	Description
8	VBSTOV_M	Inhibit Interrupt when VBST Overvoltage event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
7	VPREUVH_M	Inhibit Interrupt when VPRE Undervoltage event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
6	VBSTOC_M	Inhibit Interrupt when VBST Overcurrent event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
5	VPREOC_M	Inhibit Interrupt when VPRE Overcurrent event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
4	TRK2OC_M	Inhibit Interrupt when TRK2 Overcurrent event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
3	TRK1OC_M	Inhibit Interrupt when TRK1 Overcurrent event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
2	COREOC_M	Inhibit Interrupt when VCORE Overcurrent event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
1	LDO2OC_M	Inhibit Interrupt when LDO2 Overcurrent event occurs
		0 Interrupt NOT MASKED

Table 30. M_REG_MSK register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
0	LDO1OC_M	Inhibit Interrupt when LDO1 Overcurrent event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)

17.8 M_VSUP_FLG (0x07)

Table 31. M_VSUP_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Read	0	0	0	0	VBOSUVH_I	VSUPOV_I	VSUPUV6_I	VSUPUVH_I
Reset	0	0	0	0	0	0	0	0

Table 32. M_VSUP_FLG register bit description

Bit	Symbol	Description
3	VBOSUVH_I	Interrupt flag when VBOS has crossed its UVH threshold on the falling edge
		0 No VBOS_UVH event detected
		1 VBOS_UVH event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
2	VSUPOV_I	Interrupt flag when VSUP has crossed its OV threshold on the rising edge
		0 No VSUP_OV event detected
		1 VSUP_OV event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
1	VSUPUV6_I	Interrupt flag when VSUP has crossed its V_{SUPUV6} threshold on the falling edge
		0 No VSUP_UV6 event detected
		1 VSUP_UV6 event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')
0	VSUPUVH_I	Interrupt flag when VSUP has crossed its UVH threshold on the falling edge
		0 No VSUP_UVH event detected
		1 VSUP_UVH event occurred
		Reset on Power on Reset (POR) or clear on Write (write '1')

17.9 M_VSUP_MSK (0x08)

Table 33. M_VSUP_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Read	0	0	0	0	VBOSUVH_M	VSUPOV_M	VSUPUV6_M	VSUPUVH_M
Reset	0	0	0	0	0	0	0	0

Table 34. M_VSUP_MSK register bit description (default value in bold)

Bit	Symbol	Description
3	VBOSUVH_M	Inhibit Interrupt when VBOS UVH event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
2	VSUPOV_M	Inhibit Interrupt when VSUP Overvoltage event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
1	VSUPUV6_M	Inhibit Interrupt when VSUP UV6 event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
0	VSUPUVH_M	Inhibit Interrupt when VSUP_UVH event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)

17.10 M_WIO_FLG (0x09)

Table 35. M_WIO_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WU_CLR	0	0	0	0	0	0	0
Read	0	0	0	0	WUEVENT[3:0]			
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read	0	0	0	LDT_I	GPIO2_I	GPIO1_I	WK2_I	WK1_I
Reset	0	0	0	0	0	0	0	0

Table 36. M_WIO_FLG register bit description

Bit	Symbol	Description
15	WU_CLR	Clear wake-up flags
		0 Do nothing
		1 Clear all wake-up flags
		Reset on Power on Reset (POR), Self-clear
11 to 8	WUEVENT[3:0]	Wake-up Event Source
		0000 No Wake up detected
		0001 WAKE1
		0010 WAKE2
		0011 GPIO1
		0100 GPIO2
		0101 LDT expired
		0110 SPI activity
		1000 DFS Recovery
		1111 BATTERY fail: Reports when the device has lost valid VSUP and Main state machine is reset.
		Reset on Power on Reset (POR), Go to LP Modes or WU_CLR write "1"
4	LDT_I	LDT event Flag
		0 No event on LDT
		1 LDT Expire Event has occurred
		Reset on Power on Reset (POR), Go to LP modes or WU_CLR write "1"
3	GPIO2_I	GPIO2 event Flag
		0 No event on GPIO2
		1 Event on GPIO2 has occurred
		Reset on Power on Reset (POR), Go to LP modes or WU_CLR write "1"
2	GPIO1_I	GPIO1 event Flag
		0 No event on GPIO1
		1 Event on GPIO1 has occurred
		Reset on Power on Reset (POR), Go to LP modes or WU_CLR write "1"
1	WK2_I	WAKE2 event Flag
		0 No event on WAKE2
		1 Event on WAKE2 has occurred
		Reset on Power on Reset (POR), Go to LP modes or WU_CLR write "1"
0	WK1_I	WAKE1 event Flag
		0 No event on WAKE1
		1 Event on WAKE1 has occurred
		Reset on Power on Reset (POR), Go to LP modes or WU_CLR write "1"

17.11 M_WIO_MSK (0x0A)

Table 37. M_WIO_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	LDT_M	GPIO2_M	GPIO1_M	WK2_M	WK1_M
Read	0	0	0	LDT_M	GPIO2_M	GPIO1_M	WK2_M	WK1_M
Reset	0	0	0	0	0	0	0	0

Table 38. M_WIO_MSK register bit description (default value in bold)

Bit	Symbol	Description
4	LDT_M	Inhibit Interrupt if LDT event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
3	GPIO2_M	Inhibit Interrupt when GPIO2 event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
2	GPIO1_M	Inhibit Interrupt when GPIO1 event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
1	WK2_M	Inhibit Interrupt when WAKE2 event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
0	WK1_M	Inhibit interrupt when WAKE1 event occurs
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)

17.12 M_COM_FLG (0x0B)

Table 39. M_COM_FLG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Read	0	0	0	0	0	MSPI_CRC_I	MSPI_CLK_I	MSPI_REQ_I
Reset	0	0	0	0	0	0	0	0

Table 40. M_COM_FLG register bit description

Bit	Symbol	Description
2	MSPI_CRC_I	Interrupt flag when the Main SPI CRC calculation is incorrect
		0 Interrupt not detected
		1 Interrupt detected
		Reset on Power on Reset (POR), or Clear on Write (write'1)
1	MSPI_CLK_I	Interrupt flag when the Main SPI clock provides wrong number of clock pulses
		0 Interrupt not detected
		1 Interrupt detected
		Reset on Power on Reset (POR), or Clear on Write (write'1)
0	MSPI_REQ_I	Interrupt flag when the MCU writes to an invalid register in the Main domain
		0 Interrupt not detected
		1 Interrupt detected
		Reset on Power on Reset (POR), or Clear on Write (write'1)

17.13 M_COM_MSK (0x0C)

Table 41. M_COM_MSK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Read	0	0	0	0	0	MSPI_CRC_M	MSPI_CLK_M	MSPI_REQ_M
Reset	0	0	0	0	0	0	0	0

Table 42. M_COM_MSK register bit description (default value in bold)

Bit	Symbol	Description
2	MSPI_CRC_M	Inhibit Interrupt when the Main calculation is incorrect
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
1	MSPI_CLK_M	Inhibit Interrupt when the SPI clock provides wrong number of clock pulses
		0 Interrupt NOT MASKED
		1 Interrupt MASKED
		Reset on Power on Reset (POR)
0	MSPI_REQ_M	Inhibit Interrupt when the MCU writes to invalid register
		0 Interrupt NOT MASKED

Table 42. M_COM_MSK register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		1 Interrupt MASKED
		Reset on Power on Reset (POR)

17.14 M_SYS_CFG (0x0D)

Table 43. M_SYS_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RETRY_CNT[7:0]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	RETRY_CLR	0	0	INTB_TEST	INT_PWIDTH	FSS_FMOD	0	FSS_EN
Read	0	0	0	0	INT_PWIDTH	FSS_FMOD	0	FSS_EN
Reset	0	0	0	0	0	0	0	0

Table 44. M_SYS_CFG register bit description (default value in bold)

Bit	Symbol	Description
15 to 8	RETRY_CNT[7:0]	Retry counter time (ms)
		0000 0000 100
		0001 0000 200
		0010 0000 400
		0011 0000 800
		0100 0000 1600
		0101 0000 3200
		0110 0000 6400
		0111 0000 12800
		1000 0000 25600
		1001 0000 51200
		1010 0000 102400
		1011 0000 204800
		1100 0000 409600
		1101 0000 819200
		1110 0000 1638400
		1111 0000 3276800
		Reset on Power on Reset (POR) or RETRY_CLR Write "1"
7	RETRY_CLR	Clear Retry Counter
		0 No effect
		1 Clear Retry Counter
		Reset on Power on Reset (POR), Self-clear
4	INTB_TEST	Manual Test of INTB pin
		0 No effect
		1 Enable manual test. Generate a pulse of INT_PWIDTH duration at INTB pin for test purpose.

Table 44. M_SYS_CFG register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		Reset on Power on Reset (POR), Self-clear
3	INT_PWIDTH	INTB Test pulse width
		0 25 µs
		1 100 µs
		Reset on Power on Reset (POR)
2	FSS_FMOD	Frequency modulation during FSS Operation
		0 High Frequency Oscillator divided by 896
		1 High Frequency Oscillator divided by 224
		Reset on Power on Reset (POR)
0	FSS_EN	Frequency Spread Spectrum enable
		0 FSS is Disabled
		1 FSS is Enabled
		Reset on Power on Reset (POR)

17.15 M_TSD_CFG (0x0E)

Table 45. M_TSD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	VPRETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Read	0	0	VPRETDFS	TRK2TDFS	TRK1TDFS	CORETDFS	LDO2TDFS	LDO1TDFS
Reset	0	0	OTP	OTP	OTP	OTP	OTP	OTP

Table 46. M_TSD_CFG register bit description

Bit	Symbol	Description
5	VPRETDFS	Deep Fail-Safe request in case of VPRE Thermal Shutdown
		0 Regulator disabled
		1 Transition to DFS
		OTP Fuse Load
4	TRK2TDFS	Deep Fail-Safe request in case of TRK2 Thermal Shutdown
		0 Regulator disabled
		1 Transition to DFS
		OTP Fuse Load
3	TRK1TDFS	Deep Fail-Safe request in case of TRK1 Thermal Shutdown
		0 Regulator disabled
		1 Transition to DFS
		OTP Fuse Load
2	CORETDFS	Deep Fail-Safe request in case of VCORE Thermal Shutdown
		0 Regulator disabled

Table 46. M_TSD_CFG register bit description*...continued*

Bit	Symbol	Description
		1 Transition to DFS
		OTP Fuse Load
1	LDO2TDFS	Deep Fail-Safe request in case of LDO2 Thermal Shutdown
		0 Regulator disabled
		1 Transition to DFS
		OTP Fuse Load
0	LDO1TDFS	Deep Fail-Safe request in case of LDO1 Thermal Shutdown
		0 Regulator disabled
		1 Transition to DFS
		OTP Fuse Load

17.16 M_REG_CFG (0x0F)

Table 47. M_REG_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	VREF_PD	VBST_TMD
Read	0	0	0	0	0	0	VREF_PD	VBST_TMD
Reset	0	0	0	0	0	0	1	0

Table 48. M_REG_CFG register bit description (default value in bold)

Bit	Symbol	Description
1	VREF_PD	VREF Internal pulldown configuration (R_{REF_DIS})
		0 Disable internal pulldown when VREF output is disabled
		1 Enable internal pulldown when VREF output is disabled
		Reset on Power on Reset (POR)
0	VBST_TMD	VBST output verification mode
		0 VBST output is regulated to the configured voltage set by OTP
		1 VBST regulate to 17 V to verify availability
		Reset on Power on Reset (POR)

17.17 M_WIO_CFG (0x10)

Table 49. M_WIO_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	GPIO2 WUPOL	GPIO1 WUPOL	WAKE2POL	WAKE1POL
Read	0	0	0	0	GPIO2 WUPOL	GPIO1 WUPOL	WAKE2POL	WAKE1POL
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	CSBWUEN	LDTWUEN	GPIO2WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
Read	0	0	CSBWUEN	LDTWUEN	GPIO2WUEN	GPIO1WUEN	WK2WUEN	WK1WUEN
Reset	0	0	0	0	0	0	0	0

Table 50. M_WIO_CFG register bit description (default value in bold)

Bit	Symbol	Description
11	GPIO2WUPOL	GPIO2 event detection polarity
		0 High level on GPIO2 will wake up the part
		1 Low level on GPIO2 will wake up the part
		Reset on Power on Reset (POR)
10	GPIO1WUPOL	GPIO1 event detection polarity
		0 High level on GPIO1 will wake up the part
		1 Low level on GPIO1 will wake up the part
		Reset on Power on Reset (POR)
9	WAKE2POL	WAKE2 event detection polarity
		0 High level on WAKE2 will wake up the part
		1 Low level on WAKE2 will wake up the part
		Reset on Power on Reset (POR)
8	WAKE1POL	WAKE1 event detection polarity
		0 High level on WAKE1 will wake up the part
		1 Low level on WAKE1 will wake up the part
		Reset on Power on Reset (POR)
5	CSBWUEN	CSB Transition wake-up enabled
		0 Disabled
		1 Enabled
		Reset on Power on Reset (POR)
4	LDTWUEN	Long Duration Timer wake-up enabled
		0 Disabled
		1 Enabled
		Reset on Power on Reset (POR)
3	GPIO2WUEN	GPIO2 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on Power on Reset (POR)
2	GPIO1WUEN	GPIO1 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on Power on Reset (POR)
1	WK2WUEN	WAKE2 wake-up enabled
		0 Disabled
		1 Enabled
		Reset on Power on Reset (POR)
0	WK1WUEN	WAKE1 wake-up enabled
		0 Disabled
		1 Enabled

Table 50. M_WIO_CFG register bit description (default value in bold)...*continued*

Bit	Symbol	Description
		Reset on Power on Reset (POR)

17.18 M_REG_CTRL1 (0x11)

Table 51. M_REG_CTRL1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	GPIO2LP_ON	GPIO1LP_ON	0	0	GPIO2HI	GPIO1HI
Read	0	0	GPIO2LP_ON	GPIO1LP_ON	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VREFEN	VBSTEN	0	TRK2EN	TRK1EN	COREEN	LDO2EN	LDO1EN
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 52. M_REG_CTRL1 register bit description

Bit	Symbol	Description
13	GPIO2LP_ON	Configure GPIO2 state in STANDBY mode
		0 Follow the power down slot configuration
		1 Keep GPIO2 in the same state as it was in NORMAL mode
		Reset on Power on Reset (POR),
12	GPIO1LP_ON	Configure GPIO1 state in STANDBY mode
		0 Follow the power down slot configuration
		1 Keep GPIO1 in the same state as it was in NORMAL mode
		Reset on Power on Reset (POR),
9	GPIO2HI	Request GPIO2 pin High
		0 No effect (GPIO2 remains in current state)
		1 GPIO2 set high
		Reset on Power on Reset (POR), Self-cleared
8	GPIO1HI	Request GPIO1 pin High
		0 No effect (GPIO1 remains in current state)
		1 GPIO1 set high
		Reset on Power on Reset (POR), Self-cleared
7	VREFEN	VREF Enable request
		0 No effect (Regulator remain in its current state)
		1 VREF Enable request
		Reset on Power on Reset (POR), Self-cleared
6	VBSTEN	VBST Enable request
		0 No effect (Regulator remain in its current state)
		1 VBST Enable request
		Reset on Power on Reset (POR), Self-cleared
4	TRK2EN	TRK2 Enable request
		0 No effect (Regulator remain in its current state)

Table 52. M_REG_CTRL1 register bit description*...continued*

Bit	Symbol	Description
		1 TRK2 Enable request
		Reset on Power on Reset (POR), Self-cleared
3	TRK1EN	TRK1 Enable request
		0 No effect (Regulator remain in its current state)
		1 TRK1 Enable request
		Reset on Power on Reset (POR), Self-cleared
2	COREEN	VCORE Enable request
		0 No effect (Regulator remain in its current state)
		1 VCORE Enable request
		Reset on Power on Reset (POR), Self-cleared
1	LDO2EN	LDO2 Enable request
		0 No effect (Regulator remain in its current state)
		1 LDO2 Enable request
		Reset on Power on Reset (POR), Self-cleared
0	LDO1EN	LDO1 Enable request
		0 No effect (Regulator remain in its current state)
		1 LDO1 Enable request
		Reset on Power on Reset (POR), Self-cleared

17.19 M_REG_CTRL2 (0x12)

Table 53. M_REG_CTRL2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	GPIO2LO	GPIO1LO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	VREFDIS	VBSTDIS	0	TRK2DIS	TRK1DIS	COREDIS	LDO2DIS	LDO1DIS
Reset	0	0	0	0	0	0	0	0

Table 54. M_REG_CTRL2 register bit description

Bit	Symbol	Description
9	GPIO2LO	Request GPIO2 pin Low
		0 No effect (GPIO2 remains in current state)
		1 GPIO2 set low
		Reset on Power on Reset (POR), Self-cleared
8	GPIO1LO	Request GPIO1 pin Low
		0 No effect (GPIO1 remains in current state)
		1 GPIO1 set low
		Reset on Power on Reset (POR), Self-cleared
7	VREFDIS	VREF Disable request
		0 No effect (Regulator remain in its current state)
		1 VREF Disable request

Table 54. M_REG_CTRL2 register bit description*...continued*

Bit	Symbol	Description
		Reset on Power on Reset (POR), Self-cleared
6	VBSTDIS	VBST Disable request
		0 No effect (Regulator remain in its current state)
		1 VBST Disable request
		Reset on Power on Reset (POR), Self-cleared
4	TRK2DIS	TRK2 Disable request
		0 No effect (Regulator remain in its current state)
		1 TRK2 Disable request
		Reset on Power on Reset (POR), Self-cleared
3	TRK1DIS	TRK1 Disable request
		0 No effect (Regulator remain in its current state)
		1 TRK1 Disable request
		Reset on Power on Reset (POR), Self-cleared
2	COREDIS	VCORE Disable request
		0 No effect (Regulator remain in its current state)
		1 VCORE Disable request
		Reset on Power on Reset (POR), Self-cleared
1	LDO2DIS	LDO2 Disable request
		0 No effect (Regulator remain in its current state)
		1 LDO2 Disable request
		Reset on Power on Reset (POR), Self-cleared
0	LDO1DIS	LDO1 Disable request
		0 No effect (Regulator remain in its current state)
		1 LDO1 Disable request
		Reset on Power on Reset (POR), Self-cleared

17.20 M_AMUX_CTRL (0x13)

Table 55. M_AMUX_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	AMUX_EN	AMUX_DIV	AMUX[4:0]				
Read	0	AMUX_EN	AMUX_DIV	AMUX[4:0]				
Reset	0	0	0	0	0	0	0	0

Table 56. M_AMUX_CTRL register bit description (default value in bold)

Bit	Symbol	Description
6	AMUX_EN	Enable AMUX block
		0 Disable AMUX block and pin is pulled down to ground

Table 56. M_AMUX_CTRL register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		1 Enable AMUX block
		Reset on Power on Reset (POR), Go to Low Power Mode, Go to Standby Mode
5	AMUX_DIV	Selection of divider ratio
		0 Divider ratio option 0 (ratio = 7.5). See Table 130
		1 Divider ratio option 1 (ratio = 14). See Table Table 130
		Reset on Power on Reset (POR)
4 to 0	AMUX[4:0]	AMUX Input Channel Selection
		00000 Disabled with AMUX pin in Hi-Z
		00001 Low Power Bandgap1
		00010 Main Bandgap2
		00011 Fail Safe Bandgap
		00100 V_{ANA}: Internal Main analog voltage supply
		00101 V_{DIG}: internal Main digital voltage supply
		00110 V_{DIG_FS}: internal Fail Safe digital voltage supply
		00111 VCORE Voltage
		01000 VPRE voltage
		01001 LDO1 voltage
		01010 LDO2 voltage
		01011 VREF voltage
		01100 TRK1 voltage
		01101 TRK2 voltage
		01110 VDDIO voltage
		01111 VBOS internal voltage
		10000 VBST voltage (divider ratio configurable by SPI)
		10001 VSUP voltage (divider ratio configurable by SPI)
		10010 WAKE1 voltage (divider ratio configurable by SPI)
		10011 WAKE2 voltage (divider ratio configurable by SPI)
		10100 GPIO1 voltage (divider ratio configurable by SPI)
		10101 GPIO2 voltage (divider ratio configurable by SPI)
		10110 BATSENSE voltage (divider ratio configurable by SPI)
		10111 Die Temperature Sensor T (°C) = (V_{AMUX} – V_{TEMP25}) / V_{TEMP_COEFF} + 25
		11000 VCORE Temperature sensor
		11001 VPRE Temperature sensor
		11010 LDO1 Temperature sensor
		11011 LDO2 Temperature sensor
		11100 TRK1 Temperature sensor
		11101 TRK2 Temperature sensor
		11110 GPIO1 Temperature sensor
		11111 Reserved
		Reset on Power on Reset (POR)

17.21 M_LDT_CFG1 (0x14)

Table 57. M_LDT_CFG1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_AFTER_RUN[15:8]							
Read	LDT_AFTER_RUN[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_AFTER_RUN[7:0]							
Read	LDT_AFTER_RUN[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 58. M_LDT_CFG1 register bit description

Bit	Symbol	Description
15 to 0	LDT_AFTER_RUN[15:0]	After running LDT Timer
		LDT timer value in NORMAL mode
		Reset on Power on Reset (POR), LDT Count started

17.22 M_LDT_CFG2 (0x15)

Table 59. M_LDT_CFG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LDT_WUP_L[15:8]							
Read	LDT_WUP_L[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_L[7:0]							
Read	LDT_WUP_L[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 60. M_LDT_CFG2 register bit description

Bit	Symbol	Description
15 to 0	LDT_WUP_L[15:0]	16 less significant bits of Wake-up with Long Duration Timer
		16 less significant bits for the wake up with the Long Duration Timer
		Reset on Power on Reset (POR), LDT Count started

17.23 M_LDT_CFG3 (0x16)

Table 61. M_LDT_CFG3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0

Table 61. M_LDT_CFG3 register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	LDT_WUP_H[7:0]							
Read	LDT_WUP_H[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 62. M_LDT_CFG3 register bit description

Bit	Symbol	Description
7 to 0	LDT_WUP_H[7:0]	8 more significant bits of Long Duration Timer Wake-up Timer
		8 most significant bit for the wake up with the Long Duration Timer
		Reset on Power on Reset (POR), LDT Count started

17.24 M_LDT_CTRL (0x17)

Table 63. M_LDT_CTRL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	LDT_FNCT[2:0]			LDT_SEL	LDT_MODE	LDT_EN	0
Read	0	LDT_FNCT[2:0]			LDT_SEL	LDT_MODE	LDT_EN	LDT_RUN
Reset	0	0	0	0	0	0	0	0

Table 64. M_LDT_CTRL register bit description (default value in bold)

Bit	Symbol	Description
6 to 4	LDT_FNCT[2:0]	LDT function selection
		000 Function1 (see Section 21.4.2)
		001 Function 2 (see Section 21.4.2)
		010 Function 3 (see Section 21.4.2)
		011 Function 4 (see Section 21.4.2)
		100 Function 5 (see Section 21.4.2)
		101 Reserved (see Section 21.4.2)
		110 Reserved (see Section 21.4.2)
		111 Reserved (see Section 21.4.2)
		Reset on Power on Reset (POR)
3	LDT_SEL	LDT timer read selection
		0 Read/Sets Target value of Wake-up LDT timer
		1 Read real time value of 24-bit Timer

Table 64. M_LDT_CTRL register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		Reset on Power on Reset (POR)
2	LDT_MODE	Set operation mode
		0 Set LDT to long count
		1 Set LDT to short count
		Reset on Power on Reset (POR)
1	LDT_EN	Start LDT Timer operation
		0 Disable LDT
		1 LDT starts counting
		Reset on Power on Reset (POR)
0	LDT_RUN	LDT Status
		0 LDT is disabled or not counting
		1 LDT is Enabled and count is in progress
		Reset on Power on Reset (POR), LDT stopped

17.25 M_MEMORY0 (0x18)

Table 65. M_MEMORY0 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEM0[15:8]							
Read	MEM0[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	MEM0[7:0]							
Read	MEM0[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 66. M_MEMORY0 register bit description

Bit	Symbol	Description
15 to 0	MEM0[15:0]	Free 16 bits for application data storage
		MEM0 stored data
		Reset on Power on Reset (POR)

17.26 M_MEMORY1 (0x19)

Table 67. M_MEMORY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MEM1[15:8]							
Read	MEM1[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	MEM1[7:0]							
Read	MEM1[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 68. M_MEMORY1 register bit description

Bit	Symbol	Description
15 to 0	MEM1[15:0]	Free 16 bits for application data storage
		MEM1 stored data
		Reset on Power on Reset (POR)

18 Fail-safe register mapping

18.1 FS_GRL_FLAGS (0x40)

Table 69. FS_GRL_FLAGS register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	FS_BIST_G	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 70. FS_GRL_FLAGS register bit description

Bit	Symbol	Description
15	FS_COM_G	Report an issue in the communication (SPI)
		0 No Failure
		1 Failure
		Reset on Power On Reset (POR), cleared when all individual bits are cleared
		Source register: FS_DIAG_SAFETY1
		Flags Reporting: SPI_FS_CLK, SPI_FS_REQ, SPI_FS_CRC
14	FS_WD_G	Report an issue on the Watchdog Refresh
		0 No Failure
		1 Failure
		Reset on Power On Reset (POR), cleared when all individual bits are cleared
		Source register: FS_DIAG_SAFETY1
		Flags Reporting: BAD_WD_DATA, BAD_WD_TIMING
13	FS_IO_G	Report an issue in one of the Fail Safe IOs
		0 No Failure
		1 Failure
		Reset on Power On Reset (POR), cleared when all individual bits are cleared
		Source register: FS_SAFE_IOS_1
		Flags Reporting: RSTB_DIAG, FS0B_DIAG, FS1B_DIAG

Table 70. FS_GRL_FLAGS register bit description*...continued*

Bit	Symbol	Description
12	FS_REG_ OVUV_G	Report an issue on one of the voltage monitoring (OV or UV)
		0 No Failure
		1 Failure
		Reset on Power On Reset (POR), cleared when all individual bits are cleared
		Source register: FS_OVUV_REG_STATUS
		Flags Reporting: VPRE_OV, VPRE_UV, CORE_OV, CORE_UV, LDO1_OV, LDO1_UV, LDO2_OV, LDO2_UV, TRK1_OV, TRK1_UV, TRK2_OV, TRK2_UV, REF_OV, REF_UV, EXT_OV, EXT_UV
11	FS_BIST_G	Report an issue on BIST (Logical or Analog)
		0 No Failure
		1 Failure
		Reset on Power On Reset (POR), cleared when all individual bits are cleared
		Source register: FS_DIAG_SAFETY1
		Flags Reporting: ABIST1_PASS, ABIST2_PASS, LBIST_STATUS[1:0]

18.2 FS_I_OVUV_SAFE_REACTION1 (0x41)

Table 71. FS_I_OVUV_SAFE_REACTION1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON_PRE_OV_ FS_REACTION[1:0]		VMON_PRE_UV_ FS_REACTION[1:0]		VMON_CORE_OV_ FS_REACTION[1:0]		VMON_CORE_UV_ FS_REACTION[1:0]	
Read	VMON_PRE_OV_ FS_REACTION[1:0]		VMON_PRE_UV_ FS_REACTION[1:0]		VMON_CORE_OV_ FS_REACTION[1:0]		VMON_CORE_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Bit	7	6	5	4	3	2	1	0
Write	VMON_LDO1_OV_ FS_REACTION[1:0]		VMON_LDO1_UV_ FS_REACTION[1:0]		VMON_LDO2_OV_ FS_REACTION[1:0]		VMON_LDO2_UV_ FS_REACTION[1:0]	
Read	VMON_LDO1_OV_ FS_REACTION[1:0]		VMON_LDO1_UV_ FS_REACTION[1:0]		VMON_LDO2_OV_ FS_REACTION[1:0]		VMON_LDO2_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Table 72. FS_I_OVUV_SAFE_REACTION1 register bit description (default value in bold)

Bit	Symbol	Description
15 to 14	VMON_PRE_OV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_ PRE
		00 No effect on RSTB and FS0B
		01 VMON_PRE OV asserts FS0B only
		10 VMON_PRE OV asserts RSTB and FS0B
		11 VMON_PRE OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
13 to 12	VMON_PRE_UV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_ PRE
		00 No effect on RSTB and FS0B
		01 VMON_PRE UV asserts FS0B only

Table 72. FS_I_OVUV_SAFE_REACTION1 register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		10 VMON_PRE UV asserts RSTB and FS0B
		11 VMON_PRE UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
11 to 10	VMON_CORE_OV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_CORE
		00 No effect on RSTB and FS0B
		01 VMON_CORE OV asserts FS0B only
		10 VMON_CORE OV asserts RSTB and FS0B
		11 VMON_CORE OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
9 to 8	VMON_CORE_UV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_CORE
		00 No effect on RSTB and FS0B
		01 VMON_CORE UV asserts FS0B only
		10 VMON_CORE UV asserts RSTB and FS0B
		11 VMON_CORE UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
7 to 6	VMON_LDO1_OV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_LDO1
		00 No effect on RSTB and FS0B
		01 VMON_LDO1 OV asserts FS0B only
		10 VMON_LDO1 OV asserts RSTB and FS0B
		11 VMON_LDO1 OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
5 to 4	VMON_LDO1_UV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_LDO1
		00 No effect on RSTB and FS0B
		01 VMON_LDO1 UV asserts FS0B only
		10 VMON_LDO1 UV asserts RSTB and FS0B
		11 VMON_LDO1 UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
3 to 2	VMON_LDO2_OV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_LDO2
		00 No effect on RSTB and FS0B
		01 VMON_LDO2 OV asserts FS0B only
		10 VMON_LDO2 OV asserts RSTB and FS0B
		11 VMON_LDO2 OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
1 to 0	VMON_LDO2_UV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_LDO2
		00 No effect on RSTB and FS0B
		01 VMON_LDO2 UV asserts FS0B only
		10 VMON_LDO2 UV asserts RSTB and FS0B
		11 VMON_LDO2 UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)

18.3 FS_I_OVUV_SAFE_REACTION2 (0x43)

Table 73. FS_I_OVUV_SAFE_REACTION2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON_EXT_OV_ FS_REACTION[1:0]		VMON_EXT_UV_ FS_REACTION[1:0]		VMON_REF_OV_ FS_REACTION[1:0]		VMON_REF_UV_ FS_REACTION[1:0]	
Read	VMON_EXT_OV_ FS_REACTION[1:0]		VMON_EXT_UV_ FS_REACTION[1:0]		VMON_REF_OV_ FS_REACTION[1:0]		VMON_REF_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Bit	7	6	5	4	3	2	1	0
Write	VMON_TRK2_OV_ FS_REACTION[1:0]		VMON_TRK2_UV_ FS_REACTION[1:0]		VMON_TRK1_OV_ FS_REACTION[1:0]		VMON_TRK1_UV_ FS_REACTION[1:0]	
Read	VMON_TRK2_OV_ FS_REACTION[1:0]		VMON_TRK2_UV_ FS_REACTION[1:0]		VMON_TRK1_OV_ FS_REACTION[1:0]		VMON_TRK1_UV_ FS_REACTION[1:0]	
Reset	1	0	0	1	1	0	0	1

Table 74. FS_I_OVUV_SAFE_REACTION2 register bit description (default value in bold)

Bit	Symbol	Description
15 to 14	VMON_EXT_OV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_EXT
		00 No effect on RSTB and FS0B
		01 VMON_EXT OV asserts FS0B only
		10 VMON_EXT OV asserts RSTB and FS0B
		11 VMON_EXT OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
13 to 12	VMON_EXT_UV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_EXT
		00 No effect on RSTB and FS0B
		01 VMON_EXT UV asserts FS0B only
		10 VMON_EXT UV asserts RSTB and FS0B
		11 VMON_EXT UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
11 to 10	VMON_REF_OV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_REF
		00 No effect on RSTB and FS0B
		01 VMON_REF OV asserts FS0B only
		10 VMON_REF OV asserts RSTB and FS0B
		11 VMON_REF OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
9 to 8	VMON_REF_UV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_REF
		00 No effect on RSTB and FS0B
		01 VMON_REF UV asserts FS0B only
		10 VMON_REF UV asserts RSTB and FS0B
		11 VMON_REF UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
7 to 6	VMON_TRK2_OV_ FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_TRK2
		00 No effect on RSTB and FS0B
		01 VMON_TRK2 OV asserts FS0B only

Table 74. FS_I_OVUV_SAFE_REACTION2 register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		10 VMON_TRK2 OV asserts RSTB and FS0B
		11 VMON_TRK2 OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
5 to 4	VMON_TRK2_UV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_TRK2
		00 No effect on RSTB and FS0B
		01 VMON_TRK2 UV asserts FS0B only
		10 VMON_TRK2 UV asserts RSTB and FS0B
		11 VMON_TRK2 UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
3 to 2	VMON_TRK1_OV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of OV detection on VMON_TRK1
		00 No effect on RSTB and FS0B
		01 VMON_TRK1 OV asserts FS0B only
		10 VMON_TRK1 OV asserts RSTB and FS0B
		11 VMON_TRK1 OV asserts RSTB and FS0B
		Reset on Power On Reset (POR)
1 to 0	VMON_TRK1_UV_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE outputs in case of UV detection on VMON_TRK1
		00 No effect on RSTB and FS0B
		01 VMON_TRK1 UV asserts FS0B only
		10 VMON_TRK1 UV asserts RSTB and FS0B
		11 VMON_TRK1 UV asserts RSTB and FS0B
		Reset on Power On Reset (POR)

18.4 FS_I_WD_CFG (0x45)

Table 75. FS_I_WD_CFG register bit allocation (default value in bold)

Bit	15	14	13	12	11	10	9	8
Write	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_REACTION[1:0]	
Read	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_REACTION[1:0]	
Reset	0	1	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read		WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0

Table 76. FS_I_WD_CFG register bit description (default value in bold)

Bit	Symbol	Description
15 to 14	WD_ERR_LIMIT[1:0]	WATCHDOG ERROR COUNTER CONFIGURATION
		00 8
		01 6
		10 4
		11 2

Table 76. FS_I_WD_CFG register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		Reset on Power On Reset (POR)
12 to 11	WD_RFR_LIMIT[1:0]	WATCHDOG REFRESH COUNTER CONFIGURATION
		00 6
		01 4
		10 2
		11 1
		Reset on Power On Reset (POR)
9 to 8	WD_FS_REACTION[1:0]	Reaction on RSTB or FAIL SAFE output in case of BAD Watchdog (data or timing)
		00 No action on RSTB and FS0B
		01 FS0B only is asserted low if WD Error counter value = WD_ERR_LIMIT[1:0]
		10 RSTB and FS0B are asserted low if WD Error counter value = WD_ERR_LIMIT[1:0]
		11 RSTB and FS0B are asserted low if WD Error counter value = WD_ERR_LIMIT[1:0]
		Reset on Power On Reset (POR)
6 to 4	WD_RFR_CNT[2:0]	Reflect the value of the Watchdog Refresh Counter
		000 0
		001 1
		010 2
		011 3
		100 4
		101 5
		110 6
		111 7
		Reset on Power On Reset (POR)
3 to 0	WD_ERR_CNT[3:0]	Reflect the value of the Watchdog Error Counter
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 9
		1010 10
		1011 11
		1100 12
		1101 12
		1110 12
		1111 12
		Reset on Power On Reset (POR)

18.5 FS_I_SAFE_INPUTS (0x47)

Table 77. FS_I_SAFE_INPUTS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FCCU_CFG[2:0]			FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	FCCU12_FS_ REACTION	FCCU1_FS_ REACTION
Read	FCCU_CFG[2:0]			FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	FCCU12_FS_ REACTION	FCCU1_FS_ REACTION
Reset	0	0	1	0	0	0	1	1

Bit	7	6(*)	5	4	3	2	1	0
Write	FCCU2_ FS_ REACTION	0	ERRMON_ FLT_ POLARITY	ERRMON_ ACK_TIME[1:0]		ERRMON_ FS_ REACTION	FCCU12_FILT[1:0]	
Read	FCCU2_ FS_ REACTION	0	ERRMON_ FLT_ POLARITY	ERRMON_ ACK_TIME[1:0]		ERRMON_ FS_ REACTION	FCCU12_FILT[1:0]	
Reset	1	0	0	0	1	1	0	1

(*) Bit 6 must be set to 1 in FS_I_NOT_SAFE_INPUTS (0x48)

Table 78. FS_I_SAFE_INPUTS register bit description (default value in bold)

Bit	Symbol	Description
15 to 13	FCCU_CFG[2:0]	FCCU MONITORING CONFIGURATION
		000 No monitoring
		001 FCCU1 and FCCU2 inputs monitoring activated by pair (BI-Stable protocol)
		010 FCCU1 and FCCU2 single input monitoring activated
		011 FCCU1 input monitoring only, FCCU2 input not used
		100 FCCU2 input monitoring only, FCCU1 input not used
		101 FCCU1 and FCCU2 single input PWM monitoring activated
		110 FCCU1 input PWM monitoring only, FCCU2 input level monitoring
		111 FCCU2 input PWM monitoring only, FCCU1 input level monitoring
		Reset on Power On Reset (POR)
12	FCCU12_FLT_POL	FCCU12 FAULT POLARITY
		0 FCCU1 = 0 or FCCU2 = 1 level is a fault
		1 FCCU1 = 1 or FCCU2 = 0 level is a fault
		Reset on Power On Reset (POR)
11	FCCU1_FLT_POL	FCCU1 FAULT POLARITY
		0 LOW LEVEL IS A FAULT
		1 HIGH LEVEL IS A FAULT
		Reset on Power On Reset (POR)
10	FCCU2_FLT_POL	FCCU2 FAULT POLARITY
		0 LOW LEVEL IS A FAULT
		1 HIGH LEVEL IS A FAULT
		Reset on Power On Reset (POR)
9	FCCU12_FS_REACTION	Reaction on RSTB or FAIL SAFE output in case of FAULT DETECTION ON FCCU12
		0 FS0B only is asserted low in case of fault on FCCU1 and FCCU2
		1 RSTB and FS0B only is asserted low in case of fault on FCCU1 and FCCU2
		Reset on Power On Reset (POR)

Table 78. FS_I_SAFE_INPUTS register bit description (default value in bold)*...continued*

Bit	Symbol	Description
8	FCCU1_FS_REACTION	Reaction on RSTB or FAIL SAFE output in case of FAULT DETECTION ON FCCU1
		0 FS0B only is asserted low in case of fault on FCCU1
		1 RSTB and FS0B only is asserted low in case of fault on FCCU1
		Reset on Power On Reset (POR)
7	FCCU2_FS_REACTION	Reaction on RSTB or FAIL SAFE output in case of FAULT DETECTION ON FCCU2
		0 FS0B only is asserted low in case of fault on FCCU2
		1 RSTB and FS0B only is asserted low in case of fault on FCCU2
		Reset on Power On Reset (POR)
5	ERRMON_FLT_POLARITY	ERRMON Fault Polarity
		0 Low level is a fault after a negative edge transition
		1 High level is a fault after a positive edge transition
		Reset on Power On Reset (POR)
4 to 3	ERRMON_ACK_TIME[1:0]	Acknowledge timing following a fault detection on ERRMON
		00 1 ms
		01 8 ms
		10 16 ms
		11 32 ms
		Reset on Power On Reset (POR)
2	ERRMON_FS_REACTION	Reaction on RSTB or Fail Safe output in case of fault detection on ERRMON
		0 FS0B only is asserted low in case of fault detection on ERRMON
		1 RSTB and FS0B only is asserted low in case of fault detected on ERRMON
		Reset on Power On Reset (POR)
1 to 0	FCCU12_FILT[1:0]	FCCU pin filtering time settings
		00 3 µs
		01 6 µs
		10 10 µs
		11 20 µs
		Reset on Power On Reset (POR)

18.6 FS_I_FSSM (0x49)

Table 79. FS_I_FSSM register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_ REACTION		0	RSTB_DUR	0
Read	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_ REACTION		0	RSTB_DUR	0
Reset	0	1	0	1	0	0	0	0

Bit	7	6	5(*)	4	3	2	1	0
Write	BACKUP_SAFETY_ PATH_FS0B	BACKUP_SAFETY_ PATH_FS1B	0	DIS8S	0	0	0	0
Read	BACKUP_SAFETY_ PATH_FS0B	BACKUP_SAFETY_ PATH_FS1B	0	DIS8S	FLT_ERR_CNT[3:0]			
Reset	1	1	0	0	0	0	0	1

(*) Bit 5 must be set to 1 in FS_I_NOT_FSSM (0x4A)

Table 80. FS_I_FSSM register bit description (default value in bold)

Bit	Symbol	Description
15 to 14	FLT_ERR_CNT_LIMIT[1:0]	Configure the maximum level of the fault counter
		00 Max Value = 2
		01 Max Value = 6
		10 Max Value = 8
		11 Max Value = 12
		Reset on Power On Reset (POR)
12 to 11	FLT_ERR_REACTION	Configure the RSTB and FS0B behavior when fault error counter ≥ intermediate value
		00 No effect on RSTB and FS0B
		01 FS0B is asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
		10 RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
		11 RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
		Reset on Power On Reset (POR)
9	RSTB_DUR	Reset duration configuration
		0 10 ms
		1 1 ms
		Reset on Power On Reset (POR)
7	BACKUP_SAFETY_PATH_FS0B	Assert RSTB in case a short to high is detected on FS0B
		0 No assertion of the RSTB
		1 RSTB assertion
		Reset on Power On Reset (POR)
6	BACKUP_SAFETY_PATH_FS1B	Assert RSTB in case a short to high is detected on FS1B
		0 No assertion of the RSTB
		1 RSTB assertion
		Reset on Power On Reset (POR)
4	DIS8S	Disable 8 s RSTB timer
		0 RSTB LOW 8 s Counter enabled
		1 RSTB LOW 8 s Counter disabled
		Reset on Power On Reset (POR)
3 to 0	FLT_ERR_CNT[3:0]	Reflect the value of the Fault Error Counter
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 9
		1010 10
		1011 11
		1100 12

Table 80. FS_I_FSSM register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		1101 12
		Reset on Power On Reset (POR)

18.7 FS_WDW_DURATION (0x4B)

Table 81. FS_WDW_DURATION register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WDW_PERIOD[3:0]				0	0	0	WDW_DC[2]
Read	WDW_PERIOD[3:0]				0	0	0	WDW_DC[2]
Reset	0	0	1	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	WDW_DC[1:0]		0	0	WDW_RECOVERY[3:0]			
Read	WDW_DC[1:0]		0	0	WDW_RECOVERY[3:0]			
Reset	1	0	0	0	1	0	1	1

Table 82. FS_WDW_DURATION register bit description (default value in bold)

Bit	Symbol	Description
15 to 12	WDW_PERIOD[3:0]	Watchdog window period configuration
		0000 Infinite open window (can be set during INIT_FS only)
		0001 1 ms
		0010 2 ms
		0011 3 ms
		0100 4 ms
		0101 6 ms
		0110 8 ms
		0111 12 ms
		1000 16 ms
		1001 24 ms
		1010 32 ms
		1011 64 ms
		1100 128 ms
		1101 256 ms
		1110 512 ms
		1111 1024 ms
		Reset on Power On Reset (POR)
8 to 6	WDW_DC[2:0]	Watchdog Window Duty cycle
		000 Closed Window : 31.25 % / Open Window : 68.75 %
		001 Closed Window : 37.50 % / Open Window : 62.50 %
		010 Closed Window : 50 % / Open Window : 50 %
		011 Closed Window : 62.50 % / Open Window : 37.50 %
		100 Closed Window : 68.75 % / Open Window : 31.25 %
		101 Closed Window : 75 % / Open Window : 25 %

Table 82. FS_WDW_DURATION register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		110 Closed Window : 81.25 % / Open Window : 18.75 %
		111 Closed Window : 50 % / Open Window : 50 %
		Reset on Power On Reset (POR)
3 to 0	WDW_RECOVERY[3:0]	Watchdog window recovery period configuration
		0000 Infinite open window (can be set during INIT_FS only)
		0001 1 ms
		0010 2 ms
		0011 3 ms
		0100 4 ms
		0101 6 ms
		0110 8 ms
		0111 12 ms
		1000 16 ms
		1001 24 ms
		1010 32 ms
		1011 64 ms
		1100 128 ms
		1101 256 ms
		1110 512 ms
		1111 1024 ms
		Reset on Power On Reset (POR)

18.8 FS_WD_ANSWER (0x4D)

Table 83. FS_WD_ANSWER register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ANSWER[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	WD_ANSWER[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 84. FS_WD_ANSWER register bit description

Bit	Symbol	Description
15 to 0	WD_ANSWER[15:0]	Watchdog answer from MCU
		16 bits watchdog answer from the MCU needs to be written here
		Reset on Power On Reset (POR)

18.9 FS_WD_TOKEN (0x4E)

Table 85. FS_WD_TOKEN register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_TOKEN[15:8]							

Table 85. FS_WD_TOKEN register bit allocation...*continued*

Bit	15	14	13	12	11	10	9	8
Read	WD_TOKEN[15:8]							
Reset	0	1	0	1	1	0	1	0

Bit	7	6	5	4	3	2	1	0
Write	WD_TOKEN[7:0]							
Read	WD_TOKEN[7:0]							
Reset	1	0	1	1	0	0	1	0

Table 86. FS_WD_TOKEN register bit description

Bit	Symbol	Description
15 to 0	WD_TOKEN[15:0]	WD Token code
		Token value can be written by the MCU here. Default value is 0x5AB2
		Reset on Power On Reset (POR)

18.10 FS_ABIST_ON_DEMAND (0x4F)

Table 87. FS_ABIST_ON_DEMAND register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	LAUNCH_ ABIST2	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	ABIST2_EXT	ABIST2_ REF	ABIST2_ TRK2	ABIST2_ TRK1	ABIST2_ LDO2	ABIST2_ LDO1	ABIST2_ CORE	ABIST2_ VPRE
Read	ABIST2_EXT	ABIST2_ REF	ABIST2_ TRK2	ABIST2_ TRK1	ABIST2_ LDO2	ABIST2_ LDO1	ABIST2_ CORE	ABIST2_ VPRE
Reset	0	0	0	0	0	0	0	0

Table 88. FS_ABIST_ON_DEMAND register bit description (default value in bold)

Bit	Symbol	Description
15	LAUNCH_ABIST2	Launch ABIST on selected VMONs
		0 No action
		1 ABIST launched
		Reset on Power On Reset (POR), Self-clear
7	ABIST2_EXT	Request ABIST on VMON_EXT
		0 No ABIST
		1 ABIST on VMON_EXT Requested
		Reset on Power On Reset (POR)
6	ABIST2_REF	Request ABIST on VMON_REF
		0 No ABIST

Table 88. FS_ABIST_ON_DEMAND register bit description (default value in bold) *...continued*

Bit	Symbol	Description
		1 ABIST on VMON_REF Requested
		Reset on Power On Reset (POR)
5	ABIST2_TRK2	Request ABIST on VMON_TRK2
		0 No ABIST
		1 ABIST on VMON_TRK2 Requested
		Reset on Power On Reset (POR)
4	ABIST2_TRK1	Request ABIST on VMON_TRK1
		0 No ABIST
		1 ABIST on VMON_TRK1 Requested
		Reset on Power On Reset (POR)
3	ABIST2_LDO2	Request ABIST on VMON_LDO2
		0 No ABIST
		1 ABIST on VMON_LDO2 Requested
		Reset on Power On Reset (POR)
2	ABIST2_LDO1	Request ABIST on VMON_LDO1
		0 No ABIST
		1 ABIST on VMON_LDO1 Requested
		Reset on Power On Reset (POR)
1	ABIST2_CORE	Request ABIST on VMON_CORE
		0 No ABIST
		1 ABIST on VMON_CORE Requested
		Reset on Power On Reset (POR)
0	ABIST2_VPRE	Request ABIST on VMON_PRE
		0 No ABIST
		1 ABIST on VMON_PRE Requested
		Reset on Power On Reset (POR)

18.11 FS_OVUV_REG_STATUS (0x50)

Table 89. FS_OVUV_REG_STATUS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VPRE_OV	VPRE_UV	CORE_OV	CORE_UV	LDO1_OV	LDO1_UV	LDO2_OV	LDO2_UV
Read	VPRE_OV	VPRE_UV	CORE_OV	CORE_UV	LDO1_OV	LDO1_UV	LDO2_OV	LDO2_UV
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	TRK1_OV	TRK1_UV	TRK2_OV	TRK2_UV	REF_OV	REF_UV	EXT_OV	EXT_UV
Read	TRK1_OV	TRK1_UV	TRK2_OV	TRK2_UV	REF_OV	REF_UV	EXT_OV	EXT_UV
Reset	0	0	0	0	0	0	0	0

Table 90. FS_OVUV_REG_STATUS register bit description

Bit	Symbol	Description
15	VPRE_OV	Overvoltage Monitoring on VPRE

Table 90. FS_OVUV_REG_STATUS register bit description...*continued*

Bit	Symbol	Description
		0 No Overvoltage
		1 Overvoltage Reported on VPRE
		Reset on Power On Reset (POR) or clear on Write (write '1')
14	VPRE_UV	Undervoltage Monitoring on VPRE
		0 No Undervoltage
		1 Undervoltage Reported on VPRE
		Reset on Power On Reset (POR) or clear on Write (write '1')
13	CORE_OV	Overvoltage Monitoring on VCORE
		0 No Overvoltage
		1 Overvoltage Reported on VCORE
		Reset on Power On Reset (POR) or clear on Write (write '1')
12	CORE_UV	Undervoltage Monitoring on VCORE
		0 No Undervoltage
		1 Undervoltage Reported on VCORE
		Reset on Power On Reset (POR) or clear on Write (write '1')
11	LDO1_OV	Overvoltage Monitoring on LDO1
		0 No Overvoltage
		1 Overvoltage Reported on LDO1
		Reset on Power On Reset (POR) or clear on Write (write '1')
10	LDO1_UV	Undervoltage Monitoring on LDO1
		0 No Undervoltage
		0 Undervoltage Reported on LDO1
		Reset on Power On Reset (POR) or clear on Write (write '1')
9	LDO2_OV	Overvoltage Monitoring on LDO2
		0 No Overvoltage
		1 Overvoltage Reported on LDO2
		Reset on Power On Reset (POR) or clear on Write (write '1')
8	LDO2_UV	Undervoltage Monitoring on LDO2
		0 No Undervoltage
		1 Undervoltage Reported on LDO2
		Reset on Power On Reset (POR) or clear on Write (write '1')
7	TRK1_OV	Overvoltage Monitoring on TRK1
		0 No Overvoltage
		1 Overvoltage Reported on TRK1
		Reset on Power On Reset (POR) or clear on Write (write '1')
6	TRK1_UV	Undervoltage Monitoring on TRK1
		0 No Undervoltage
		1 Undervoltage Reported on TRK1
		Reset on Power On Reset (POR) or clear on Write (write '1')
5	TRK2_OV	Overvoltage Monitoring on TRK2
		0 No Overvoltage
		1 Overvoltage Reported on TRK2
		Reset on Power On Reset (POR) or clear on Write (write '1')
4	TRK2_UV	Undervoltage Monitoring on TRK2
		0 No Undervoltage

Table 90. FS_OVUV_REG_STATUS register bit description*...continued*

Bit	Symbol	Description
		1 Undervoltage Reported on TRK2
		Reset on Power On Reset (POR) or clear on Write (write '1')
3	REF_OV	Overvoltage Monitoring on VREF
		0 No Overvoltage
		1 Overvoltage Reported on VREF
		Reset on Power On Reset (POR) or clear on Write (write '1')
2	REF_UV	Undervoltage Monitoring on VREF
		0 No Undervoltage
		1 Undervoltage Reported on VREF
		Reset on Power On Reset (POR) or clear on Write (write '1')
1	EXT_OV	Overvoltage Monitoring on VMON_EXT
		0 No Overvoltage
		1 Overvoltage Reported on VMON_EXT
		Reset on Power On Reset (POR) or clear on Write (write '1')
0	EXT_UV	Undervoltage Monitoring on VMON_EXT
		0 No Undervoltage
		1 Undervoltage Reported on VMON_EXT
		Reset on Power On Reset (POR) or clear on Write (write '1')

18.12 FS_RELEASE_FS0B_FS1B (0x51)

Table 91. FS_RELEASE_FS0B_FS1B register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	RELEASE_FS0B_FS1B[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	RELEASE_FS0B_FS1B[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 92. FS_RELEASE_FS0B_FS1B register bit description

Bit	Symbol	Description
15 to 0	RELEASE_ FS0B_FS1B[15:0]	Secure 16 bits word to release FS0B and/or FS1B
		Depends on LFSR or WD key (if simple WD used), and FS outputs code
		Reset on Power On Reset (POR)

18.13 FS_SAFE_IOS_1 (0x52)

Table 93. FS_SAFE_IOS_1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	EXT_RSTB	0	0	RSTB_ EVENT	RSTB_DIAG	RSTB_REQ	0	0
Read	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_ EVENT	RSTB_DIAG	0	FS0B_DRV	FS0B_SNS

Table 93. FS_SAFE_IOS_1 register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FS0B_DIAG	FS0B_REQ	0	0	FS1B_DIAG	FS1B_REQ	GOTO_INIT	0
Read	FS0B_DIAG	0	FS1B_DRV	FS1B_SNS	FS1B_DIAG	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 94. FS_SAFE_IOS_1 register bit description

Bit	Symbol	Description
15	EXT_RSTB	Report an External Reset
		0 No External Reset
		1 External Reset
		Reset on Power On Reset (POR) or clear on Write (write '1')
14	RSTB_DRV	RSTB Driver - Digital Command
		0 RSTB Driver command sensed Low
		1 RSTB Driver command sensed High
		Reset on Power On Reset (POR)
13	RSTB_SNS	Sense of RSTB pad
		0 RSTB pad sensed low
		1 RSTB pad sensed High
		Reset on Power On Reset (POR)
12	RSTB_EVENT	Report a Reset Event (latched)
		0 No Reset
		1 Reset Occurred (Reset assertion by device or external reset by MCU)
		Reset on Power On Reset (POR) or clear on Write (write '1')
11	RSTB_DIAG	Report a Reset short to HIGH
		0 No Failure
		1 Short to High detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
10	RSTB_REQ	Request an assertion of Reset
		0 No action
		1 RSTB assertion (pulse)
		Reset on Power On Reset (POR), Self-clear
9	FS0B_DRV	FS0B Driver - Digital Command
		0 FS0B Driver command sensed Low
		1 FS0B Driver command sensed High
		Reset on Power On Reset (POR)
8	FS0B_SNS	Sense of FS0B pad
		0 FS0B pad sensed low
		1 FS0B pad sensed High
		Reset on Power On Reset (POR)
7	FS0B_DIAG	Report a FS0B short to HIGH
		0 No Failure

Table 94. FS_SAFE_IOS_1 register bit description*...continued*

Bit	Symbol	Description
		1 Short to High detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
6	FS0B_REQ	Request an assertion of FS0B
		0 No action
		1 FS0B assertion
		Reset on Power On Reset (POR), Self-clear
5	FS1B_DRV	FS1B Driver - Digital Command
		0 FS1B Driver command sensed Low
		1 FS1B Driver command sensed High
		Reset on Power On Reset (POR)
4	FS1B_SNS	Sense of FS1B pad
		0 FS1B pad sensed low
		1 FS1B pad sensed High
		Reset on Power On Reset (POR)
3	FS1B_DIAG	Report a FS1B short to HIGH
		0 No Failure
		1 Short to High detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
2	FS1B_REQ	Request an assertion of FS1B
		0 No action
		1 FS1B assertion
		Reset on Power On Reset (POR), Self-clear
1	GOTO_INIT	Go Back to INIT Fail Safe Request
		0 No action
		1 Go back to INIT FS
		Reset on Power On Reset (POR), Self-clear

18.14 FS_SAFE_IOS_2 (0x53)

Table 95. FS_SAFE_IOS_2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	FS1B_TDELAY[4:3]	
Read	0	0	0	0	0	0	FS1B_TDELAY[4:3]	
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FS1B_TDELAY[2:0]			FS1B_TDUR[4:0]				
Read	FS1B_TDELAY[2:0]			FS1B_TDUR[4:0]				
Reset	0	0	0	0	1	0	1	1

Table 96. FS_SAFE_IOS_2 register bit description (default value in bold)

Bit	Symbol	Description
9 to 5	FS1B_TDELAY[4:0]	FS1B delay after assertion of FS0B
		00000 0 ms (asserted with FS0B - no delay)
		00001 5 ms
		00010 10 ms
		00011 15 ms
		00100 20 ms
		00101 25 ms
		00110 30 ms
		00111 40 ms
		01000 50 ms
		01001 60 ms
		01010 80 ms
		01011 100 ms
		01100 125 ms
		01101 150 ms
		01110 175 ms
		01111 200 ms
		10000 225 ms
		10001 250 ms
		10010 300 ms
		10011 400 ms
		10100 500 ms
		10101 600 ms
		10110 700 ms
		10111 800 ms
		11000 900 ms
		11001 1 s
		11010 2 s
		11011 4 s
		11100 5 s
		11101 6 s
		11110 8 s
		11111 10 s
		Reset on Power On Reset (POR)

Table 96. FS_SAFE_IOS_2 register bit description (default value in bold)*...continued*

Bit	Symbol	Description
4 to 0	FS1B_TDUR[4:0]	FS1B duration timing when low
		00000 0 ms (no assertion of FS1B)
		00001 5 ms
		00010 10 ms
		00011 15 ms
		00100 20 ms
		00101 25 ms
		00110 30 ms
		00111 40 ms
		01000 50 ms
		01001 60 ms
		01010 80 ms
		01011 100 ms
		01100 125 ms
		01101 150 ms
		01110 175 ms
		01111 200 ms
		10000 225 ms
		10001 250 ms
		10010 300 ms
		10011 400 ms
		10100 500 ms
		10101 600 ms
		10110 700 ms
		10111 800 ms
		11000 1 s
		11001 2 s
		11010 4 s
		11011 5 s
		11100 6 s
		11101 8 s
		11110 10 s
		11111 Infinite (FS1B released by MCU)
		Reset on Power On Reset (POR)

18.15 FS_DIAG_SAFETY1 (0x54)

Table 97. FS_DIAG_SAFETY1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	BAD_ WD_DATA	BAD_WD_ TIMING	0
Read	0	0	0	0	0	BAD_ WD_DATA	BAD_WD_ TIMING	ABIST1_ PASS
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	ABIST2_PASS	ABIST2_DONE	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	FS_OSC_DRIFT	0	0
Read	ABIST2_PASS	ABIST2_DONE	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	FS_OSC_DRIFT	LBIST_STATUS[1:0]	
Reset	0	0	0	0	0	0	0	0

Table 98. FS_DIAG_SAFETY1 register bit description

Bit	Symbol	Description
10	BAD_WD_DATA	WD Refresh status - Data
		0 Good WD Refresh
		1 Bad WD refresh, Error in the Data
		Reset on Power On Reset (POR) or clear on Write (write '1')
9	BAD_WD_TIMING	WD Refresh status - Timing
		0 Good WD Refresh
		1 Bad WD refresh, Error in the Timing (window)
		Reset on Power On Reset (POR) or clear on Write (write '1')
8	ABIST1_PASS	Diagnostic on ABIST 1
		0 ABIST1 Fail or not executed
		1 ABIST 1 Pass
		Reset on Power On Reset (POR)
7	ABIST2_PASS	Report ABIST2 status
		0 ABIST2 Fail or not executed
		1 ABIST2 Pass
		Reset on Power On Reset (POR) or clear on Write (write '1')
6	ABIST2_DONE	Diagnostic on ABIST2 on Demand
		0 ABIST2 not finished
		1 ABIST2 done
		Reset on Power On Reset (POR) or clear on Write (write '1')
5	SPI_FS_CLK	FS SPI SCLK Error detection
		0 No Error
		1 Wrong number of CLK Cycles < 32 or > 32
		Reset on Power On Reset (POR) or clear on Write (write '1')
4	SPI_FS_REQ	Invalid FS SPI access (wrong write or read, Write to INIT registers in normal mode, or Wrong address)
		0 No Error
		1 SPI Violation
		Reset on Power On Reset (POR) or clear on Write (write '1')
3	SPI_FS_CRC	FS SPI communication error - CRC
		0 No Error
		1 Error detected in the CRC
		Reset on Power On Reset (POR) or clear on Write (write '1')
2	FS_OSC_DRIFT	Drift of the Fail Safe Oscillator
		0 No Drift
		1 Oscillator Drift
		Reset on Power On Reset (POR) or clear on Write (write '1')

Table 98. FS_DIAG_SAFETY1 register bit description*...continued*

Bit	Symbol	Description
1 to 0	LBIST_STATUS[1:0]	LBIST Status (MSB = LBIST_CHK_PAT_OK, LSB = LBIST_CHECKER_OK)
		00 Reserved (Not used)
		01 LBIST BYPASSED
		10 LBIST FAIL
		11 LBIST OK
		Reset on Power On Reset (POR)

18.16 FS_DIAG_SAFETY2 (0x55)

Table 99. FS_DIAG_SAFETY2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FCCU12	FCCU1	FCCU2	0	0	ERRMON_ ACK	ERRMON	0
Read	FCCU12	FCCU1	FCCU2	FCCU1_ RT	FCCU2_ RT	0	ERRMON	ERRMON_ PIN_ STATUS
Reset	0	0	0	0	0	0	0	0

Table 100. FS_DIAG_SAFETY2 register bit description

Bit	Symbol	Description
7	FCCU12	Report an error in the FCCU12 input
		0 No error
		1 Error Detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
6	FCCU1	Report an error in the FCCU1 input
		0 No error
		1 Error Detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
5	FCCU2	Report an error in the FCCU2 input
		0 No error
		1 Error Detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
4	FCCU1_RT	Sense of FCCU1 (Real time value)
		0 FCCU1 Low
		1 FCCU1 High
		Reset on Power On Reset (POR)

Table 100. FS_DIAG_SAFETY2 register bit description*...continued*

Bit	Symbol	Description
3	FCCU2_RT	Sense of FCCU2 (Real time value)
		0 FCCU2 Low
		1 FCCU2 High
		Reset on Power On Reset (POR)
2	ERRMON_ACK	Acknowledge ERRMON Failure Timer
		0 No error
		1 acknowledge ERRMON timeout
		Reset on Power On Reset (POR), Self-clear
1	ERRMON	Report an error in the ERRMON input
		0 No error
		1 Error Detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
0	ERRMON_ PIN_STATUS	Report ERRMON pin status
		0 Low level
		1 High Level
		Reset on Power On Reset (POR)

18.17 FS_INTB_MASK (0x56)

Table 101. FS_INTB_MASK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VPRE_M	CORE_M	LDO1_M	LDO2_M	TRK1_M	TRK2_M	REF_M	EXT_M
Read	VPRE_M	CORE_M	LDO1_M	LDO2_M	TRK1_M	TRK2_M	REF_M	EXT_M
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FCCU1_M	FCCU2_M	BAD_WD_M	ERRMON_M	0	0	0	0
Read	FCCU1_M	FCCU2_M	BAD_WD_M	ERRMON_M	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 102. FS_INTB_MASK register bit description (default value in bold)

Bit	Symbol	Description
15	VPRE_M	Interrupt Mask on VMON_PRE event (VPRE_OV and VPRE_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
14	CORE_M	Interrupt Mask on VMON_CORE event (CORE_OV and CORE_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
13	LDO1_M	Interrupt Mask on VMON_LDO1 event (LDO1_OV and LDO1_UV)

Table 102. FS_INTB_MASK register bit description (default value in bold)*...continued*

Bit	Symbol	Description
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
12	LDO2_M	Interrupt Mask on VMON_LDO2 event (LDO2_OV and LDO2_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
11	TRK1_M	Interrupt Mask on VMON_TRK1 event (TRK1_OV and TRK1_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
10	TRK2_M	Interrupt Mask on VMON_TRK2 event (TRK2_OV and TRK2_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
9	REF_M	Interrupt Mask on VMON_REF event (REF_OV and REF_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
8	EXT_M	Interrupt Mask on VMON_EXT event (EXT_OV and EXT_UV)
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
7	FCCU1_M	Interrupt Mask on FCCU1
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
6	FCCU2_M	Interrupt Mask on FCCU2
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
5	BAD_WD_M	Interrupt Mask on BAD_WD_REFRESH
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)
4	ERRMON_M	Interrupt Mask on ERRMON
		0 Interrupt Not Masked
		1 Interrupt Masked
		Reset on Power On Reset (POR)

18.18 FS_STATES (0x57)

Table 103. FS_STATES register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	EXIT_DBG_ MODE	0	OTP_ CORRUPT	REG_ CORRUPT	0	0	0

Table 103. FS_STATES register bit allocation*...continued*

Bit	15	14	13	12	11	10	9	8
Read	0	0	DBG_MODE	OTP_CORRUPT	REG_CORRUPT	0	0	0
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	0	0	0
Read	0	0	0	FS_STATES				
Reset	0	0	0	0	0	0	0	0

Table 104. FS_STATES register bit description

Bit	Symbol	Description
14	EXIT_DBG_MODE	Leave Debug Mode
		0 No action
		1 Leave Debug mode
		Reset on Power On Reset (POR), Self-clear
13	DBG_MODE	DEBUG MODE Status
		0 Not in DEBUG MODE
		1 In DEBUG MODE
		Reset on Power On Reset (POR)
12	OTP_CORRUPT	OTP bits corruption detection (5ms cyclic check)
		0 No OTP content CRC error Detected
		1 OTP Content CRC error detected
		Reset on Power On Reset (POR) or clear on Write (write '1')
11	REG_CORRUPT	INIT Register Corruption detection
		0 No corruption detected in init registers (i.e. no mismatch between register/register_NOT) pair
		1 Data content corruption detected in init registers (i.e. mismatch between register/register_NOT) pair
		Reset on Power On Reset (POR) or clear on Write (write '1')
4 to 0	FS_STATES	Actual Sate of the Fail Safe State machine
		00100 Debug entry
		00110 Enable Monitoring
		01000 RSTB Release
		01001 Init FS
		01010 Safety Outputs not released
		01011 Normal
		Reset on Power On Reset (POR)

18.19 FS_LP_REQ (0x58)

Table 105. FS_LP_REQ register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	STBY_WAKE_UP
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Write	FS_LP_REQ[7:0]							
Read	FS_LP_REQ[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 106. FS_LP_REQ register bit description

Bit	Symbol	Description
8	STBY_WAKE_UP	Wake up source
		0 Wake-up from POR or wake-up from LPOFF
		1 Wake-up from Standby
		Reset on Power On Reset (POR)
7 to 0	FS_LP_REQ[7:0]	Low power command
		0xA5 transition to PRE LPOFF 0x5A Transition to FS go LPOFF 0xAA Transition to PRE Standby 0x55 Transition to FS go Standby
		Reset on Power On Reset (POR)

18.20 FS_LDT_LPSEL (0x59)

Table 107. FS_LDT_LPSEL register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Table 108. FS_LDT_LPSEL register bit allocation

Bit	7	6	5	4	3	2	1	0
Write	LDT_LPSEL[7:0]							
Read	LDT_LPSEL[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 109. FS_LDT_LPSEL register bit description

Bit	Symbol	Description
7 to 0	LDT_LPSEL[7:0]	Low power command
		0xA5 transition to go to LPOFF when LDT_EN = 1 0xAA transition to go to Standby when LDT_EN = 1.
		Reset on Power On Reset (POR)

19 OTP bits description

19.1 Main OTP overview

Table 110. Main OTP configuration map

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_SYS_CFG1	20	RETRY_MSK_OTP[3:0]				RETRY_MODE_OTP	RETRY_DIS_OTP	WK1DFS_DIS_OTP	VSUP_UVTH_OTP
OTP_SYS_CFG2	21	MDFS_DIS_OTP	CLK_FREQ_OTP[1:0]		SLOT_BYP_OTP[2:0]			TSLOT_OTP[1:0]	
OTP_SYS_CFG3	22	GPIO2_VCORE_PGOOD_OTP	GPIO2_MODE_OTP	GPIO1_MODE_OTP	VREF_PLIFT_DIS_OTP	LDO2_PLIFT_DIS_OTP	LDO1_PLIFT_DIS_OTP	BOS_IN_OTP[1:0]	
OTP_VBST_CFG1	23	VBST_MAX_DC_OTP[1:0]		—	VBSTLS_SR_OTP	VBST_PH_OTP[1:0]		VBST_OV_OTP	VBST_CFG_OTP
OTP_VBST_CFG2	24	VBST_TON_MIN_OTP[1:0]		VBST_RCOMP_OTP[1:0]		VBST_CCOMP_OTP[1:0]		VBST_GMCOMP_OTP[1:0]	
OTP_VBST_CFG3	25	VBST_ILIM_OTP[1:0]		VBST_SC_OTP[5:0]					
OTP_VBST_VOLT	26	VBST_SS_OTP[1:0]		—	VBST_OTP[4:0]				
OTP_VPRE_CFG1	27	VPRE_OC_OTP[2:0]			VPRE_SR_OTP	VPRE_PH_OTP[1:0]		VPRE_SS_OTP[1:0]	
OTP_VPRE_CFG2	28	—	VPRE_RCOMP_OTP[2:0]			VPRE_CCOMP_OTP[1:0]		VPRE_GM_OTP[1:0]	
OTP_VPRE_CFG3	29	VPRE_OC_DGLT_OTP[1:0]		VPRE_SC_OTP[5:0]					
OTP_VPRE_CFG4	2A	VPRETSD_PD_OTP	VPRETDFS_OTP	VPRE_CLK_OTP	—	VPRE_PFM_TOFF_OTP[1:0]		VPRE_PFM_TON_OTP[1:0]	
OTP_VPRE_VOLT1	2B	—		VPRE_OTP[5:0]					
OTP_VPRE_VOLT2	2C	VPRE_LP_DVS_OTP[1:0]		VPRE_LP_OTP[5:0]					
OTP_VPRE_VOLT3	2D	VPRE_PDWN_DLY_OTP[1:0]		VPRE_BOS_OTP[5:0]					
OTP_CORE_CFG1	2E	—		COREHS_SR_OTP[1:0]		CORE_PH_OTP[1:0]		CORE_ILIM_OTP[1:0]	
OTP_CORE_CFG2	2F	—		CORE_RCOMP_OTP[1:0]		CORE_CCOMP_OTP[1:0]		CORE_GM_OTP[1:0]	
OTP_CORE_CFG3	30	—		CORE_SS_OTP[1:0]		0	CORE_CTRL_OTP	CORE_LSEL_OTP[1:0]	
OTP_CORE_VOLT1	31	VCORE_OTP[7:0]							
OTP_CORE_CFG5	32	CORETSD_PD_OTP	CORETDFS_OTP	—			CORE_SLOT_OTP[2:0]		
OTP_LDO1_CFG	33	LDO1TSD_PD_OTP	LDO1TDFS_OTP	LDO1_LP_EN_OTP	VLDO1_LP_OTP	VLDO1_OTP	LDO1_SLOT_OTP[2:0]		
OTP_LDO2_CFG	34	LDO2TSD_PD_OTP	LDO2TDFS_OTP	LDO2_LP_EN_OTP	VLDO2_LP_OTP	VLDO2_OTP	LDO2_SLOT_OTP[2:0]		
OTP_TRK1_CFG	35	TRK1TSD_PD_OTP	TRK1TDFS_OTP	TRK1_SEL_OTP[1:0]		—	TRK1_SLOT_OTP[2:0]		
OTP_TRK2_CFG	36	TRK2TSD_PD_OTP	TRK2TDFS_OTP	TRK2_SEL_OTP[1:0]		—	TRK2_SLOT_OTP[2:0]		
OTP_VREF_CFG	37	—		VLDO_REF_OTP[1:0]		VREF_OTP	VREF_SLOT_OTP[2:0]		
OTP_GPIO1_CFG	38	GPIO1TSD_PD_OTP	GPIO1PD_OTP	GPIO1PU_OTP	GPIO1STAGE_OTP[1:0]		GPIO1_SLOT_OTP[2:0]		

Table 110. Main OTP configuration map*...continued*

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_ GPIO2_CFG	39	—	GPIO2PD_ OTP	GPIO2PU_ OTP	GPIO2STAGE_OTP[1:0]		GPIO2_SLOT_OTP[2:0]		
OTP_ INPUT_CFG	3A	WK2PD_ SEL_OTP	WK1PD_ SEL_OTP	GPIO2TH_ OTP	GPIO1TH_OTP	WK2PD_OTP	WK1PD_OTP	WK2TH_ OTP	WK1TH_ OTP
OTP_ PROG_IDH	3B	PROG_IDH_OTP[7:0]							
OTP_ PROG_IDL	3C	PROG_IDL_OTP[7:0]							

19.2 Main OTP bits description

Table 111. Main OTP bits description

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
0x20	OTP_SYS_CFG1	RETRY_MSK_OTP[3:0]	Auto-retry timer limit	0x01	200 ms
				0x02	400 ms
				0x03	800 ms
				0x04	1600 ms
				0x05	3200 ms
				0x06	6400 ms
				0x07	12800 ms
				0x08	25600 ms
				0x09	51200 ms
				0x0A	102400 ms
				0x0B	204800 ms
				0x0C	409600 ms
				0x0D	819200 ms
				0x0E	1638400 ms
				0x0F	3276800 ms
		RETRY_MODE_OTP	Auto-retry mode	0x00	Limited retry
				0x01	Infinite retry
		RETRY_DIS_OTP	Auto-retry power up from DFS	0x00	Enabled
				0x01	Disabled
		WK1DFS_DIS_OTP	Exit DFS on WAKE1 event	0x00	Enabled
				0x01	Disabled
		VSUP_UVTH_OTP	VSUP UV threshold	0x00	4.8 V / 4.3 V
				0x01	6.1 V / 5.65 V
0x21	OTP_SYS_CFG2	MDFS_DIS_OTP	Disable Deep Fail Safe entry	0x00	DFS entry enabled
				0x01	DFS entry disabled
		CLK_FREQ_OTP[1:0]	Clock frequency selection	0x00	16 MHz
				0x01	17 MHz
				0x02	18 MHz
				0x03	19 MHz
		SLOT_BYP_OTP[2:0]	Power up slot bypass	0x00	Bypass disabled
				0x01	Bypass slot 1 to 6
				0x02	Bypass slot 2 to 6
				0x03	Bypass slot 3 to 6

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x04	Bypass slot 4 to 6
				0x05	Bypass slot 5 to 6
				0x06	Bypass slot 6
				0x07	Bypass disabled
		TSLOT_OTP[1:0]	Power up slot time	0x00	250 µs
				0x01	500 µs
				0x02	1000 µs
				0x03	2000 µs
0x22	OTP_SYS_CFG3	GPIO2_VCORE_ PGOOD_OTP	GPIO2 VCORE PGOOD	0x00	GPIO2 is not driven by VCORE PGOOD
				0x01	GPIO2 is driven by VCORE PGOOD
		GPIO2_MODE_OTP	GPIO2 Low Side polarity	0x00	GPIO2 LS active high
				0x01	GPIO2 LS active low
		GPIO1_MODE_OTP	GPIO1 Low Side polarity	0x00	GPIO1 LS active high
				0x01	GPIO1 LS active low
		VREF_PLIFT_DIS_OTP	VREF pin lift detection	0x00	VREF pin lift detection enabled
				0x01	VREF pin lift detection disabled
		LDO2_PLIFT_DIS_OTP	LDO2 pin lift detection	0x00	LDO2 pin lift detection enabled
				0x01	LDO2 pin lift detection disabled
		LDO1_PLIFT_DIS_OTP	LDO1 pin lift detection	0x00	LDO1 pin lift detection enabled
				0x01	LDO1 pin lift detection disabled
		BOS_IN_OTP[1:0]	VBOS input selection	0x00	Auto Transition from VPRE to VSUP when $V_{PRE} < V_{PRE\_UVBOS}$
				0x01	Force VBOS_IN = VSUP always
0x23	OTP_VBST_CFG1	VBST_MAX_ DC_OTP[1:0]	Max duty-cycle	0x00	72.5 %
				0x01	77.5 %
				0x02	82.5 %
				0x03	87.5 %
		VBSTLS_SR_OTP	Low-side slew rate	0x00	PU = 2 Ω / PD = 1.7 Ω
				0x01	PU = 1.5 Ω / PD = 1.0 Ω
		VBST_PH_OTP[1:0]	Phase delay	0x00	No delay
				0x01	1 Clock Cycle
				0x02	2 Clock Cycles
				0x03	3 Clock Cycles
		VBST_OV_OTP	VBSTFB OV monitor mode	0x00	Auto-enable mode
				0x01	OVP mode
		VBST_CFG_OTP	VBST configuration	0x00	Front-end boost
				0x01	Back-end boost
0x24	OTP_VBST_CFG2	VBST_TON_ MIN_OTP[1:0]	Minimum on time	0x00	200 ns
		VBST_RCOMP_OTP[1:0]	Comp resistance	0x00	1000 kΩ
				0x01	740 kΩ
				0x02	500 kΩ
				0x03	250 kΩ
		VBST_CCOMP_OTP[1:0]	Comp capacitor	0x00	200 pF
				0x01	150 pF

Table 111. Main OTP bits description...*continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x02	100 pF
				0x03	50 pF
		VBST_GMCOMP_OTP[1:0]	Comp transconductance	0x00	3.9 µS
				0x01	5.1 µS
				0x02	7.7 µS
				0x03	15.3 µS
0x25	OTP_VBST_CFG3	VBST_ILIM_OTP[1:0]	Current limit	0x00	60 mV/RSNS
				0x01	120 mV/RSNS
				0x02	150 mV/RSNS
				0x03	180 mV/RSNS
		VBST_SC_OTP[4:0]	Slope compensation	0x00	0 mV/µs
				0x01	14 mV/µs
				0x02	28 mV/µs
				0x03	42 mV/µs
				0x04	56 mV/µs
				0x05	70 mV/µs
				0x06	84 mV/µs
				0x07	99 mV/µs
				0x08	113 mV/µs
				0x09	127 mV/µs
				0x0A	141 mV/µs
				0x0B	155 mV/µs
				0x0C	169 mV/µs
				0x0D	183 mV/µs
				0x0E	197 mV/µs
				0x0F	211 mV/µs
				0x10	225 mV/µs
				0x11	239 mV/µs
				0x12	253 mV/µs
				0x13	268 mV/µs
				0x14	282 mV/µs
				0x15	296 mV/µs
				0x16	310 mV/µs
				0x17	324 mV/µs
				0x18	338 mV/µs
				0x19	352 mV/µs
				0x1A	366 mV/µs
				0x1B	380 mV/µs
				0x1C	394 mV/µs
				0x1D	408 mV/µs
				0x1E	422 mV/µs
				0x1F	436 mV/µs
				0x20	451 mV/µs
				0x21	465 mV/µs

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x22	479 mV/µs
				0x23	493 mV/µs
				0x24	507 mV/µs
				0x25	521 mV/µs
				0x26	535 mV/µs
				0x27	549 mV/µs
				0x28	563 mV/µs
				0x29	577 mV/µs
				0x2A	591 mV/µs
		VBST_SC_OTP[4:0]	Slope compensation	0x2B	605 mV/µs
				0x2C	620 mV/µs
				0x2D	634 mV/µs
				0x2E	648 mV/µs
				0x2F	662 mV/µs
				0x30	676 mV/µs
				0x31	690 mV/µs
				0x32	704 mV/µs
				0x33	718 mV/µs
				0x34	732 mV/µs
				0x35	746 mV/µs
				0x36	760 mV/µs
				0x37	774 mV/µs
				0x38	788 mV/µs
				0x39	803 mV/µs
				0x3A	817 mV/µs
				0x3B	831 mV/µs
				0x3C	845 mV/µs
				0x3D	859 mV/µs
				0x3E	873 mV/µs
				0x3F	887 mV/µs
0x26	OTP_VBST_VOLT	VBST_SS_OTP[1:0]	VBST soft start	0x00	425 µs
				0x01	850 µs
				0x02	1.7 ms
				0x03	3.4 ms
		VBST_OTP[4:0]	VBST voltage	0x00	5.00 V
				0x01	5.25 V
				0x02	5.50 V
				0x03	5.75 V
				0x04	6.00 V
				0x05	6.25 V
				0x06	6.50 V
				0x07	6.75 V
				0x08	7.00 V
				0x09	7.50 V

Table 111. Main OTP bits description *...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x0A	8.00 V
				0x0B	8.50 V
				0x0C	9.00 V
				0x0D	9.50 V
				0x0E	10.0 V
				0x0F	10.5 V
				0x10	11.0 V
				0x11	11.5 V
				0x12	12.0 V
		VBST_OTP[4:0]	VBST voltage	0x13	12.5 V
				0x14	13.0 V
				0x15	13.5 V
				0x16	14.0 V
				0x17	14.5 V
				0x18	15.0 V
				0x19	15.5 V
				0x1A	16.0 V
				0x1B	16.5 V
				0x1C	17.0 V
				0x1D	17.5 V
				0x1E	18.0 V
				0x1F	18.0 V
0x27	OTP_VPRE_CFG1	VPRE_OC_OTP[2:0]	VPRE overcurrent flag	0x00	0.66 A
				0x01	0.88 A
				0x02	1.1 A
				0x03	1.32 A
				0x04	1.54 A
				0x05	1.76 A
				0x06	1.98 A
				0x07	2.2 A
	OTP_VPRE_CFG1	VPRE_SR_OTP	VPRE LX slew rate	0x00	2 ns - Fast mode
				0x01	4 ns - Slow mode
	OTP_VPRE_CFG1	VPRE_PH_OTP[1:0]	VPRE phase delay	0x00	No delay
				0x01	1 Clock Cycle
				0x02	2 Clock Cycles
				0x03	3 Clock Cycles
	OTP_VPRE_CFG1	VPRE_SS_OTP[1:0]	VPRE soft start	0x00	269 µs
				0x01	538 µs
				0x02	1077 µs
				0x03	2150 µs
0x28	OTP_VPRE_CFG2	VPRE_RCOMP_OTP[2:0]	Comp resistance	0x00	1300 kΩ
				0x01	1137 kΩ
				0x02	975 kΩ
				0x03	812 kΩ

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x04	650 kΩ
				0x05	512 kΩ
				0x06	325 kΩ
				0x07	162 kΩ
	OTP_VPRE_CFG2	VPRE_CCOMP_ OTP[1:0]	Comp capacitor	0x00	12.0 pF
				0x01	23.0 pF
				0x02	33.5 pF
				0x03	44.5 pF
		VPRE_GM_OTP[1:0]	Transconductance amp	0x00	10 µS
				0x01	15 µS
				0x02	20 µS
				0x03	25 µS
0x29	OTP_VPRE_CFG3	VPRE_OC_ DGLT_OTP[1:0]	Overcurrent deglitch	0x00	250 µs
				0x01	500 µs
				0x02	1000 µs
				0x03	2000 µs
		VPRE_SC_OTP[5:0]	Slope compensation	0x2A	279 mV/µs
				0x2B	266 mV/µs
				0x2C	254 mV/µs
				0x2D	241 mV/µs
				0x2E	228 mV/µs
				0x2F	214 mV/µs
				0x30	201 mV/µs
				0x31	189 mV/µs
				0x32	176 mV/µs
				0x33	163 mV/µs
0x2A	OTP_VPRE_CFG4	VPRETSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
		VPRETDFS_OTP	TSD behavior	0x00	VPRE disabled only
				0x01	Go to DFS
		VPRE_CLK_OTP	VPRE clock selection	0x00	FSW/40
				0x01	FSW/8
		VPRE_PFM_ TOFF_OTP[1:0]	VPRE high-side minimum off time in PFM	0x02	720 ns
		VPRE_PFM_ TON_OTP[1:0]	VPRE high-side minimum on time in PFM (450 kHz / 2.25 MHz)	0x00 0x01 0x02 0x03	900 ns / 440 ns 1000 ns / 500 ns 1125 ns / 550 ns 1250 ns / 600 ns
0x2B	OTP_VPRE_VOLT1	VPRE_OTP[5:0]	VPRE output voltage in Normal mode	0x0A	3.70 V
				0x0B	3.75 V
				0x0C	3.80 V
				0x0D	3.85 V
				0x0E	3.90 V
				0x0F	3.95 V
				0x10	4.00 V
				0x11	4.05 V

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x12	4.10 V
				0x13	4.15 V
				0x14	4.20 V
				0x15	4.25 V
				0x16	4.30 V
				0x17	4.35 V
				0x18	4.40 V
				0x19	4.45 V
				0x1A	4.50 V
				0x1B	4.55 V
				0x1C	4.60 V
				0x1D	4.65 V
				0x1E	4.70 V
				0x1F	4.75 V
				0x20	4.80 V
				0x21	4.85 V
				0x22	4.90 V
				0x23	4.95 V
				0x24	5.00 V
				0x25	5.05 V
				0x26	5.10 V
				0x27	5.15 V
				0x28	5.20 V
				0x29	5.25 V
				0x2A	5.30 V
				0x2B	5.35 V
				0x2C	5.40 V
				0x2D	5.45 V
				0x2E	5.50 V
				0x2F	5.55 V
				0x30	5.60 V
				0x31	5.65 V
				0x32	5.70 V
				0x33	5.75 V
				0x34	5.80 V
				0x35	5.85 V
				0x36	5.90 V
				0x37	5.95 V
				0x38	6.00 V
				0x39	6.05 V
				0x3A	6.10 V
				0x3B	6.15 V
				0x3C	6.20 V
				0x3D	6.25 V

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x3E	6.30 V
				0x3F	6.35 V
0x2C	OTP_VPRE_VOLT2	VPRE_LP_ DVS_OTP[1:0]	DVS ramp rate	0x00	22 mV/µs
				0x01	11 mV/µs
				0x02	5.5 mV/µs
				0x03	2.75 mV/µs
	OTP_VPRE_VOLT2	VPRE_LP_OTP[5:0]	VPRE output voltage in Standby mode	0x0A	3.70 V
				0x0B	3.75 V
				0x0C	3.80 V
				0x0D	3.85 V
				0x0E	3.90 V
				0x0F	3.95 V
				0x10	4.00 V
				0x11	4.05 V
				0x12	4.10 V
				0x13	4.15 V
				0x14	4.20 V
				0x15	4.25 V
				0x16	4.30 V
				0x17	4.35 V
				0x18	4.40 V
				0x19	4.45 V
				0x1A	4.50 V
				0x1B	4.55 V
				0x1C	4.60 V
				0x1D	4.65 V
				0x1E	4.70 V
				0x1F	4.75 V
				0x20	4.80 V
				0x21	4.85 V
				0x22	4.90 V
				0x23	4.95 V
				0x24	5.00 V
				0x25	5.05 V
				0x26	5.10 V
				0x27	5.15 V
				0x28	5.20 V
				0x29	5.25 V
				0x2A	5.30 V
				0x2B	5.35 V
0x2D	OTP_VPRE_VOLT3	VPRE_PDWN_ DLY_OTP[1:0]	VPRE power down delay	0x00	100 µs
				0x01	1 ms
				0x02	2 ms
				0x03	5 ms

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
	OTP_VPRE_VOLT3	VPRE_BOS_OTP[5:0]	VPRE transition voltage	0x0A	3.70 V
				0x0B	3.75 V
				0x0C	3.80 V
				0x0D	3.85 V
				0x0E	3.90 V
				0x0F	3.95 V
				0x10	4.00 V
				0x11	4.05 V
				0x12	4.10 V
				0x13	4.15 V
				0x14	4.20 V
				0x15	4.25 V
				0x16	4.30 V
				0x17	4.35 V
				0x18	4.40 V
				0x19	4.45 V
				0x1A	4.50 V
				0x1B	4.55 V
				0x1C	4.60 V
				0x1D	4.65 V
				0x1E	4.70 V
				0x1F	4.75 V
				0x20	4.80 V
				0x21	4.85 V
				0x22	4.90 V
				0x23	4.95 V
				0x24	5.00 V
				0x25	5.05 V
				0x26	5.10 V
				0x27	5.15 V
				0x28	5.20 V
				0x29	5.25 V
				0x2A	5.30 V
				0x2B	5.35 V
0x2E	OTP_CORE_CFG1	COREHS_SR_OTP[1:0]	High side slew rate	0x00	Rise = 5 V/ns; Fall = 2.2 V/ns
				0x01	Rise = 4 V/ns; Fall = 0.6 V/ns
				0x02	Rise = 4.5 V/ns; Fall = 1.2 V/ns
				0x03	Rise = 5 V/ns; Fall = 2.2 V/ns
		CORE_PH_OTP[1:0]	Phase delay	0x00	No delay
				0x01	1 Clock Cycle
				0x02	2 Clock Cycles
				0x03	3 Clock Cycles
		CORE_ILIM_OTP[1:0]	VCORE current limit	0x00	1.4 A
				0x01	1.7 A

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x02	2.7 A
				0x03	3.4 A
0x2F	OTP_CORE_CFG2	CORE_RCOMP_OTP[1:0]	Comp resistance	0x00	150 kΩ
				0x01	200 kΩ
				0x02	300 kΩ
				0x03	450 kΩ
		CORE_CCOMP_OTP[1:0]	Comp capacitor	0x00	50 pF
				0x01	60 pF
				0x02	90 pF
				0x03	120 pF
		CORE_GM_OTP[1:0]	Transconductance amp	0x00	26 µS
				0x01	26 µS
				0x02	53 µS
				0x03	107 µS
0x30	OTP_CORE_CFG3	CORE_SS_OTP[1:0]	Soft-start	0x00	2.5 mV/µs
				0x01	5 mV/µs
				0x02	10 mV/µs
				0x03	20 mV/µs
		CORE_CTRL_OTP	Control type	0x00	Valley mode control
				0x01	Peak mode control
		CORE_LSEL_OTP[1:0]	VCORE inductor	0x00	1 µH
				0x01	1.5 µH
				0x02	2.2 µH
				0x03	2.2 µH
0x31	OTP_CORE_VOLT1	VCORE_OTP[7:0]	VCORE voltage LSB = 10 mV	0x00	0.80 V
				….	….
				0xFF	3.35 V
0x32	OTP_CORE_CFG5	CORETSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
				0x01	Pulldown disabled in TSD
		CORETDFS_OTP	TSD behavior	0x00	VCORE disabled only
				0x01	Go to DFS
		CORE_SLOT_OTP[2:0]	VCORE power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x33	OTP_LDO1_CFG	LDO1TSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
				0x01	Pulldown disabled in TSD
		LDO1TDFS_OTP	TSD behavior	0x00	LDO1 disabled only
				0x01	Go to DFS

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
		LDO1_LP_EN_OTP	LDO1 in Standby mode	0x00	Disabled
				0x01	Enabled
		VLDO1_LP_OTP	LDO1 voltage in Standby mode	0x00	3.3 V
				0x01	5.0 V
		VLDO1_OTP	LDO1 voltage in Normal mode	0x00	3.3 V
				0x01	5.0 V
	OTP_LDO1_CFG	LDO1_SLOT_OTP[2:0]	LDO1 power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x34	OTP_LDO2_CFG	LDO2TSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
				0x01	Pulldown disabled in TSD
		LDO2TDFS_OTP	TSD behavior	0x00	LDO2 disabled only
				0x01	Go to DFS
		LDO2_LP_EN_OTP	LDO2 in Standby mode	0x00	Disabled
				0x01	Enabled
		VLDO2_LP_OTP	LDO2 voltage in Standby mode	0x00	3.3 V
				0x01	5.0 V
		VLDO2_OTP	LDO2 voltage in Normal mode	0x00	3.3 V
				0x01	5.0 V
		LDO2_SLOT_OTP[2:0]	LDO2 power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x35	OTP_TRK1_CFG	TRK1TSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
				0x01	Pulldown disabled in TSD
		TRK1TDFS_OTP	TSD behavior	0x00	TRK1 disabled only
				0x01	Go to DFS
		TRK1_SEL_OTP[1:0]	TRK1 input selection	0x00	VREF
				0x01	Internal LDO Reference
				0x02	LDO2
				0x03	VREF
	OTP_TRK1_CFG	TRK1_SLOT_OTP[2:0]	TRK1 power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x36	OTP_TRK2_CFG	TRK2TSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
				0x01	Pulldown disabled in TSD
		TRK2TDFS_OTP	TSD behavior	0x00	TRK2 disabled only
				0x01	Go to DFS
		TRK2_SEL_OTP[1:0]	TRK2 input selection	0x00	VREF
				0x01	Internal LDO reference
				0x02	LDO2
				0x03	VREF
		TRK2_SLOT_OTP[2:0]	TRK2 power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x37	OTP_VREF_CFG	VLDO_REF_OTP[1:0]	Internal LDO reference	0x00	1.2 V
				0x01	1.8 V
				0x02	3.3 V
				0x03	5.0 V
		VREF_OTP	VREF voltage	0x00	3.3 V
				0x01	5.0 V
		VREF_SLOT_OTP[2:0]	VREF power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x38	OTP_GPIO1_CFG	GPIO1TSD_PD_OTP	TSD pulldown	0x00	Pulldown enabled in TSD
				0x01	Pulldown disabled in TSD
		GPIO1PD_OTP	GPIO1 pulldown	0x00	Pulldown disabled
				0x01	Pulldown enabled
		GPIO1PU_OTP	GPIO1 pullup	0x00	Pullup disabled
				0x01	Pullup enabled
		GPIO1STAGE_OTP[1:0]	GPIO1 configuration	0x00	Input configuration
				0x01	Low-side driver
				0x02	High-side driver
				0x03	Push-pull driver

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
		GPIO1_SLOT_OTP[2:0]	GPIO1 power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x39	OTP_GPIO2_CFG	GPIO2PD_OTP	GPIO2 pulldown	0x00	Pulldown disabled
				0x01	Pulldown enabled
		GPIO2PU_OTP	GPIO2 pullup	0x00	Pullup disabled
				0x01	Pullup enabled
		GPIO2STAGE_OTP[1:0]	GPIO2 configuration	0x00	Input configuration
				0x01	Low-side driver
				0x02	High-side driver
				0x03	Push-pull driver
		GPIO2_SLOT_OTP[2:0]	GPIO2 power up slot	0x00	Slot 0
				0x01	Slot 1
				0x02	Slot 2
				0x03	Slot 3
				0x04	Slot 4
				0x05	Slot 5
				0x06	Slot 6
				0x07	Slot 7 / OFF
0x3A	OTP_INPUT_CFG	WK2PD_SEL_OTP	WAKE2 pulldown value selection	0x00	200 kΩ
				0x01	10 kΩ
		WK1PD_SEL_OTP	WAKE1 pulldown value selection	0x00	200 kΩ
				0x01	10 kΩ
		GPIO2TH_OTP	GPIO2 detection threshold	0x00	Low-voltage threshold
				0x01	High-voltage threshold
	OTP_INPUT_CFG	GPIO1TH_OTP	GPIO1 detection threshold	0x00	Low-voltage threshold
				0x01	High-voltage threshold
		WK2PD_OTP	WAKE2 pulldown	0x00	Disabled
				0x01	Enabled
		WK1PD_OTP	WAKE1 pulldown	0x00	Disabled
				0x01	Enabled
		WK2TH_OTP	WAKE2 detection threshold	0x00	Low-voltage threshold
				0x01	High-voltage threshold
		WK1TH_OTP	WAKE1 detection threshold	0x00	Low-voltage threshold
				0x01	High-voltage threshold
0x3B	OTP_PROG_IDH	PROG_IDH_OTP[7:0]	Program ID high decoding	0x00	A
				0x01	B
				0x02	C
				0x03	D

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x04	E
				0x05	F
				0x06	G
				0x07	H
				0x08	J
				0x09	K
				0x0A	L
				0x0B	M
				0x0C	N
				0x0D	P
				0x0E	Q
				0x0F	R
				0x10	S
				0x11	T
				0x12	U
				0x13	V
				0x14	W
				0x15	X
				0x16	Y
				0x17	Z
0x3C	OTP_PROG_IDL	PROG_IDL_OTP[7:0]	Program ID low decoding	0x00	0
				0x01	1
				0x02	2
				0x03	3
				0x04	4
				0x05	5
				0x06	6
				0x07	7
				0x08	8
				0x09	9
				0x0A	A
				0x0B	B
				0x0C	C
				0x0D	D
				0x0E	E
				0x0F	F
				0x10	G
				0x11	H
				0x12	J
				0x13	K
				0x14	L
				0x15	M
				0x16	N
				0x17	P

Table 111. Main OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x18	Q
				0x19	R
				0x1A	S
				0x1B	T
				0x1C	U
				0x1D	V
				0x1E	W
				0x1F	X
				0x20	Y
				0x21	Z

19.3 Fail-safe OTP overview

Table 112. Fail-safe OTP configuration map

Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CFG_OVUV_1_OTP	0F	VMON_LDO2_ UVDTH_OTP	VMON_LDO1_ UVDTH_OTP	VPRE_V_OTP[5:0]					
CFG_OVUV_2_OTP	10	VCORE_V_OTP[7:0]							
CFG_OVUV_3_OTP	11	DFS_DIS_OTP	TRK2_V_OTP[1:0]		TRK1_V_OTP[1:0]		LDO1_V_OTP	LDO2_V_OTP	VREF_V_OTP
CFG_OVUV_4_OTP	12	VMON_PRE_UVTH_OTP[3:0]				VMON_PRE_OVTH_OTP[3:0]			
CFG_OVUV_5_OTP	13	VMON_CORE_UVTH_OTP[3:0]				VMON_CORE_OVTH_OTP[3:0]			
CFG_OVUV_6_OTP	14	VMON_LDO1_UVTH_OTP[3:0]				VMON_LDO1_OVTH_OTP[3:0]			
CFG_OVUV_7_OTP	15	VMON_LDO2_UVTH_OTP[3:0]				VMON_LDO2_OVTH_OTP[3:0]			
CFG_OVUV_8_OTP	16	VMON_TRK1_UVTH_OTP[3:0]				VMON_TRK1_OVTH_OTP[3:0]			
CFG_OVUV_9_OTP	17	VMON_TRK2_UVTH_OTP[3:0]				VMON_TRK2_OVTH_OTP[3:0]			
CFG_OVUV_10_OTP	18	VMON_VREF_UVTH_OTP[3:0]				VMON_VREF_OVTH_OTP[3:0]			
CFG_OVUV_11_OTP	19	VMON_EXT_UVTH_OTP[3:0]				VMON_EXT_OVTH_OTP[3:0]			
CFG_OV_DGLT_OTP	1A	VMON_EXT_ OVDGLT_OTP	VMON_REF_ OVDGLT_OTP	VMON_TRK2_ OVDGLT_OTP	VMON_TRK1_ OVDGLT_OTP	VMON_LDO2_ OVDGLT_OTP	VMON_LDO1_ OVDGLT_OTP	VMON_PRE_ OVDGLT_OTP	VMON_CORE_ OVDGLT_OTP
CFG_UV_DGLT1_OTP	1B	VMON_LDO2_ UVDGLT_OTP[1:0]		VMON_LDO1_ UVDGLT_OTP[1:0]		VMON_PRE_UVDGLT_OTP[1:0]		VMON_CORE_UVDGLT_OTP[1:0]	
CFG_UV_DGLT2_OTP	1C	VMON_EXT_UVDGLT_OTP[1:0]		VMON_REF_UVDGLT_OTP[1:0]		VMON_TRK2_ UVDGLT_OTP[1:0]		VMON_TRK1_UVDGLT_OTP[1:0]	
CFG_ABIST1_OTP	1D	ABIST1_ EXT_EN_OTP	ABIST1_ VREF_ EN_OTP	ABIST1_ TRK2_EN_OTP	ABIST1_ TRK1_EN_OTP	ABIST1_ LDO2_ EN_OTP	ABIST1_ LDO1_EN_OTP	ABIST1_ VCORE_ EN_OTP	ABIST1_VPRE_ EN_OTP
CFG_MODE_OTP	1E	—		WD_DIS_OTP	DIS8S_ DIS_OTP	PRE_RSTB_ DLY_EN_OTP	FS1B_FS0B_ EN_OTP	FAULT_DFS_ EN_OTP	—
CFG_LBIST_ STDBY_OTP	1F	LBIST_STDBY_OTP[7:0]							

19.4 Fail-safe OTP bits description

Table 113. Fail-safe OTP bits description

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
0x11	CFG_OVUV_3_OTP	DFS_DIS_OTP	Disable Deep Fail Safe entry	0x00	DFS entry enabled
				0x01	DFS entry disabled
0x0F	CFG_OVUV_1_OTP	VPRE_V_OTP[5:0]	VPRE monitoring voltage	0x0A	3.70 V
				0x0B	3.75 V
				0x0C	3.80 V
				0x0D	3.85 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x0E	3.90 V
				0x0F	3.95 V
				0x10	4.00 V
				0x11	4.05 V
				0x12	4.10 V
				0x13	4.15 V
				0x14	4.20 V
				0x15	4.25 V
				0x16	4.30 V
				0x17	4.35 V
				0x18	4.40 V
				0x19	4.45 V
				0x1A	4.50 V
				0x1B	4.55 V
				0x1C	4.60 V
				0x1D	4.65 V
				0x1E	4.70 V
				0x1F	4.75 V
				0x20	4.80 V
				0x21	4.85 V
				0x22	4.90 V
				0x23	4.95 V
				0x24	5.00 V
				0x25	5.05 V
				0x26	5.10 V
				0x27	5.15 V
				0x28	5.20 V
				0x29	5.25 V
				0x2A	5.30 V
				0x2B	5.35 V
				0x2C	5.40 V
				0x2D	5.45 V
				0x2E	5.50 V
				0x2F	5.55 V
				0x30	5.60 V
				0x31	5.65 V
				0x32	5.70 V
				0x33	5.75 V
				0x34	5.80 V
				0x35	5.85 V
				0x36	5.90 V
				0x37	5.95 V
				0x38	6.00 V
				0x39	6.05 V
				0x3A	6.10 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x3B	6.15 V
				0x3C	6.20 V
				0x3D	6.25 V
				0x3E	6.30 V
				0x3F	6.35 V
0x12	CFG_OVUV_4_OTP	VMON_PRE_OVTH_OTP[3:0]	VPRE OV threshold	0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_PRE_UVTH_OTP[3:0]	VPRE UV threshold	0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_PRE_OVDGLT_OTP	VMONPRE OV deglitch	0x00	25 µs
				0x01	45 µs
0x1B	CFG_UV_DGLT1_OTP	VMON_PRE_UVDGLT_OTP[1:0]	VMONPRE UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x10	CFG_OVUV_2_OTP	VCORE_V_OTP[7:0]	VCORE monitoring voltage	0x00	0.80 V
				0x01	0.81 V
				0x02	0.82 V
				0x03	0.83 V
				0x04	0.84 V
				0x05	0.85 V
				0x06	0.86 V
				0x07	0.87 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x08	0.88 V
				0x09	0.89 V
				0x0A	0.90 V
				0x0B	0.91 V
				0x0C	0.92 V
				0x0D	0.93 V
				0x0E	0.94 V
				0x0F	0.95 V
				0x10	0.96 V
				0x11	0.97 V
				0x12	0.98 V
				0x13	0.99 V
				0x14	1.00 V
				0x15	1.01 V
				0x16	1.02 V
				0x17	1.03 V
				0x18	1.04 V
				0x19	1.05 V
				0x1A	1.06 V
				0x1B	1.07 V
				0x1C	1.08 V
				0x1D	1.09 V
				0x1E	1.10 V
				0x1F	1.11 V
				0x20	1.12 V
				0x21	1.13 V
				0x22	1.14 V
				0x23	1.15 V
				0x24	1.16 V
				0x25	1.17 V
				0x26	1.18 V
				0x27	1.19 V
				0x28	1.20 V
				0x29	1.21 V
				0x2A	1.22 V
				0x2B	1.23 V
				0x2C	1.24 V
				0x2D	1.25 V
				0x2E	1.26 V
				0x2F	1.27 V
				0x30	1.28 V
				0x31	1.29 V
				0x32	1.30 V
				0x33	1.31 V
				0x34	1.32 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x35	1.33 V
				0x36	1.34 V
				0x37	1.35 V
				0x38	1.36 V
				0x39	1.37 V
				0x3A	1.38 V
				0x3B	1.39 V
				0x3C	1.40 V
				0x3D	1.41 V
				0x3E	1.42 V
				0x3F	1.43 V
				0x40	1.44 V
				0x41	1.45 V
				0x42	1.46 V
				0x43	1.47 V
				0x44	1.48 V
				0x45	1.49 V
				0x46	1.50 V
				0x47	1.51 V
				0x48	1.52 V
				0x49	1.53 V
				0x4A	1.54 V
				0x4B	1.55 V
				0x4C	1.56 V
				0x4D	1.57 V
				0x4E	1.58 V
				0x4F	1.59 V
				0x50	1.60 V
				0x51	1.61 V
				0x52	1.62 V
				0x53	1.63 V
				0x54	1.64 V
				0x55	1.65 V
				0x56	1.66 V
				0x57	1.67 V
				0x58	1.68 V
				0x59	1.69 V
				0x5A	1.70 V
				0x5B	1.71 V
				0x5C	1.72 V
				0x5D	1.73 V
				0x5E	1.74 V
				0x5F	1.75 V
				0x60	1.76 V
				0x61	1.77 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x62	1.78 V
				0x63	1.79 V
				0x64	1.80 V
				0x65	1.81 V
				0x66	1.82 V
				0x67	1.83 V
				0x68	1.84 V
				0x69	1.85 V
				0x6A	1.86 V
				0x6B	1.87 V
				0x6C	1.88 V
				0x6D	1.89 V
				0x6E	1.90 V
				0x6F	1.91 V
				0x70	1.92 V
				0x71	1.93 V
				0x72	1.94 V
				0x73	1.95 V
				0x74	1.96 V
				0x75	1.97 V
				0x76	1.98 V
				0x77	1.99 V
				0x78	2.00 V
				0x79	2.01 V
				0x7A	2.02 V
				0x7B	2.03 V
				0x7C	2.04 V
				0x7D	2.05 V
				0x7E	2.06 V
				0x7F	2.07 V
				0x80	2.08 V
				0x81	2.09 V
				0x82	2.10 V
				0x83	2.11 V
				0x84	2.12 V
				0x85	2.13 V
				0x86	2.14 V
				0x87	2.15 V
				0x88	2.16 V
				0x89	2.17 V
				0x8A	2.18 V
				0x8B	2.19 V
				0x8C	2.20 V
				0x8D	2.21 V
				0x8E	2.22 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x8F	2.23 V
				0x90	2.24 V
				0x91	2.25 V
				0x92	2.26 V
				0x93	2.27 V
				0x94	2.28 V
				0x95	2.29 V
				0x96	2.30 V
				0x97	2.31 V
				0x98	2.32 V
				0x99	2.33 V
				0x9A	2.34 V
				0x9B	2.35 V
				0x9C	2.36 V
				0x9D	2.37 V
				0x9E	2.38 V
				0x9F	2.39 V
				0xA0	2.40 V
				0xA1	2.41 V
				0xA2	2.42 V
				0xA3	2.43 V
				0xA4	2.44 V
				0xA5	2.45 V
				0xA6	2.46 V
				0xA7	2.47 V
				0xA8	2.48 V
				0xA9	2.49 V
				0xAA	2.50 V
				0xAB	2.51 V
				0xAC	2.52 V
				0xAD	2.53 V
				0xAE	2.54 V
				0xAF	2.55 V
				0xB0	2.56 V
				0xB1	2.57 V
				0xB2	2.58 V
				0xB3	2.59 V
				0xB4	2.60 V
				0xB5	2.61 V
				0xB6	2.62 V
				0xB7	2.63 V
				0xB8	2.64 V
				0xB9	2.65 V
				0xBA	2.66 V
				0xBB	2.67 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0xBC	2.68 V
				0xBD	2.69 V
				0xBE	2.70 V
				0xBF	2.71 V
				0xC0	2.72 V
				0xC1	2.73 V
				0xC2	2.74 V
				0xC3	2.75 V
				0xC4	2.76 V
				0xC5	2.77 V
				0xC6	2.78 V
				0xC7	2.79 V
				0xC8	2.80 V
				0xC9	2.81 V
				0xCA	2.82 V
				0xCB	2.83 V
				0xCC	2.84 V
				0xCD	2.85 V
				0xCE	2.86 V
				0xCF	2.87 V
				0xD0	2.88 V
				0xD1	2.89 V
				0xD2	2.90 V
				0xD3	2.91 V
				0xD4	2.92 V
				0xD5	2.93 V
				0xD6	2.94 V
				0xD7	2.95 V
				0xD8	2.96 V
				0xD9	2.97 V
				0xDA	2.98 V
				0xDB	2.99 V
				0xDC	3.00 V
				0xDD	3.01 V
				0xDE	3.02 V
				0xDF	3.03 V
				0xE0	3.04 V
				0xE1	3.05 V
				0xE2	3.06 V
				0xE3	3.07 V
				0xE4	3.08 V
				0xE5	3.09 V
				0xE6	3.10 V
				0xE7	3.11 V
				0xE8	3.12 V

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0xE9	3.13 V
				0xEA	3.14 V
				0xEB	3.15 V
				0xEC	3.16 V
				0xED	3.17 V
				0xEE	3.18 V
				0xEF	3.19 V
				0xF0	3.20 V
				0xF1	3.21 V
				0xF2	3.22 V
				0xF3	3.23 V
				0xF4	3.24 V
				0xF5	3.25 V
				0xF6	3.26 V
				0xF7	3.27 V
				0xF8	3.28 V
				0xF9	3.29 V
				0xFA	3.30 V
				0xFB	3.31 V
				0xFC	3.32 V
				0xFD	3.33 V
				0xFE	3.34 V
				0xFF	3.35 V
0x13	CFG_OVUV_5_OTP	VMON_CORE_OVTH_OTP[3:0]	CORE OV threshold	0x00	104.5 %
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_CORE_UVTH_OTP[3:0]	CORE UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_CORE_OVDGLT_OTP	VMONCORE OV deglitch	0x00	25 µs
				0x01	45 µs
0x1B	CFG_UV_DGLT1_OTP	VMON_CORE_UVDGLT_OTP[1:0]	VMONCORE UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x11	CFG_OVUV_3_OTP	LDO1_V_OTP	LDO1 monitoring voltage	0x00	3.3 V
				0x01	5.0 V
0x14	CFG_OVUV_6_OTP	VMON_LDO1_OVTH_OTP[3:0]	LDO1 OV threshold	0x00	104.5 %
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_LDO1_UVTH_OTP[3:0]	LDO1 UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_LDO1_OVDGLT_OTP	VMONLDO1 OV deglitch	0x00	25 µs
				0x01	45 µs
0x1B	CFG_UV_DGLT1_OTP	VMON_LDO1_UVDGLT_ OTP[1:0]	VMONLDO1 UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x0F	CFG_OVUV_1_OTP	VMON_LDO1_UVDTH_OTP	LDO1 degraded UV monitoring	0x00	Normal UV
				0x01	Degraded UV
0x11	CFG_OVUV_3_OTP	LDO2_V_OTP	LDO2 monitoring voltage	0x00	3.3 V
				0x01	5.0 V
0x15	CFG_OVUV_7_OTP	VMON_LDO2_OVTH_OTP[3:0]	LDO2 OV threshold	0x00	104.5 %
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
0x15	CFG_OVUV_7_OTP	VMON_LDO2_UVTH_OTP[3:0]	LDO2 UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_LDO2_OVDGLT_OTP	VMONLDO2 OV deglitch	0x00	25 µs
				0x01	45 µs
0x1B	CFG_UV_DGLT1_OTP	VMON_LDO2_UVDGLT_ OTP[1:0]	VMONLDO2 UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x0F	CFG_OVUV_1_OTP	VMON_LDO2_UVDTH_OTP	LDO2 degraded UV monitoring	0x00	Normal UV
				0x01	Degraded UV
0x11	CFG_OVUV_3_OTP	TRK1_V_OTP[1:0]	TRK1 monitoring voltage	0x00	1.2 V
				0x01	1.8 V
				0x02	3.3 V
				0x03	5.0 V
0x16	CFG_OVUV_8_OTP	VMON_TRK1_OVTH_OTP[3:0]	TRK1 OV threshold	0x00	104.5 %
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_TRK1_UVTH_OTP[3:0]	TRK1 UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_TRK1_OVDGLT_OTP	VMONTRK1 OV deglitch	0x00	25 µs
				0x01	45 µs
0x1C	CFG_UV_DGLT2_OTP	VMON_TRK1_UVDGLT_OTP[1:0]	VMONTRK1 UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x11	CFG_OVUV_3_OTP	TRK2_V_OTP[1:0]	TRK2 monitoring voltage	0x00	1.2 V
				0x01	1.8 V
				0x02	3.3 V
				0x03	5.0 V
0x17	CFG_OVUV_9_OTP	VMON_TRK2_OVTH_OTP[3:0]	TRK2 OV threshold	0x00	104.5 %
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_TRK2_UVTH_OTP[3:0]	TRK2 UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_TRK2_OVDGLT_OTP	VMONTRK2 OV deglitch	0x00	25 µs
				0x01	45 µs

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
0x1C	CFG_UV_DGLT2_OTP	VMON_TRK2_UVDGLT_OTP[1:0]	VMONTRK2 UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x11	CFG_OVUV_3_OTP	VREF_V_OTP	VREF monitoring voltage	0x00	3.3 V
				0x01	5.0 V
0x18	CFG_OVUV_10_OTP	VMON_VREF_OVTH_OTP[3:0]	VREF OV threshold	0x00	104.5 %
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_VREF_UVTH_OTP[3:0]	VREF UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_REF_OVDGLT_OTP	VMONREF OV deglitch	0x00	25 µs
				0x01	45 µs
0x1C	CFG_UV_DGLT2_OTP	VMON_REF_UVDGLT_OTP[1:0]	VMONTRK2 UV deglitch	0x00	5 µs
				0x01	15 µs
				0x02	25 µs
				0x03	40 µs
0x19	CFG_OVUV_11_OTP	VMON_EXT_OVTH_OTP[3:0]	External VMON OV threshold	0x00	104.5 %

Table 113. Fail-safe OTP bits description...*continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
				0x01	105.0 %
				0x02	105.5 %
				0x03	106.0 %
				0x04	106.5 %
				0x05	107.0 %
				0x06	107.5 %
				0x07	108.0 %
				0x08	108.5 %
				0x09	109.0 %
				0x0A	109.5 %
				0x0B	110.0 %
				0x0C	110.5 %
				0x0D	111.0 %
				0x0E	111.5 %
				0x0F	112.0 %
		VMON_EXT_UVTH_OTP[3:0]	External VMON UV threshold	0x00	95.5 %
				0x01	95.0 %
				0x02	94.5 %
				0x03	94.0 %
				0x04	93.5 %
				0x05	93.0 %
				0x06	92.5 %
				0x07	92.0 %
				0x08	91.5 %
				0x09	91.0 %
				0x0A	90.5 %
				0x0B	90.0 %
				0x0C	89.5 %
				0x0D	89.0 %
				0x0E	88.5 %
				0x0F	88.0 %
0x1A	CFG_OV_DGLT_OTP	VMON_EXT_OVDGLT_OTP	VMONEXT OV deglitch	0x00	25 μs
				0x01	45 μs
0x1C	CFG_UV_DGLT2_OTP	VMON_EXT_UVDGLT_OTP[3:0]	VMONEXT UV deglitch	0x00	5 μs
				0x01	15 μs
				0x02	25 μs
				0x03	40 μs
0x1D	CFG_ABIST1_OTP	ABIST1_VPRE_EN_OTP	ABIST1 on VMONPRE	0x00	Disabled
				0x01	Enabled
		ABIST1_VCORE_EN_OTP	ABIST1 on VMONCORE	0x00	Disabled
				0x01	Enabled
		ABIST1_LDO1_EN_OTP	ABIST1 on VMONLDO1	0x00	Disabled
				0x01	Enabled
		ABIST1_LDO2_EN_OTP	ABIST1 on VMONLDO2	0x00	Disabled
				0x01	Enabled

Table 113. Fail-safe OTP bits description*...continued*

Address	Register Name	Bit Group Name	Description	Hexadecimal Value	Settings
		ABIST1_TRK1_EN_OTP	ABIST1 on VMONTRK1	0x00	Disabled
				0x01	Enabled
		ABIST1_TRK2_EN_OTP	ABIST1 on VMONTRK2	0x00	Disabled
				0x01	Enabled
		ABIST1_VREF_EN_OTP	ABIST1 on VMONREF	0x00	Disabled
				0x01	Enabled
		ABIST1_EXT_EN_OTP	ABIST1 on VMONEXT	0x00	Disabled
				0x01	Enabled
0x1E	CFG_MODE_OTP	FAULT_DFS_EN_OTP	DFS entry mode	0x00	Go to DFS when FLT_ERR_ CNT[3:0] = max
				0x01	Go to DFS when FS0B or RSTB asserted
		FS1B_FS0B_EN_OTP	FS1B assertion mode	0x00	Delayed assertion enabled
				0x01	Delayed assertion disabled
		PRE_RSTB_DLY_EN_OTP	RSTB delay from FS0B	0x00	0 µs
				0x01	100 µs
		DIS8S_DIS_OTP	RSTB low detection timer	0x00	8 second timer enabled
				0x01	Timer disabled
		WD_DIS_OTP	Watchdog timer	0x00	WD timer enable
				0x01	WD timer disabled
0x1F	CFG_LBIST_STDBY_OTP	LBIST_STDBY_OTP[7:0]	Bypass LBIST from Standby mode	0x00	Always perform LBIST
				0xC9	Bypass LBIST from Standby

20 Power management

20.1 Internal biasing: Best of supply regulator

The VBOS regulator manages the best of supply (BOS) from VSUP or VPRE to efficiently generate 5.0 V output and to supply the internal biasing of the device. VBOS supplies the high-side and low-side gate drivers of switching regulators.

The V_{BOS_UVL} detection threshold powers down the device.

When the device is starting up, VBOS voltage, which is supplied by the VSUP until *Normal mode* state, needs to rise above the V_{BOS_UVH} threshold to move to *Fuses Load* state.

The BOS_IN_OTP[1:0] bits define the BOS supply voltage source when the device is in *Normal mode* state:

- When the VPRE output voltage setting is above or equal to 5.0 V, it is recommended to BOS_IN_OTP[1:0] OTP bits = ‘00’ (Auto transition). This setting will ensure an optimized power dissipation of the internal biasing.
- When the VPRE output voltage setting is below 5.0 V, it is recommended to have the BOS_IN_OTP[1:0] OTP bits = ‘01’ (Force VBOS_IN = VSUP). This setting is not

optimized for VBOS power dissipation but will guarantee correct boost converter operation.

Table 114. VBOS electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BOS_NORM}	V_{BOS} voltage range in Normal mode (V_{SUP} > 4.5 V and V_{PRE} > V_{PRE_UVBOS})	V_{PRE_UVBOS} - 0.2	5	5.5	V
$V_{BOS\_STANDBY}$	V_{BOS} voltage range in Standby mode (V_{SUP} > 4.5 V, 3.3 V < V_{PRE} < 5.0 V)	V_{PREPFM} - 0.2	—	V_{PREPFM}	V
V_{BOS_LPOFF}	V_{BOS} voltage range in LPOFF mode (V_{SUP} > 4.5 V)	2.9	4.5	5.5	V
V_{BOS_UVH}	V_{BOS} undervoltage threshold (rising edge)	3.8	4.0	4.2	V
V_{BOS_UVL}	V_{BOS} undervoltage threshold (falling edge)	3	3.2	3.4	V
V_{BOS_POR}	V_{BOS} Power-on reset threshold	2.5	—	3.2	V
V_{DIG_POR}	V_{DIG} Power-on reset threshold	1.35	—	1.54	V
External components					
C_{OUT_VBOS}	VBOS nominal[1] output capacitor value	4.7	4.7	4.7	µF
	VBOS effective[2] output capacitor value	3.3	—	6.1	
C_{OUT_VDIG}	VDIG nominal[1] output capacitor value	1	1	1	µF
	VDIG effective[2] output capacitor value	0.75	—	1.25	

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective value is the value after tolerance, DC bias and aging removal.

20.2 High-voltage buck controller: VPRE

The VPRE block is a high-voltage integrated synchronous buck. It operates in forced PWM or PFM modes, and uses internal FETs. The output voltage and the switching frequency (450 kHz or 2.25 MHz) are configurable by OTP. Compensation is ensured by internal circuitry.

VPRE can be used to supply VCORE, LDO1, LDO2, TRK1, TRK2, VREF, and the VBST (Section 15.4). VPRE can also supply local loads inside the ECU.

At startup, VPRE soft start can be configured through VPRE_SS_OTP[1:0] bits. In case VPRE is supplied by a pre-regulator (not FS26 VBST), the slowest soft start must be used VPRE_SS_OTP[1:0] = 11.

VPRE operates in PWM (pulse width modulation) when the FS26 is in Normal mode and in PFM (pulsed frequency modulation) when the FS26 is in Standby mode. The transition from PWM mode to PFM mode is ensured by a controlled DVS down ramp configurable by OTP ($V_{PRE\_DVS\_DOWN}$).

The current in the inductor is sensed through both high-side and low-side switches. The output DC current is then deducted for internal treatment.When the current in the inductor is rising above the I_{OCPRE_FLAG} threshold, the SPI bit VPREOC_I is set. This overcurrent detection does not affect VPRE regulation.

VPRE has a DC current limitation protection feature I_{LIM_PRE}. When VPRE reaches its current limitation, it induces a duty cycle reduction and therefore an output voltage drop. If the overcurrent disappears before reaching V_{PRE_UVL}, the regulator restarts by doing a soft-start toward its nominal output voltage.

To protect the circuitry that is supplied by the VPRE power rail, an additional overvoltage protection is integrated in the main domain. If $V_{PRE} > V_{PRE\_OVP}$ for a time longer than t_{VPRE_OVP}, the FS26 goes directly into the ***Deep Fail Safe*** state.

V_{PREIN} must be above $V_{PREPWM} + V_{PRE\_HDR}$ to guarantee VPRE output voltage regulation and its trip level can be configured through VPRE_OC_OTP[2:0] bits.

A thermal shutdown protection is integrated to protect the internal MOSFETs from damage. In case of a TSD event, a pulldown resistor (RPRE_DIS) is enabled to discharge VPRE output capacitors.

The transition from Normal mode to LPOFF mode is ensured by a controlled DVS down ramp ($V_{PRE\_DVS\_DOWN}$) until VPRE is disabled. A power down delay can be configured through VPRE_PDWN_DLY[1:0] OTP bit to avoid immediate restart. The delay is executed as soon as VPRE DVS down is completed. VPRE regulator is not intended to restart with residual voltage. Therefore, VPRE_PDWN_DLY[1:0] OTP bit must be configured according to NXP recommendations.

Table 115. VPRE power-down delay configuration when F_{PRE} @2.25 MHz

ASIL level	VBST configuration	VPRE_PDWN_DLY_OTP
D	Front-end	—
	Back-end/not used	≥ 1ms
B	Front-End	≥ 2ms
	Back-end/not used	5 ms

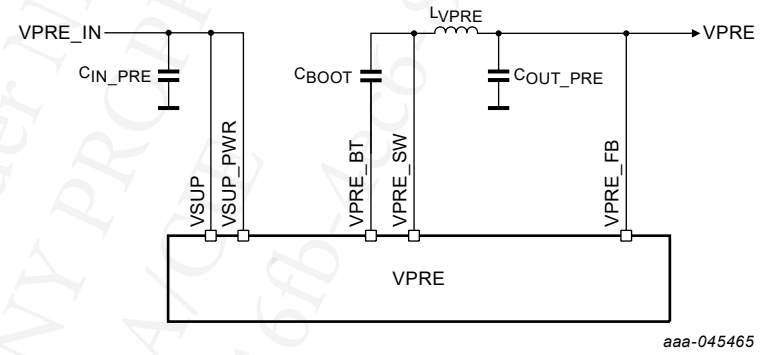


Figure 25. VPRE schematic with connection to V_{SUP}

Table 116. VPRE electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, $V_{PRE} + V_{PRE\_HDR}$ < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static Electrical Characteristics					
V_{PREIN}	Input voltage range With I_{PRE} ≤ 1.5 A and V_{BOS} = 5 V	V_{PRE} + V_{PRE_HDR}	—	36	V
V_{PRE_HDR}	Input voltage headroom range, 600 mA < I_{PRE} ≤ 1.5 A	(Max R_{HS_VPRE} + Max R_{DCR_LVPRE}) x I_{PRE} x 1.25	—	—	V
	Input voltage headroom range, I_{PRE} ≤ 600 mA	400	—	—	mV
V_{PREPWM}	Output voltage in Normal mode (VPRE_OTP[5:0] configuration, 50 mV step)	3.7	—	6.35	V

Table 116. VPRE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{PREPFM}	Output voltage in Standby mode (VPRE_LP_OTP[5:0] configuration, 50 mV step)	3.7	—	5.35	V
V_{PRE_ACCPWM}	Output voltage accuracy in PWM mode for I_{PRE} ≤ 1.5 A	-2	—	2	%
$V_{PRE\_ACCPFM\_150m}$ [1]	Output voltage accuracy in PFM mode for 10 mA ≤ I_{PRE_PFM} ≤ 100 mA V_{SUP} = V_{SUP_PWR} = 12 V V_{PREPFM} = 3.7 V VPRE_PFM_TON_OTP[1:0] = 10 C_{OUT_PRE} ≥ 20 µF (effective value) L_{VPRE} = 2.2 µH at F_{PRE} = 2.25 MHz and L_{VPRE} = 10 µH at F_{PRE} = 450 kHz	-4	—	4	%
$V_{PRE\_ACCPFM\_10m}$ [1]	Output voltage accuracy in PFM mode for I_{PRE_PFM} ≤ 10 mA V_{SUP} = V_{SUP_PWR} = 12 V V_{PREPFM} = 5.05 V VPRE_PFM_TON_OTP[1:0] = 10 C_{OUT_PRE} ≥ 20 µF (effective value) L_{VPRE} = 2.2 µH at F_{PRE} = 2.25 MHz and L_{VPRE} = 10 µH at F_{PRE} = 450 kHz	-1.5	—	1.5	%
I_{PRE}	Output current capability in PWM mode	—	—	1.5	A
I_{PRE_PFM}	Current capability in PFM mode (Standby mode only)	—	—	150	mA
$\eta_{PEAK\_VPRE\_PWM}$	Efficiency in PWM mode C_{OUT_PRE} = 22 µF with ESR = 2 mΩ L_{VPRE} = 10 µH with RDCR_LVPRE = 60 mΩ F_{PRE} = 450 kHz V_{SUP} = V_{SUP_PWR} = 12 V V_{PREPWM} = 5.4 V with I_{PRE} = 600 mA	—	95	—	%
$\eta_{PEAK\_VPRE\_PFM}$ [1]	Efficiency in PFM mode C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{VPRE} = 10 µH with RDCR_LVPRE = 60 mΩ, F_{PRE} = 450 kHz VSUP = VSUP_PWR = 12 V and 5.4V V_{PREPFM} = 5.05 V with I_{PRE_PFM} = 1 mA VPRE_PFM_TON_OTP[1:0] = 10	—	90	—	%
R_{HS_VPRE}	High-side on-resistance (V_{BOS} = 5 V, including bonding)	—	310	500	mΩ
R_{LS_VPRE}	Low-side on-resistance (V_{BOS} = 5 V, including bonding)	—	170	300	mΩ
R_{PRE_DIS}	Discharge resistor (when VPRE is disabled – LPOFF)	20	40	60	Ω
TSD_{VPRE}	Thermal shutdown threshold	175	—	—	°C
TSD_{VPRE_HYST}	Thermal shutdown threshold hysteresis	5	—	12	°C
I_{OCPRE_FLAG} [2]	DC overcurrent flag threshold in PWM mode VPRE_OC_OTP[2:0] = 000 VPRE_OC_OTP[2:0] = 001 VPRE_OC_OTP[2:0] = 010 VPRE_OC_OTP[2:0] = 011 VPRE_OC_OTP[2:0] = 100 VPRE_OC_OTP[2:0] = 101 VPRE_OC_OTP[2:0] = 110 VPRE_OC_OTP[2:0] = 111	 0.45 0.65 0.85 1.12 1.30 1.49 1.68 1.87	 0.66 0.88 1.1 1.32 1.54 1.76 1.98 2.2	 1.0 1.25 1.45 1.70 1.95 2.12 2.38 2.64	A
I_{LIM_PRE}	VPRE output DC current limitation threshold in PWM mode	1.95	2.42	2.9	A
V_{PRE_OVP}	Main overvoltage protection on VPRE output (relative to VPRE output voltage setting)	20	25	30	%
Dynamic electrical characteristics					
t_{VPRE_OVP}	Overvoltage deglitch time	1	2	3	µs
t_{VPRE_DEAD}	Dead time to avoid cross conduction	1	—	20	ns

Table 116. VPRE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_{PRE_SS}	Soft-start ramp from 0 % to 100 % defined at IPRE = 0 A VPRE_SS_OTP[1:0] = 00 (C_{OUT_PRE} ≤ 44 µF nominal) VPRE_SS_OTP[1:0] = 01 VPRE_SS_OTP[1:0] = 10 VPRE_SS_OTP[1:0] = 11	 200 431 873 1753	 269 538 1077 2150	 410 645 1281 2547	µs
$V_{PRE\_DVS\_DOWN}$	DVS down ramp rate during low-power mode transition VPRE_LP_DVS_OTP[1:0] = 00 (C_{OUT_PRE} ≤ 44 µF nominal) VPRE_LP_DVS_OTP[1:0] = 01 VPRE_LP_DVS_OTP[1:0] = 10 VPRE_LP_DVS_OTP[1:0] = 11	 18 9 4.5 2.25	 22 11 5.5 2.75	 27 13.5 6.75 3.375	mV/µs
$V_{PRE\_LINE\_REG\_450K\_PWM}$	Transient line in PWM mode @ 450 kHz V_{BAT} = 6 V - 18 V – 6 V and 14 V - 35 V - 14 V I_{PRE} = 0 A and 1.5 A for V_{PREPWM} = 3.3 V I_{PRE} = 0 A and 0.6 A for V_{PREPWM} = 5.0 V dV/dt = 100 mV/µs, L_{VPRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_450K\_DO}$	Transient line after drop out exit @ 450 kHz V_{BAT} = V_{PRE} - 0.4 V to 14 V I_{PRE} = 0 A and 0.6 A for V_{PREPWM} = 5.0 V dV/dt = 100 mV/µs, L_{VPRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PWM}$	Transient load response in PWM mode @ 450 kHz 10 mA to 800 mA step and 800 mA to 10 mA step 800 mA to 1.5 A step and 1.5 A to 800 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{VPRE} = 10 µH	-3	—	3	%
$V_{PRE\_LINE\_REG\_2.2M\_PWM}$	Transient line in PWM mode @ 2.25 MHz V_{BAT} = 6 V - 18 V - 6 V and 14 V - 35 V - 14 V I_{PRE} = 0 A and 1.5 A for V_{PREPWM} = 3.3 V I_{PRE} = 0 A and 0.6 A for V_{PREPWM} = 5.0 V dV/dt = 100 mV/µs, L_{VPRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG\_2.2M\_DO}$	Transient line after drop out exit @ 2.25 MHz V_{BAT} = V_{PRE} - 0.4 V to 14 V I_{PRE} = 0 A and 0.6 A for V_{PREPWM} = 5.0 V dV/dt = 100 mV/µs, L_{VPRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_2.2M\_PWM}$	Transient load response in PWM mode @ 2.25 MHz 10 mA to 800 mA step and 800 mA to 10 mA step 800 mA to 1.5 A step and 1.5 A to 800 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{VPRE} = 2.2 µH	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_HV}$[1]	Transient line in PFM mode @ 450 kHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE} = 10 µA and 10 mA for V_{PREPFM} = 5.05 V dV/dt = 100 mV/µs, L_{VPRE} = 10 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_450K\_PFM\_LV}$[1]	Transient line in PFM mode @ 450 kHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE} = 10 µA and 10 mA for V_{PREPFM} = 5.05 V dV/dt = 100 mV/µs, L_{VPRE} = 10 µH, Cin = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%

Table 116. VPRE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{PRE\_LINE\_REG\_450K\_PFM\_DO}$ [1]	Transient line after drop out exit @ 450 MHz V_{BAT} = V_{PRE} - 0.4 V to 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE} = 10 µA and 10 mA for V_{PREPFM} = 5.05V dV/dt = 100 mV/µs, L_{VPRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PFM\_150m}$ [1]	Transient load response in PFM mode @450 kHz 10 mA to 100 mA step and 100 mA to 10 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{VPRE} = 10 µH VPRE_PFM_TON_OTP[1:0] = 10	-3	—	3	%
$V_{PRE\_LOTR\_450K\_PFM\_10m}$ [1]	Transient load response in PFM mode @ 450 kHz VSUP = V_{SUP_PWR} = 5.4 V, V_{PRE} = 5.05 V 10 µA to 10 mA step and 10 mA to 10 µA step di/dt = 10 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{VPRE} = 10 µH VPRE_PFM_TON_OTP[1:0] = 10	-1.5	—	1.5	%
$V_{PRE\_LINE\_REG 2.2M\_PFM\_HV}$ [1]	Transient line in PFM mode @ 2.25 MHz V_{BAT} = 12 V - 28 V – 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE} = 10 µA and 10 mA for V_{PREPFM} = 5.05 V dV/dt = 100 mV/µs, L_{VPRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_2.2M\_PFM\_LV}$ [1]	Transient line in PFM mode @ 2.25 MHz V_{BAT} = 6 V - 12 V – 6 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE} = 10 µA and 10 mA for V_{PREPFM} = 5.05 V dV/dt = 100 mV/µs, L_{VPRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LINE\_REG\_2.2M\_PFM\_DO}$ [1]	Transient line after drop out exit @ 2.25 MHz V_{BAT} = V_{PRE} - 0.4 V to 12 V VPRE_PFM_TON_OTP[1:0] = 10 I_{PRE} = 10 µA and 10 mA for V_{PREPFM} = 5.05V dV/dt = 100 mV/µs, L_{VPRE} = 2.2 µH, C_{IN_PRE} = 47 µF + PI filter, C_{OUT_PRE} = 44 µF	-3	—	3	%
$V_{PRE\_LOTR\_2.2M\_PFM\_100m}$ [1]	Transient load response in PFM mode @ 2.25 MHz 10 mA to 100 mA step and 100 mA to 10 mA step di/dt = 300 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{VPRE} = 2.2 µH VPRE_PFM_TON_OTP[1:0] = 10	-3	—	3	%
$V_{PRE\_LOTR\_2.2M\_PFM\_10m}$ [1]	Transient load response in PFM mode @ 2.25 MHz V_{SUP} = V_{SUP_PWR} = 5.4 V, V_{PRE} = 5.05V 10 µA to 10 mA step and 10 mA to 10 µA step di/dt = 10 mA/µs, C_{OUT_PRE} ≥ 22 µF, L_{VPRE} = 2.2 µH VPRE_PFM_TON_OTP[1:0] = 10	-1.5	—	1.5	%
F_{PRE}	Operating frequency in PWM mode VPRE_CLK_OTP = 0 VPRE_CLK_OTP = 1	 390 1.90	 450 2.25	 500 2.5	 kHz MHz
t_{PRESW_SLR}	Switching node rising and falling edge setting VPRE_SR_OTP = 0 VPRE_SR_OTP = 1	 — —	 — —	 2 4	ns
$t_{PRE\_ON\_MIN\_450K}$	HS minimum ON time in PFM mode @ 450 kHz VPRE_CLK_OTP = 0, V_{PREIN} = 12 V VPRE_PFM_TON_OTP[1:0] = 00 VPRE_PFM_TON_OTP[1:0] = 01 VPRE_PFM_TON_OTP[1:0] = 10 VPRE_PFM_TON_OTP[1:0] = 11	 715 800 875 975	 900 1000 1125 1250	 1080 1250 1375 1525	ns

Table 116. VPRE electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description		Min	Typ	Max	Unit
$t_{PRE\_ON\_MIN\_2.2M}$	HS minimum ON time in PFM mode @ 2.25 MHz VPRE_FREQ_OTP = 1, V_{PREIN} = 12 V VPRE_PFM_TON_OTP[1:0] = 00 VPRE_PFM_TON_OTP[1:0] = 01 VPRE_PFM_TON_OTP[1:0] = 10 VPRE_PFM_TON_OTP[1:0] = 11		 350 385 420 470	 440 500 550 600	 530 620 690 755	ns
$t_{PRE\_OFF\_MIN}$	HS minimum OFF time in PFM mode V_{PREIN} = 12 V VPRE_PFM_TOFF_OTP[1:0] = 10		465	720	1035	ns
External components						
L_{VPRE}	VPRE_SW = 450 kHz	Nominal[3] Inductor value	8.2	10	10	µH
		Effective[4] Inductor value	5.8	—	13	
	VPRE_SW = 2.25 MHz	Nominal[3] Inductor value	2.2	2.2	4.7	
		Effective[4] Inductor value	1.5	—	6.1	
R_{DCR_LVPRE}	Inductor DC resistance		—	60	—	mΩ
C_{IN_PRE}	Effective[4] input capacitor value		10	—	—	µF
C_{BOOT_PRE}	Nominal[3] bootstrap capacitor value		22	22	22	nF
	Effective[4] bootstrap capacitor value		15	—	30	
C_{OUT_PRE}	Effective[4] output capacitor value @ 450 kHz		20	—	100	µF
	Effective[4] output capacitor value @ 2.25 MHz		20	—	50	

[1] For all these parameters, the maximum ambient temperature is T_A = 85 °C.
[2] VPREOC flag is correctly reported for V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 18 V.
[3] For all regulators, the nominal value is the value normalized.
[4] For all regulators, the effective value is the value after tolerance, DC bias and aging removal.

20.2.1 VPRE efficiency in forced PWM mode

For information, VPRE efficiency versus current load measurement is given based on external components and configuration listed below. If the conditions are different, the new efficiency should be calculated using the FS26 GUI POWER tool.

Table 117. VPRE efficiency in forced PWM mode

Ext. C and L		
C_{IN_PRE}	20	µF
$C_{IN\_PRE\_ESR}$	5	mΩ
C_{OUT_PRE}	44	µF
$C_{OUT\_PRE\_ESR}$	2.5	mΩ
L_{VPRE_450kHz}	10	µH
$L_{VPRE\_DCR\_450kHz}$	75	mΩ
$L_{VPRE\_2.25MHz}$	2.2	µH
$L_{VPRE\_DCR\_2.25MHz}$	40	mΩ
C_{BOOT_PRE}	22	nF
Int. MOSFETs		
R_{HS_VPRE}	310	mΩ
Q_{HS}	0.8	nC
R_{LS_VPRE}	170	mΩ
Q_{LS}	1	nC

Table 117. VPRE efficiency in forced PWM mode...*continued*

Ext. C and L		
LS_{BODY_DIODE}	0.8	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{PRE_IN}	14	V
$V_{PRE\_SR\_OTP}$		0b00

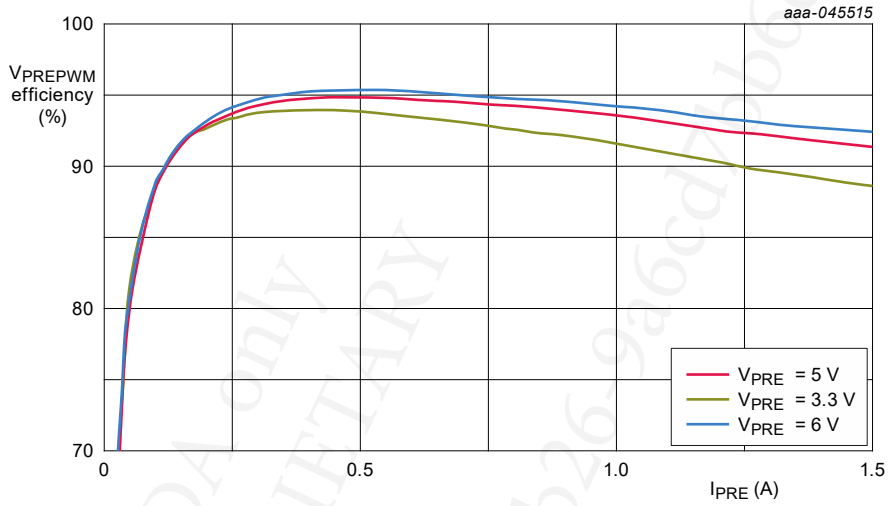


Figure 26. VPRE efficiency at VPRE_CLK_OTP = 0

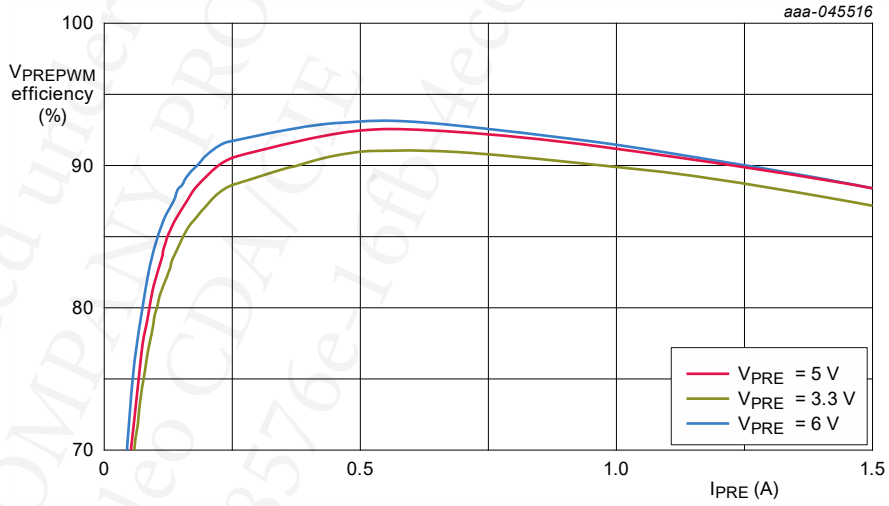


Figure 27. VPRE efficiency at VPRE_CLK_OTP = 1

20.3 Boost controller: VBST

The VBST block is an asynchronous, current mode boost controller. VBST works in forced PWM mode. The output voltage is configurable by OTP and the switching frequency is 450 kHz. A peak overcurrent detection is implemented using the voltage

sensed across R_{SNS_BST}. The overcurrent detection can be selected with $V_{BST\_ILIM\_OTP}$ divided by R_{SNS_BST}.

When the VBST_FB pin is disconnected, by means of $V_{BST\_FB} < V_{BST\_UV\_TH}$, the boost controller is stopped after t_{BST_UVOV}. VBST will restart automatically when $V_{BST\_FB} > V_{BST\_UV\_TH}$.

A maximum duty cycle protection is implemented in order to protect the boost controller in case of bad component selection.

Two boost topologies (front-end and back-end) are supported:

1. **In Front-End mode (VBST_CFG_OTP = '0'):**
   When VBST is used as the front-end supply, the battery voltage (V_{BAT}) is applied at the input of the boost controller. During normal operation with $V_{SUP} > V_{BST\_OTP}$, the boost controller stops switching and operates in Pass-Through mode. When V_{SUP} drops below the VBST regulation threshold, the boost controller will start switching to regulate the V_{SUP} node to V_{BST_OTP}.
   NXP recommends setting the V_{BST_OTP} output voltage between 6 V and 10 V maximum, to supply VPRE with enough headroom during cranking pulses. If a higher output voltage is required for the application, the boost should be used in Back-End mode.
   In the front-end configuration, $V_{BST\_OV\_OTP}$ must be set to '0' (Auto-enable). In Auto-Enable mode, VBST will stop switching automatically when $V_{BST} > V_{BST\_OV\_TH}$, and will resume switching when V_{BST} drops below V_{BST_OTP}.
   In the front-end configuration, the boost will be enabled only during cranking events. To avoid a latent fault, the V_{BST_TMD} bit can be used to force VBST to regulate at 17 V, no matter what the battery voltage is. This allows verification of V_{BST} availability using the VBST_S status flag.
   An open drain output pin called VBST_PG is available to indicate the boost controller activity. This open drain pin should be connected externally to the VDDIO voltage through a resistor. When VBST_PG is high (open drain OFF) it indicates that the boost controller is switching. When VBST is operating in pulse skipping mode, VBST PG behavior may not be guaranteed. When VBST_PG is low (open drain ON) it indicates that the boost controller is not switching or disabled.
   The V_{BST} current limitation is sensed at the input and therefore the current capability can be estimated depending on V_{BST_IN}, the V_{BST} voltage configuration and the external components (L_{BST}, R_{SNS_BST}, D_{BST}). As an example, Table 118 summarizes the maximum current capability during a cranking operation using L_{BST} = 4.7 µH and the recommended R_{SNS_BST} for C_{OUT_BST} = 40 µF.

Table 118. Maximum VBST output current in front-end configuration (DC_{BST_MAX} = 87.5 %, D_{BST} = 0.7 V, LS_{RDSON} = 50 mΩ, L_{BST_DCR} = 60 mΩ)

V_{BST_IN}	V_{BST}	V_{ILIM_TH} / R_{SNS_BST}	Maximum I_{BST}
2.7 V	6 V	180 mV / 20 mΩ	1.9 A
		150 mV / 20 mΩ	1.7 A
		120 mV / 20 mΩ	1.4 A
		60 mV / 20 mΩ	0.7 A
	7 V	180 mV / 20 mΩ	1.65 A
		150 mV / 20 mΩ	1.45 A
		120 mV / 20 mΩ	1.2 A

Table 118. Maximum VBST output current in front-end configuration (DC_{BST_MAX} = 87.5 %, D_{BST} = 0.7 V, LS_{RDSON} = 50 mΩ, L_{BST_DCR} = 60 mΩ)*...continued*

V_{BST_IN}	V_{BST}	V_{ILIM_TH} / R_{SNS_BST}	Maximum I_{BST}
		60 mV / 20 mΩ	0.6 A
	8 V	180 mV / 20 mΩ	1.45 A
		150 mV / 20 mΩ	1.25 A
		120 mV / 20 mΩ	1.05 A
		60 mV / 20 mΩ	0.5 A

2. **In Back-End mode or boost not used (VBST_CFG_OTP = '1'):**
In the back-end configuration, V_{BST} can be supplied by V_{PRE} or by an external supply. When V_{BST} is supplied by an external supply (VSUP, for example), the maximum duty cycle could limit the output current capability and/or the delta voltage between V_{IN} and V_{BST}.
In the back-end configuration, the output voltage is set by V_{BST_OTP} and NXP recommends setting $V_{BST\_OV\_OTP}$ to '1' (overvoltage protection). In Overvoltage Protection mode, V_{BST} will be disabled if an overvoltage is detected (V_{BST} > $V_{BST\_OV\_TH}$). A SPI command is needed to turn on V_{BST} again.
VBST_PG is indicating a boost overload during soft-start or in normal operation. The power good pin (VBST_PG) can be used to avoid an undervoltage cascading effect at the V_{BST} input (VPRE) by opening the V_{BST} current path. This overload protection feature will require the external circuitry described in the application note AN12995.
During a soft-start, VBST_PG is at the high level (open drain OFF) to enable the external switch and propagate the output voltage to the load. If an overload condition is detected (V_{BST} < $V_{BST\_UV\_PG}$), while the minimum duty cycle is not reached, the V_{BST} power good pin is asserted low to warn of the overload event. The BOOST controller remains enabled until completion of soft-start.
In normal operation, VBST_PG is at the high level (open drain OFF) when the output voltage remains in an acceptable range and at the low level (open drain ON) when the output voltage is 25 % below its nominal voltage (V_{BST} < $V_{BST\_UV\_PG}$).
The V_{BST} current limitation is sensed at the input, and therefore the current capability can be estimated depending on V_{BST_IN}, V_{BST} voltage configuration and external components (L_{BST}, R_{SNS_BST}, D_{BST}). As an example, Table 119 summarizes the maximum current capability for an input average current of 500 mA using L_{BST} = 4.7 µH and the recommended R_{SNS_BST} for C_{OUT_BST} = 40 µF.
When the boost controller is not used in the application, VBST_CFG_OTP and VSUP_UVTH_OTP should both be set to '1.' The unused pins should be handled as described in Section 8.

Table 119. Maximum V_{BST} output current in back-end configuration for an input average current of 500 mA (DC_{BST_MAX} = 87.5 %, Efficiency = 85 %)

V_{BST_IN}	V_{BST}	R_{SNS_BST}	Maximum I_{BST}
3.3 V	7 V	60 mΩ	200 mA
	10 V	40 mΩ	140 mA
	12 V	20 mΩ	115 mA
5 V	7 V	80 mΩ	300 mA
	10 V	60 mΩ	210 mA

Table 119. Maximum V_{BST} output current in back-end configuration for an input average current of 500 mA (DC_{BST_MAX} = 87.5 %, Efficiency = 85 %)*...continued*

V_{BST_IN}	V_{BST}	R_{SNS_BST}	Maximum I_{BST}
	12 V	40 mΩ	175 mA
	15 V	20 mΩ	140 mA
6 V	7 V	100 mΩ	360 mA
	10 V	80 mΩ	250 mA
	12 V	60 mΩ	210 mA
	15 V	40 mΩ	170 mA
	18 V	20 mΩ	140 mA

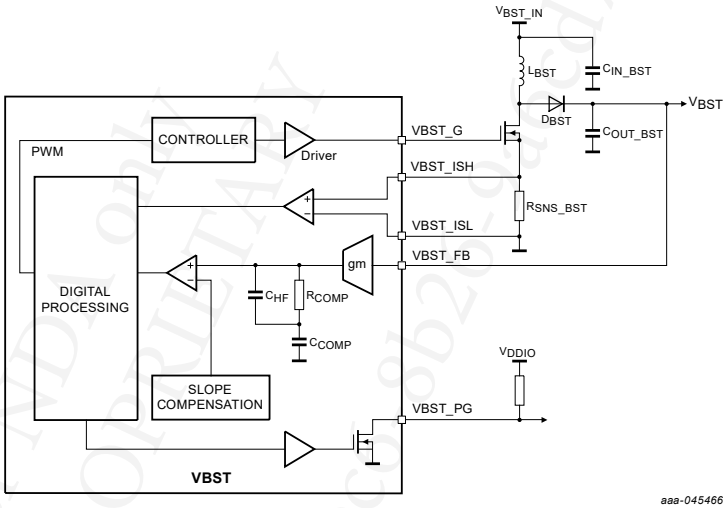


Figure 28. VBST schematic with configuration from VPRE

Table 120. VBST Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{BST_IN}	Input voltage range	2.7	—	40	V
V_{BST}	Output voltage (OTP configuration, 250 mV step)	5	—	18	V
V_{BST_ACC}	Output voltage accuracy	-3	—	3	%
I_{BST}	Nominal output current in front-end VBST_CFG_OTP = 0 (VBST configured as front-end supply) V_{BST} ≤ 10 V and V_{BST_IN} ≥ 2.7 V	—	1	—	A
	Nominal output current in back-end VBST_CFG_OTP = 1 (VBST configured in back-end) V_{BST} ≤ 18 V and V_{BST_IN} ≥ 3.6 V (powered by VPRE)	—	—	0.5	A
$V_{BST\_ILIM\_TH}$	Voltage threshold at V_{BST_ISH} pin to detect an inductor peak current limit condition VBST_ILIM_OTP [1:0] = 00 VBST_ILIM_OTP [1:0] = 01 VBST_ILIM_OTP [1:0] = 10 VBST_ILIM_OTP [1:0] = 11	 48 96 120 144	 60 120 150 180	 72 144 180 216	mV
$V_{BST\_OV\_TH}$	Overvoltage threshold range (sensed on V_{BST_FB} pin)	105	110	115	%

Table 120. VBST Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{BSTG}	VBST_G driver output voltage	V_{PRE_UVBOS} - 0.2	V_{BOS}	5.5	V
R_{BSTG}	VBST_G driver pulldown (when VBST is disabled)	6	14.5	23	kΩ
I_{BSTG}	VBST_G current drive at V_{BOS} = 5 V and VBST_G = VBOS/2 VBSTLS_SR_OTP = 00 VBSTLS_SR_OTP = 01	 0.7 0.9	 — —	 2.0 3.4	A
$V_{BST\_UV\_TH}$	Undervoltage threshold range (sensed on V_{BST_FB} pin)	1.3	1.5	1.7	V
$V_{BST\_UV\_PG}$	VBST undervoltage threshold range to assert VBST_PG pin in back-end mode (sensed on V_{BST_FB} pin)	72.5	75	77.5	%
RPU_{VBST_PG}	External pull-up resistor to VDDIO	5	10	20	kΩ
VOL_{VBST_PG}	Low output level threshold (I_{INTB} = 2.0 mA)	—	—	0.4	V
ILK_{VBST_PG}	Input leakage current	—	—	1.0	µA

Table 120. VBST Electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description		Min	Typ	Max	Unit
Dynamic electrical characteristics						
F_{BST}	Switching frequency range		380	450	500	kHz
t_{BST_UVOV}	$V_{BST\_UV\_TH}$, $V_{BST\_OV\_TH}$ filtering time		5	10	15	µs
DC_{BST_MAX}	Maximum duty cycle VBST_MAX_DC_OTP[1:0] = 00 VBST_MAX_DC_OTP[1:0] = 01 VBST_MAX_DC_OTP[1:0] = 10 VBST_MAX_DC_OTP[1:0] = 11		 — — — —	 72.5 77.5 82.5 87.5	 — — — —	%
t_{BST_SS}	Soft start from VBST enable to 100 % in front-end Soft start from V_{PRE} - D_{BST} to 100 % in back-end					
	VBST_SS_OTP[1:0] = 00	Output Voltage from VBST enable to 100 %		425	600	µs
		Digital DAC soft start completion		1150	1250	µs
	VBST_SS_OTP[1:0] = 01	Output Voltage from VBST enable to 100 %		850	1200	µs
		Digital DAC soft start completion		2300	2500	µs
	VBST_SS_OTP[1:0] = 10	Output Voltage from VBST enable to 100 %		1700	2400	µs
		Digital DAC soft start completion		4600	5000	µs
	VBST_SS_OTP[1:0] = 11	Output Voltage from VBST enable to 100 %		3400	4800	µs
		Digital DAC soft start completion		9200	10100	µs
$V_{BST\_LINE\_ON}$	VBST transient line in front end configuration always ON V_{BAT} = 3.2 V - 6.5 V - 3.2 V dv/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF		-5	—	5	%
$V_{BST\_LINE\_OFF\_ON}$	VBST transient line in front end configuration with OFF/ON transition V_{BAT} = 12.5 V - 6.5 V dv/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF		-5	—	—	%
$V_{BST\_LINE\_ON\_OFF}$	VBST transient line in front end configuration with ON/OFF transition V_{BAT} = 6.5 V - 12.5 V dv/dt = 100 mV/µs , L_{BST} = 4.7 µH, I_{BST} = 0 A and 1 A $C_{IN\_BST\_FE}$ = 47 µF, $C_{OUT\_BST\_FE}$ = 50 µF		—	—	1.5	V
$V_{BST\_LOTR\_FE}$	Transient load response in Front end mode 200 mA to 1 A step and 1 A to 200 mA step, di/dt = 800 mA/µs $C_{OUT\_BST\_FE}$ = 40 µF, L_{BST} = 4.7 µH, $C_{IN\_BST\_FE}$ = 20 µF 2.7 V ≤ V_{BST_IN} ≤ V_{BST} - 1 V, V_{BST} = 7 V		-10	—	10	%
$V_{BST\_LOTR\_BE}$	Transient load response in Back end mode 50 mA to 200 mA step and 200 mA to 50 mA step, di/dt = 150 mA/µs $C_{OUT\_BST\_BE}$ = 22 µF, L_{BST} = 4.7 µH, $C_{IN\_BST\_BE}$ = 44 µF V_{BST_IN} = 4.5 V, V_{BST} = 14 V		-5	—	5	%
t_{ON_MIN}	LS minimum ON time VBST_TON_MIN_OTP[1:0] = 00		153	200	235	ns
External components						
L_{BST}	F_{BST} = 450 kHz	Nominal[1] Inductor value	4.7	4.7	4.7	µH
		Effective[2] Inductor value	3.3	—	6.1	
L_{BST_DCR}	InductorDC resistance		—	60	—	mΩ
R_{SNS_BST}	Nominal[1] current sense resistor value (±1 %)		20	—	100	mΩ
D_{BST}	Diode forward voltage drop		—	0.4	—	V
L_{SRDSON}	Low-side MOSFET RDSON		—	50	—	mΩ
$C_{IN\_BST\_FE}$	Effective[2] input capacitor value for VBST in front-end		10	—	—	µF
$C_{IN\_BST\_BE}$	Effective[2] input capacitor value for VBST in back-end (in addition to C_{OUT_PRE})		10	—	—	µF

Table 120. VBST Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$C_{OUT\_BST\_FE}$	Effective[2] output capacitor value for VBST in front-end	20	—	150	µF
$C_{OUT\_BST\_BE}$	Effective[2] output capacitor value for VBST in back-end	20	—	80	µF

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective value is the value after tolerance, DC bias and aging removal.

20.3.1 VBST efficiency

VBST efficiency vs. current load measurement is shown in Table 121 based on external components and the configuration listed below. If the conditions are different, calculate the efficiency using the FS26 GUI POWER tool.

Table 121. VBST efficiency measurement settings

Ext. Components		
$C_{IN\_BST\_BE}$	22	µF
$C_{IN\_BST\_BE\_ESR}$	2.5	mΩ
$C_{OUT\_BST\_BE}$	44	µF
$C_{OUT\_BST\_BE\_ESR}$	1	mΩ
L_{BST}	4.7	µH
L_{BST_DCR}	60	mΩ
R_{SNS_BST}	20	mΩ
D_{BST}	0.5	V
Ext. MOSFET		
LS_{RDSON}	30	mΩ
Q_{LS}	7	nC
LS_{BODY_DIODE}	0.7	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{BST_IN}	6	V
F_{BST}	450	kHz
VBSTLS_SR_OTP		0b01
VBST_ILIM_OTP		0b11
VBST_MAX_DC_OTP		0b11

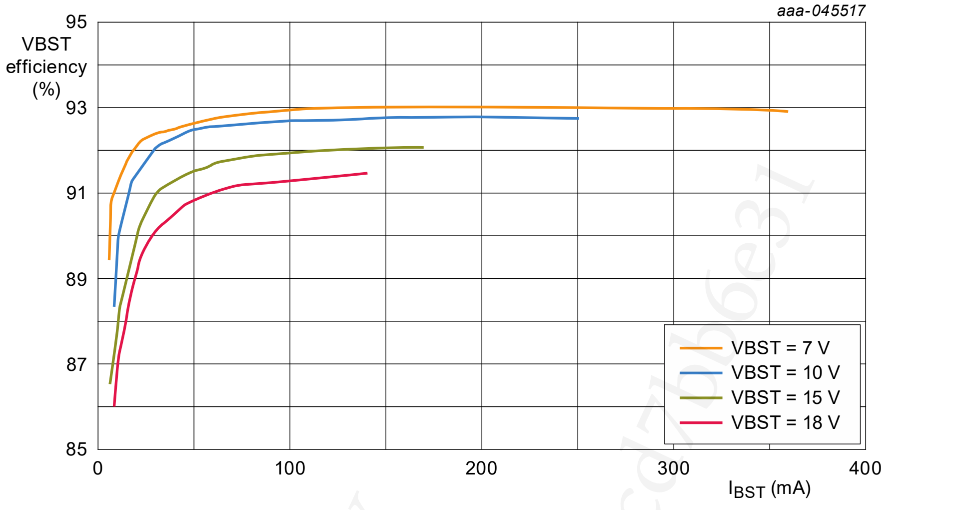


Figure 29. VBST efficiency in back-end mode

20.4 Low-voltage buck regulator: VCORE

The VCORE block is a low-voltage integrated synchronous buck operating in forced PWM mode and using internal FETs. The output voltage is configurable by OTP in a range from 0.8 V to 3.35 V, and the switching frequency is 2.25 MHz. Compensation is ensured by internal circuitry.

A dynamic voltage scaling (DVS) feature is configurable by OTP, to control the ramp-up and ramp-down of the regulator. The passive pulldown resistor is enabled during the ramp down.

The current in the inductor is sensed via the internal FETs. A thermal shutdown is implemented to protect the internal FETs. When the current in the inductor rises above the I_{PEAK_CORE} threshold configured with the CORE_ILIM_OTP[1:0] bits, the SPI bit COREOC_I is set. This overcurrent detection does not turn OFF the VCORE but will induce a duty cycle reduction and therefore an output voltage drop.

During the overcurrent condition, the regulator switching frequency may be divided by 2. The regulator will be back to its nominal switching frequency when the overcurrent condition is removed. When the lower CORE_ILIM_OTP[1:0] setting is selected, it is recommended to select L_{CORE} at 1.5 µH or 2.2 µH.

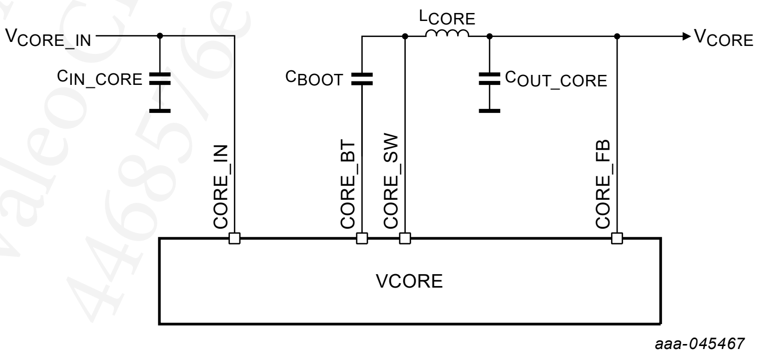


Figure 30. VCORE schematic

Table 122. VCORE electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{CORE_IN}	Input voltage range	2.5	—	6.35	V
V_{CORE}	Output voltage (OTP configuration, 10 mV step)	0.8	—	3.35	V
I_{CORE}	Output current capability FS260x and FS261x FS262x and FS263x	 —	 —	 0.8 1.65	 A
V_{CORE_ACC}	Output voltage accuracy I_{OUT} ≤ 1.5 A 1.5 A < I_{OUT} ≤ 1.65 A	 -2 -2.5	 —	 2 2.5	 %
V_{CORE_HDR}	Minimum headroom (V_{COREIN} – V_{CORE}) I_{CORE} ≤ 800 mA I_{CORE} ≤ 1.5 A I_{CORE} ≤ 1.65 A	 400 800 900	 —	 —	 mV
$I_{PEAK\_CORE\_08}$	Inductor peak current limitation for FS260x and FS261x CORE_ILIM_OTP[1:0] = 00 CORE_ILIM_OTP[1:0] = 01 = 10 = 11	 0.9 1.15	 1.4 1.7	 1.9 2.3	 A
$I_{PEAK\_CORE\_165}$	VCORE inductor peak current limitation for FS262x and FS263x CORE_ILIM_OTP[1:0] = 00 CORE_ILIM_OTP[1:0] = 01 CORE_ILIM_OTP[1:0] = 10 CORE_ILIM_OTP[1:0] = 11	 0.9 1.15 2.0 2.5	 1.4 1.7 2.7 3.4	 1.9 2.2 3.4 4.3	 A
η_{PEAK_VCORE}	Peak efficiency in PWM mode V_{PRE} = 5.5 V, V_{CORE} = 1.5 V, I_{CORE} = 800 mA L_{CORE} = 1 µH with DCR = 30 mΩ C_{OUT_CORE} = 20 µF (effective capacitance)	—	87	—	%
R_{HS_CORE}	High-side MOSFET RDSON (V_{BOS} = 5 V, including bonding)	—	75	150	mΩ
R_{LS_CORE}	Low-side MOSFET RDSON (V_{BOS} = 5 V, including bonding)	—	75	150	mΩ
R_{CORE_DIS}	Discharge resistor (when V_{CORE} is disabled – LP OFF)	50	100	200	Ω
TSD_{CORE}	Thermal shutdown threshold	175	—	—	°C
TSD_{CORE_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical characteristics					
t_{VCORE_DEAD}	Dead time to avoid cross conduction COREHS_SR_OTP[1:0] = 01 COREHS_SR_OTP[1:0] = 10 COREHS_SR_OTP [1:0] = 00 or 11	 10 5 5	 — — —	 40 30 25	 ns
t_{CORESW_HSSRR}[1]	Switching node slew rate (rising)				
	COREHS_SR_OTP[1:0] = 00 COREHS_SR_OTP[1:0] = 01 COREHS_SR_OTP[1:0] = 10 COREHS_SR_OTP[1:0] = 11	2.5 2 2.25 2.5	5 4 4.5 5	— — — —	V/ns
t_{CORESW_HSSRF}[1]	Switching node slew rate (falling)				

Table 122. VCORE electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	COREHS_SR_OTP[1:0] = 00 COREHS_SR_OTP[1:0] = 01 COREHS_SR_OTP[1:0] = 10 COREHS_SR_OTP[1:0] = 11	1 0.25 0.5 1	2.2 0.6 1.2 2.2	— — — —	V/ns
V_{CORE_SS}	Soft start ramp rate from 10 % to 90 % (DVS up and down) CORE_SS_OTP[1:0] = 00 CORE_SS_OTP[1:0] = 01 CORE_SS_OTP[1:0] = 10 CORE_SS_OTP[1:0] = 11 (COUT_CORE < 80 µF nominal)	 2 4 8 16	 2.5 5 10 20	 3 6 12 24	mV/µs
V_{CORE_LOTR1}	Transient load response for V_{CORE} ≥ 1.0 V 10 mA to 800 mA step and 800 mA to 10 mA step with di/dt = 300 mA/µs, C_{OUT_CORE} ≥ 22 µF, L_{CORE} = 1.0 µH	-3	—	3	%
V_{CORE_LOTR2}	Transient load response for VCORE ≤ 1.0 V 10 mA to 800 mA step and 800 mA to 10 mA step with di/dt = 300 mA/µs, C_{OUT_CORE} ≥ 40 µF, L_{CORE} = 1.0 µH	-30	—	30	mV
F_{CORE}	Operating frequency in PWM mode	2.0	2.25	2.50	MHz
$t_{CORE\_ONOFF\_MIN\_P}$	HS minimum ON and OFF time in peak current mode (not including the switching node slew rates)	10	45	80	ns
$t_{CORE\_ONOFF\_MIN\_V}$	HS minimum ON and OFF time in valley current mode (not including the switching node slew rates)	30	55	80	ns
External Components					
L_{CORE}	CORE_LSEL_OTP [1:0] = 00 Nominal[2] inductor value Effective[3] inductor value	 1 0.68	 1 —	 1 1.5	µH
	CORE_LSEL_OTP [1:0] = 01 Nominal[2] inductor value Effective[3] inductor value	 1.5 1	 1.5 —	 1.5 2	
	CORE_LSEL_OTP[1:0] = 10 = 11 Nominal[2] inductor value Effective[3] inductor value	 2.2 1.5	 2.2 —	 2.2 2.9	
R_{DCR_LCORE}	Inductor DC resistance	—	30	—	mΩ
C_{IN_CORE}	Effective[3] input capacitor value	2.2	—	—	µF
C_{BOOT_CORE}	Nominal input capacitor	47	47	47	nF
	Effective[3] bootstrap capacitor value	33	—	62	
C_{OUT_CORE}	Effective[3] output capacitor	20	—	100	µF

[1] Covered by characterization only, at I_{CORE} = 1 A, with KITFS26AEEVM.
[2] For all regulators, the nominal value is the value normalized.
[3] For all regulators, the effective value is the value after tolerance, DC bias and aging removal.

20.4.1 VCORE efficiency

VCORE efficiency vs. current load measurement is shown in Table 123 based on external components and the configuration listed below. If the conditions are different, calculate the efficiency using the FS26 GUI POWER tool.

Table 123. VCORE efficiency measurement settings

Ext. C and L		
C_{IN_CORE}	10	μF
$C_{IN\_CORE\_ESR}$	2.5	mΩ
C_{OUT_CORE}	44	μF
$C_{OUT\_CORE\_ESR}$	2.5	mΩ
L_{CORE}	1	μH
L_{CORE_DCR}	50	mΩ
C_{BOOT_CORE}	47	nF
Int. MOSFETs		
R_{HS_CORE}	75	mΩ
Q_{HS}	1.2	nC
R_{LS_CORE}	75	mΩ
Q_{LS}	0.7	nC
LS_{BODY_DIODE}	0.8	V
V_{DRIVE}	V_{BOS}	V
Configuration		
V_{CORE_IN}	6	V
F_{CORE}	2.25	MHz
COREHS_SR_OTP[1:0]		0b00
CORE_CTRL_OTP		0b0

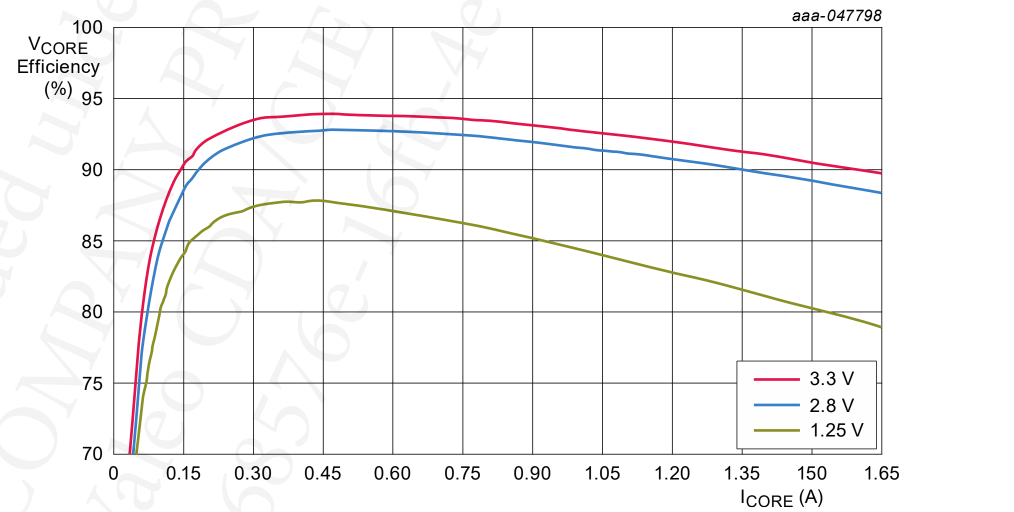


Figure 31. VCORE efficiency

20.5 LDO regulators: LDO1 and LDO2

LDO1 and LDO2 are linear voltage regulators with output voltage between 3.3 V and 5.0 V selectable via OTP, and with up to 400 mA output current capability.

The LDOIN pin is the input voltage supply for both LDO1 and LDO2, and it is intended to be connected to the VPRE output. An overcurrent detection and a thermal shutdown protection are integrated in each LDO.

These regulators are intended to supply microcontroller rails, CAN or FLEXRAY transceivers, as well as other integrated circuits within the ECU.

During Standby mode, LDOs can be enabled (based on OTP configuration) with minimum additional power consumption.

When the output current rises above the I_{LIM_LDOX} threshold, the corresponding SPI bit LDOxOC_I is set. An overcurrent detection does not turn OFF the corresponding LDO, but will induce an output voltage drop.

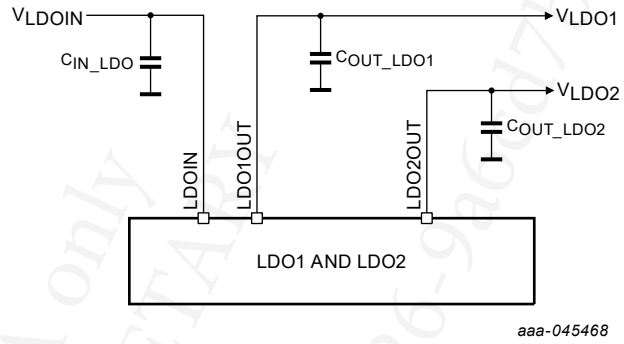


Figure 32. LDOx block diagram

Table 124. LDOx Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{LDOIN}	Input voltage range	V_{LDOx} + $V_{LDOx\_HDR\_NORMAL}$	—	6.35	V
$V_{LDOx\_HDR\_NORMAL}$	Minimum headroom in Normal mode (V_{LDOIN} – V_{LDOx}) 0 mA ≤ I_{LDOx} ≤ 400 mA	350	—	—	mV
$V_{LDOx\_HDR\_STBY}$ [1]	Minimum headroom in Standby mode (V_{LDOIN} – V_{LDOx}) 0 mA ≤ I_{LDOx} ≤ 10 mA	50	—	—	mV
V_{LDOx}	Output voltage in Normal mode				
	VLDOx_OTP = 0 VLDOx_OTP = 1	— —	3.3 5.0	— —	V
$V_{LDOx\_ACC\_NORMAL}$	Output voltage accuracy in Normal mode 0 mA ≤ I_{LDOx} ≤ 400 mA , $V_{LDOx\_HDR\_NORMAL}$ = 350 mV	-1.75	—	1.75	%
$V_{LDOx\_ACC\_STBY}$ [1]	Output voltage accuracy in Standby mode 0 mA ≤ I_{LDOx} ≤ 10 mA , $V_{LDOx\_HDR\_STBY}$ = 50 mV	-1	—	1	%
$V_{LDOx\_VREF\_match}$	LDOx versus VREF matching factor in Normal mode 0 mA ≤ I_{LDOx} ≤ 400 mA , 0 mA ≤ I_{REF} ≤ 30 mA	-1	—	1	%
I_{LDOx}	Nominal current at V_{LDOx} = 5 V V_{LDOx} = 3.3 V and V_{LDOIN} ≤ 5.5 V V_{LDOx} = 3.3 V and V_{LDOIN} > 5.5 V	 — — —	 — — —	 400 400 300	mA
I_{Q_LDOx} [1]	Quiescent current consumption in Low-Power modes $V_{LDOx\_HDR\_STBY}$ = 50mV or 350 mV	—	7	55	µA
I_{LIM_LDOx}	Current limitation threshold reported in LDOx_OC	450		1750	mA
$PSRR_{LDOx\_450kHz}$	Power supply rejection ratio V_{LDOx_HDR} = 350 mV, 1 µA < I_{LDOx} < 400 mA @ 450 kHz	22	—	—	dB
$PSRR_{LDOx\_2.2MHz}$	Power supply rejection ratio V_{LDOx_HDR} = 350 mV, 1 µA < I_{LDOx} < 400 mA @ 2.25 MHz	32	—	—	dB
R_{LDOx_DCHG}	Discharge resistance (when V_{LDOx} is disabled)	—	20	60	Ω
R_{ON_LDOx}	Dropout resistance including bounding			600	mΩ
TSD_{LDOx}	Thermal shutdown threshold	175	—	—	°C
TSD_{LDOx_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical characteristics					
t_{LDOx_TSD}	Thermal shutdown filtering time	3	5	8	µs
V_{LDOx_SS}	Soft start ramp rate	10	20	30	mV/µs

Table 124. LDOx Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
V_{LDOx_LOTR}	Transient load response I_{LDOx} = 10 mA to 200 mA step and 200 mA to 10 mA di/dt = 100 mA/µs C_{OUT_LDOx} = 4.7 µF, C_{IN_LDO} = 1 µF	-3	—	3	%
$V_{LDOx\_LOTR\_STBY\_HI}$	Transient load response in Standby mode I_{LDOx} = 10 mA to 100 mA step and 100 mA to 10 mA di/dt = 100 mA/µs V_{PREPFM} = 5.35 V, V_{LDOx} = 5 V C_{OUT_LDOx} = 4.7 µF, C_{IN_LDO} = 1 µF	-100	—	100	mV
$V_{LDOx\_LOTR\_STBY\_LO}$[1]	Transient load response in Standby mode with reduced headroom I_{LDOx} = 10 µA to 10 mA step and 10 µA to 10 mA di/dt = 10 mA/µs V_{PREPFM} = 5.05 V , V_{LDOx} = 5 V C_{OUT_LDOx} = 4.7 µF , C_{IN_LDO} = 1 µF	-1.5	—	1.5	%
t_{ON_LDOx}	Turn on rise time (soft start ramp)	—	—	500	µs
External components					
C_{IN_LDO}	Effective[2] input capacitor (close to LDO_IN pin)	0.5	—	—	µF
C'_{COUT_LDOx}	Effective[2] output capacitance	2.35	4.7	15	µF

[1] For all these parameters, the maximum ambient temperature is T_A = 85 °C.
[2] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

20.6 Voltage reference: VREF

The VREF block is a high accuracy linear voltage regulator with 0.75 % accuracy over the device operating voltage and temperature range. The VREF output voltage is selectable between 3.3 V and 5.0 V via OTP, with 30 mA output current capability.

The TRKIN pin is the input voltage supply for VREF, and it is intended to be connected to the VPRE output. An overcurrent detection is integrated. When the output current rises above the I_{LIM_REF} threshold, the overcurrent detection does not turn OFF the VREF but will induce an output voltage drop.

VREF is intended to supply the microcontroller ADC reference, and to be the reference for the voltage tracking regulators (TRKx) in the FS26 device.

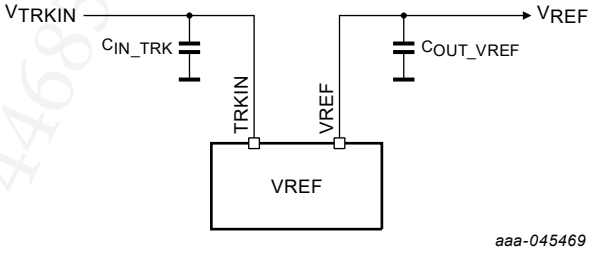


Figure 33. VREF block diagram

Table 125. VREF electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{TRKIN}	Input voltage range	V_{REF} + V_{REF_HDR}	—	6.35	V
V_{REF}	Output voltage VREF_OTP = 0 VREF_OTP = 1	— —	3.3 5.0	— —	V
V_{REF_HDR}	Minimum headroom (V_{TRKIN} – V_{REF})	350	—	—	mV
V_{REF_ACC}	Output voltage accuracy, I_{REF} ≤ 30 mA	-0.75	—	0.75	%
I_{REF}	nominal current capability	—	—	30	mA
I_{LIM_VREF}	Output current limitation	38	—	95	mA
R_{REF_DIS}	Discharge resistor (when V_{REF} is disabled)	80	—	220	Ω
Dynamic electrical characteristics					
V_{REF_SS}	Soft start ramp rate from 10 % to 90 % V_{REF} = 3.3 V V_{REF} = 5.0 V	3.2	—	58	mV/µs
$PSRR_{VREF\_450kHz}$	Power supply rejection ratio V_{REF_HDR} = 350 mV, 100 µA < I_{REF} < 30 mA @ 450 kHz	25	—	—	dB
$PSRR_{VREF\_2.2MHz}$	Power supply rejection ratio V_{REF_HDR} = 350 mV, 100 µA < I_{REF} < 30 mA @ 2.25 MHz	35	—	—	dB
V_{REF_LOTR}	Transient load response I_{REF} = 100 µA to 10 mA step and 10 mA to 100 µA di/dt = 100 mA/µs	-0.5	—	0.5	%
External components					
C_{OUT_VREF}[1]	V_{REF} effective output capacitance	1.1	2.2	3.3	µF

[1] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

20.7 Voltage tracking regulators: TRK1 and TRK2

TRK1 and TRK2 are linear voltage regulators following a known voltage reference. The output voltage of the tracking regulators can track either VREF, LDO2, or an internal LDO reference.

TRK1 and TRK2 are intended to supply sensors located outside the ECU, therefore each voltage tracker is independently protected against short circuit to ground and short circuit to battery. An overcurrent detection and a thermal shutdown protection are integrated in each tracker.

When the output current rises above the I_{TRKx_ILIM} threshold, the corresponding SPI bit TRKxOC_I is set. An overcurrent detection does not turn OFF the corresponding tracker but will induce an output voltage drop.

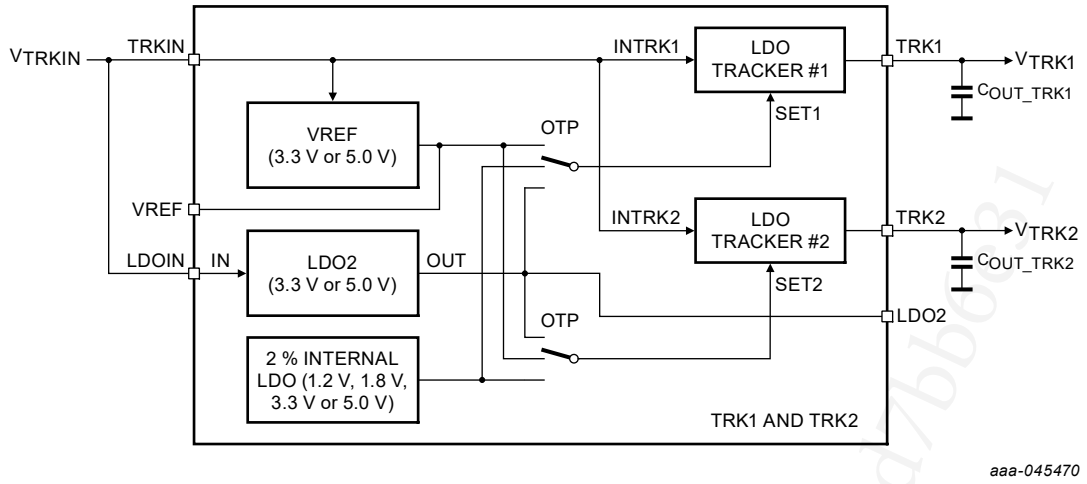


Figure 34. TRK1 and TRK2 block diagram

Table 126. TRKx Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical conditions					
V_{TRKIN}	Input reference voltage range	V_{TRK} + V_{TRKx_HDR}	—	6.35	V
$V_{TRKx\_HDR\_125}$	Minimum headroom (V_{TRKIN} – V_{TRKx}) for I_{TRKx} = 125 mA	350	—	—	mV
$V_{TRKx\_HDR\_150}$	Minimum headroom (V_{TRKIN} – V_{TRKx}) for I_{TRKx} = 150 mA	500	—	—	mV
V_{TRKx}	Output voltage				
	V_{SETx} = V_{REF} = 3.3 V	—	3.3	—	V
	V_{SETx} = V_{REF} = 5.0 V	—	5.0	—	
	V_{SETx} = Internal LDO = 1.2 V	—	1.2	—	
	V_{SETx} = Internal LDO = 1.8 V	—	1.8	—	
	V_{SETx} = Internal LDO = 3.3 V	—	3.3	—	
	V_{SETx} = Internal LDO = 5.0 V	—	5.0	—	
	V_{SETx} = V_{LDO2} = 3.3 V	—	3.3	—	
	V_{SETx} = V_{LDO2} = 5.0 V	—	5.0	—	
V_{TRKx_ACC}	Tracker output voltage accuracy when V_{SETx} = Internal LDO	-2	—	2	%
V_{TRKx_OFF}	Offset voltage between tracker output voltage and tracking reference (V_{TRKx} - V_{SETx}) V_{SETx} = V_{REF} or V_{LDO2} 0 mA < I_{TRKx} < 150 mA	-10	—	10	mV
I_{TRKx}	Output current capability				
	V_{TRKx_HDR} = 500 mV, V_{TRKx} = 3.3 V or 5 V	—	—	150	mA
	V_{TRKx_HDR} = 350 mV, V_{TRKx} = 3.3 V or 5 V	—	—	125	
	V_{TRKx} = 1.2 V or 1.8 V	—	—	65	
I_{TRKx_ILIM}	Output current limitation	160	—	360	mA
I_{TRKx_LEAK}	Reverse current leakage (V_{TRKx} = 40 V). Valid when TRKx is disabled and also in Standby and LPOFF modes.	—	—	1.7	mA
$PSRR_{TRKx\_450KHz}$	Power supply rejection ratio V_{TRKx_HDR} = 350 mV, 100 µA < I_{TRKx} < 125 mA @ 450 kHz C_{OUT_TRKx} [1] = 2.2 µF	20	—	—	dB
$PSRR_{TRKx\_2.2MHz}$	Power supply rejection ratio V_{TRKx_HDR} = 350 mV, 100 µA < I_{TRKx} < 125 mA @ 2.2 MHz C_{OUT_TRKx} [1] = 2.2 µF	25	—	—	dB

Table 126. TRKx Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
R_{TRKx_DCHG}	Discharge resistance (when TRKx is disabled)	-	100	155	Ω
TSD_{TRKx}	Thermal shutdown threshold	175	—	—	°C
TSD_{TRKx_HYS}	Thermal shutdown threshold hysteresis	5	—	12	°C
Dynamic electrical conditions					
t_{TRKX_TSD}	Thermal shutdown filtering time	3	5	8	µs
V_{TRKx_SLR}	Output voltage ramp rate from 10 % to 90 %	6		15	mV/µs
V_{TRKx_LOTR}	Transient load response I_{TRKx} = 100 µA to 125 mA step and 125 mA to 100 µA di/dt = 125 mA/µs	-3	—	3	%
External components					
C_{IN_TRKx}	Effective[1] input capacitor (close to TRKIN pin)	0.5	—	—	µF
C_{OUT_TRKx}	Effective[1] output capacitance	1.1	2.2	10	µF

[1] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

21 System enhancement functions

21.1 Clock management of the Main domain

The main clock management block is comprised of one high-frequency oscillator, one low-frequency system oscillator, and multiple dividers to generate clocking for the internal main digital state machine, for the low-power clock, and for the switching regulators.

The low-frequency oscillator runs at 98 kHz. This oscillator is used for the Long Duration Timer (LDT) and remains ON in Low Power modes to filter the wake-up sources.

The high-frequency oscillator runs at 18 MHz by default. The frequency and the spread spectrum can be configured by SPI to reduce the emission of the oscillator fundamental frequency. The oscillator is used for the SMPS regulators and all the main domain timings. This oscillator is OFF in Low Power modes to reduce the current consumption.

Two frequency dividers provide lower frequency clocks for the switching regulators:

- CLK1 is set at the high-frequency oscillator divided by 8.
- CLK2 is set at the high-frequency oscillator divided by 40.

The frequency of the switching voltage regulators is assigned as shown in Table 127.

Table 127. Switching clock assignment

Regulator	CLK1	CLK2
VBST	No	Yes
VCORE	Yes	No
VPRE	VPRE_CLK_OTP = 1	VPRE_CLK_OTP = 0

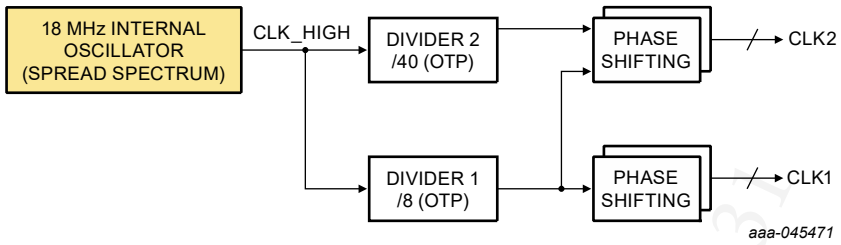


Figure 35. Clock management block diagram

21.1.1 Manual frequency tuning

The internal oscillator frequency runs at 18 MHz by default, and it is configurable via OTP from 16 MHz to 19 MHz with a 1 MHz frequency step. NXP recommends using 18 MHz as a reference value.

Table 128. Manual frequency tuning configuration

CLK_FREQ_OTP[1:0]	High Frequency Oscillator	CLK1	CLK2
00	16 MHz	2.000 MHz	400 kHz
01	17 MHz	2.125 MHz	425 kHz
10 (default)	**18 MHz**	**2.250 MHz**	**450 kHz**
11	19 MHz	2.375 MHz	475 kHz

21.1.2 Phase shifting

The clocks of the switching regulators VPRE, VCORE, and VBST can be delayed to keep all the regulators from turning ON at once. This can reduce peak current and improve EMC performance. Each regulator's clock can be shifted from 1 to 3 clock cycles of the high-frequency clock (configurable by OTP).

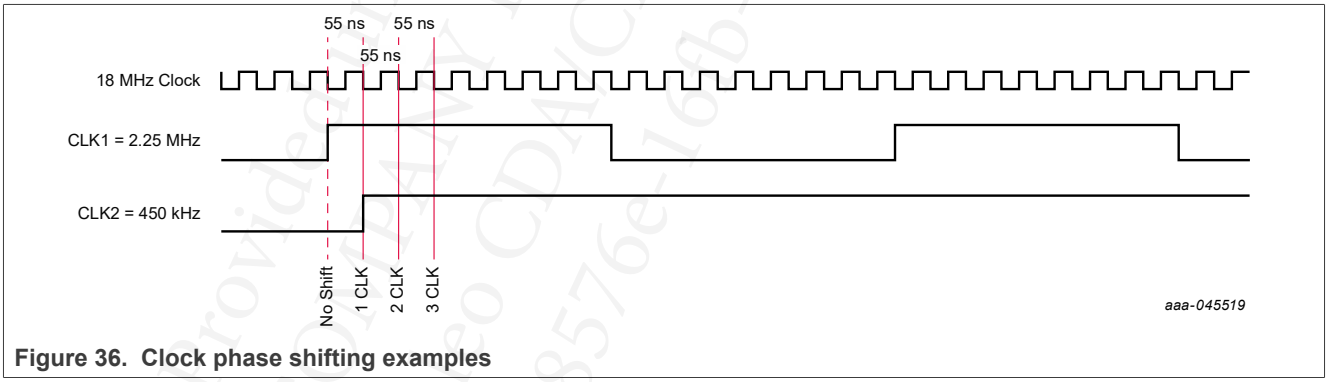


Figure 36. Clock phase shifting examples

21.1.3 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23 kHz or 94 kHz, with a ±5 % deviation range around the oscillator frequency. The spread spectrum feature and the carrier frequency can be selected by SPI. The FSS_EN bit enables the spread spectrum feature and the FSS_FMOD bit selects high- or low-frequency modulation. These two bits are in the M_SYS_CFG SPI register. By default, the spread spectrum feature is disabled.

The main purpose of the spread spectrum feature is to improve EMC performance by spreading out the energy of the internal oscillator and VPRE frequency. Because of this, NXP recommends enabling spread spectrum and selecting the 23 kHz carrier frequency as the default for both VPRE switching frequencies.

Table 129. Clock management electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Internal oscillator					
F_{OSC_HIGH}	High-frequency oscillator (OTP programmable) CLK_FREQ_OTP[1:0] = 00 CLK_FREQ_OTP[1:0] = 01 **CLK_FREQ_OTP[1:0] = 10** CLK_FREQ_OTP[1:0] = 11	 — — — —	 16 17 **18** 19	 — — — —	MHz
$F_{OSC\_HIGH\_ACC}$	High-frequency oscillator accuracy	-6	—	6	%
F_{OSC_LOW}	Low-frequency oscillator	—	98	—	kHz
$F_{OSC\_LOW\_ACC}$	Low-frequency oscillator accuracy	-5	—	5	%
Spread spectrum					
F_{OSC_MOD}	Spread spectrum frequency modulation for 450 kHz CLK_FREQ_OTP[1:0] = 00 (FSS_FMOD = 0, FSS_EN = 1) CLK_FREQ_OTP[1:0] = 01 (FSS_FMOD = 0, FSS_EN = 1) CLK_FREQ_OTP[1:0] = 10 (FSS_FMOD = 0, FSS_EN = 1) CLK_FREQ_OTP[1:0] = 11 (FSS_FMOD = 0, FSS_EN = 1)	 19.5 20.8 22.1 23.3	 20.8 22.1 23.4 24.7	 22.1 23.5 24.9 26.3	kHz
	Spread spectrum frequency modulation for 2.25 MHz CLK_FREQ_OTP[1:0] = 00 (FSS_FMOD = 1, FSS_EN = 1) CLK_FREQ_OTP[1:0] = 01 (FSS_FMOD = 1, FSS_EN = 1) CLK_FREQ_OTP[1:0] = 10 (FSS_FMOD = 1, FSS_EN = 1) CLK_FREQ_OTP[1:0] = 11 (FSS_FMOD = 1, FSS_EN = 1)	 78.4 83.3 88.2 93.1	 83.3 88.5 93.8 99	 88.4 93.9 99.4 105	kHz
$F_{OSC\_MOD\_RANGE}$	Spread spectrum range (around the nominal frequency)	-6	—	6	%

21.2 Analog multiplexer: AMUX

Various internal and application voltages can be monitored through the AMUX pin. Examples include critical FS26 parameters and system level safety parameters. The channel to be monitored can be selected via the SPI. The maximum AMUX output voltage range is V_{DDIO}.

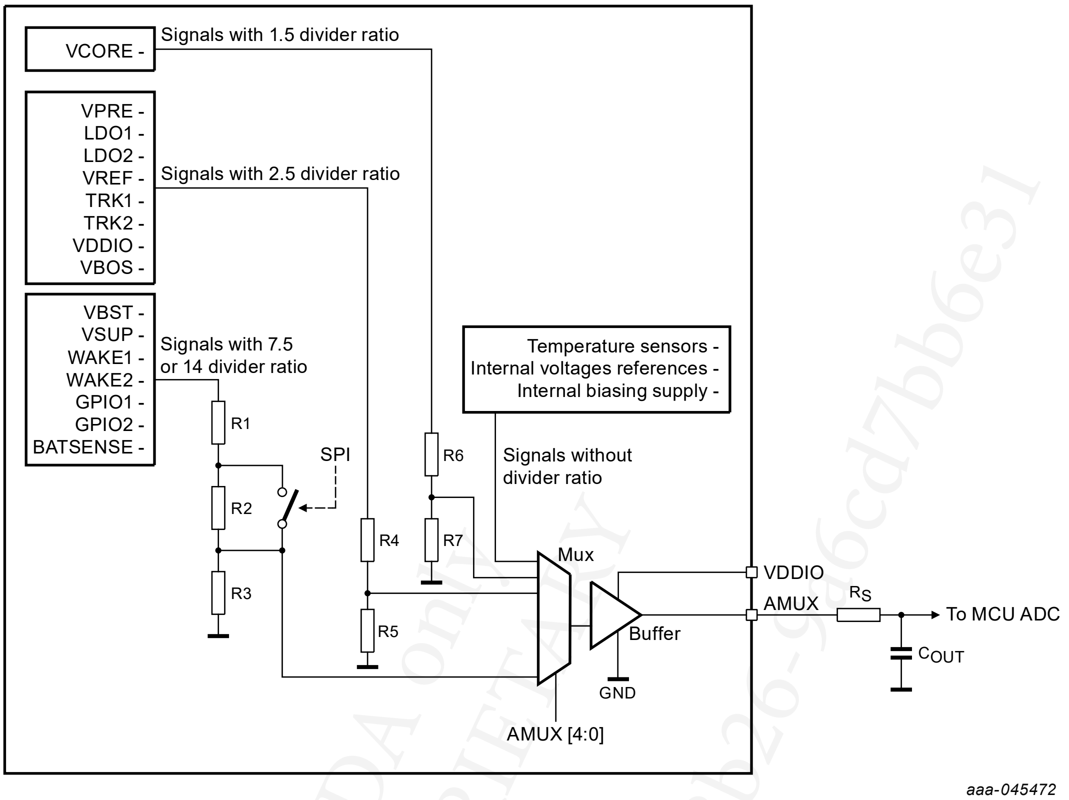


Figure 37. AMUX block diagram

21.2.1 AMUX channel selection

Table 130. AMUX output selection

AMUX_EN	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
0	xxxxx	Disable (AMUX pulled to ground)	N/A	N/A
1	**00000 (default)**	**Disabled with AMUX pin in Hi-Z**	N/A	N/A
1	00001	Low-power bandgap for Main domain (1.0 V ± 0.5 %)	1	1
1	00010	Bandgap for main domain (1.0 V ± 0.5 %)	1	1
1	00011	Bandgap for fail-safe domain (1.0 V ± 0.5 %)	1	1
1	00100	Analog voltage supply for main domain (1.6 V ± 50 mV)	1	1
1	00101	Digital voltage supply for main domain (1.6 V ± 50 mV)	1	1
1	00110	Digital voltage supply for fail-safe domain (1.6 V ± 50 mV)	1	1
1	00111	VCORE voltage	1.5	1.5
1	01000	VPRE voltage	2.5	2.5
1	01001	LDO1 voltage	2.5	2.5
1	01010	LDO2 voltage	2.5	2.5
1	01011	VREF voltage	2.5	2.5
1	01100	TRK1 voltage	2.5	2.5
1	01101	TRK2 voltage	2.5	2.5
1	01110	VDDIO voltage	2.5	2.5

Table 130. AMUX output selection*...continued*

AMUX_EN	AMUX[4:0]	Signal selection for AMUX output	AMUX_DIV = 0	AMUX_DIV = 1
1	01111	VBOS internal voltage	2.5	2.5
1	10000	VBST voltage (divider ratio configurable by SPI)	7.5	14
1	10001	VSUP voltage (divider ratio configurable by SPI)	7.5	14
1	10010	WAKE1 voltage (divider ratio configurable by SPI)	7.5	14
1	10011	WAKE2 voltage (divider ratio configurable by SPI)	7.5	14
1	10100	GPIO1 voltage (divider ratio configurable by SPI)	7.5	14
1	10101	GPIO2 voltage (divider ratio configurable by SPI)	7.5	14
1	10110	BATSENSE pin voltage (divider ratio configurable by SPI)	7.5	14
1	10111	Central die temperature sensor.[1]	1	1
1	11000	VCORE temperature sensor.[1]	1	1
1	11001	VPRE temperature sensor.[1]	1	1
1	11010	LDO1 temperature sensor.[1]	1	1
1	11011	LDO2 temperature sensor.[1]	1	1
1	11100	TRK1 temperature sensor.[1]	1	1
1	11101	TRK2 temperature sensor.[1]	1	1
1	11110	GPIO1 temperature sensor.[1]	1	1
1	11111	Reserved	N/A	N/A

[1] Temp (°C) = (V_{AMUX} – V_{TEMP25}) / V_{TEMP_COEFF} + 25

Table 131. AMUX Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{AMUX_VDDIO}	VDDIO operating voltage range	3.0	—	5.5	V
V_{AMUX_OUT}	Output voltage range	0.3	—	3.0	V
V_{AMUX_IN}	Input voltage range for VSUP, BATSENSE, VBST, WAKE1, WAKE2, GPIO1, GPIO2 Ratio 7.5 Ratio 14	 2.5 4.2	 —	 21 36	V
I_{AMUX}	Output buffer current capability	—	—	1	mA
V_{AMUX_OFF}	Offset voltage (I_{AMUX} = 1 mA)	-7	—	7	mV
V_{AMUX_RATIO}	Ratio accuracy Ratio 1 Ratio 1.5 Ratio 2.5 Ratio 7.5 Ratio 14	 -0.5 -1.5 -1.5 -1.5 -1.5	 — — — — —	 0.5 1.5 1.5 1.5 1.5	%
R_{AMUX_DIV}	Analog multiplexer total bridge resistance for BATSENSE, VSUP, VBST, WAKE1, WAKE2, GPIO1, GPIO2	0.75	1.5	3	MΩ
R_{AMUX_PD}	Analog multiplexer internal pulldown resistance	5	10	20	kΩ
V_{TEMP25}	Temperature sensor voltage at 25 °C	2.01	2.055	2.1	V
V_{TEMP_COEFF}	Temperature sensor coefficient	-6.25	-5.88	-5.5	mV/°C

Table 131. AMUX Electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
T_{AMUX_SET}	Settling time (from 10 % to 90 % of V_{DDIO}, R_S = 220 Ω, C_{OUT} = 10 nF)	—	—	10	µs
External components					
R_S	Nominal output resistor (±10 %)	—	220	—	Ω
C_{out}	Nominal[1] output capacitance	2.2	2.2	10	nF
	Effective[2] output capacitance	1.1	—	15	

[1] For all regulators, the nominal value is the value normalized.
[2] For all regulators, the effective capacitor value is the capacitor value after tolerance, DC bias and aging removal.

21.3 System I/O pins

21.3.1 WAKE1 and WAKE2

WAKE1 and WAKE2 pins are programmable input buffers used to detect wake-up events on either high or low levels. Both WAKEx pins are protected up to 40 V and are suitable to connect to a wake-up signal outside the ECU.

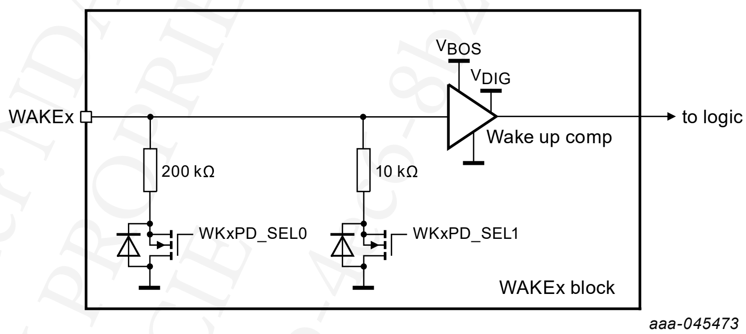


Figure 38. WAKEx pin block diagram

21.3.2 GPIO1 and GPIO2

GPIO1 and GPIO2 are general purpose input/output pins. They can be configured to operate as wake-up inputs, as high-side drivers with up to 20 mA capability, or as low-side drivers with up to 2 mA capability, for use within the ECU. GPIOx configuration can be selected with the GPIOxSTAGE_OTP[1:0] bits.

GPIO1 and GPIO2 low-side drivers can be configured to be either active high or active low with the GPIOxMODE_OTP bit. Active Low mode can be used to directly drive a PMOS gate without inverting the command.

A thermal shutdown protection is implemented on GPIO1. When a thermal shutdown is triggered, GPIO1 is automatically disabled and will remain disabled until the TSD is present (GPIO1TSD_I = 1). When the TSD is gone (GPIO1TSD_I = 0), a SPI command is mandatory to re-enable GPIO1.

Table 132. GPIO mode configuration

GPIOxSTAGE_OTP[1:0]		GPIOxMODE_OTP		GPIO Configuration
0x00	Input configuration	x	—	Output disabled
0x01	Low-side driver	0x00	Active High mode	Low-side driver (Active High)
		0x01	Active Low mode	Low-side driver (Active Low)
0x02	High-side driver	x	—	High-side driver (Active High)
0x03	Push-pull	x	—	Push-pull (Active High)

An internal pullup or pulldown can be enabled by OTP for each GPIO, depending on the GPIOx_STAGE_OTP configuration.. The pull-up resistor is always connected to V_{DDIO}.

GPIO1 can be configured to keep its state in LPOFF or in Standby mode with GPIO1LP_ON SPI bit. GPIO2 can be configured to keep its state in Standby mode with the GPIO2LP_ON bit.

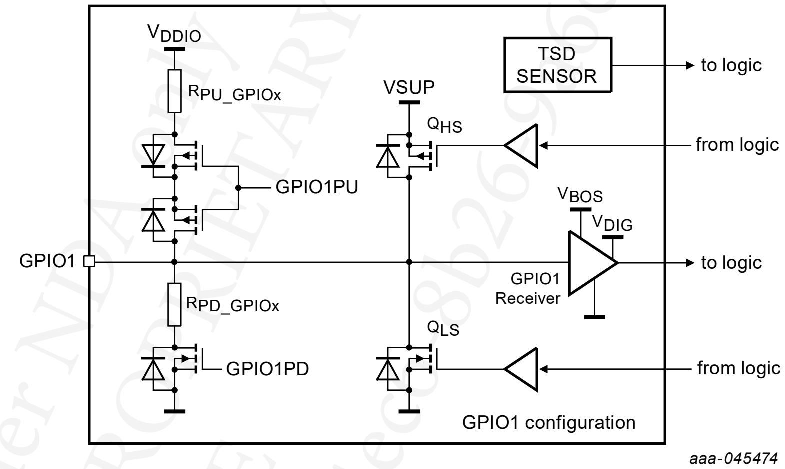


Figure 39. GPIO1 block diagram

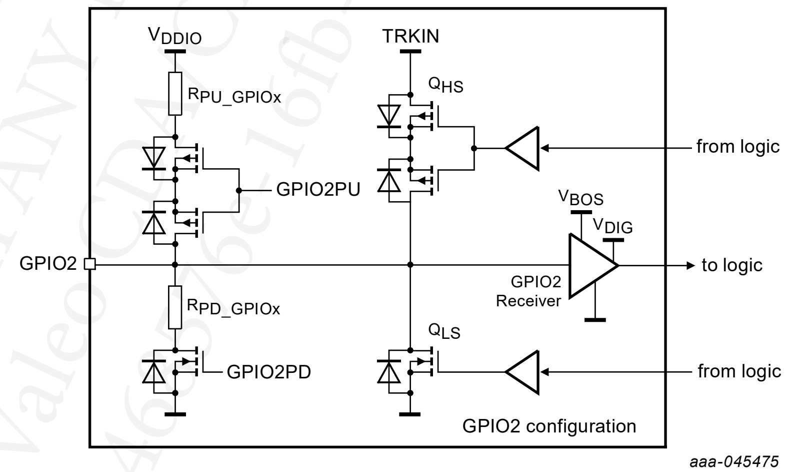


Figure 40. GPIO2 block diagram

21.3.3 GPIO input configuration

When GPIOx is set as input configuration, the pin is set to Hi-Z or Low depending on GPIOxPD_OTP bit. The internal pullup is disabled regardless of the GPIOxPD_OTP bit.

GPIOx pins are protected up to 40 V, and are suitable to connect a wake-up signal outside the ECU.

When a GPIO is used as a global input pin, an RC protection network is required to protect the input. When a GPIO is used as local input pin, a capacitor is required for immunity. Each GPIO voltage can be sensed through the analog multiplexer.

21.3.4 GPIO Active High mode

When GPIOx is set as Active High, as soon as the OTP is loaded, the pin is set to Hi-Z or Low, depending on the GPIOxPD_OTP bit. If the GPIOx is assigned to a slot in the power-up sequence, the pin remains Hi-Z or Low until it reaches the selected slot. Once the selected slot is reached, the GPIOx is asserted high.

In Normal mode, the internal pulldown resistor is disabled regardless of the GPIOxPD_OTP bit when the GPIOx is set as low-side driver.

If the internal pulldown is enabled by OTP, the resistor remains enabled in Low Power modes to avoid floating nodes. The internal pullup resistor should be disabled if the GPIOx is used as a high-side or push-pull driver. Table 133 describes the GPIOx behavior based on the OTP configuration.

Table 133. GPIO Active High mode behavior summary

Configuration	GPIOxPU_ OTP	GPIOxPD_ OTP	Default state after OTP loaded			Normal mode			Standby mode GPIOxLP_ON = 0			LPOFF / DFS GPIOxLP_ON = 0		
			PIN	HS	LS	PIN	HS	LS	PIN	HS	LS	PIN	HS	LS
Low-side Driver	0	0	Low	OFF	ON	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	1	0	Low	OFF	ON	High	OFF	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	0	1	Low	OFF	ON	Hi-Z	OFF	OFF	Low	OFF	OFF	Low	OFF	OFF
	1	1	Low	OFF	ON	High	OFF	OFF	Low	OFF	OFF	Low	OFF	OFF
High-side Driver	-	0	Hi-Z	OFF	OFF	High	ON	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	-	1	Low	OFF	OFF	High	ON	OFF	Low	OFF	OFF	Low	OFF	OFF
Push-pull Driver	-	0	Low	OFF	ON	High	ON	OFF	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	-	1	Low	OFF	ON	High	ON	OFF	Low	OFF	OFF	Low	OFF	OFF

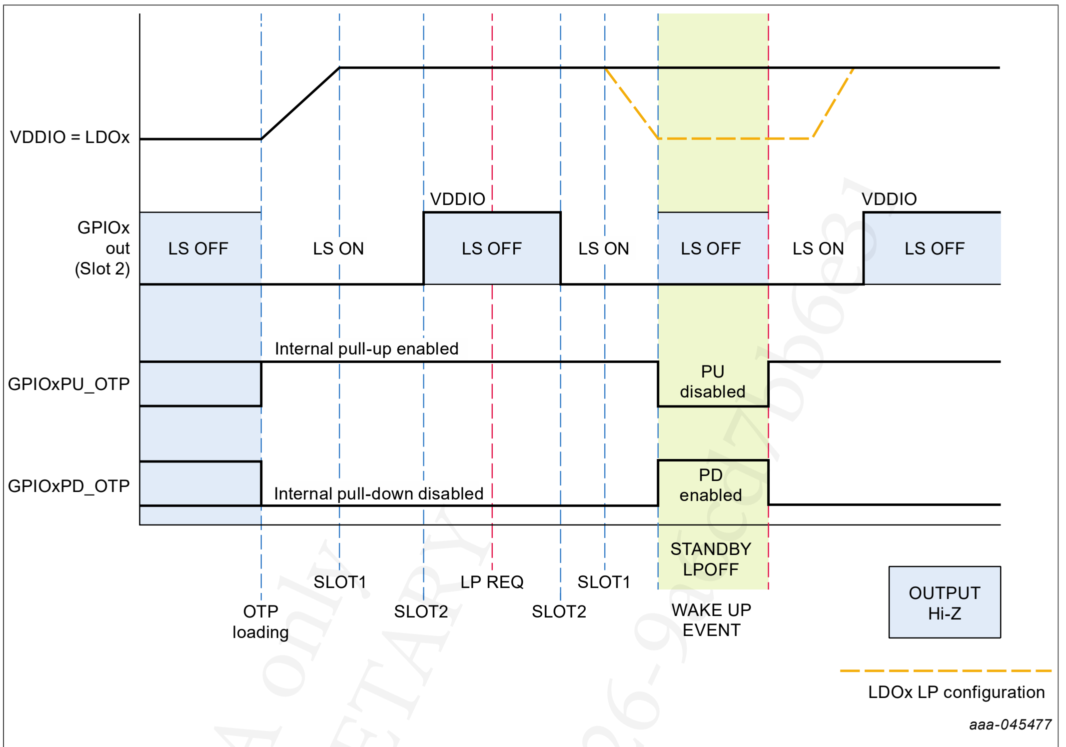

VDDIO = LDOx
GPIOx out (Slot 2)
LS OFF
LS ON
VDDIO
LS OFF
LS ON
LS OFF
LS ON
VDDIO
LS OFF
Internal pull-up enabled
GPIOxPU_OTP
PU disabled
GPIOxPD_OTP
Internal pull-down disabled
PD enabled
STANDBY LPOFF
SLOT1
LP REQ
SLOT1
OTP loading
SLOT2
SLOT2
WAKE UP EVENT
OUTPUT Hi-Z
LDOx LP configuration
aaa-045477

Figure 41. GPIO low-side active high operation. GPIOxMODE_OTP = ‘0’

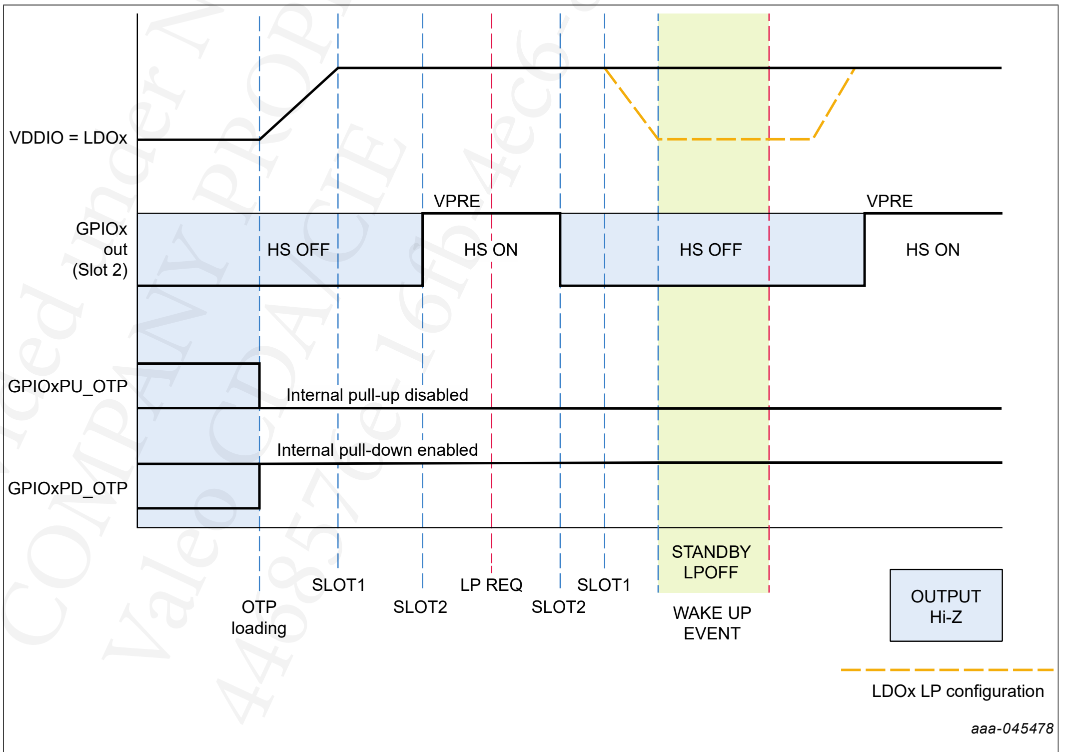

VDDIO = LDOx
VPRE
VPRE
GPIOx out (Slot 2)
HS OFF
HS ON
HS OFF
HS ON
GPIOxPU_OTP
Internal pull-up disabled
Internal pull-down enabled
GPIOxPD_OTP
STANDBY LPOFF
SLOT1
LP REQ
SLOT1
OTP loading
SLOT2
SLOT2
WAKE UP EVENT
OUTPUT Hi-Z
LDOx LP configuration
aaa-045478

Figure 42. GPIO High-side Active High operation. GPIOxMODE_OTP = ‘0’

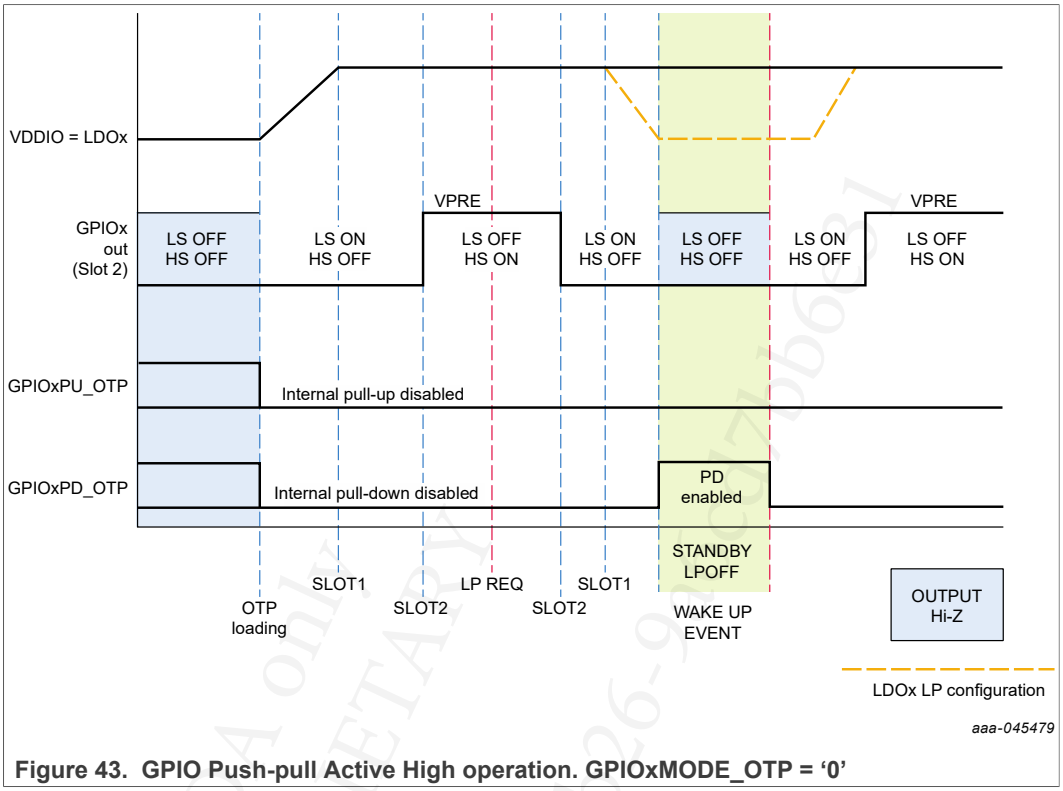


Figure 43. GPIO Push-pull Active High operation. GPIOxMODE_OTP = '0'

21.3.5 GPIO Active Low mode

The Active Low mode is available only when the GPIOx is configured as a low-side driver.

When GPIOx is set as Active Low, as soon as the OTP is loaded, the pin is set to Hi-Z or High, depending on the GPIOx_PU OTP bit. If the GPIOx is assigned to a slot in the power-up sequence, the pin remains High or Hi-Z until it reaches the selected slot. Once the selected slot is reached, the GPIOx low-side driver is asserted low.

In Normal mode, the internal pulldown resistor is disabled regardless of the GPIOxPD_OTP bit when the GPIOx is set as low-side driver. If the internal pulldown is enabled by OTP, the resistor remains enabled in Low Power modes, except in Standby mode, to avoid floating nodes.

Table 134. GPIO Active Low mode behavior summary

Configuration	GPIOxPU_ OTP	GPIOxPD_ OTP	Default state after OTP loaded			Normal mode			Standby mode GPIOxLP_ON = 0			LPOFF / DFS GPIOxLP_ON = 0		
			PIN	HS	LS	PIN	HS	LS	PIN	HS	LS	PIN	HS	LS
Low-side Driver	0	0	Hi-Z	OFF	OFF	Low	OFF	ON	Hi-Z	OFF	OFF	Hi-Z	OFF	OFF
	1	0	High	OFF	OFF	Low	OFF	ON	High	OFF	OFF	Hi-Z	OFF	OFF
	0	1	Hi-Z	OFF	OFF	Low	OFF	ON	Hi-Z	OFF	OFF	Low	OFF	OFF
	1	1	High	OFF	OFF	Low	OFF	ON	High	OFF	OFF	Low	OFF	OFF

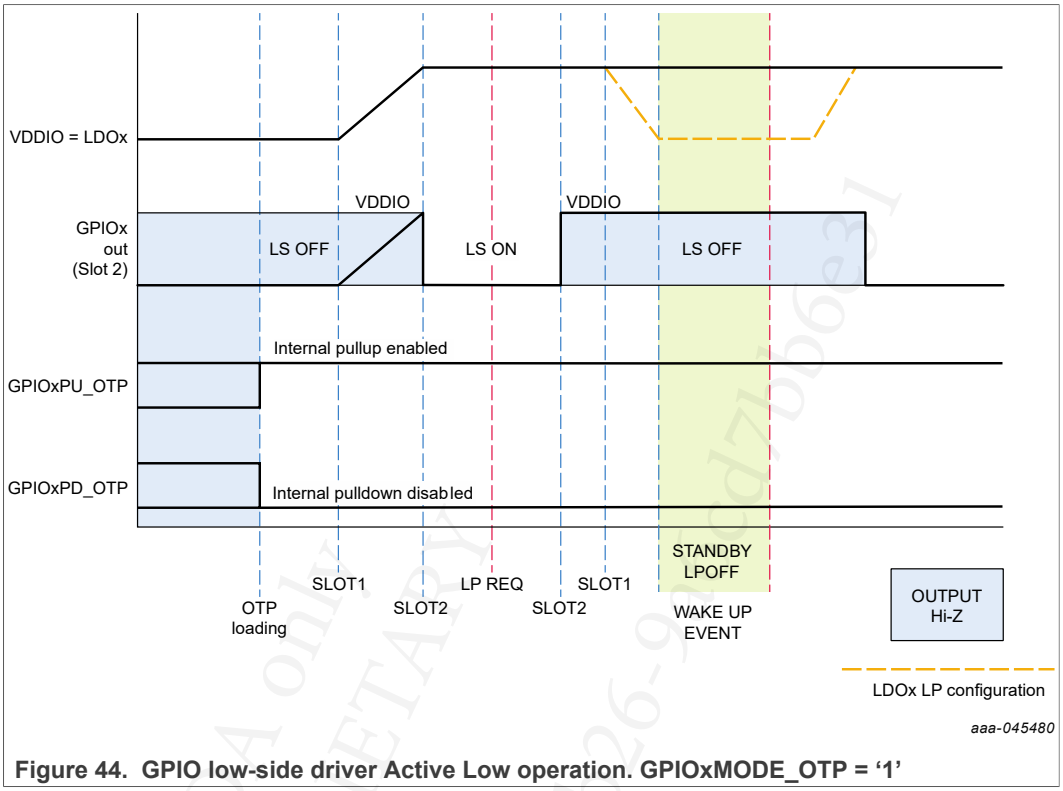


Figure 44. GPIO low-side driver Active Low operation. GPIOxMODE_OTP = '1'

Table 135. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IL_x}	Low input voltage detection Low voltage detection (WKxTH_OTP = 0) High-voltage detection (WKxTH_OTP = 1)	 — —	 — —	 0.8 0.3 * V_{BOS}	V
V_{IH_x}	High input voltage detection threshold Low input threshold (WKxTH_OTP = 0) High input threshold (WKxTH_OTP = 1)	 2 0.7 * V_{BOS}	 — —	 — —	V
V_{IN_HYS}	Threshold hysteresis	50	120	500	mV
I_{WAKE}	Input current on WAKEx and GPIOx pins (LS OFF, HS OFF, No pulldown resistor, wake-up enabled)	—	5	10	µA
T_{WAKE}	Wake-up filtering time	50	70	100	µs
R_{PD_WAKE}	Pulldown resistor on WAKE1 and WAKE2 pins WKxPD_SEL_OTP = 0 WKxPD_SEL_OTP = 1	 100 5	 200 10	 320 15	kΩ
I_{HS_GPIOx}	High-side drive current capability	—	—	20	mA
I_{HS_ILIM}	High-side current limitation threshold	25	50	75	mA
I_{LS_GPIOx}	Low-side drive current capability	—	—	2	mA
I_{LS_ILIM}	Low-side current limitation threshold	3	5	7.5	mA
I_{LEAK_GPIOx}	Input current leakage HS and LS disabled, PU and PD disabled	—	—	10	µA
R_{PU_GPIOx}	Internal pullup resistor value	100	200	320	kΩ
R_{PD_GPIOx}	Internal pulldown resistor value	100	200	320	kΩ
V_{GPIO_DROP}	Drop voltage				

Table 135. Electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	I = 20 mA in the high-side I = 2 mA in the low-side	— —	0.2 0.2	0.6 0.4	V
TSD_{GPIO1}	Thermal shutdown threshold for GPIO1	175	—	—	°C
TSD_{GPIO1_HYS}	Thermal shutdown threshold hysteresis for GPIO1	5	—	12	°C

21.3.6 VCORE PGOOD

GPIO2 can be used to generate a VCORE PGOOD signal to drive an external N-type MOSFET to be able to start with a pre-biased voltage for a non-NXP MCU.

NXP recommends using an external load switch between FS26 VCORE and the MCU input supply. The VCORE power good feature can be enabled by OTP using the GPIO2_VCORE_PGOOD_OTP bit.

When GPIO2 is used as VCORE PGOOD, the HS switch (connected internally to VPRE) is used to close the switch. The power good signal is released as soon as VCORE crosses its undervoltage threshold. VCORE PGOOD is asserted low when VCORE is disabled, or when an error is reported from VCORE voltage monitoring (undervoltage or overvoltage).

An external pulldown is mandatory to assert the pin low when the high-side switch is turned off.

The same GPIO electrical characteristics apply as in Table 135.

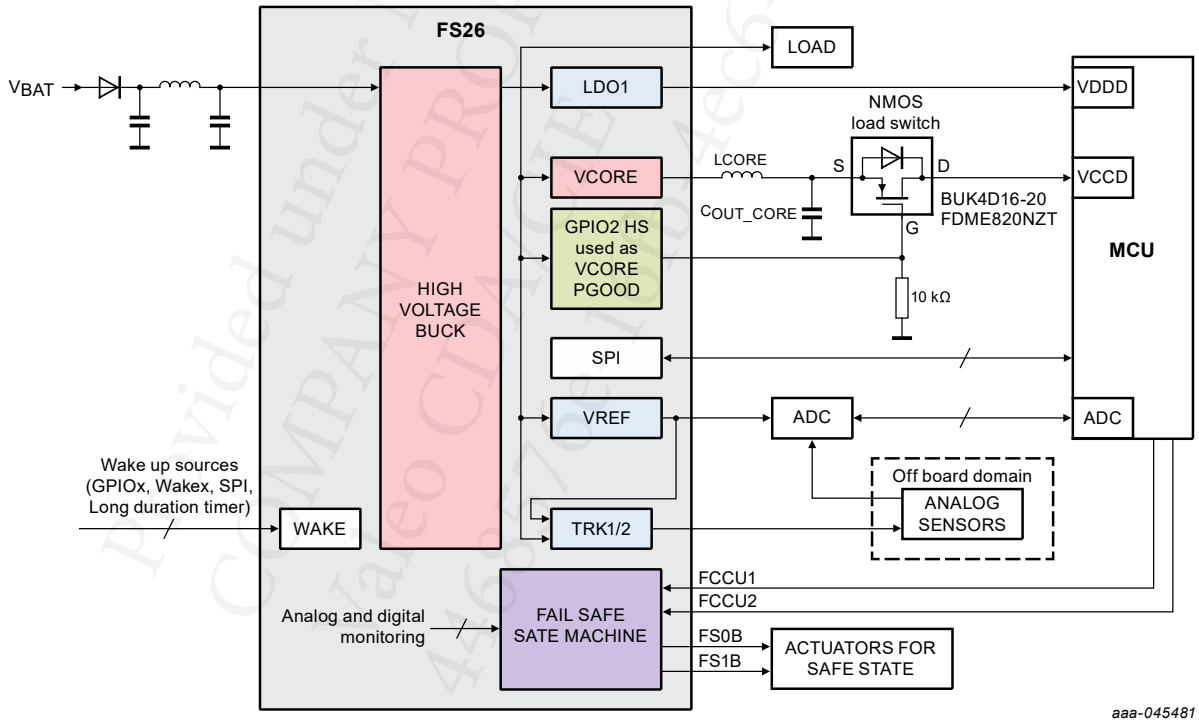


Figure 45. VCORE PGOOD Load switch

21.3.7 INTB

INTB is an open drain output pin with an internal pullup to V_{DDIO}. When an internal interrupt occurs, this pin generates a pulse to inform the microcontroller.

Main interrupts, listed in Table 136, generate a pulse on INTB, if the flag is cleared, and fail-safe interrupts, listed in Table 137, generate a pulse on INTB even if the flag is already set. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in the M_xxx_MASK and FS_INTB_MASK registers.

When the RSTB pin is asserted, interrupts are no longer sent to the MCU until the product goes back to the INIT_FS state.

Table 136 and Table 137 list all interrupt sources that can generate a pulse on the INTB pin.

Table 136. List of Interrupt sources from Main logic

Interrupt name	Corresponding event description
TWARN	Central Temp sensor has crossed the thermal warning threshold on the rising edge
GPIO1TSD	GPIO1 thermal shutdown event occurs
VPRETSD	VPRE thermal shutdown event occurs
TRK2TSD	TRK2 thermal shutdown event occurs
TRK1TSD	TRK1 thermal shutdown event occurs
CORETSD	VCORE thermal shutdown event occurs
LDO2TSD	LDO2 thermal shutdown event occurs
LDO1TSD	LDO1 thermal shutdown event occurs
VBSTOV	VBST_FB has crossed overvoltage threshold
VPREUVH	VPRE crosses it UVH threshold on the falling edge
VBSTOC	VBST overcurrent event occurs
VPREOC	VPRE overcurrent event occurs
TRK2OC	TRK2 overcurrent event occurs
TRK1OC	TRK1 overcurrent event occurs
COREOC	VCORE overcurrent event occurs
LDO2OC	LDO2 overcurrent event occurs
LDO1OC	LDO1 overcurrent event occurs
VBOSUVH	VBOS has crossed its UVH threshold on the falling edge
VSUPOV	VSUP has crossed its overvoltage threshold on the rising edge
VSUPUV6	VSUP has crossed its V_{SUPUV6} threshold on the falling edge
VSUPUVH	VSUP has crossed its UVH threshold on the falling edge
LDT	LDT event occurs
GPIO2	GPIO2 event occurs
GPIO1	GPIO1 event occurs
WK2	WAKE2 event occurs

Table 136. List of Interrupt sources from Main logic*...continued*

Interrupt name	Corresponding event description
WK1	WAKE1 event occurs
MSPI_CRC	Main SPI CRC calculation is incorrect
MSPI_CLK	Main SPI clock provides wrong number of clock pulses
MSPI_REQ	MCU writes to an invalid register in the Main domain
NORMAL MODE	Main state machine enters in Normal mode

Table 137. List of Interrupt sources from Fail-Safe

Interrupt name	Corresponding event description
VPRE	An event occurs on VPRE monitoring
CORE	An event occurs on VCORE monitoring
LDO1	An event occurs on LDO1 monitoring
LDO2	An event occurs on LDO2 monitoring
TRK1	An event occurs on TRK1 monitoring
TRK2	An event occurs on TRK2 monitoring
REF	An event occurs on VREF monitoring
EXT	An event occurs on Analog Input monitoring
FCCU1	An event occurs on FCCU1 monitoring
FCCU2	An event occurs on FCCU2 monitoring
BAD_WD	A bad watchdog refresh occurs
ERRMON_M	An event occurs on External IC monitoring
INIT_FS	Fail safe state machine enters in INIT_FS state

Table 138. INTB Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
RPU_{INTB}	Internal pullup resistor to V_{DDIO}	5	10	20	kΩ
VOL_{INTB}	Low output level threshold I_{INTB} = 2.0 mA	—	—	0.4	V
ILK_{INTB}	Input leakage current V_{DDIO} = 5.5 V	—	—	1.0	µA
I_{INTB_ILIM}	INTB current limitation	4	—	20	mA
t_{INTB_PULSE}	Interrupt pulse duration Short pulse (INT_PWIDTH = 0) Long pulse (INT_PWIDTH = 1)	 17.5 70	 25 100	 32.5 130	µs

21.4 Long Duration Timer

The FS26 features a Long Duration Timer (LDT) with an integrated oscillator. The timer is configurable by the SPI and can operate in Normal and in Low Power modes. It provides several functions and offers a wide range of configurable counting periods, as well as a calibration mechanism for internal oscillator compensation.

The timer is not part of the safety circuitry and is not covered by LBIST (logic built-in self-test). It can be activated in Normal mode, though, and all prescaler options can be selected to allow timer circuitry verification. The timer is based on a 24 bit counter, with a 32768 Hz oscillator, allowing a 1.0 second time base.

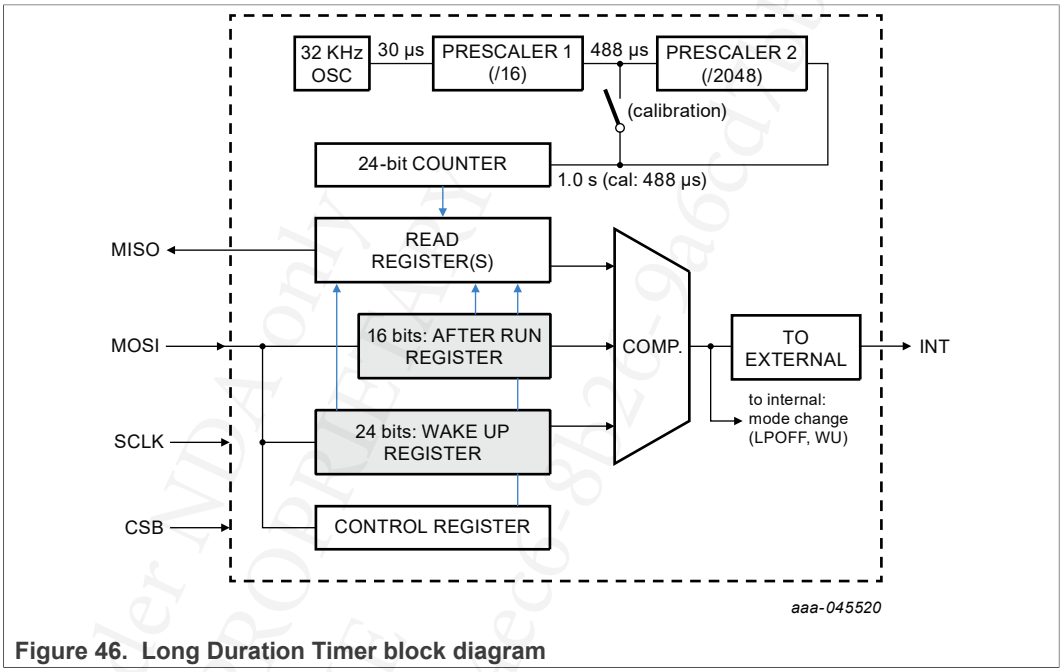


Figure 46. Long Duration Timer block diagram

21.4.1 Timer characteristics

In Normal mode operation, the timer can count up to 194 days, with a 1 second resolution. In Calibration mode, the prescaler 2 is bypassed and the timer can count up to 2.28 hours, with a 488 µs resolution.

Table 139. Long Duration Timer characteristics

	Osc Frequency	Osc Period	Prescaler	Counter resolution	Max count	
Operation	32.768 kHz	30.52 µs	16 x 2048	1 s	4660 hours	194 days
Calibration	32.768 kHz	30.52 µs	16	488 µs	8192 s	2.28 hours

The LDT has two modes of operation, based on the prescaler used during the count:

- When LDT_MODE = 0, the LDT is set in Long Count mode.
- When LDT_MODE = 1, the LDT is set in Short Count mode.

The LDT_AFTER_RUN[15:0] bits can set and read the after run value in Normal mode.

The LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits can set and read the wake-up value:

- LDT_WUP_H[7:0] contains the 8 most significant bits of the wake-up value.
- LDT_WUP_L[15:0] contains the 16 least significant bits of the wake-up value.

The LDT_SEL bit allows the MCU to read the value of the 24 bit LDT counter in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.

- When LDT_SEL = 0, The MCU can read or write the wake-up value in the LDT_WUP_H[7:0] and the LDT_WUP_L[15:0] bits.
- When LDT_SEL = 1, the MCU can read the counter current value.

The LDT_EN bit is provided to start the LDT timer operation:

- When LDT_EN = 0, the LDT is disabled.
- When LDT_EN = 1, the LDT starts counting as defined in the LDT_CTRL and LDT_CFGx registers.

The LDT_LPSEL[7:0] bits indicate the appropriate Low Power mode. The LDT_LPSEL[7:0] bits reset to 0x00 every time the device enters the Normal mode. When timer function 2 or 3 is selected, the MCU must first write the safe key value on the LDT_LPSEL[7:0] bits to confirm that the device will go into the corresponding Low Power mode after the run timer has expired.

- When LDT_LPSEL[7:0] = 0xAA, the device goes into Standby mode after the run timer expires.
- When LDT_LPSEL[7:0] = 0xA5, the device goes into LPOFF mode after the run timer expires.
- When timer function 4 or 5 is selected and LDT_EN = 1, the LDT does not start any count until the device enters the corresponding Low Power mode.

21.4.2 Calibration procedure

The calibration procedure consists of activating the counter for a specific duration and comparing the result with the MCU's accurate clock and timing. Once the timer expires, the MCU reads back its final value to compare with its own accurate time of activation and to calculate a time offset.

NXP recommends performing the calibration between -20 °C and 85 °C. Calibration example:

- Select the timer function 1 and set the after run value to 65535 (~32 s).
- Start the counter.
- Read the counter when the MCU RTC reaches 20 s (must be less than 30 s with ±5.0 % oscillator accuracy).
- If the oscillator period is at exact typical value (absolutely no deviation error), expected reading is 40960.
- The exact reading calculates the error correction factor ECF = exact_reading/ expected_reading.
- ECF < 1 if the oscillator is faster than the exact typical value.
- ECF > 1 if the oscillator is slower than the exact typical value.
- After calibration, the new after run or wake-up values to set the counter are "after run x ECF" and "wake-up x ECF".

21.4.3 Timer functions

Table 140. LDT functions

LDT_FNCT[2:0]	LDT Function
000	**Function 1:** In Normal mode, count and generate a flag or an interrupt when the counter reaches the after run value.
001	**Function 2:** In Normal mode, count until the counter reaches the after run value and enters Low Power mode.
010	**Function 3:** In Normal mode, count until the counter reaches the after run value and enters low power mode. Once in Low Power mode, count until the counter reaches the wake-up value or until another wake-up event occurs, and wakes up.
011	**Function 4:** In Low Power mode, count until the counter reaches the wake-up value or until another wake-up event occurs, and wakes up.
100	**Function 5:** In Low Power mode, count and do not wake up unless the counter overflow occurs or if the device wakes up by another wake-up input source.

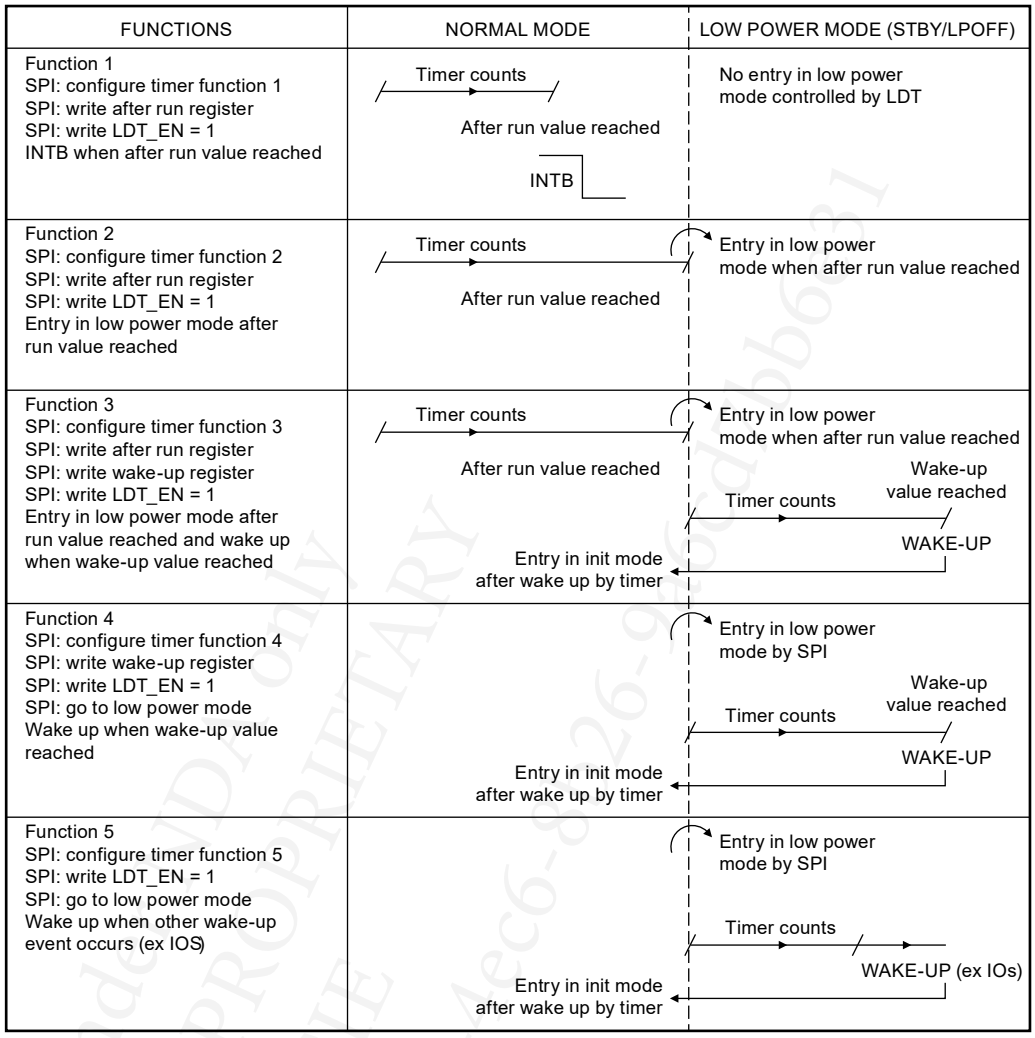


Figure 47. Long Duration Timer functions

21.4.4 Timer operation

The timer is configured and operates with the LONG_DURATION_TIMER registers.

The 16-bit after-run value is configured with M_LDT_CFG1 register and the 24-bit wake-up value are configured and read in the corresponding M_LDT_CFG2 and M_LDT_CFG3 registers.

Figure 48 describes the independent state machine for the long duration timer (LDT). After a POR of the device, the LDT is in idle mode waiting for configuration. The after-run timer function starts when the LDT_ENABLE bit is set by SPI. The wake-up timer function starts when the device enters Low Power mode.

- When function 1 is selected and the counter reaches the after run value (EOT), an interrupt is generated and the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).
- When function 2 is selected and the counter reaches the after run value (EOT), the device goes to Low Power mode and the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).

- When function 3 is selected and the counter reaches the after run value (EOT), the device goes to Low Power mode. The counter is reset and the count restarts. When the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. If the device is awakened by another wake up source, the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before enabling it again (LDT_EN = 1).
- When function 4 is selected and the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. If the device is awakened by another wake up source, the counter is stopped. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).
- When function 5 is selected and the counter overflows (OVRFLW), the device wakes up and the counter is stopped. The counter must be disabled (LDT_EN = 0) before reading its value and enabled again. Overflow means that the counter maximum value is reached (all 24 bits at logic 1).
- When function 5 is selected and the devices is awakened by an GPIO, the counter is running. In order to reset the counter, it must be disabled (LDT_EN = 0) before it is enabled again (LDT_EN = 1).

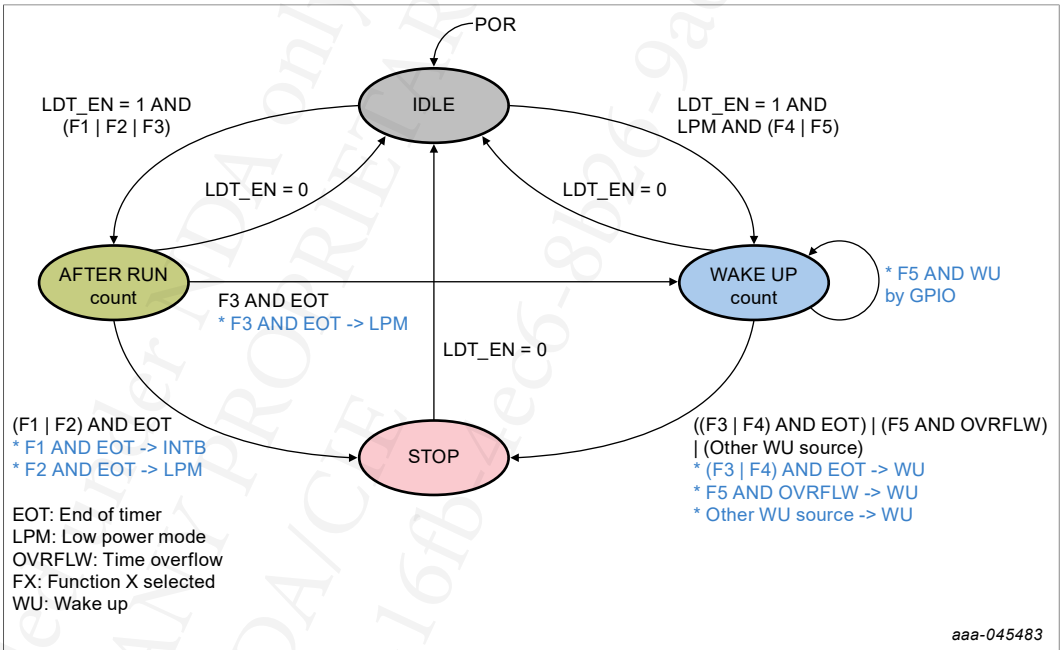


Figure 48. Long Duration Timer state machine

Table 141. Long Duration Timer characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
T_{BASE_LDT}	Long Duration Timer time base LDT_MODE = 0 LDT_MODE = 1	 — —	 1 488	 — —	 s µs
I_{Q_LDT}	Long Duration Timer quiescent current consumption	—	1	2	µA
LDT_{ACC1}	Long Duration Timer accuracy without calibration	-5	—	5	%

Table 141. Long Duration Timer characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
LDT_{ACC2}	Long Duration Timer accuracy with calibration Including 1 month aging Including temperature drift 0 °C < ΔTemp < 80 °C	-2	—	2	%

22 Functional safety

22.1 General description

The FS26 provides capabilities to enable functional safety in the application, in addition to power management and system enhancement functions. This part of the integrated circuit has its own biasing and clocking circuitries.

This creates an appropriate level of independence between the FS26 main functions and its safety mechanisms. FS26 is compliant with Automotive Safety Integrity Levels (ASIL) B and D, depending on the device part number.

This functional safety block provides three main capability sets: voltage monitoring of power management circuitry, software and hardware monitoring of the microcontroller, and control signals to place the system in a safe state in case of error.

Figure 49 illustrates functional blocks that pertain to functional safety.

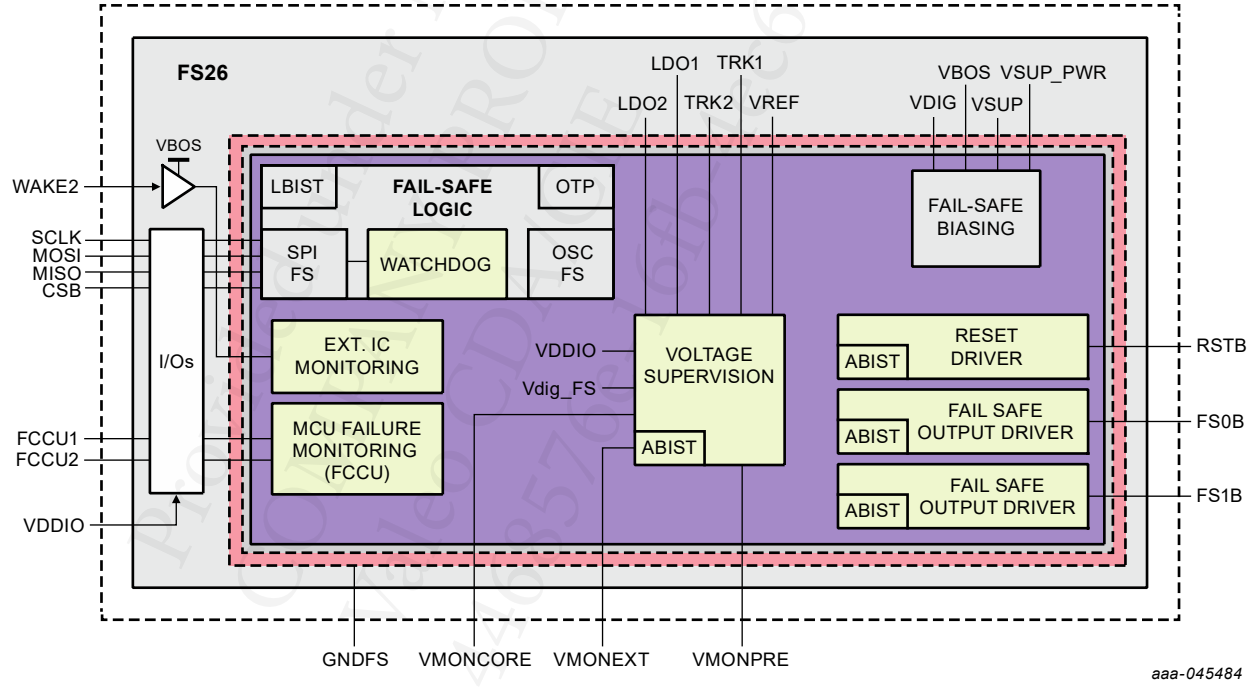


Figure 49. Fail-safe block diagram

22.2 Fail-safe logic

The dedicated fail-safe logic consists of OTP data to store the desired configuration, dedicated SPI registers, the watchdog mechanism, and an independent state machine.

22.3 ASIL B versus ASIL D

Table 142 lists the primary differences between the ASIL B and ASIL D versions of the FS26.

Table 142. ASIL B vs. ASIL D safety features

Safety Features	ASIL B (FS26xyB)	ASIL D (FS26xyD)
RSTB output pin	Yes	Yes
FS0B output pin	Yes	Yes
FS1B output pin	Optional	Optional
VPRE voltage monitoring	Yes	Yes
VCORE voltage monitoring	Yes	Yes
VLDO1 voltage monitoring	Yes	Yes
VLDO2 voltage monitoring	Yes	Yes
VTRK1 voltage monitoring	Yes	Yes – C(D)
VTRK2 voltage monitoring	Yes	Yes – C(D)
VREF voltage monitoring	Yes	Yes
VMONEXT voltage monitoring	Yes	Yes
Watchdog monitoring	Simple WD	Challenger WD
FCCU monitoring	Optional	Yes
MCU fault recovery strategy	No	Yes
External IC monitoring (ERRMON)	Optional	Optional
Analog BIST (ABIST)	Yes	Yes
Logical BIST (LBIST)	No	Yes

22.4 Fail-safe initialization

After a POR or a wake-up from Low Power mode, when the RSTB pin is released, the fail-safe state machine enters the INIT_FS phase for initialization. An interrupt is automatically sent to the microcontroller when the product enters this state. To secure the writing process during the INIT_FS phase, in addition to CRC computation during SPI transfer, the MCU must perform the following sequence for all INIT_FS registers (FS_I_xxxx):

1. Write the desired data in the FS_I_Register_A (DATA).
2. Write the opposite in the FS_I_NOT_Register_A (DATA_NOT).

As an example, if the data of FS_I_Register_A = 0xABCD, the data not of FS_I_NOT_Register_A = 0x5432. A real-time comparison process (XOR) is performed by the FS26 to ensure DATA FS_I_Register_A = DATA_NOT FS_I_NOT_Register_A. Only the utility bits must be inverted in the DATA_NOT content. The RESERVED bits are not considered and can be written at ‘0’. If the comparison result is correct,

then the REG_CORRUPT is set to ‘0’. If the comparison result is wrong, then the REG_CORRUPT bit is set to ‘1’. The REG_CORRUPT monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh.

INIT_FS must be closed by the first good watchdog refresh before the 256 ms timeout. In case no watchdog refresh or a bad watchdog is sent during the INIT_FS window, RSTB is asserted low and the fault error counter is incremented by 1. A new initialization phase is automatically started when RSTB is released. After INIT_FS closure, it is possible to come back to INIT_FS with the GOTO_INIT bit in the FS_SAFE_IOS_1 register from any FS_state after INIT_FS.

In case the fail-safe state machine is required to go back to INIT_FS state, NXP recommends sending the GOTO_INIT command immediately after a good watchdog refresh.

22.5 Fail-safe oscillator

A dedicated oscillator is implemented in the fail-safe circuitry. This oscillator is used for all time-based features implemented in the fail-safe domain.

The fail-safe domain is clocked by its own oscillator and is independent from the main domain. The clock has a monitoring feature for low and high frequency enabled by default.

A SPI flag is available to report a drift on the fail-safe oscillator. If the clock's frequency drifts to the high or low level, safety outputs are asserted.

Table 143. Clock management for fail-safe electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Internal oscillator					
F_{FSOSC}	Fail-safe oscillator nominal frequency	—	20	—	MHz
F_{FSOSC_ACC}	Fail-safe oscillator accuracy	-5	—	5	%
F_{FSOSC_MON}	Fail-safe oscillator failure detection range	-32	—	58	%
$t_{FSOSC\_DET\_TO}$	Fail-safe oscillator failure detection timeout	—	—	2	ms

22.6 Watchdog

A watchdog is implemented through the SPI bus to continuously check the microcontroller software activity and its ability to perform basic computing. The FS26 performs this check by waiting for a specific answer from the microcontroller during a predefined period called the watchdog window. The first half of the watchdog window is said to be CLOSED and the second half is said to be OPEN.

A good watchdog refresh is a good watchdog answer during the OPEN window. A bad watchdog refresh is a bad watchdog answer during the OPEN window, no watchdog refresh during the OPEN window, or a good watchdog answer during the CLOSED window. After a good or a bad watchdog refresh, a new window period starts immediately for the microcontroller to keep the synchronization with the windowed watchdog. The first good watchdog refresh closes the initialization phase of the FS26. After that, the watchdog window is running, and the microcontroller must refresh the watchdog in the OPEN window of the watchdog window period.

The duration of the watchdog window is configurable from 1.0 ms to 1024 ms with the WDW_PERIOD[3:0] SPI bits. The new watchdog window is effective after the next watchdog refresh. The watchdog window can be disabled only during the initialization phase of the FS26. The watchdog disabling is effective when the initialization phase is closed.

The watchdog can be configured in the same way as the INIT registers: writing to FS_WDW_DURATION and FS_NOT_WDW_DURATION registers. This window concept is applicable for both Simple and Challenger watchdog types.

Table 144. Watchdog window period configuration

WDW_PERIOD[3:0]	Watchdog window duration
0000	Infinite open window (can be set during INIT_FS only)
0001	1.0 ms
0010	2.0 ms
0011 (default)	**3.0 ms**
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011	64 ms
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms

The duty cycle of the watchdog window is configurable from 31.25 % to 81.25 % with the WDW_DC[2:0] bits. The new duty cycle is effective after the next watchdog refresh.

Table 145. Watchdog window period configuration

WDW_DC[2:0]	CLOSED window	OPEN window
000	31.25 %	68.75 %
001	37.5 %	62.5 %
010 (default)	**50 %**	**50 %**
011	62.5 %	37.5 %
100	68.75 %	31.25 %
101	75 %	25 %
110	81.25 %	18.75 %
111	50 %	50 %

22.6.1 Challenger watchdog

The Challenger watchdog monitoring feature is enabled for ASIL D devices. The Challenger watchdog is based on a question/answer process with the microcontroller. A 16-bit pseudo-random word is generated by implementing a Linear Feedback Shift Register (LFSR) in the FS26. During the initialization phase, the microcontroller can send its own seed for the LFSR, or it can use the default LFSR value generated by the FS26 (0x5AB2), available in the FS_WD_TOKEN register. With the LFSR value, the microcontroller performs a simple calculation based on the formula below and sends the results in the FS_WD_ANSWER register. The result is sent through the SPI bus during the OPEN watchdog window and is verified by the FS26. When the result is right, the watchdog window is restarted and a new LFSR is generated. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted, and the LFSR value is not changed.

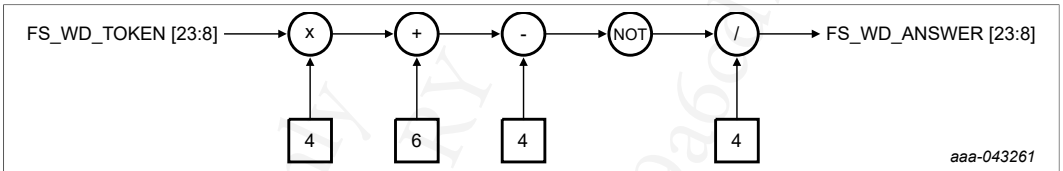


Figure 50. Fail-safe block diagram

In the Challenger watchdog configuration, it is impossible to write 0x0000 in the FS_WD_TOKEN register. If so, a communication error is reported and the configuration is ignored.

22.6.2 Simple watchdog

The Simple watchdog monitoring feature is enabled for ASIL B devices. The Simple watchdog uses a unique seed. The microcontroller can send its own seed in FS_WD_TOKEN register or can use the default value 0x5AB2. This seed must be written in the FS_WD_ANSWER register during the OPEN watchdog window. When the result is right, the watchdog window is restarted. When the result is wrong, the WD error counter is incremented and the watchdog window is restarted. In Simple watchdog configuration, it is impossible to write 0xFFFF and 0x0000 in FS_WD_TOKEN register. A communication error is reported in case of 0x0000 and 0xFFFF write tentative and the configuration is ignored.

22.6.3 Watchdog error counter

The following watchdog error strategy is available for both Challenger and Simple watchdog configurations. The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by ‘2’. The watchdog error counter is decremented by 1 each time the watchdog is properly refreshed. This principle guarantees a cyclic ’OK/NOK’ behavior, converging to a failure detection. To allow flexibility in the application, the maximum value of this counter is configurable using the WD_ERR_LIMIT[1:0] bits during the initialization phase.

Table 146. Watchdog window period configuration

WD_ERR_LIMIT[1:0]	Watchdog error counter maximum value
00	8
01 (default)	**6**

Table 146. Watchdog window period configuration...*continued*

WD_ERR_LIMIT[1:0]	Watchdog error counter maximum value
10	4
11	2

The watchdog error counter value (WD_ERR_CNT[3:0] bits) can be read by the microcontroller for diagnostic purposes.

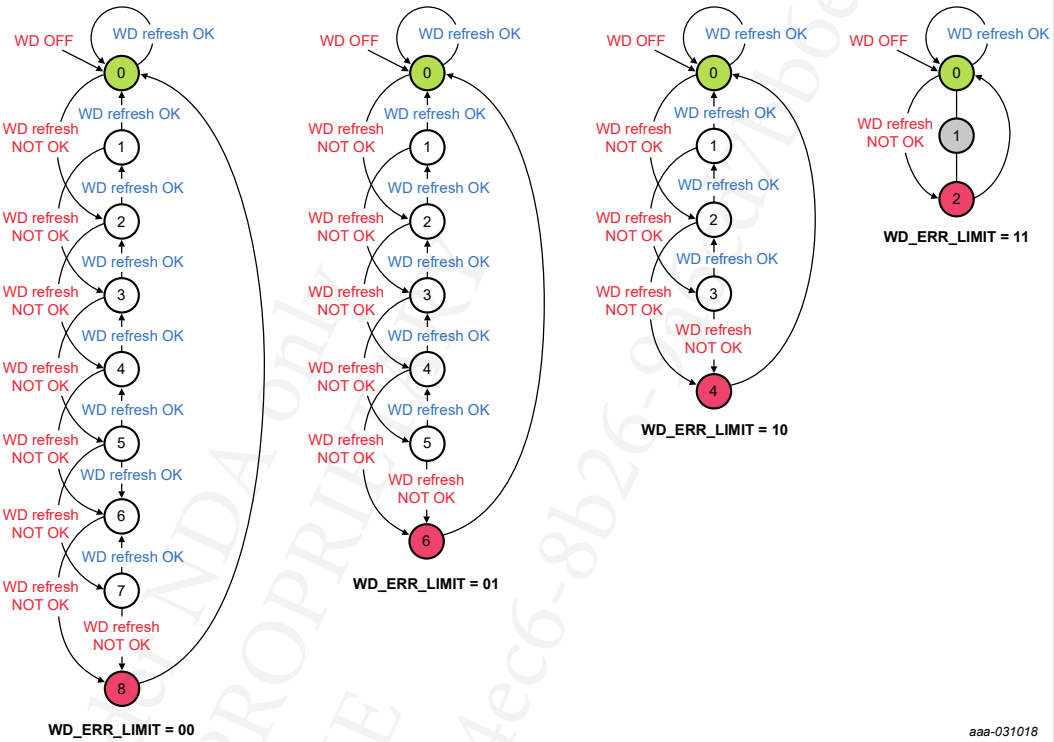


Figure 51. Watchdog error counter

22.6.4 Watchdog refresh counter

The watchdog refresh strategy is available for the Challenger watchdog and the Simple watchdog. The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by '1'. Each time the watchdog refresh counter reaches its maximum value ('6' by default) and if the next WD refresh is also good, the fault error counter is decremented by '1'. Whatever position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to '0'. To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable using the WD_RFR_LIMIT[1:0] bits during the initialization phase.

Table 147. Watchdog refresh counter configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
00 (by default)	**6**
01	4
10	2

Table 147. Watchdog refresh counter configuration*...continued*

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
11	1

The watchdog error counter value (WD_RFR_CNT[2:0] bits) can be read by the microcontroller for diagnostic purposes.

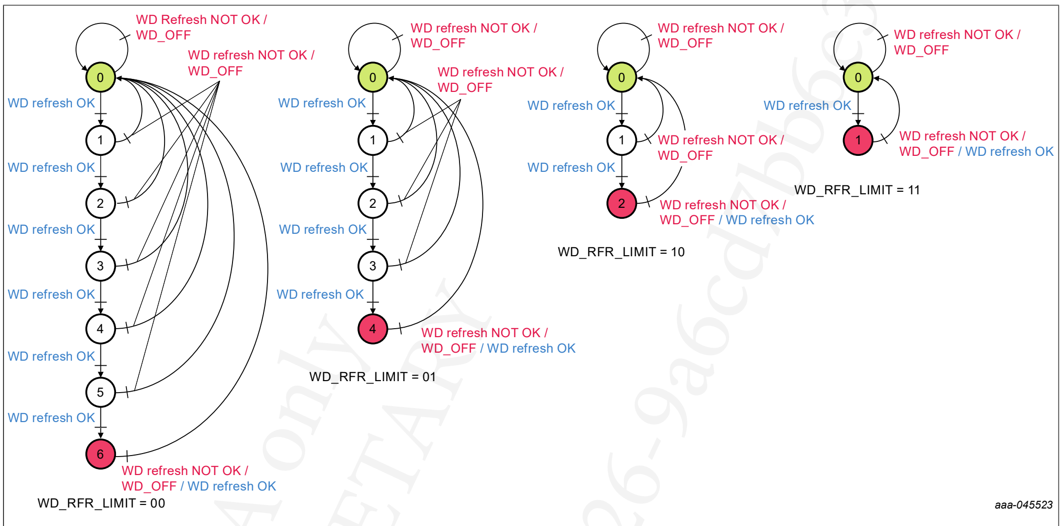


Figure 52. Watchdog refresh counter

22.6.5 Watchdog error impact

When the watchdog error counter reaches its maximum value, the fail-safe reaction on RSTB and/or the safety output(s) is configurable with the WD_FS_REACTION[1:0] bits during the initialization phase.

Table 148. Watchdog error impact configuration

WD_FS_ REACTION[1:0]	Watchdog error impact on RSTB and FS0B
00	No action on RSTB and the safety output(s)
01	Safety output(s) only is (are) asserted low if WD error counter value = WD_ERR_LIMIT[1:0]
1x (default)	**RSTB and safety output(s) are asserted low if WD error counter value = WD_ERR_LIMIT[1:0]**

22.6.6 Microcontroller fault recovery strategy

The fault recovery strategy feature is enabled by the FLT_RECOVERY_DIS_OTP bit. This function extends the watchdog window to allow the microcontroller to perform a fault recovery strategy. The goal is to avoid resetting the microcontroller while it is trying to recover the application after a failure event. When a fault is triggered by the microcontroller via its FCCU pins, the safety output(s) pin(s) is (are) asserted by the device, and the watchdog window duration becomes automatically an OPEN window (no more duty cycle). This OPEN window duration is configurable using the WDW_RECOVERY[3:0] bits during the initialization phase.

Table 149. Watchdog window duration with FCCU error and recovery strategy enabled

WDW_RECOVERY[3:0]	Watchdog window duration with FCCU error and recovery strategy enabled
0000	Infinite open window (can be set during INIT_FS only)
0001	1.0 ms
0010	2.0 ms
0011	3.0 ms
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011 (default)	**64 ms**
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms

The transition from WDW_PERIOD to WDW_RECOVERY happens when the FCCU pin indicates an error and the safety output(s) is (are) asserted. If the microcontroller sends a good watchdog refresh before the end of the WDW_RECOVERY duration, the device switches back to the WDW_PERIOD duration and associated duty cycle, if the FCCU pins do not indicate an error anymore. Otherwise, a new WDW_RECOVERY period is started. If the microcontroller does not send a good watchdog refresh before the end of the WDW_RECOVERY duration, then a reset pulse is generated and the Fail-safe state machine moves back to the initialization phase.

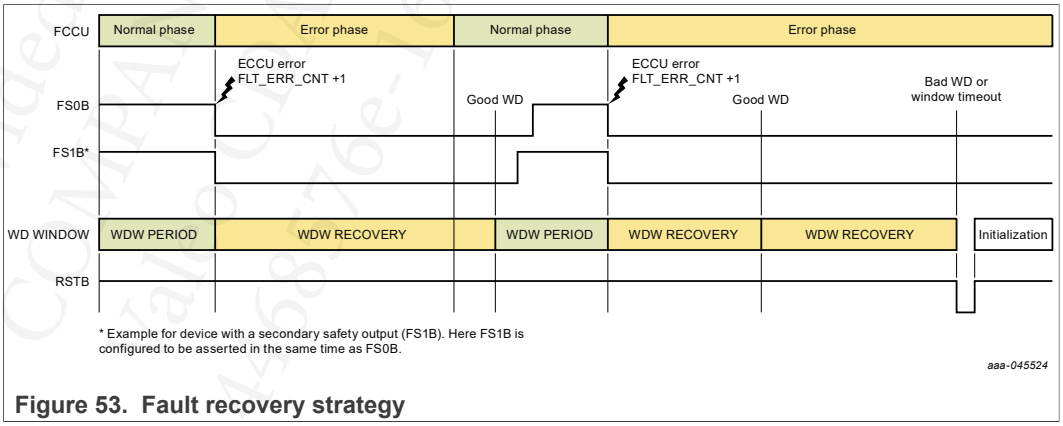


Figure 53. Fault recovery strategy

22.7 FCCU monitoring

The FCCU monitoring feature is available for FS26xyD devices. The FCCU input pins are in charge of monitoring hardware failures from the MCU. The FCCU input pins can be configured either by pair or as single independent inputs, and can monitor a PWM signal on one of FCCU1 or FCCU2. The FCCU monitoring is active as soon as the initialization phase is closed (exit INIT_FS state) by the first good watchdog refresh. The FCCU input pins are configured with the FCCU_CFG[2:0] bits, as described in Table 150.

Table 150. FCCU pin monitoring configuration

FCCU_CFG[2:0]	FCCU monitoring configuration
000	No monitoring
001 (default)	**FCCU1 and FCCU2 inputs monitoring activated by pair (bi-stable protocol)**
010	FCCU1 and FCCU2 single inputs level monitoring activated
011	FCCU1 single input level monitoring only, FCCU2 input not used
100	FCCU2 single input level monitoring only, FCCU1 input not used
101	FCCU1 and FCCU2 single inputs PWM monitoring activated
110	FCCU1 single input PWM monitoring and FCCU2 single input level monitoring
111	FCCU2 single input PWM monitoring and FCCU1 single input level monitoring

22.7.1 FCCU inputs monitoring activated by pair

When this configuration is selected, both FCCU1 and FCCU2 levels are considered to monitor MCU error signals. These levels can be configured with the FCCU12_FLT_POL bit during the initialization phase.

Table 151. FCCU12 bi-stable protocol error state configuration

FCCU12_FLT_POL	FCCU monitoring configuration
0 (default)	**FCCU1 = 0 or FCCU2 = 1 level is a fault**
1	FCCU1 = 1 or FCCU2 = 0 level is a fault

The reaction on the safety outputs can be also configured using the FCCU12_FS_REACTION SPI bit during the initialization phase.

Table 152. FCCU12 error reaction configuration

FCCU12_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU1 and FCCU2
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU1 and FCCU2**

Figure 54 illustrates the bistable protocol and the various phases that may occur in an application. This example is valid for FCCU12_FLT_POL = ‘1’ and FCCU12_FS_REACTION = ‘1’.

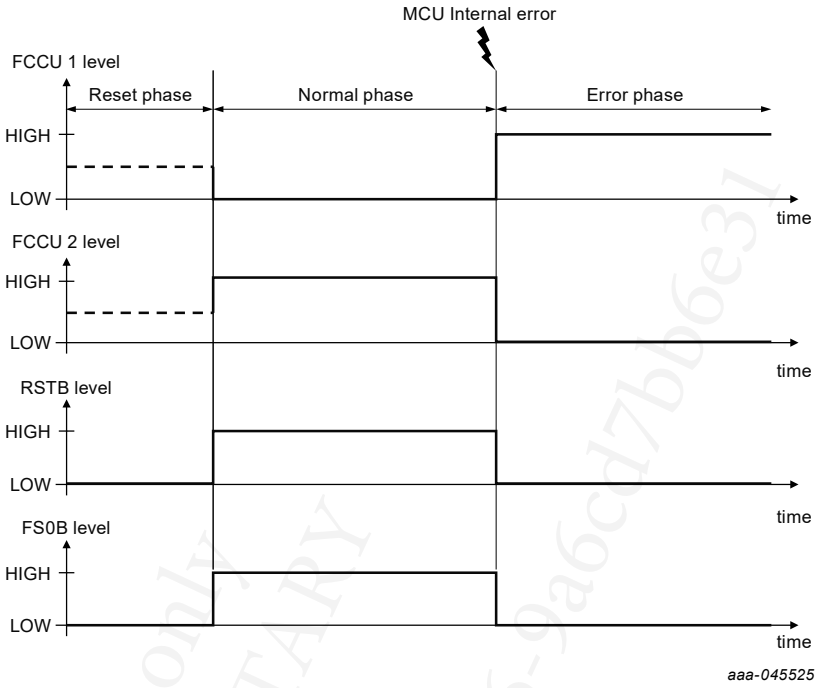


Figure 54. Bi-stable protocol monitored by FCCU pins

22.7.2 FCCU single input monitoring activated

When FCCU_CFG[2:0] = ‘010’, the FCCU inputs are used separately and monitor two different and independent level error signals.

When FCCU_CFG[2:0] = ‘011’, only the FCCU1 input level is monitored and the FCCU2 input is not used.

When FCCU_CFG[2:0] = ‘100’, only the FCCU2 input level is monitored and the FCCU1 input is not used.

The error level can be defined by the FCCU1_FLT_POL or FCCU2_FLT_POL bits. The description of SPI bits in this section is valid only if FCCU_CFG[2:0] ≠ ‘000’ or ‘001’.

Table 153. FCCU1 error state configuration

FCCU1_FLT_POL	FCCU1 monitoring configuration
0 (default)	**FCCU1 low level is a fault**
1	FCCU1 high level is a fault

Table 154. FCCU2 error state configuration

FCCU2_FLT_POL	FCCU2 monitoring configuration
0 (default)	**FCCU2 low level is a fault**
1	FCCU2 high level is a fault

The reaction on the safety outputs can be also configured using the FCCU1_FS_REACTION and FCCU2_FS_REACTION SPI bits during the initialization phase.

Table 155. FCCU1 error reaction configuration

FCCU1_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU1
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU1**

Table 156. FCCU2 error reaction configuration

FCCU2_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU2
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU2**

This Figure 55 timing diagram illustrates FCCU1 monitoring and the various phases that may occur in an application. This example is valid for FCCU_CFG[2:0] = '011', FCCU1_FLT_POL = '0' and FCCU1_FS_REACTION = '1'.

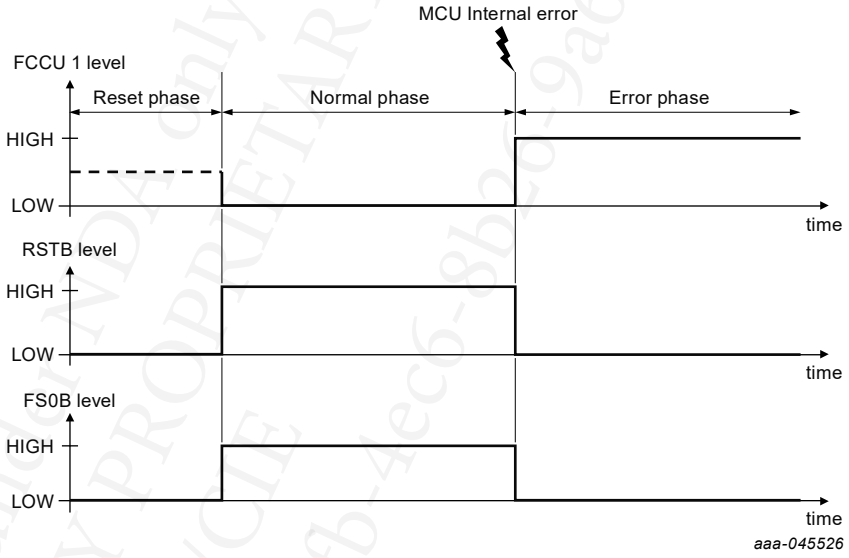


Figure 55. FCCU1 monitoring example

22.7.3 FCCU single PWM monitoring activated

When FCCU_CFG[2:0] = '101' the FCCU inputs are used separately and monitor two different and independent PWM error signals.

When FCCU_CFG[2:0] = '110' the FCCU inputs are used separately. FCCU1 monitors a PWM error signal and FCCU2 monitors a level error signal.

When FCCU_CFG[2:0] = '111' the FCCU inputs are used separately. FCCU2 monitors a PWM error signal and FCCU1 monitors a level error signal.

In this mode, a pulse width modulated waveform is expected to be seen on the FCCU1 or FCCU2 pin. The FS26 can measure each high time and low time for both signals monitored on its FCCU pins. When one of the high time or low times is outside the $t_{PULSE\_FCCU\_HF}$ or $t_{PULSE\_FCCU\_LF}$ limits, the FS26 will consider that the MCU has an internal error. The reaction on the safety outputs can be also configured using the FCCU1_FS_REACTION or FCCU2_FS_REACTION bits during the initialization phase. The description of SPI bits in this section is valid only if FCCU_CFG[2:0] ≠ '000' or '001'.

When an FCCU input pin is configured in PWM monitoring, $t_{FCCU\_ERR\_PWM}$ filtering time is automatically selected. When an FCCU input pin is configured in level monitoring, t_{FCCU_ERR} filtering time can be configured.

Table 157. FCCU1 error reaction configuration

FCCU1_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU1
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU1**

Table 158. FCCU2 error reaction configuration

FCCU2_FS_REACTION	Reaction
0	FS0B only is asserted low in case of fault on FCCU2
1 (default)	**RSTB and FS0B are asserted low in case of fault on FCCU2**

This Figure 56 timing diagram illustrates FCCU1 monitoring and the various phases that can occur with the application. This example is valid for FCCU_CFG[2:0] = '101' and FCCU1_FS_REACT = '1'.

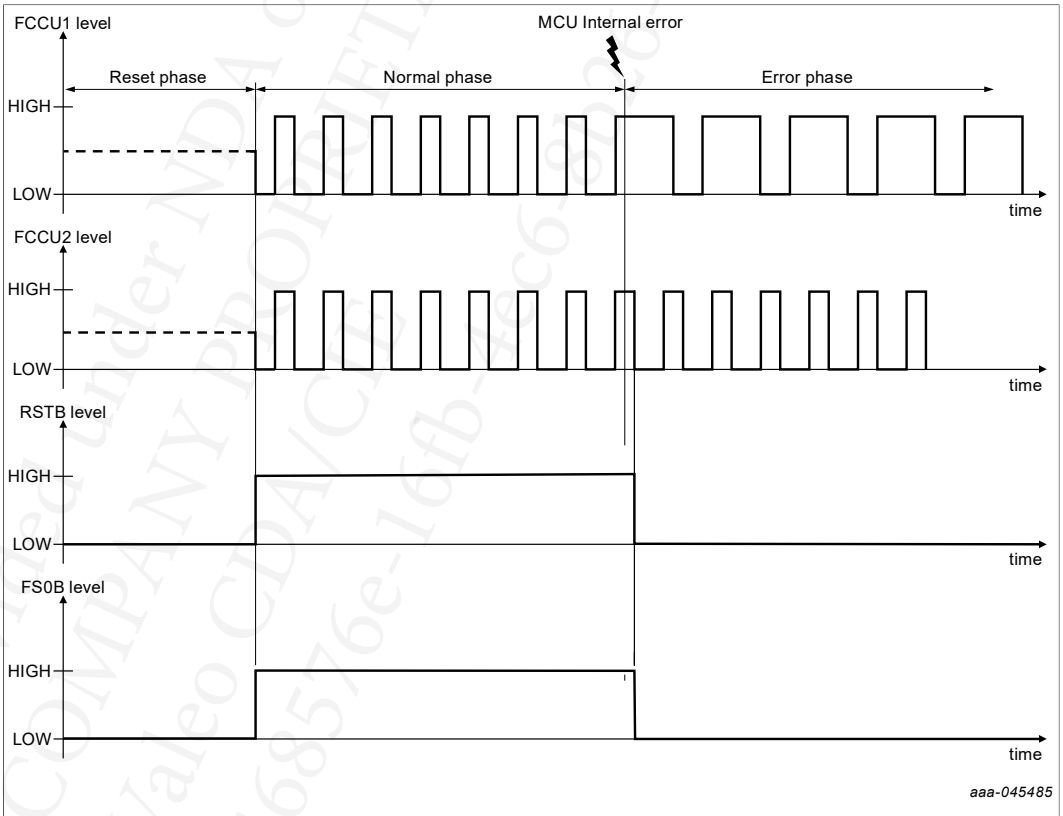


Figure 56. Dual input PWM monitoring example

The PWM monitoring functionality is constantly checking both high level and low level durations of pulses that are monitored on FCCU1 and FCCU2 input pins with regard to $t_{PULSEFCCU\_HF}$ or $t_{PULSEFCCU\_LF}$ limits.

Table 159. FCCU monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{IL_FCCU}	FCCU digital low input level threshold	0	—	0.3 * V_{DDIO}	V
V_{IH_FCCU}	FCCU digital high input level threshold	0.7 * V_{DDIO}	—	5.0	V
V_{HYST_FCCU}	FCCU input voltage hysteresis	0.1	—	0.6	V
R_{PD_FCCU1}	FCCU1 pin internal pulldown	400	800	1300	kΩ
R_{PU_FCCU2}	FCCU2 pin internal pullup to V_{DDIO}	100	200	400	kΩ
Dynamic electrical characteristics					
t_{FCCU_ERR}	FCCU inputs filtering time FCCU12_FILT[1:0] = 00 FCCU12_FILT[1:0] = 01 FCCU12_FILT[1:0] = 10 FCCU12_FILT[1:0] = 11	 1 4 8 16	 3 6 12 20	 4 8 16 24	 µs
$t_{FCCU\_ERR\_PWM}$	FCCU1,2 filtering time when configured in PWM monitoring	0.8	1	1.2	µs
F_{FCCU12_GF}	FCCU1,2 good frequency range (PWM detection)	10	—	45	kHz
F_{FCCU12_BLF}	FCCU1,2 bad low frequency range (PWM detection)	—	—	5	kHz
F_{FCCU12_BHF}	FCCU1,2 bad high frequency range (PWM detection)	90	—	—	kHz
$t_{PULSE\_FCCU\_HF}$	FCCU1,2 high and low level detection time (high frequency) measured on both pulse polarity.	6	8	10	µs
$t_{PULSE\_FCCU\_LF}$	FCCU1,2 high and low level detection time (low frequency) measured on both pulse polarity.	51	64	80	µs

22.8 Voltage supervision

The voltage supervisor is dedicated to monitoring the power rails generated by the FS26 for the application. For regulated voltages, an overvoltage detection and an undervoltage detection are embedded into the voltage supervisor. Thanks to these fault detections, a configurable reaction on the safety outputs and the RSTB pin can be programmed for each regulator. The VBST voltage output is not monitored by the voltage supervision. Dedicated pins are available to monitor synchronous bucks (VPRE and VCORE). Linear regulators (LDO1, LDO2, VREF, TRK1, and TRK2) are monitored through internal connections. When an overvoltage fault occurs, the corresponding regulator is switched off, and a SPI flag bit is set. As soon as the overvoltage goes away, the regulator restarts, doing a soft start toward the output voltage set by OTP.

One extra monitoring pin, called VMONEXT, can be used to monitor a voltage generated by another part into the application. When an overvoltage is detected on the VMONEXT pin, a SPI flag bit is set.

22.8.1 VPRE monitoring

Using the VMONPRE pin, the FS26 can detect faults on the VPRE output voltage. Both overvoltage and undervoltage can be detected.

To support various system configurations, VPRE monitoring can be activated, or not activated, with an OTP bit. Also, to support various output voltages of the VPRE, OTP bits are available to set the target voltage value to monitor. A wide range of upper and lower thresholds can be selected with OTP bits, to fit multiple system requirements.

To allow flexibility in the application, reactions to both over- and undervoltage faults are configurable with the VMON_PRE_OV_FS_REACTION[1:0] and VMON_PRE_UV_FS_REACTION[1:0] bits during the initialization phase.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the “Enable Monitoring” state is reached.

Table 160. VPRE overvoltage reaction configuration

VMON_PRE_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 161. VPRE undervoltage reaction configuration

VMON_PRE_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts safety output(s) and RSTB

Table 162. VPRE monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{MONPRE_RANGE}	VPRE monitoring target voltage setting range	3.7	—	6.35	V
V_{MONPRE_STEP}	VPRE overvoltage monitoring target voltage setting step with VPRE_V_OTP[5:0] bits	—	50	—	mV
$V_{MONPRE\_OVTH\_RANGE}$	VPRE overvoltage monitoring threshold range setting with VMON_PRE_OVTH_OTP[3:0] bits	106	—	112	%
$V_{MONPRE\_OVTH\_STEP}$	VPRE overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONPRE\_OVTH\_ACC}$	VPRE overvoltage detection accuracy	-1	—	1	%
$V_{MONPRE\_UVTH\_RANGE}$	VPRE undervoltage monitoring threshold range setting with VMON_PRE_UVTH_OTP[3:0] bits	88	—	94	%
$V_{MONPRE\_UVTH\_STEP}$	VPRE undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONPRE\_UVTH\_ACC}$	VPRE undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
t_{PREOV_DGLT}	VPRE overvoltage deglitch time VMON_PRE_OVDGLT_OTP = 0 VMON_PRE_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
t_{PREUV_DGLT}	VPRE undervoltage deglitch time				

Table 162. VPRE monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	VMON_PRE_UVDGLT_OTP [1:0] = 00	2.5	5	7.5	µs
	VMON_PRE_UVDGLT_OTP [1:0] = 01	10	15	20	
	VMON_PRE_UVDGLT_OTP [1:0] = 10	20	25	30	
	VMON_PRE_UVDGLT_OTP [1:0] = 11	35	40	45	

22.8.2 VCORE monitoring

The FS26 can detect faults on the VCORE output voltage using the VMONCORE pin. Both overvoltage and undervoltage can be detected.

To support various system configurations, VCORE monitoring can be activated, or not activated, with an OTP bit. Also, to support various output voltages of the VCORE, OTP bits are available to set the target voltage value to monitor. A wide range of upper and lower thresholds can be selected using the OTP bits, to support multiple system requirements.

To allow flexibility in the application, reactions to both over and undervoltage faults are configurable with the VMON_CORE_OV_FS_REACTION[1:0] and VMON_CORE_UV_FS_REACTION[1:0] bits during the initialization phase.

This monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the “Enable Monitoring” state is reached.

Table 163. VCORE overvoltage reaction configuration

VMON_CORE_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 164. VCORE undervoltage reaction configuration

VMON_CORE_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 165. VCORE monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{MONCORE\_RANGE}$	VCORE monitoring target voltage setting range	0.8	—	3.35	V

Table 165. VCORE monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
$V_{MONCORE\_STEP}$	VCORE overvoltage monitoring target voltage setting step with VCORE_V_OTP[7:0] bits	—	10	—	mV
$V_{MONCORE\_OVTH\_RANGE}$	VCORE overvoltage monitoring threshold range setting with VMON_CORE_OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONCORE\_OVTH\_STEP}$	VCORE overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONCORE\_OVTH\_ACC}$	VCORE overvoltage detection accuracy	-1	—	1	%
$V_{MONCORE\_UVTH\_RANGE}$	VCORE undervoltage monitoring threshold range setting with VMON_CORE_UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONCORE\_UVTH\_STEP}$	VCORE undervoltage monitoring OTP threshold setting step	—	0.5	—	%
Dynamic electrical characteristics					
t_{COREOV_DGLT}	VCORE overvoltage deglitch time VMON_CORE_OVDGLT_OTP = 0 VMON_CORE_OVDGLT_OTP = 1	20 40	25 45	30 50	µs
t_{COREUV_DGLT}	VCORE undervoltage deglitch time VMON_CORE_UVDGLT_OTP[1:0] = 00 VMON_CORE_UVDGLT_OTP[1:0] = 01 VMON_CORE_UVDGLT_OTP[1:0] = 10 VMON_CORE_UVDGLT_OTP[1:0] = 11	2.5 10 20 35	5 15 25 40	7.5 20 30 45	µs

22.8.3 LDO1 monitoring

Because of an internal dedicated connection to the LDO1OUT pad, the FS26 can detect faults on the LDO1 output voltage. Both overvoltage and undervoltage can be detected.

To support various system configurations, LDO1 monitoring can be activated, or not activated, with an OTP bit. Also, to support both output voltages of the LDO1, an OTP bit is available to set the target voltage value to monitor. To fit multiple system requirements, a wide range of upper and lower thresholds can be selected with OTP bits.

To reach ASIL D at the LDO1OUT pin level, the pin lift detection mechanism must be activated using the LDO1_PLIFT_DIS_OTP bit.

If the LDO1OUT pin is disconnected, the LDO1 output voltage will be pulled to LDOIN within $t_{LDO1\_PINLIFT}$ and will create an overvoltage, and the device will react as VMON_LDO1_OV_FS_REACTION[1:0]. A minimum headroom $V_{LDOIN\_MIN\_PINLIFT}$ is mandatory to guarantee the pin lift detection.

A degraded undervoltage threshold can be selected by OTP to avoid an MCU reset during cranking event. The threshold is fixed at 62 %, and is not configurable by software. This feature must be used only when LDO1 is set at 5 V to supply the microcontroller.

Table 166. LDO1 degraded undervoltage configuration

VMON_LDO1_UVDTH_OTP	VLDO1_OTP	Undervoltage threshold configuration
0	x	Normal UV (Configuration using VMON_LDO1_UVTH_OTP[3:0])
1	1	Fixed Degraded UV

To allow flexibility in the application, both reactions to over and undervoltage faults are configurable with the VMON_LDO1_OV_FS_REACTION[1:0] and VMON_LDO1_UV_FS_REACTION[1:0] bits during the initialization phase.

The monitoring is able to report UV/OV flags as soon as the power up sequence is completed and the “Enable Monitoring” state is reached.

Table 167. LDO1 overvoltage reaction configuration

VMON_LDO1_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 168. LDO1 undervoltage reaction configuration

VMON_LDO1_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 169. LDO1 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{MONLDO1\_CFG}$	LDO1 monitoring target voltage setting LDO1_V_OTP bit = 0 LDO1_V_OTP bit = 1	 — —	 3.3 5.0	 — —	V
$V_{LDOIN\_MIN\_PINLIFT}$	Minimum headroom to guarantee LDO1OUT pin lift detection	LDO1_V_OTP x ($V_{MON\_LDO1\_OVTH\_OTP}$ + 1 %) + 0.5 V	—	—	V
$V_{MONLDO1\_OVTH\_RANGE}$	LDO1 overvoltage monitoring threshold range setting with VMON_LDO1_OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONLDO1\_OVTH\_STEP}$	LDO1 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONLDO1\_OVTH\_ACC}$	LDO1 overvoltage detection accuracy	-1	—	1	%
$V_{MONLDO1\_UVTH\_RANGE}$	LDO1 undervoltage monitoring threshold range setting with VMON_LDO1_UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONLDO1\_UVTH\_STEP}$	LDO1 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONLDO1\_UVTH\_ACC}$	LDO1 undervoltage detection accuracy	-1	—	1	%
$V_{MON\_LDO1\_UVDTH}$	Degraded undervoltage threshold	61	62	63	%
Dynamic electrical characteristics					
t_{LDO1OV_DGLT}	LDO1 overvoltage deglitch time:				

Table 169. LDO1 monitoring electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	VMON_LDO1_OVDGLT_OTP = 0	20	25	30	µs
	VMON_LDO1_OVDGLT_OTP = 1	40	45	50	
t_{LDO1UV_DGLT}	LDO1 undervoltage deglitch time:				
	VMON_LDO1_UVDGLT_OTP[1:0] = 00	2.5	5	7.5	µs
	VMON_LDO1_UVDGLT_OTP[1:0] = 01	10	15	20	
	VMON_LDO1_UVDGLT_OTP[1:0] = 10	20	25	30	
	VMON_LDO1_UVDGLT_OTP[1:0] = 11	35	40	45	
$t_{LDO1\_PINLIFT}$	LDO1 pin lift detection time	—	—	5	ms

22.8.4 LDO2 monitoring

Because of an internal dedicated connection to the LDO2OUT pad, the FS26 can detect faults on the LDO2 output voltage. Both overvoltage and undervoltage can be detected.

To support various system configurations, LDO2 monitoring can be activated, or not activated, with an OTP bit. Also, to support both output voltages of the LDO2, an OTP bit is available to set the target voltage value to monitor. To fit multiple system requirements, a wide range of upper and lower thresholds can be selected with OTP bits.

To reach ASIL D at the LDO2OUT pin level, the pin lift detection mechanism must be activated using the LDO2_PLIFT_DIS_OTP bit.

If the LDO2OUT pin is disconnected, the LDO2 output voltage will be pulled to LDOIN within $t_{LDO2\_PINLIFT}$ and will create an overvoltage, and the device will react as VMON_LDO2_OV_FS_REACTION[1:0]. A minimum headroom $V_{LDOIN\_MIN\_PINLIFT}$ is mandatory to guarantee the pin lift detection.

A degraded undervoltage threshold can be selected by OTP to avoid an MCU reset during a cranking event. The threshold is fixed at 62 %, and is not configurable by software. This feature must be used only when LDO2 is set at 5 V to supply the microcontroller.

Table 170. LDO2 degraded undervoltage configuration

VMON_LDO2_UVDTH_OTP	VLDO2_OTP	Undervoltage threshold configuration
0	x	Normal UV (Configuration using VMON_LDO2_UVTH_OTP[3:0])
1	1	Fixed Degraded UV

To allow flexibility in the application, both reactions to over and undervoltage faults are configurable with the VMON_LDO2_OV_FS_REACTION[1:0] and VMON_LDO2_UV_FS_REACTION[1:0] bits during the initialization phase.

The monitoring is able to report UV/OV flags as soon as the power up sequence is completed and the “Enable Monitoring” state is reached.

Table 171. LDO2 overvoltage reaction configuration

VMON_LDO2_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 172. LDO2 undervoltage reaction configuration

VMON_LDO2_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 173. LDO2 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{MONLDO2\_CFG}$	LDO2 monitoring target voltage setting LDO2_V_OTP bit = 0 LDO2_V_OTP bit = 1	— —	 3.3 5.0	— —	V
$V_{LDOIN\_MIN\_PINLIFT}$	Minimum headroom to guarantee LDO2OUT pin lift detection	LDO2_V_OTP x ($V_{MON\_LDO2\_OVTH\_OTP}$ + 1 %) + 0.5 V	—	—	V
$V_{MONLDO2\_OVTH\_RANGE}$	LDO2 overvoltage monitoring threshold range setting with VMON_ LDO2_OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONLDO2\_OVTH\_STEP}$	LDO2 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONLDO2\_OVTH\_ACC}$	LDO2 overvoltage detection accuracy	-1	—	1	%
$V_{MONLDO2\_UVTH\_RANGE}$	LDO2 undervoltage monitoring threshold range setting with VMON_ LDO2_UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONLDO2\_UVTH\_STEP}$	LDO2 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONLDO2\_UVTH\_ACC}$	LDO2 undervoltage detection accuracy	-1	—	1	%
$V_{MON\_LDO2\_UVDTH}$	Degraded undervoltage threshold	61	62	63	%
Dynamic Electrical Characteristics					
t_{LDO2OV_DGLT}	LDO2 overvoltage deglitch time: VMON_LDO2_OVDGLT_OTP = 0 VMON_LDO2_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs
t_{LDO2UV_DGLT}	LDO2 undervoltage deglitch time: VMON_LDO2_UVDGLT_OTP[1:0] = 00 VMON_LDO2_UVDGLT_OTP[1:0] = 01 VMON_LDO2_UVDGLT_OTP[1:0] = 10 VMON_LDO2_UVDGLT_OTP[1:0] = 11	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	µs
$t_{LDO2\_PINLIFT}$	LDO2 pin lift detection time	—	—	5	ms

22.8.5 TRK1 monitoring

Because of an internal and dedicated connection to the TRK1 pad, the FS26 can detect faults on the TRK1 output voltage. Both overvoltage and undervoltage conditions can be detected.

To support various system configurations, TRK1 monitoring can be activated, or not activated, with an OTP bit. Also, to support various output voltages of the TRK1, OTP bits are available to set the target voltage value to monitor. To fit multiple systems requirements, a wide range of upper and lower thresholds can be selected using the OTP bits.

To allow flexibility in the application, both reactions to over and undervoltage faults are configurable with the VMON_ TRK1_OV_FS_REACTION[1:0] and VMON_ TRK1_UV_FS_REACTION[1:0] bits during the initialization phase. If a 'short to

high' type of fault on TRK1 should not impact RSTB, NXP recommends configuring VMON_TRK1_OV_FS_REACTION[1:0] = 01 before turning ON TRK1 by SPI.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the “Enable Monitoring” state is reached.

If the regulator is used as a global pin, outside of the module, it is recommended to not include it in the power-up sequence and to turn on the regulator by SPI, to avoid a stuck in reset condition in case of a short circuit.

If the tracker is safety related in the application, the voltage monitoring should be checked during ABIST2 on demand.

Table 174. TRK1 overvoltage reaction configuration

VMON_TRK1_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 175. TRK1 undervoltage reaction configuration

VMON_TRK1_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 176. TRK1 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{MONTRK1\_CFG}$	TRK1 monitoring target voltage setting				
	TRK1_V_OTP [1:0] = 00	—	1.2	—	V
	TRK1_V_OTP [1:0] = 01	—	1.8	—	
	TRK1_V_OTP [1:0] = 10	—	3.3	—	
	TRK1_V_OTP [1:0] = 11	—	5	—	
$V_{MONTRK1\_OVTH\_RANGE}$	TRK1 overvoltage monitoring threshold range setting with VMON_TRK1_OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONTRK1\_OVTH\_STEP}$	TRK1 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONTRK1\_OVTH\_ACC}$	TRK1 overvoltage detection accuracy	-1	—	1	%
$V_{MONTRK1\_UVTH\_RANGE}$	TRK1 undervoltage monitoring threshold range setting with VMON_TRK1_UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONTRK1\_UVTH\_STEP}$	TRK1 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONTRK1\_UVTH\_ACC}$	TRK1 undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
t_{TRK1OV_DGLT}	TRK1 overvoltage deglitch time				
	VMON_TRK1_OVDGLT_OTP = 0	20	25	30	µs
	VMON_TRK1_OVDGLT_OTP = 1	40	45	50	
T_{TRK1UV_DGLT}	TRK1 undervoltage deglitch time				

Table 176. TRK1 monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	VMON_TRK1_UVDGLT_OTP[1:0] = 00 VMON_TRK1_UVDGLT_OTP[1:0] = 01 VMON_TRK1_UVDGLT_OTP[1:0] = 10 VMON_TRK1_UVDGLT_OTP[1:0] = 11	2.5 10 20 35	5 15 25 40	7.5 20 30 45	µs

22.8.6 TRK2 monitoring

Because of an internal dedicated connection to TRK2 pad, the FS26 can detect faults on the TRK2 output voltage. Both overvoltage and undervoltage conditions can be detected.

To support various system configurations, TRK2 monitoring can be activated, or not activated, with an OTP bit. Also, to support various TRK2 output voltages, OTP bits are available to set the target voltage value to monitor. To fit multiple system requirements, a wide range of upper and lower thresholds can be selected with the OTP bits.

To allow flexibility in the application, reactions to both overvoltage and undervoltage faults are configurable with the VMON_ TRK2_OV_FS_REACTION[1:0] and VMON_ TRK2_UV_FS_REACTION[1:0] bits during the initialization phase. If a 'short to high' type of fault on TRK1 should not impact RSTB, NXP recommends configuring VMON_ TRK2_OV_FS_REACTION[1:0] = 01 before turning ON TRK2 using SPI.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the “Enable Monitoring” state is reached.

If the regulator is used as a global pin, outside of the module, NXP recommends not including it in the power-up sequence and turning on the regulator using SPI, to avoid a stuck in reset condition in case of a short circuit.

If the tracker is safety related in the application, the voltage monitoring should be checked during ABIST2 on demand.

Table 177. TRK2 overvoltage reaction configuration

VMON_TRK2_OV_FS_REACTION [1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 178. TRK2 undervoltage reaction configuration

VMON_TRK2_UV_FS_REACTION [1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 179. TRK2 monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
$V_{MONTRK2\_CFG}$	TRK2 monitoring target voltage setting TRK2_V_OTP [1:0] = 00 TRK2_V_OTP [1:0] = 01 TRK2_V_OTP [1:0] = 10 TRK2_V_OTP [1:0] = 11	— — — —	1.2 1.8 3.3 5	— — — —	V
$V_{MONTRK2\_OVTH\_RANGE}$	TRK2 overvoltage monitoring threshold range setting with VMON_TRK2_ OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONTRK2\_OVTH\_STEP}$	TRK2 overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONTRK2\_OVTH\_ACC}$	TRK2 overvoltage detection accuracy	-1	—	1	%
$V_{MONTRK2\_UVTH\_RANGE}$	TRK2 undervoltage monitoring threshold range setting with VMON_TRK2_ UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONTRK2\_UVTH\_STEP}$	TRK2 undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONTRK2\_UVTH\_ACC}$	TRK2 undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
t_{TRK2OV_DGLT}	TRK2 overvoltage deglitch time: VMON_TRK2_OVDGLT_OTP = 0 VMON_TRK2_OVDGLT_OTP = 1	20 40	25 45	30 50	µs
t_{TRK2UV_DGLT}	TRK2 undervoltage deglitch time: VMON_TRK2_UVDGLT_OTP[1:0] = 00 VMON_TRK2_UVDGLT_OTP[1:0] = 01 VMON_TRK2_UVDGLT_OTP[1:0] = 10 VMON_TRK2_UVDGLT_OTP[1:0] = 11	2.5 10 20 35	5 15 25 40	7.5 20 30 45	µs

22.8.7 VREF monitoring

Because of an internal dedicated connection to the VREF pad, the FS26 can detect faults on the VREF output voltage. Both overvoltage and undervoltage conditions can be detected.

To support various system configurations, VREF monitoring can be activated, or not activated, with an OTP bit. Also, to support both output voltages of the VREF, an OTP bit is available to set the target voltage value to monitor. To fit multiple system requirements, a wide range of upper and lower thresholds can be selected with OTP bits.

To allow flexibility in the application, reactions to both overvoltage and undervoltage faults are configurable with VMON_VREF_OV_FS_REACTION[1:0] and VMON_VREF_UV_FS_REACTION[1:0] bits during the initialization phase.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the “Enable Monitoring” state is reached.

To reach ASIL D at the VREF pin level, the pin lift detection mechanism must be activated using the VREF_PLIFT_DIS_OTP bit.

If the VREF pin is disconnected, the VREF output voltage will be pulled to LDOIN within $t_{VREF\_PINLIFT}$ and will create an overvoltage, and the device will react according to VMON_VREF_OV_FS_REACTION[1:0]. A minimum headroom $V_{TRKIN\_MIN\_PINLIFT}$ is mandatory to guarantee the pin lift detection.

Table 180. VREF overvoltage reaction configuration

VMON_VREF_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 181. VREF undervoltage reaction configuration

VMON_VREF_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 182. VREF monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{MONREF_CFG}	VREF monitoring target voltage setting VREF_V_OTP = 0 VREF_V_OTP = 1	 — —	 3.3 5.0	 — —	 V
$V_{TRKIN\_MIN\_PINLIFT}$	Minimum headroom to guarantee VREF pin lift detection	VREF_V_OTP x ($V_{MON\_VREF\_OVTH\_OTP}$ + 1 %) + 0.5 V	—	—	V
$V_{MONREF\_OVTH\_RANGE}$	VREF overvoltage monitoring threshold range setting with VMON_VREF_OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONREF\_OVTH\_STEP}$	VREF overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONREF\_OVTH\_ACC}$	VREF overvoltage detection accuracy	-1	—	1	%
$V_{MONREF\_UVTH\_RANGE}$	VREF undervoltage monitoring threshold range setting with VMON_VREF_UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONREF\_UVTH\_STEP}$	VREF undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONREF\_UVTH\_ACC}$	VREF undervoltage detection accuracy	-1	—	1	%
Dynamic electrical characteristics					
t_{VREFOV_DGLT}	VREF overvoltage deglitch time VMON_VREF_OVDGLT_OTP = 0 VMON_VREF_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	 µs
t_{VREFUV_DGLT}	VREF undervoltage deglitch time VMON_REF_UVDGLT_OTP[1:0] = 00 VMON_REF_UVDGLT_OTP[1:0] = 01 VMON_REF_UVDGLT_OTP[1:0] = 10 VMON_REF_UVDGLT_OTP[1:0] = 11	 2.5 10 20 35	 5 15 25 40	 7.5 20 30 45	 µs
$t_{VREF\_PINLIFT}$	VREF pin lift detection time	—	—	5	ms

22.8.8 External monitoring input

The FS26 has one dedicated external monitoring input that can be used to monitor a voltage from another device inside the application. It can detect faults on the VMONEXT pin voltage. Both overvoltage and undervoltage conditions can be detected.

To support various system configurations, analog input monitoring can be activated, or not activated, with an OTP bit. The expected voltage value on VMONEXT pin is fixed and a proper resistor bridge to downscale it shall be provided externally. To fit multiple system

requirements, a wide range of upper and lower thresholds can be selected with the OTP bits.

To allow flexibility in the application, reactions to both overvoltage and undervoltage faults are configurable with the VMON_EXT_OV_FS_REACTION[1:0] and VMON_EXT_UV_FS_REACTION[1:0] bits during the initialization phase. If a 'short to high' type of fault on VMON_EXT should not impact RSTB, NXP recommends configuring VMON_ EXT_OV_FS_REACTION[1:0] = 01 before turning ON the external regulator.

The monitoring is able to report UV/OV flags as soon as the power-up sequence is completed and the “Enable Monitoring” state is reached.

Table 183. VMONEXT overvoltage reaction configuration

VMON_EXT_OV_FS_REACTION[1:0]	Overvoltage faults reaction
00	No action on Safety Output(s) and RSTB
01	An overvoltage detection asserts safety output(s) only
1x (default)	**An overvoltage detection asserts safety output(s) and RSTB**

Table 184. VMONEXT undervoltage reaction configuration

VMON_EXT_UV_FS_REACTION[1:0]	Undervoltage faults reaction
00	No action on Safety Output(s) and RSTB
01 (default)	**An undervoltage detection asserts safety output(s) only**
1x	An undervoltage detection asserts Safety output(s) and RSTB

Table 185. VMONEXT monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
	Static electrical characteristics				
V_{MONEXT_CFG}	VMONEXT monitoring target voltage setting (voltage between VMONEXT pin and ground)	—	0.8	—	V
$V_{MONEXT\_OVTH\_RANGE}$	VMONEXT overvoltage monitoring threshold range setting with VMON_EXT_OVTH_OTP[3:0] bits	104.5	—	112	%
$V_{MONEXT\_OVTH\_STEP}$	VMONEXT overvoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONEXT\_OVTH\_ACC}$	VMONEXT overvoltage detection accuracy	-1.2	—	1.2	%
$V_{MONEXT\_UVTH\_RANGE}$	VMONEXT undervoltage monitoring threshold range setting with VMON_EXT_UVTH_OTP[3:0] bits	88	—	95.5	%
$V_{MONEXT\_UVTH\_STEP}$	VMONEXT undervoltage monitoring OTP threshold setting step	—	0.5	—	%
$V_{MONEXT\_UVTH\_ACC}$	VMONEXT undervoltage detection accuracy	-1.2	—	1.2	%
R_{MONEXT_PD}	Internal pulldown resistor on VMONEXT pin	1	2	4	MΩ
Dynamic electrical characteristics					
t_{EXTOV_DGLT}	VMONEXT overvoltage deglitch time VMON_EXT_OVDGLT_OTP = 0 VMON_EXT_OVDGLT_OTP = 1	 20 40	 25 45	 30 50	µs

Table 185. VMONEXT monitoring electrical characteristics*...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_{EXTUV_DGLT}	VMONEXT undervoltage deglitch time				
	VMON_EXT_UVDGLT_OTP[1:0] = 00	2.5	5	7.5	µs
	VMON_EXT_UVDGLT_OTP[1:0] = 01	10	15	20	
	VMON_EXT_UVDGLT_OTP[1:0] = 10	20	25	30	
	VMON_EXT_UVDGLT_OTP[1:0] = 11	35	40	45	

22.9 External IC monitoring

To monitor another device (on top of the microcontroller) in the application, the WAKE2 pin can be configured as a digital input. This external IC monitoring feature is enabled by OTP. When this feature is activated, the WAKE2 pin is used to monitor an external IC.

This monitoring is active as soon as the initialization phase is closed by the first good watchdog refresh. A transition detected at the WAKE2 pin indicates an error from the external IC.

The following parameters can be configured during FS26 initialization to facilitate monitoring of an external IC in the application:

- The polarity of the fault signal is configurable with the ERRMON_FLT_POLARITY bit during the initialization phase.
- The desired reaction on RSTB and safety output(s).
- The time allowed to the microcontroller for receiving error acknowledgment.

When an error is detected, the microcontroller should acknowledge the FS26 device. If the acknowledgment is not received by the FS26 within the predefined time, the FS26 will assert its safety output(s) and the RSTB pin will react as defined during the initialization phase.

The following tables show the various SPI bits used by this external IC monitoring function:

Table 186. Signal polarity to detect an error on WAKE2 pin

ERRMON_FLT_POLARITY	Condition to detect a fault
0 (default)	**High to low level**
1	Low to high level

Table 187. Reaction when an error is detected WAKE2 pin

ERRMON_FS_REACTION	Reaction
0	Error on WAKE 2 pin asserts safety output(s) only
1 (default)	**Error on WAKE 2 pin asserts safety output(s) and RSTB**

Table 188. Allowed time to receive microcontroller acknowledge when an external IC error is detected

ERRMON_ACK_TIME[1:0]	Time allowed for acknowledgment
00	1 ms
01 (default)	**8 ms**
10	16 ms
11	32 ms

Table 189. Error flag for external IC monitoring

ERRMON	Error flag on WAKE 2
0	No error
1	Error detected. FS26 is waiting for an acknowledge within the allowed time.

Table 190. Acknowledge error detection from MCU

ERRMON_ACK	Error flag on WAKE 2
0	No error
1	Error detected

The acknowledgment by the MCU is done through SPI communication according to Figure 57.

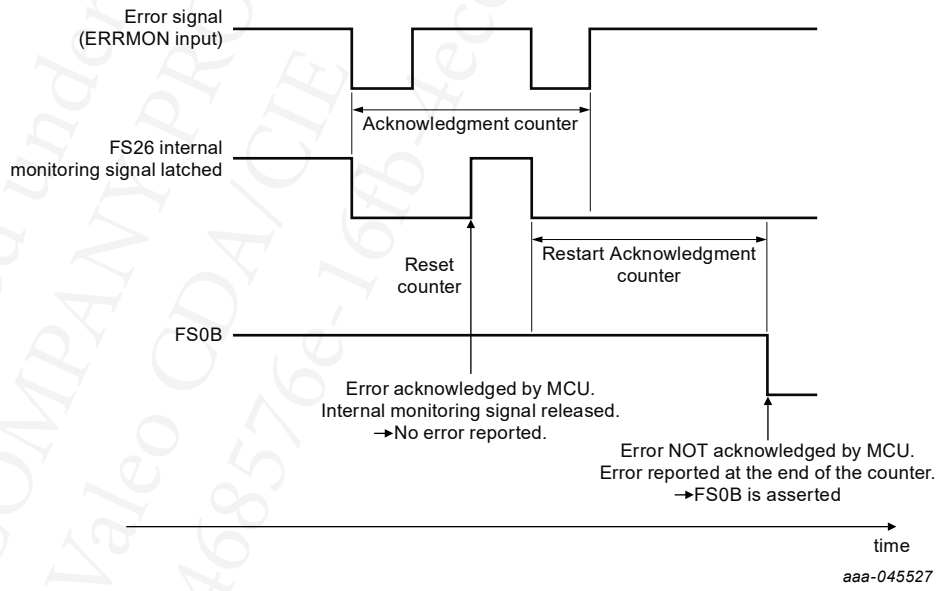


Figure 57. External IC monitoring timing diagram

Table 191. External IC monitoring electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{IH_ERRMON}	High-level input voltage threshold	—	—	1.4	V
V_{IL_ERRMON}	Low-level input voltage threshold	0.5	—	—	V
$V_{IN\_HYS\_ERRMON}$	Threshold hysteresis	50	190	500	mV
t_{ERRMON_ERR}	Filtering time	4	—	8	µs
$t_{ERRMON\_ACK\_ACC}$	acknowledgment counter accuracy	-10	—	10	%
R_{PD_ERRMON}	ERRMON pulldown resistor value	100	200	320	kΩ

22.10 Fault management

22.10.1 Fault error counter

The FS26 integrates a configurable fault error counter which counts the number of faults related to the device itself, and also those caused by external events. The fault error counter starts at level "1" after a POR or when resuming from Low Power modes. The final value of the fault error counter is used to transition to DFS mode. The maximum value of this counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bits during the initialization phase.

Table 192. Fault error counter configuration

FLT_ERR_CNT_LIMIT[1:0]	Error counter maximum value	Error counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6

The fault error counter has two output values: intermediate and final. The intermediate value can be used to force the FS0B activation or to generate an RSTB pulse according to the FLT_ERR_REACTION[1:0] bits configuration.

Table 193. Fault error counter reaction configuration

FLT_ERR_REACTION[1:0]	Reaction
00	No effect on RSTB and FS0B
01 (default)	**FS0B is asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value**
10	RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value
11	RSTB and FS0B are asserted low if FLT_ERR_CNT[3:0] ≥ intermediate value

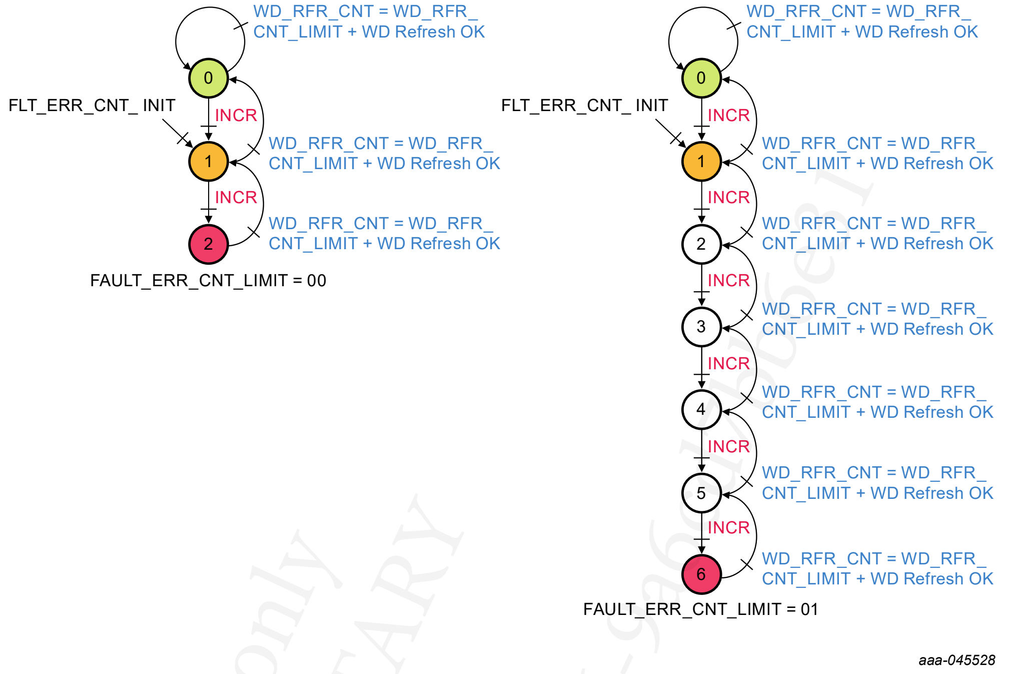


Figure 58. Fault error counter (FLT_ERR_CNT_LIMIT[1:0] = 00 or 01)

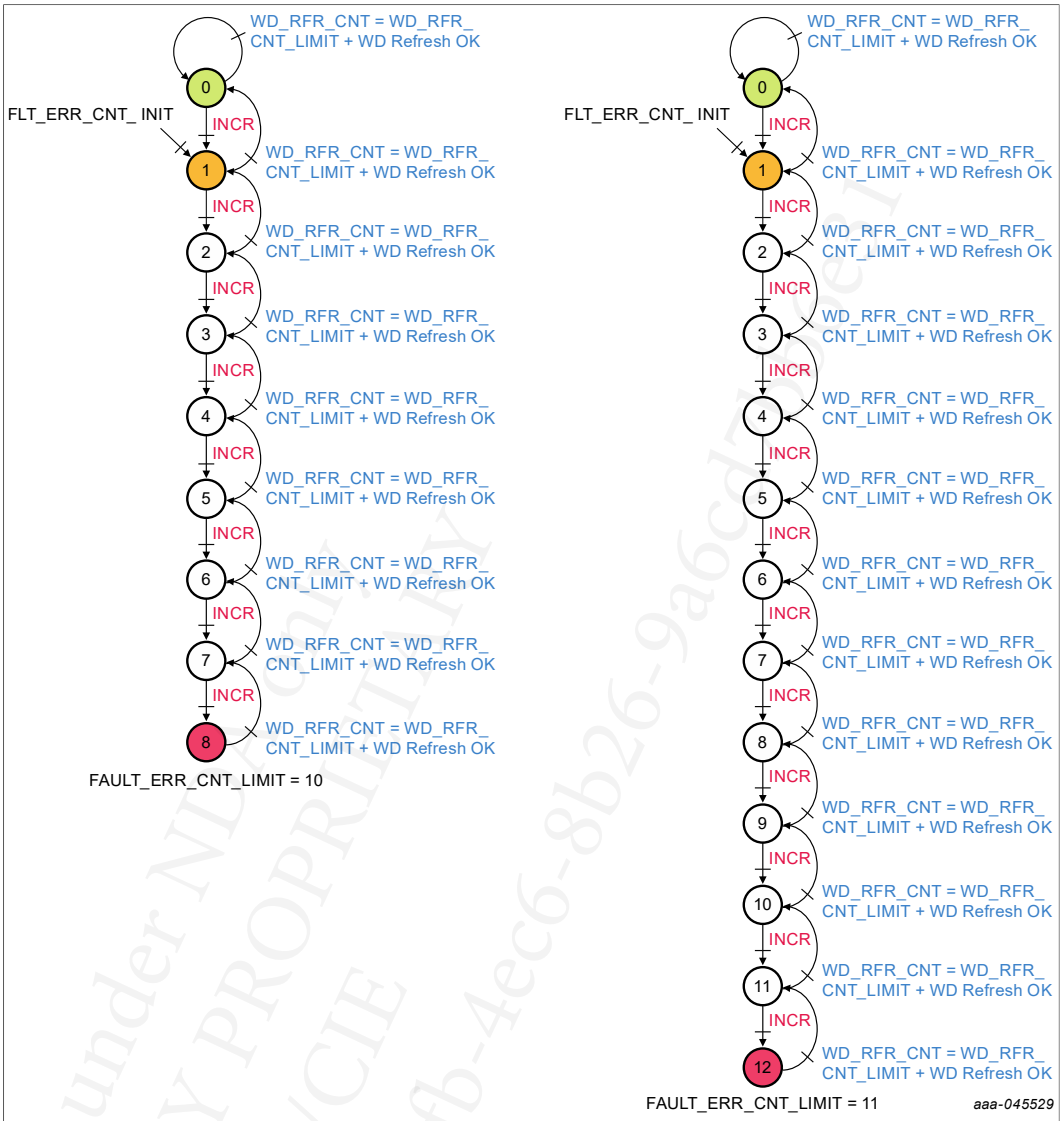


Figure 59. Fault error counter (FLT_ERR_CNT_LIMIT[1:0] = 10 or 11)

22.10.2 Fault sources and reactions

In Normal mode, when FS0B and RSTB (and FS1B if used) are released, the fault error counter is incremented when a fault is detected by the FS26 fail-safe state machine. Table 194 lists the faults and their impact on RSTB, FS0B and FS1B pins according to the device configuration. The faults that are configured to not assert RSTB and FS0B (and FS1B if used) will not increment the fault error counter. In that case, only the flags are available for MCU diagnostics. When FS0B is asserted, the fault error counter continues to be incremented by +1 each time the WD error counter reaches its maximum value. With default configuration, when FS0B is asserted, the fault error counter is not incremented by 1 in case of UV detection on a regulator. When a RSTB failure occurs, the fault error counter is increased by 1 and a new 256 ms watchdog window is opened.

Table 194. Application related fail-safe fault list and reaction

In orange, the reaction is not configurable.

In green, the reaction is configurable by SPI during the INIT_FS state.

Apps related Fail-safe faults	Fault error counter increment	FS0B assertion	RSTB assertion
VPRE power rail overvoltage	+1	VMON_PRE_OV_FS_REACTION[0]	VMON_PRE_OV_FS_REACTION[1]
VCORE power rail overvoltage	+1	VMON_CORE_OV_FS_REACTION[0]	VMON_CORE_OV_FS_REACTION[1]
VLDO1 power rail overvoltage	+1	VMON_LDO1_OV_FS_REACTION[0]	VMON_LDO1_OV_FS_REACTION[1]
VLDO2 power rail overvoltage	+1	VMON_LDO2_OV_FS_REACTION[0]	VMON_LDO2_OV_FS_REACTION[1]
VTRK1 power rail overvoltage	+1	VMON_TRK1_OV_FS_REACTION[0]	VMON_TRK1_OV_FS_REACTION[1]
VTRK2 power rail overvoltage	+1	VMON_TRK2_OV_FS_REACTION[0]	VMON_TRK2_OV_FS_REACTION[1]
VREF power rail overvoltage	+1	VMON_VREF_OV_FS_REACTION[0]	VMON_VREF_OV_FS_REACTION[1]
Overvoltage on the analog input monitoring	+1	VMON_EXT_OV_FS_REACTION[0]	VMON_EXT_OV_FS_REACTION[1]
VPRE power rail undervoltage	+1	VMON_PRE_UV_FS_REACTION[0]	VMON_PRE_UV_FS_REACTION[1]
VCORE power rail undervoltage	+1	VMON_CORE_UV_FS_REACTION[0]	VMON_CORE_UV_FS_REACTION[1]
VLDO1 power rail undervoltage	+1	VMON_LDO1_UV_FS_REACTION[0]	VMON_LDO1_UV_FS_REACTION[1]
VLDO2 power rail undervoltage	+1	VMON_LDO2_UV_FS_REACTION[0]	VMON_LDO2_UV_FS_REACTION[1]
VTRK1 power rail undervoltage	+1	VMON_TRK1_UV_FS_REACTION[0]	VMON_TRK1_UV_FS_REACTION[1]
VTRK2 power rail undervoltage	+1	VMON_TRK2_UV_FS_REACTION[0]	VMON_TRK2_UV_FS_REACTION[1]
VREF power rail undervoltage	+1	VMON_VREF_UV_FS_REACTION[0]	VMON_VREF_UV_FS_REACTION[1]
Undervoltage on the analog input monitoring	+1	VMON_EXT_UV_FS_REACTION[0]	VMON_EXT_UV_FS_REACTION[1]
An error is sent by the MCU on FCCU1 and FCCU2 pins (dual wire protocol)	+1	Yes	FCCU12_FS_REACTION
An error is sent by the MCU on FCCU1 pin (single wire protocol)	+1	Yes	FCCU1_FS_REACTION
An error is sent by the MCU on FCCU2 pin (single wire protocol)	+1	Yes	FCCU2_FS_REACTION
An external IC is driving to the error state the signal connected on ERRMON pin	+1	Yes	ERRMON_FS_REACTION

Table 194. Application related fail-safe fault list and reaction...*continued*

In orange, the reaction is not configurable.

In green, the reaction is configurable by SPI during the INIT_FS state.

Apps related Fail-safe faults	Fault error counter increment	FS0B assertion	RSTB assertion
Watchdog error counter reaches its maximum value (WD_ERR_CNT[3:0] = @WD_ERR_LIMIT[1:0])	+1	WD_FS_REACTION[0]	WD_FS_REACTION[1]
The fault error counter reaches its intermediate value: (@WD_ERR_LIMIT[1:0])/2	No	FLT_ERR_REACTION[0]	FLT_ERR_REACTION[1]
Wrong WD refresh in INIT_FS state	+1	Yes	Yes
No WD refresh in INIT_FS	+1	Yes	Yes
RSTB pin asserted externally	+1	No[1]	Yes (low externally)
RSTB pulse request by MCU	No	No[1]	Yes
RSTB short to high	+1	Yes	No (high externally)
FS0B short to high	+1	No (high externally)	BACKUP_SAFETY_PATH_FS0B
FS0B request by the MCU	No	Yes	No
FS1B Short to high	+1	No	BACKUP_SAFETY_PATH_FS1B
FS1B request by the MCU	No	Yes	No
REG_CORRUPT = 1	+1	Yes	No
OTP_CORRUPT = 1	+1	Yes	No
GOTO_INIT request by MCU	No	No[1]	No

[1] By cascaded effect, the FS0B is asserted low in INIT_FS state.

22.11 Safety outputs (RSTB, FS0B, FS1B)

These two or three (depending on the product part number) safety output pins are meant to set the ECU in a protected and known safe state. All these safety outputs are active low, and the internal implementation is an open drain topology.

22.11.1 RSTB pin

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU. RSTB requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pulldown R_{RSTB_PD} ensures an RSTB low level in LPOFF. RSTB remains high in Standby mode. RSTB assertion depends on the device configuration during the initialization phase. When RSTB is asserted low, FS0B is also asserted low. An internal pullup on the gate of the low-side MOS ensures an RSTB low level in case of logic failure. When RSTB is stuck low for more than T_{RSTB_8S}, the device transitions into Deep Fail Safe mode.

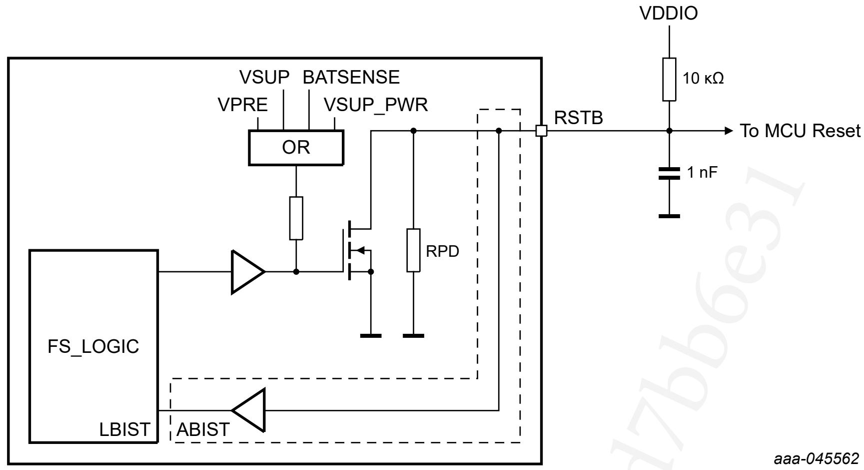


Figure 60. RSTB implementation

Table 195. RSTB safety outputs electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{RSTB_IL}	RSTB low detection threshold	0	—	0.7	V
V_{RSTB_IH}	RSTB high detection threshold	1.5	—	—	V
V_{RSTB_HYS}	RSTB level detection Hysteresis	100	—	300	mV
V_{RSTB_VOL}	RSTB low level output voltage (with I_{RSTB} = 2.0 mA)	—	—	0.4	V
R_{RSTB_PD}	RSTB internal pull-down resistor	200	400	800	kΩ
I_{RSTB_ILIM}	RSTB current limitation	4	—	22	mA
Dynamic electrical characteristics					
t_{RSTB_FB}	RSTB sensing filtering time	8	—	15	µs
t_{RSTB_SHORT}	RSTB short to high detection timer	500	650	800	µs
t_{RSTB_LPULSE}	RSTB long pulse (with RSTB_DUR = 0)	9	—	11	ms
t_{RSTB_SPULSE}	RSTB short pulse (with RSTB_DUR = 1)	0.9	—	1.1	ms
t_{RSTB_8s}	8 second timer to detect RSTB shorted to ground	7	8	9	s
$t_{RSTB\_RELEASE}$	Minimum time to release RSTB from POR - with all regulators started in Slot 0 - with TSLOT_OTP[2:0] = 000 - with SLOT_BYP_OTP[2:0] = 001 - with VPRE_SS_OTP[1:0] = 00 - with VBST_CFG_OTP[1:0] = 1	—	5.5	7	ms

22.11.2 FS0B pin

The purpose of this pin is to drive safe electrical circuitry independent from the MCU to deactivate the whole system and set the ECU in a protected and known state.

After each power-on reset or after each wake-up event (either from Standby or LPOFF mode) the FS0B pin is asserted low. The MCU can release the FS0B pin when the application is ready to start. External pullup circuitry must be connected to VDDIO or VSUP.

- If the pullup is connected to VDDIO, the value recommended is 5.1 kΩ. There is no current in LPOFF, because VDDIO is off in LPOFF mode;
- If the pullup is connected to VSUP, the value must be above 10 kΩ. There is a current in the pullup resistor to consider at the application level in LPOFF mode.

Some faults can be configured to either assert or not assert FS0B. Other faults assert FS0B without the possibility to be configured.

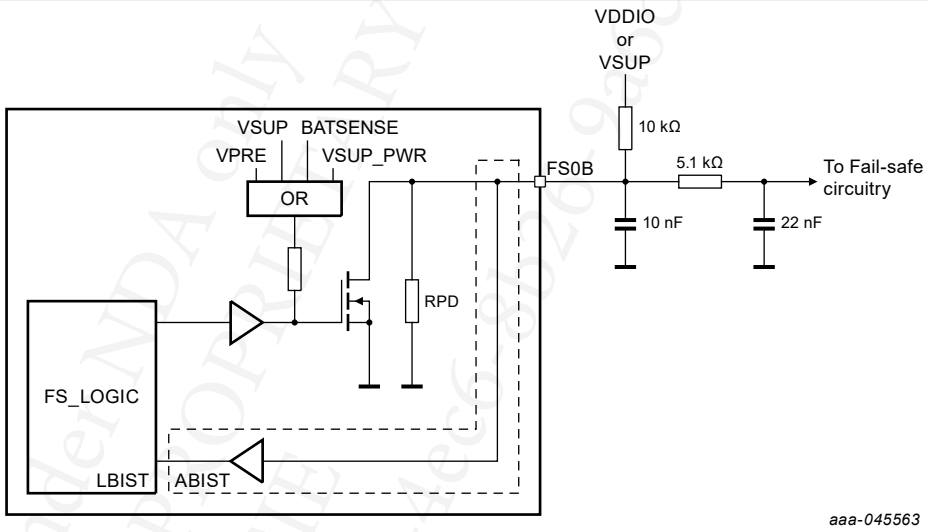


Figure 61. FS0B implementation

Table 196. FS0B safety outputs electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{FS0B_IL}	FS0B low detection threshold	0	—	0.7	V
V_{FS0B_IH}	FS0B high detection threshold	1.5	—	—	V
V_{FS0B_HYS}	FS0B level detection Hysteresis	100	—	300	mV
V_{FS0B_VOL}	FS0B low level output voltage (with I_{FS0B} = 2.0 mA)	—	—	0.4	V
R_{FS0B_PD}	FS0B internal pulldown resistor	1	2	4	MΩ
I_{FS0B_ILIM}	FS0B current limitation	4	—	22	mA
Dynamic electrical characteristics					

Table 196. FS0B safety outputs electrical characteristics...*continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
t_{FS0B_FB}	FS0B sensing filtering time	8	10	15	µs
t_{FS0B_SHORT}	FS0B short to high detection timer	500	650	800	µs

22.11.3 FS1B pin

The FS1B pin is the secondary safety output pin. FS1B is asserted low with a configurable delay (t_{DELAY}) or duration (t_{DUR}) when FS0B is asserted low. This pin can be used to:

- Open the phases of a motor after a configurable delay, starting when FS0B is asserted, to demagnetize the motor coils and reduce the inductive effect when the switch opens.
- Disable an external physical layer during a configurable duration, starting when FS0B is asserted, to avoid miscommunication when the module is in fail mode.
- Be a redundant safety output pin to FS0B when t_{DELAY} = 0. In this case, FS1B is asserted at the same time as FS0B.
- Any other use case where a second safety pin is needed.

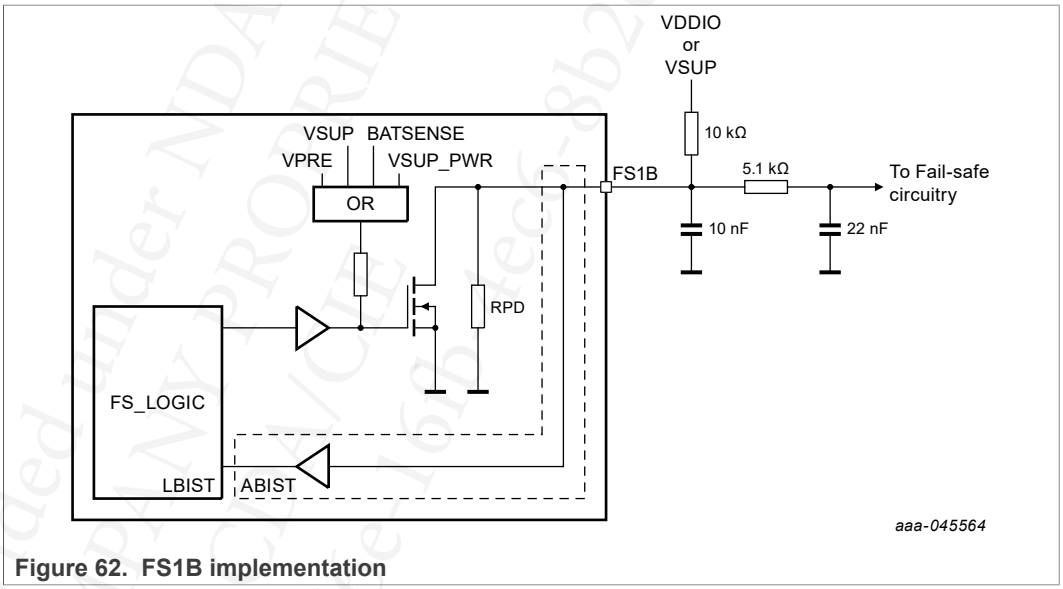


Figure 62. FS1B implementation

After each power-on reset or after each wake-up event (from Standby or LPOFF mode) the FS1B pin is asserted low. Then the MCU can decide to release the FS1B pin when the application is ready to start. External pullup circuitry connected to VSUP or VDDIO is mandatory.

To offer full flexibility to the system implementation, both t_{DELAY} and t_{DUR} are configurable through the FS_SAFE_IOS_2 SPI register as described in Section 18.14.

Because of this flexibility, five use cases can be supported to fit perfectly with system requirements, as described below:

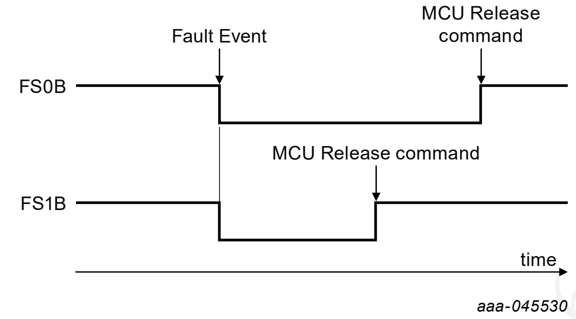


Figure 63. FS1B use case 2: asserted when FS0B is asserted and released with MCU request (FS1B_FS0B_EN_OTP = 1, no impact from FS1B_TDELAY[4:0] and FS1B_TDUR settings)

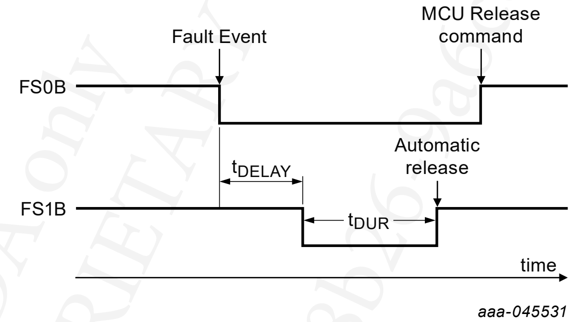


Figure 64. FS1B use case 3: asserted with a delay after FS0B and released after t_{DUR} elapsed (FS1B_FS0B_EN_OTP = 0, FS1B_TDELAY[4:0] ≠ 00000 and FS1B_TDUR[4:0] ≠ 00000 and 11111)

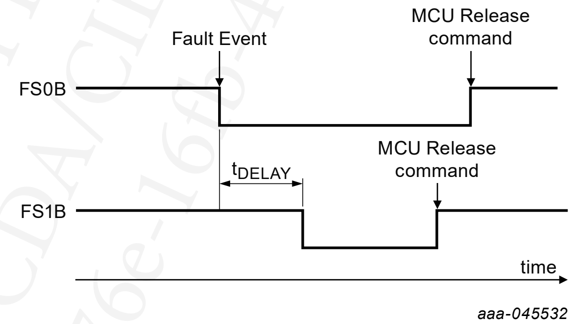


Figure 65. FS1B use case 4: asserted with a delay after FS0B and released with MCU request (FS1B_FS0B_EN_OTP = 0, FS1B_TDELAY[4:0] ≠ 00000 and FS1B_TDUR[4:0] = 11111)

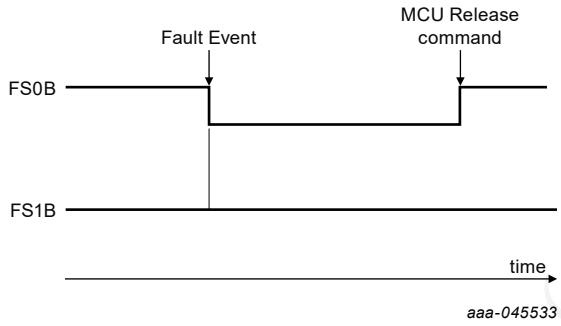


Figure 66. FS1B use case 5: FS1B never asserted (FS1B_FS0B_EN_OTP = 0, FS1B_TDUR[4:0] = 00000)

When sending a GOTO_INIT SPI command (in the FS_SAFE_IOS_1 register), FS1B assertion and release will depend on FS1B_TDUR and FS1B_TDELAY settings. To avoid unexpected FS1B release during initialization phase, FS1B_TDUR and FS1B_TDELAY must be updated accordingly. When the FS26 is requested to go into LPOFF or Standby mode, transition timing and FS1B assertion will depend on the FS1B_TDUR and FS1B_TDELAY settings.

Going into LPOFF:

- If ‘FS1B_TDUR = 0s’, FS1B_TDELAY will not be taken into account, and the device will assert FS1B and go into LPOFF as soon as the 2nd SPI command is received and acknowledged.
- If ‘0s < FS1B_TDUR < Infinite’, the transition into LPOFF will be delayed by FS1B_TDELAY + FS1B_TDUR, and FS1B will be asserted after t_{DELAY}. Regardless of the FS1B_TDUR setting, FS1B will not be released.
- If ‘FS1B_TDUR = Infinite’, the transition into LPOFF will be delayed only by FS1B_TDELAY, and FS1B will be asserted after t_{DELAY}.

Going into Standby:

- If ‘FS1B_TDUR = 0s’, FS1B_TDELAY will not be taken into account, and the device will either assert FS1B or not (if pulled up to an active regulator in Standby mode) and go into Standby as soon as the 2nd SPI command is received and acknowledged.
- If ‘0s < FS1B_TDUR < Infinite’, the transition into Standby will be delayed by FS1B_TDELAY + FS1B_TDUR, and FS1B will be asserted after t_{DELAY}. FS1B will then be released after t_{DUR}.
- If ‘FS1B_TDUR = Infinite’, transition into Standby will be delayed by FS1B_TDELAY only and FS1B will be asserted after t_{DELAY}.

Figure 67, Figure 68, and Figure 69 describe the different behaviors possible when going into Standby or LPOFF mode.

In Low Power mode, when FS1B is configured to be released after FS1B_TDUR (FS1B_TDUR [4:0] != 11111) and if the supply connected to the FS1B pullup resistor is kept enabled, it will be reported as a short-to-high failure by the ABIST1 at the next power up. Therefore, the ABIST1 will fail and the ABIST1_PASS bit will be set to 0.

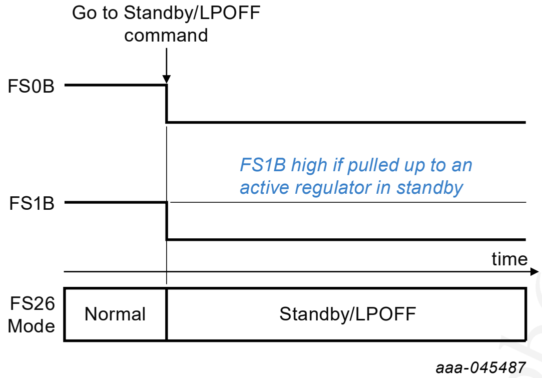


Figure 67. FS1B behavior and transition to LPOFF/Standby when 'FS1B_TDUR = 0 s'

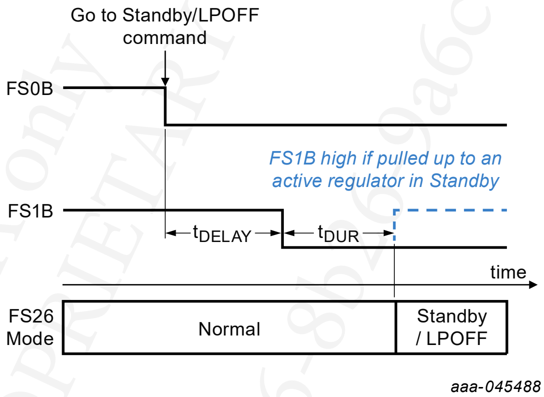


Figure 68. FS1B behavior and transition to LPOFF/Standby when '0 s < FS1B_TDUR < Infinite'

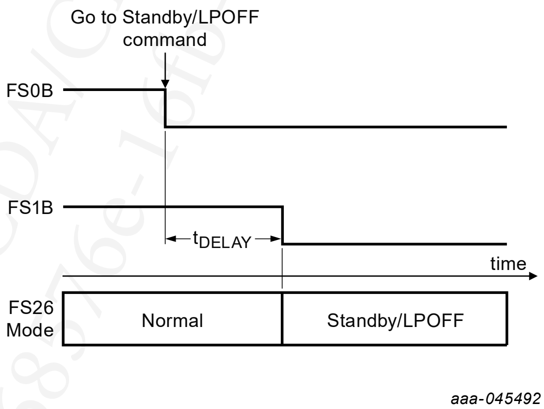


Figure 69. FS1B behavior and transition to LPOFF/Standby when 'FS1B_TDUR = Infinite'

Table 197. FS1B safety outputs electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Static electrical characteristics					
V_{FS1B_IL}	FS1B low detection threshold	0	—	0.7	V
V_{FS1B_IH}	FS1B high detection threshold	1.5	—	—	V
V_{FS1B_HYS}	FS1B level detection Hysteresis	100	—	300	mV
V_{FS1B_VOL}	FS1B low level output voltage (with I_{FS1B} = 2.0 mA)	—	—	0.4	V
R_{FS1B_PD}	FS1B internal pulldown resistor	1	2	4	MΩ
I_{FS1B_ILIM}	FS1B current limitation	4	—	22	mA
Dynamic electrical characteristics					
t_{FS1B_FB}	FS1B sensing filtering time	8	10	15	µs
t_{FS1B_SHORT}	FS1B short to high detection timer	500	650	800	µs

22.11.4 Safety outputs release

When the safety output FS0B is asserted low by the device, the exit conditions must be validated before it allows this pin to be released. These conditions are:

- LBIST_OK.
- ABIST_OK.
- Fault is removed.
- Fault Error Counter = 0.
- SPI write to RELEASE_FS0B_FS1B [15:0] register.

When the safety output FS1B is asserted low by the device, the exit conditions must be validated before it allows this pin to be released. These conditions are:

- LBIST_OK.
- Fault is removed.
- SPI write to RELEASE_FS0B_FS1B [15:0] register.

The procedure to compute the RELEASE_FS0B_FS1B [15:0] value to release the safety outputs is described below, with Table 198 illustrating all these steps with an example:

1. Get the FS_WD_TOKEN value.
2. Swap MSB/LSB of the value get in step No. 1.
3. Invert all computed bits at step No. 2.
4. Write bits 12 to 0 computed in step No. 3 into RELEASE_FS0B_FS1B [12:0] register. Bits 15 to 13 are used to select the safety output(s) to release as shown in Table 199.

Table 198. RELEASE_FS0B_FS1B bits code to release safety outputs

Step #1	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Read FS_WD_ TOKEN register	1	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0

Step #2	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reverse LSB/MSB	0	0	0	0	1	1	1	1	0	0	1	0	0	1	1	1

Step #3	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Complement bits	1	1	1	1	0	0	0	0	1	1	0	1	1	0	0	0

Step #4	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Write to RELEASE_ FS0B_FS1B[12:0]	**1**	**0**	**1**	1	0	0	0	0	1	1	0	1	1	0	0	0

Table 199. Bits 15 to 13 RELEASE_FS0B_FS1B register bit description

Bit	Symbol	Description
15 to 13	RELEASE_FS0B_FS1B[15:13]	**Bits to select the desired safety output to release**
		011 Release FS0B only
		110 Release FS1B only
		101 Release FS0B and FS1B

22.12 Built-in self-tests

To reduce latent faults, built-in self-tests are implemented in the functional safety circuitry. Both logical and analog areas can be checked when the device is powering up, or when it goes back to Normal mode from Low Power modes.

22.12.1 LBIST

The fail-safe state machine includes a logic built-in self-test (LBIST) to verify the correct functionality of the safety logic circuitry. It is performed after each start-up of the device or after each wake-up from Low Power modes. In the case of an LBIST failure, RSTB is released, but FS0B and FS1B remain low and cannot be released. The flag LBIST_OK is available through SPI for microcontroller diagnostics. The maximum LBIST duration is 3 ms. LBIST availability is dependent on part number. The microcontroller can check the LBIST status, using the LBIST_STATUS[1:0] SPI bits.

Table 200. LBIST SPI Flags bits

LBIST_STATUS[1:0]	LBIST Status
00	Reserved (Not used)
01	LBIST bypassed
10	LBIST fail
11	LBIST passed

22.12.2 Analog built-in self-test (ABIST1)

The fail-safe state machine includes one built-in self-test (BIST) to verify the correct functionality of the safety analog circuitry. The analog BIST (ABIST) is executed automatically when the device is powered on, or after each transition from Low Power modes to Normal mode. This self-test checks all the voltage comparators that are used

to detect undervoltage and overvoltage faults. It also checks, via a dedicated sense path, the voltage level of the safety output(s) pin(s) and compares it (or them) to the logic control. This self-test between logic control and voltage on the pin is also done for the RSTB pin.

In the case of ABIST failure, RSTB is released, but FS0B remains low and cannot be released. To support various system configurations, ABIST can be activated or deactivated via OTP bits. The ABIST coverage is detailed in the safety manual.

22.12.3 Analog built-in self-test on demand (ABIST2)

On top of the ABIST launched when the device is starting up, self-test of voltage monitoring comparators can be requested by the microcontroller. This request is accessible via a SPI request as soon as the FS26 is in Normal mode. ABIST on demand allows checking of the latent fault time interval during Normal operation, and not only at power-up sequence. This feature is available for specific part numbers. To launch this check, the microcontroller must select which monitoring has to be checked. Then, with a single SPI access, the check sequence launches. The result of this self-test is available via SPI on one bit.

Table 201. ABIST on demand for VPRE monitoring SPI enable bits

ABIST2_VPRE	ABIST on demand request
0	Not requested
1	Requested

Table 202. ABIST on demand for VCORE monitoring SPI enable bits

ABIST2_CORE	ABIST on demand request
0	Not requested
1	Requested

Table 203. ABIST on demand for LDO1 monitoring SPI enable bits

ABIST2_LDO1	ABIST on demand request
0	Not requested
1	Requested

Table 204. ABIST on demand for LDO2 monitoring SPI enable bits

ABIST2_LDO2	ABIST on demand request
0	Not requested
1	Requested

Table 205. ABIST on demand for TRK1 monitoring SPI enable bits

ABIST2_TRK1	ABIST on demand request
0	Not requested

Table 205. ABIST on demand for TRK1 monitoring SPI enable bits*...continued*

ABIST2_TRK1	ABIST on demand request
1	Requested

Table 206. ABIST on demand for TRK2 monitoring SPI enable bits

ABIST2_TRK2	ABIST on demand request
0	Not requested
1	Requested

Table 207. ABIST on demand for VREF monitoring SPI enable bits

ABIST2_REF	ABIST on demand request
0	Not requested
1	Requested

Table 208. ABIST on demand for VMON_EXT monitoring SPI enable bits

ABIST2_EXT	ABIST on demand request
0	Not requested
1	Requested

Table 209. ABIST on demand launch SPI enable bits

LAUNCH_ABIST2	ABIST on demand sequence launch
0	No action
1	Start ABIST on demand sequence

Table 210. ABIST on demand status SPI status bits

ABIST2_DONE	ABIST status
0	Self-test on going
1	Self-test sequence completed

Table 211. ABIST on demand result SPI status bits

ABIST2_PASS	ABIST result
0	Self-test failed or not executed
1	Self-test passed

Table 212. ABIST coverage

Monitoring	Overvoltage	Undervoltage	Short to high	ABIST1	ABIST2
VPRE	X [1]	X		OTP [2]	SPI request [3]
VCORE	X	X		OTP	SPI request
TRK1	X	X		OTP	SPI request
TRK2	X	X		OTP	SPI request
LDO1	X	X		OTP	SPI request
LDO2	X	X		OTP	SPI request
VREF	X	X		OTP	SPI request
VMONEXT	X	X		OTP	SPI request
VANA_FS and VDIG_FS	X			X	
RSTB			X	X	
FS0B			X	X	
FS1B			X	X	

[1] Means the check of the monitoring is done
[2] Means the check of the monitoring can be configured by OTP
[3] Means the check of the monitoring can be requested by SPI

Table 213. ABIST1/2 electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
$ABIST1_{TDUR}$	ABIST1 duration • MIN with no voltage monitoring assigned by OTP • MAX with all voltage monitoring assigned by OTP	50	—	300	μs
$ABIST2_{TDUR}$	ABIST2 duration • MIN with no voltage monitoring assigned by OTP • MAX with all voltage monitoring assigned by OTP	50	—	300	μs

23 OTP and Debug mode

OTP mode and Debug mode are intended for use during the development process, not in production applications or vehicles. OTP mode is intended for OTP emulation and OTP programming.

When an OTP configuration is emulated, the configuration remains available until the POR of the digital circuitry. The fail-safe configuration is lost in low power mode (LPOFF and Standby) since the fail-safe digital is OFF in these modes.

The main digital configuration is lost when VSUP is removed, which means $V_{BOS} < V_{BOS\_POR}$. When an OTP configuration is programmed, the device will start with the programmed OTP configuration by default. A programmed part cannot be re-programmed, but can be emulated. To enter OTP mode, the voltage at the DEBUG pin must be set to V_{OTP} prior to applying VSUP voltage.

During the power-up sequence, the main and the fail-safe state machines will stop prior to starting the regulators, waiting for SPI communication to send an OTP configuration to the device. When the OTP configuration is complete, the fail-safe state machine will start in Debug mode when the voltage at the DEBUG pin is below V_{NORM_max} (NXP recommends applying 0 V or GND).

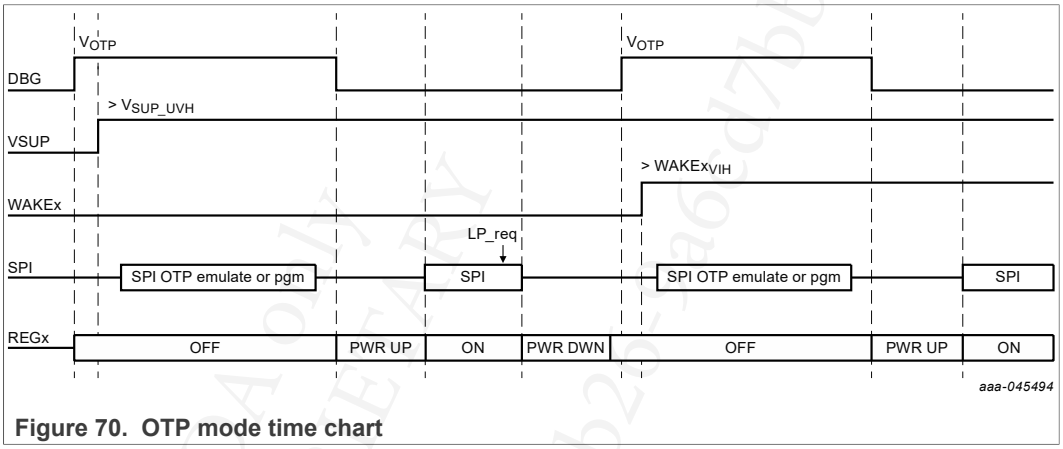


Figure 70. OTP mode time chart

The Debug mode is intended for software debugging or first MCU programming during ECU assembly. To enter Debug mode without first entering OTP mode, the voltage at the DEBUG pin must be set to V_{DBG} prior to applying the VSUP voltage. During the power-up sequence, the fail-safe state machine will start in Debug mode and reach the INIT_FS state.

In Debug mode, the watchdog window is infinite opened, the RSTB 8s counter is disabled, FS0B is maintained low and cannot be released. The deep fail safe is deactivated. The Debug mode status is reported by the DBG_MODE bit in FS_STATES (latched information) or by VDBG_VOLT_S in M_STATUS (real time information). To exit Debug mode, write to the EXIT_DBG_MODE bit in the FS_STATES register.

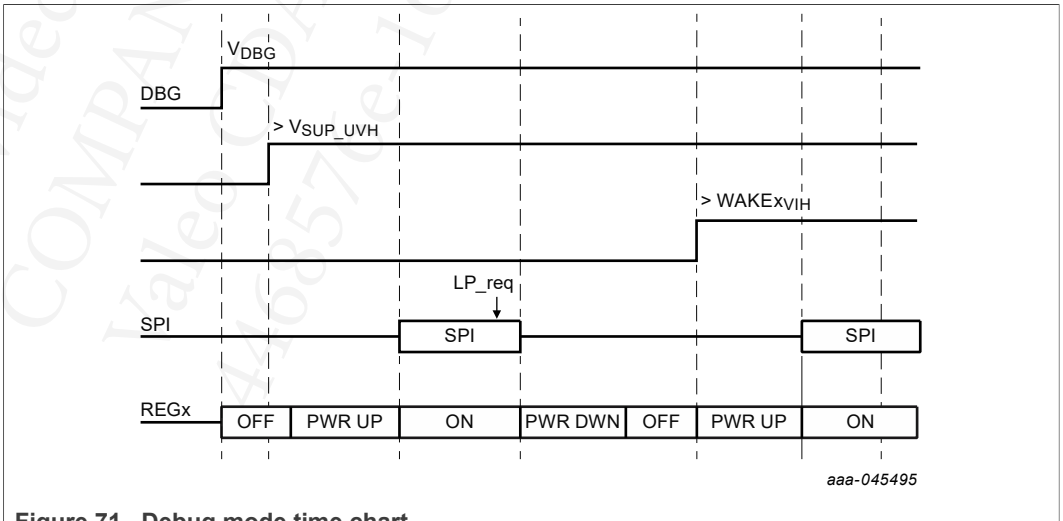


Figure 71. Debug mode time chart

Table 214. Electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP_UVH} < VSUP pin voltage < 36 V, V_{PRE} + V_{PRE_HDR} < VSUP_PWR pin voltage < 36 V, unless otherwise specified. All voltages are referenced to ground.

Symbol	Description	Min	Typ	Max	Unit
Electrical characteristics					
V_{NORM}	Voltage to apply at DEBUG pin to exit OTP mode and to start in Normal mode	0	—	1.8	V
V_{OTP}	Voltage to apply at DEBUG pin to enter OTP mode (State machines stopped for OTP emulation/programming)	7.4	—	8.4	V
V_{DBG}	Voltage to apply at DEBUG pin to enter Debug mode (Automatic start in Debug mode with watchdog disabled)	2.5	—	6	V
t_{OTP_DBG}	DEBUG pin filtering time to enter OTP mode or Debug mode	4	6	8	µs

23.1 OTP mode flowchart

The diagram in Figure 72 explains the steps to enter OTP mode, emulate or program an OTP configuration, start the Fail-safe machine in Debug mode, exit Debug mode with the watchdog disabled, and release the safety outputs.

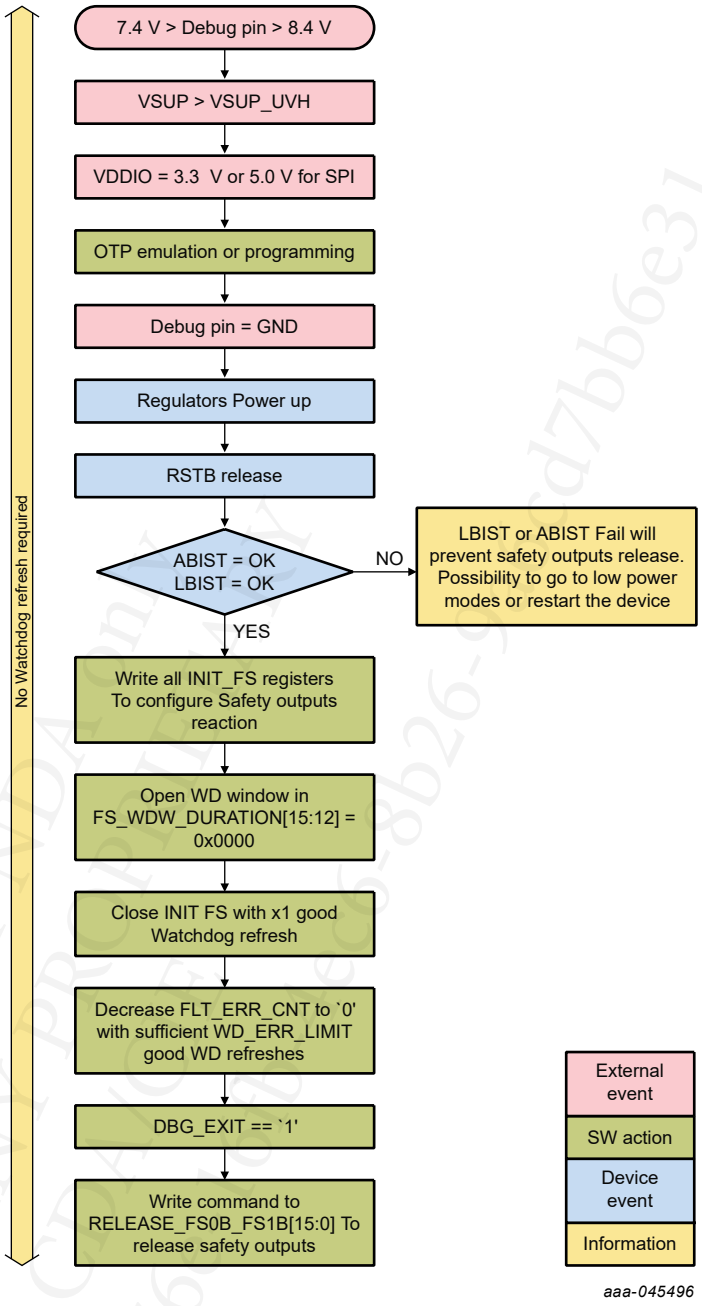


Figure 72. OTP mode flowchart until safety outputs release

23.2 Debug mode flowchart

The diagram in Figure 73 explains the steps to enter Debug mode without first entering OTP mode, start the fail-safe machine in Debug mode, exit Debug mode with the watchdog disabled, and release the safety outputs.

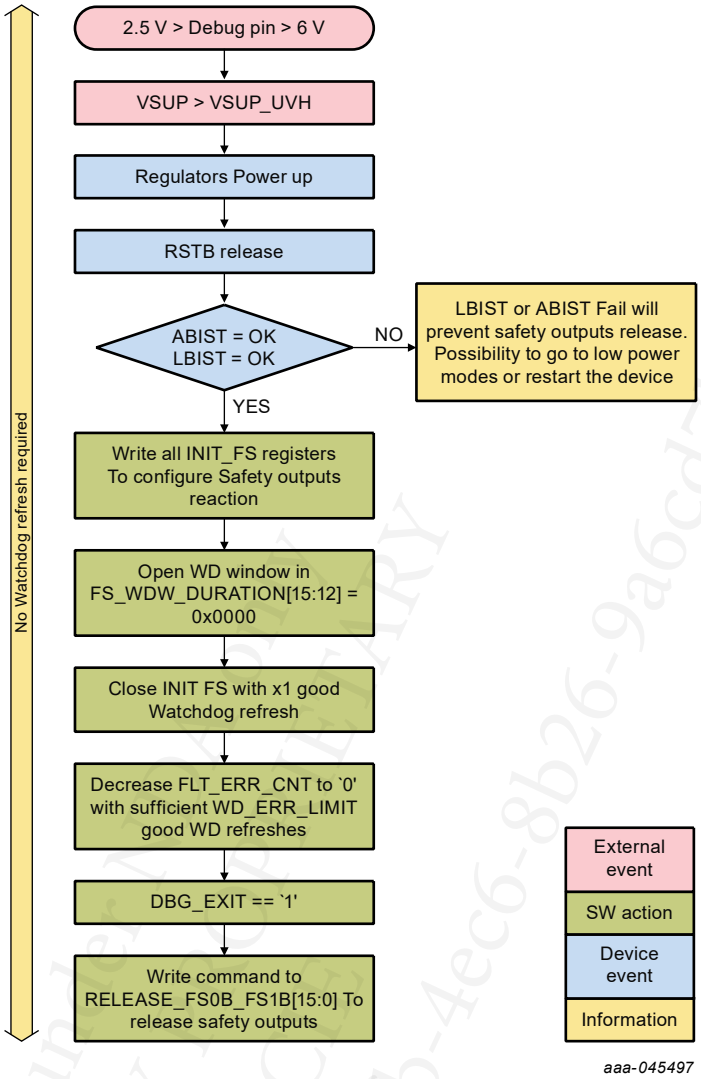


Figure 73. Debug mode flowchart till safety outputs release

24 Application schematics

Refer to AN12995 for further information.

24.1 Front-end configuration

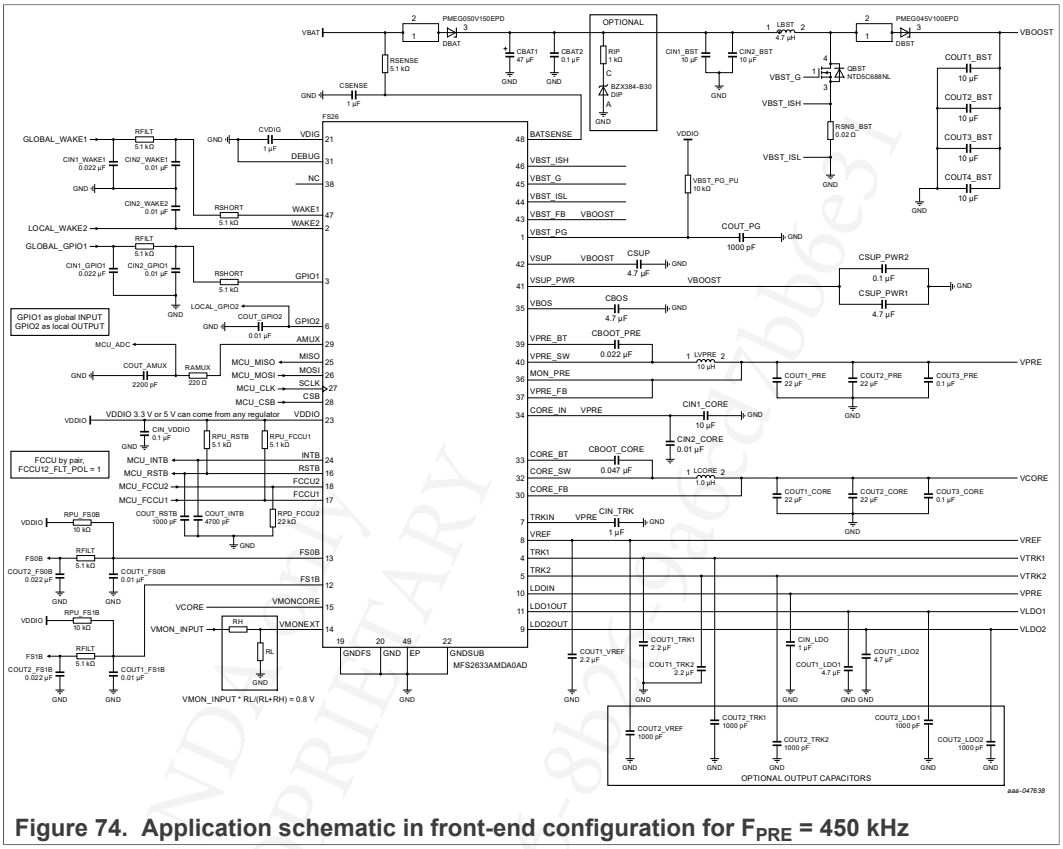


Figure 74. Application schematic in front-end configuration for F_{PRE} = 450 kHz

24.2 Back-end configuration

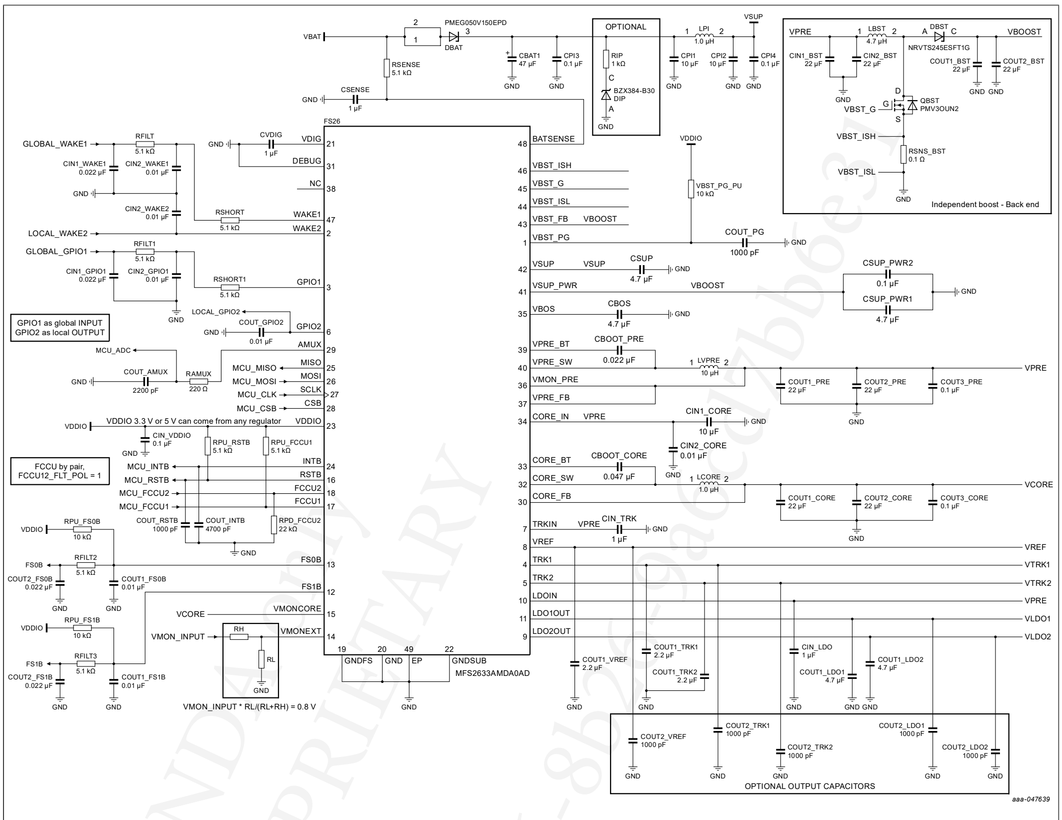

VBAT
PMEG050V150EPD
DBAT
RSENSE
5.1 kΩ
CSENSE
1 µF
CBAT1
47 µF
CPI3
0.1 µF
OPTIONAL
RIP
1 kΩ
BZX384-B30
DIP
LPI
1.0 µH
CPI1
10 µF
CPI2
10 µF
CPI4
0.1 µF
VSUP
VPRE
LBST
4.7 µH
DBST
NRVTS245ESFT1G
VBOOST
CIN1_BST
22 µF
CIN2_BST
22 µF
COUT1_BST
22 µF
COUT2_BST
22 µF
QBST
PMV30UN2
VBST_G
VBST_ISH
RSNS_BST
0.1 Ω
VBST_ISL
Independent boost - Back end
FS26
GLOBAL_WAKE1
RFILT
5.1 kΩ
CIN1_WAKE1
0.022 µF
CIN2_WAKE1
0.01 µF
CIN2_WAKE2
0.01 µF
RSHORT
5.1 kΩ
LOCAL_WAKE2
GLOBAL_GPIO1
RFILT1
5.1 kΩ
CIN1_GPIO1
0.022 µF
CIN2_GPIO1
0.01 µF
RSHORT1
5.1 kΩ
LOCAL_GPIO2
COUT_GPIO2
0.01 µF
GPIO1 as global INPUT
GPIO2 as local OUTPUT
MCU_ADC
COUT_AMUX
2200 pF
RAMUX
220 Ω
MCU_MISO
MCU_MOSI
MCU_CLK
MCU_CSB
VDDIO
VDDIO 3.3 V or 5 V can come from any regulator
CIN_VDDIO
0.1 µF
RPU_RSTB
5.1 kΩ
RPU_FCCU1
5.1 kΩ
FCCU by pair,
FCCU12_FLT_POL = 1
MCU_INTB
MCU_RSTB
MCU_FCCU2
MCU_FCCU1
COUT_RSTB
1000 pF
COUT_INTB
4700 pF
RPD_FCCU2
22 kΩ
RPU_FS0B
10 kΩ
FS0B
RFILT2
5.1 kΩ
COUT2_FS0B
0.022 µF
COUT1_FS0B
0.01 µF
RPU_FS1B
10 kΩ
FS1B
RFILT3
5.1 kΩ
COUT2_FS1B
0.022 µF
COUT1_FS1B
0.01 µF
VCORE
VMON_INPUT
RH
RL
VMON_INPUT * RL/(RL+RH) = 0.8 V
CVDIG
1 µF
VDIG
DEBUG
NC
WAKE1
WAKE2
GPIO1
GPIO2
AMUX
MISO
MOSI
SCLK
CSB
INTB
RSTB
FCCU2
FCCU1
FS0B
FS1B
VMONCORE
VMONEXT
GNDFS
GND
EP
GNDSUB
MFS2633AMDA0AD
BATSENSE
VBST_ISH
VBST_G
VBST_ISL
VBST_FB
VBST_PG
VBST_PG_PU
10 kΩ
COUT_PG
1000 pF
VSUP_PWR
CSUP
4.7 µF
CSUP_PWR2
0.1 µF
CSUP_PWR1
4.7 µF
VBOS
CBOS
4.7 µF
VPRE_BT
CBOOT_PRE
0.022 µF
VPRE_SW
LVPRE
10 µH
VMON_PRE
VPRE_FB
COUT1_PRE
22 µF
COUT2_PRE
22 µF
COUT3_PRE
0.1 µF
CORE_IN
CIN1_CORE
10 µF
CIN2_CORE
0.01 µF
CORE_BT
CBOOT_CORE
0.047 µF
CORE_SW
LCORE
1.0 µH
CORE_FB
COUT1_CORE
22 µF
COUT2_CORE
22 µF
COUT3_CORE
0.1 µF
TRKIN
CIN_TRK
1 µF
VREF
TRK1
TRK2
LDOIN
LDO1OUT
LDO2OUT
VTRK1
VTRK2
VLDO1
VLDO2
COUT1_VREF
2.2 µF
COUT1_TRK1
2.2 µF
COUT1_TRK2
2.2 µF
CIN_LDO
1 µF
COUT1_LDO1
4.7 µF
COUT1_LDO2
4.7 µF
COUT2_VREF
1000 pF
COUT2_TRK1
1000 pF
COUT2_TRK2
1000 pF
COUT2_LDO1
1000 pF
COUT2_LDO2
1000 pF
OPTIONAL OUTPUT CAPACITORS
GND
aaa-047639

Figure 75. Application schematic in back-end configuration for F_{PRE} = 450 kHz

25 OTP configurations

Table 215. OTP configurations

	Configurations	MFS2613 AMDA2AD	MFS2613 AMDA3AD	MFS2613 AMDA4AD	MFS2613 AMDA6AD	MFS2621 AMDABAD	MFS2613 AMDDCAD
System configuration	VSUP UV Threshold	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V	4.8 V / 4.3 V
	Exit DFS On WAKE1 Event	DFS Exit on Wake1 Event Enabled	DFS Exit on Wake1 Event Enabled	DFS Exit on Wake1 Event Enabled	DFS Exit on Wake1 Event Enabled	DFS Exit on Wake1 Event Enabled	DFS Exit on Wake1 Event Enabled
	Auto-retry Power Up From DFS	Auto-retry Enabled	Auto-retry Enabled	Auto-retry Enabled	Auto-retry Enabled	Auto-retry Enabled	Auto-retry Enabled
	Auto-retry Mode	Infinite retry	Infinite retry	Limited retry	Limited retry	Infinite retry	Limited retry
	Auto-retry Timer Limit	800 ms	800 ms	800 ms	800 ms	1600 ms	800 ms
	Clock Frequency Selection	18 MHz	18 MHz	18 MHz	18 MHz	18 MHz	18 MHz
	VBOS Input Selection	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}	Auto Transition on V_{PRE_UVH}
Power-up sequence	Power-up Slot Time	250 us	250 us	250 us	250 us	1000 us	250 us
	Power-up Slot Bypass	Bypass Disabled	Bypass Disabled	Bypass Disabled	Bypass Disabled	Bypass Disabled	Bypass Disabled
	VCORE Power-up Slot	Slot 0	Slot 0	Slot 0	Slot 0	Slot 6	Slot 0
	LDO1 Power-up Slot	Slot 0	Slot 0	Slot 0	Slot 0	Slot 0	Slot 0
	LDO2 Power-up Slot	Slot 0	Slot 1	Slot 0	Slot 0	Slot 0	Slot 0
	TRK1 Power-up Slot	Slot 2	Slot 2	Slot 2	Slot 0	Slot 0	Slot 2
	TRK2 Power-up Slot	Slot 3	Slot 3	Slot 3	Slot 0	OFF	Slot 3
	VREF Power-up Slot	Slot 1	Slot 0	Slot 1	Slot 0	Slot 0	Slot 1
	GPIO1 Power-up Slot	OFF	Slot 4	OFF	OFF	Slot 1	OFF
	GPIO2 Power-up Slot	OFF	Slot 4	OFF	OFF	Slot 1	OFF
I/O configuration	GPIO Configuration	GPIO configured as an Input	Push-pull driver	GPIO configured as an Input	GPIO configured as an Input	Low Side Driver	GPIO configured as an Input
	GPIO Low Side Polarity	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high
	GPIO1 Pullup	Pullup Disabled	Pullup Disabled	Pullup Disabled	Pullup Disabled	Pullup Disabled	Pullup Disabled

Table 215. OTP configurations*...continued*

	GPIO1 Pulldown	Pulldown Enabled	Pulldown Disabled	Pulldown Disabled	Pulldown Enabled	Pulldown Enabled	Pulldown Disabled
	GPIO1 Detection Threshold	Low voltage threshold	Low voltage threshold	Low voltage threshold	Low voltage threshold	High voltage threshold	Low voltage threshold
	GPIO1 TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD
	GPIO Configuration	Low Side Driver	Push-pull driver	GPIO configured as an Input	GPIO configured as an Input	Low Side Driver	GPIO configured as an Input
	GPIO Low Side Polarity	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high	GPIO LS active high
	GPIO2 VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD	GPIO is not driven by VCORE PGOOD
	GPIO2 Pullup	Pullup Disabled	Pullup Disabled	Pullup Disabled	Pullup Disabled	Pullup Disabled	Pullup Disabled
	GPIO2 Pulldown	Pulldown Disabled	Pulldown Disabled	Pulldown Disabled	Pulldown Enabled	Pulldown Enabled	Pulldown Disabled
	GPIO2 Detection Threshold	Low voltage threshold	Low voltage threshold	Low voltage threshold	Low voltage threshold	High voltage threshold	Low voltage threshold
	WAKE1 Detection Threshold	High voltage threshold	Low voltage threshold	High voltage threshold	Low voltage threshold	High voltage threshold	High voltage threshold
	WAKE2 Detection Threshold	High voltage threshold	High voltage threshold	High voltage threshold	Low voltage threshold	High voltage threshold	High voltage threshold
	WAKE1 Pulldown	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled
	WAKE2 Pulldown	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled	Pulldown Enabled
	WAKE1 Pulldown Selection	200 kΩ	200 kΩ	200 kΩ	10 kΩ	200 kΩ	200 kΩ
	WAKE2 Pulldown Selection	200 kΩ	200 kΩ	200 kΩ	200 kΩ	200 kΩ	200 kΩ
VPRE configuration	VPRE In Normal Mode	6.00 V	5.40 V	6.00 V	6.00 V	6.00 V	6.00 V
	VPRE In Standby mode	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V
	DVS Ramp Rate	22 mV/us	22 mV/us	22 mV/us	22 mV/us	22 mV/us	22 mV/us
	VPRE Over Current Flag	2.2 A	1.54 A	2.2 A	1.54 A	2.2 A	2.2 A
	Over Current Deglitch	2000 us	250 us	2000 us	250 us	2000 us	2000 us
	Soft-start Ramp	2150 us	538 us	2150 us	269 us	2150 us	2150 us

Table 215. OTP configurations*...continued*

	VPRE Power Down Delay	100 us	100 us	100 us	100 us	100 us	100 us
	VPRE Transition Voltage	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V	5.35 V
	VPRE Phase Delay	No delay	No delay	No delay	No delay	No delay	No delay
	VPRE LX Slew Rate	Fast mode	Fast mode	Slow mode	Fast mode	Fast mode	Slow mode
	Transconductance Amp	15 µS	15 µS	15 µS	15 µS	15 µS	15 µS
	Comp Capacitance	12.0 pF	23.0 pF	12.0 pF	12.0 pF	12.0 pF	12.0 pF
	Comp Resistance	1300 kΩ	1137 kΩ	1300 kΩ	1300 kΩ	1300 kΩ	1300 kΩ
	Slope Compensation	266 mV/us	266 mV/us	266 mV/us	266 mV/us	266 mV/us	266 mV/us
	Minimum On Time In PFM	1125 ns	1125 ns	1125 ns	1125 ns	1125 ns	1125 ns
	Minimum Off Time In PFM	720 ns	720 ns	720 ns	720 ns	720 ns	720 ns
	VPRE Clock Selection	FSW/40	FSW/40	FSW/40	FSW/40	FSW/40	FSW/40
	TSD Behavior	Go to DFS	VPRE disabled only	Go to DFS	VPRE disabled only	Go to DFS	Go to DFS
	TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD
VBST configuration	VBST Voltage	8.00 V	7.00 V	8.00 V	8.00 V	8.00 V	8.00 V
	VBST Configuration	Front-end boost	Front-end boost	Front-end boost	Front-end boost	Front-end boost	Front-end boost
	VBSTFB OV Monitor Mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode	Auto-enable mode
	Phase Delay	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle	1 Clock Cycle
	Low-side Slew Rate	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 2 Ω / PD = 1.7 Ω	PU = 1.5 Ω / PD = 1.0 Ω	PU = 1.5 Ω / PD = 1.0 Ω
	Minimum TON	200 ns	200 ns	200 ns	200 ns	200 ns	200 ns
	VBST Soft Start	425 us	850 us	425 us	425 us	425 us	425 us
	Max Duty-cycle	87.50 %	87.50 %	87.50 %	87.50 %	87.50 %	87.50 %
	Comp Capacitance	200 pF	200 pF	200 pF	200 pF	200 pF	200 pF
	Comp Transconductance	3.9 µS	5.1 µS	3.9 µS	3.9 µS	3.9 µS	3.9 µS
	Comp Resistance	740 kΩ	500 kΩ	500 kΩ	740 kΩ	740 kΩ	500 kΩ
	Current Limit	180 mV/RSNS	120 mV/RSNS	150 mV/RSNS	120 mV/RSNS	180 mV/RSNS	150 mV/RSNS

Table 215. OTP configurations*...continued*

	Slope Compensation	155 mV/us	127 mV/us	169 mV/us	155 mV/us	155 mV/us	169 mV/us
VCORE configuration	VCORE Voltage	1.50 V	1.50 V	1.50 V	1.50 V	1.25 V	1.50 V
	Control Type	Valley mode control	Valley mode control	Valley mode control	Valley mode control	Valley mode control	Valley mode control
	Operating mode	CCM only	CCM only	CCM only	CCM only	CCM only	CCM only
	Soft Start	5 mV/us	10 mV/us	10 mV/us	5 mV/us	5 mV/us	20 mV/us
	VCORE Current Limit	2.7 A	2.7 A	1.7 A	1.7 A	2.7 A	1.7 A
	Phase Delay	2 Clock Cycles	3 Clock Cycles	2 Clock Cycles	2 Clock Cycles	2 Clock Cycles	2 Clock Cycles
	High-side Slew Rate	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.0 V/ns Fall = 0.6 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns	Rise = 4.5 V/ns Fall = 1.2 V/ns
	Transconductance Amp	53 µS	53 µS	26 µS	26 µS	53 µS	26 µS
	Comp Capacitance	50 pF	50 pF	50 pF	50 pF	50 pF	50 pF
	Comp Resistance	200 kΩ	150 kΩ	200 kΩ	200 kΩ	150 kΩ	200 kΩ
	VCORE Inductor	1 µH	1 µH	1 µH	1 µH	1 µH	1 µH
	TSD Behavior	Go to DFS	Go to DFS	Go to DFS	Go to DFS	Go to DFS	Go to DFS
	TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD
LDO1 config	LDO1 Voltage In Normal	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	LDO1 Voltage In Standby	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	LDO1 In Standby mode	LDO1 Enabled	LDO1 Disabled	LDO1 Enabled	LDO1 Enabled	LDO1 Enabled	LDO1 Enabled
	TSD Behavior	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only	LDO1 disabled only
	TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD
LDO2 config	LDO2 Voltage In Normal	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	LDO2 Voltage In Standby	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	LDO2 In Standby mode	LDO2 Enabled	LDO2 Enabled	LDO2 Enabled	LDO2 Enabled	LDO2 Enabled	LDO2 Enabled
	TSD Behavior	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only	LDO2 disabled only
	TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD

Table 215. OTP configurations*...continued*

VREF	VREF Voltage	5.0 V	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V
	Internal LDO Reference	1.2 V	3.3 V	5.0 V	3.3 V	1.2 V	3.3 V
TRK1	TRK1 Input Selection	VREF	LDO2	Internal LDO_REF	VREF	VREF	Internal LDO_REF
	TSD Behavior	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only	TRK1 disabled only
	TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD
TRK2	TRK2 Input Selection	LDO2	LDO2	Internal LDO_REF	LDO2	VREF	Internal LDO_REF
	TSD Behavior	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only	TRK2 disabled only
	TSD Pulldown	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD	Pulldown enabled in TSD
VMONPRE	VPRE Monitoring Voltage	6.00 V	5.40 V	6.00 V	6.00 V	6.00 V	6.00 V
	VPRE OV Threshold	110.5 %	110.5 %	110 %	110 %	110 %	110 %
	VPRE UV Threshold	90 %	94 %	90 %	90 %	90 %	90 %
	VMONPRE OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONPRE UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
VMONLDO1	LDO1 Monitoring Voltage	5.0 V	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V
	LDO1 OV Threshold	106.00 %	108.00 %	107.50 %	107.50 %	106.00 %	107.50 %
	LDO1 UV Threshold	94.00 %	91.00 %	92.50 %	93.00 %	94.00 %	92.50 %
	LDO1 Degraded UV Monitoring	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV
	VMONLDO1 OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONLDO1 UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
	LDO1 Pin Lift Detection	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled	LDO1 pin lift detection enabled
VMONTRK1	TRK1 Monitoring Voltage	5.0 V	5.0 V	5.0 V	5.0 V	3.3 V	3.3 V
	TRK1 OV Threshold	104.5 %	108.00 %	106 %	107.50 %	106.00 %	106 %
	TRK1 UV Threshold	95.5 %	92.00 %	94 %	93.00 %	94 %	94 %
	VMONTRK1 OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us

Table 215. OTP configurations*...continued*

	VMONTRK1 UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
VMONCORE	VCORE Monitoring Voltage	1.50 V	1.50 V	1.50 V	1.50 V	1.25 V	1.50 V
	CORE OV Threshold	104.5 %	108.00 %	106 %	106 %	106 %	106 %
	CORE UV Threshold	95.5 %	95.5 %	94.00 %	94.00 %	94.00%	94.00 %
	VMONCORE OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONCORE UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
VMONLDO2	LDO2 Monitoring Voltage	3.3 V	5.0 V	3.3 V	3.3 V	3.3 V	3.3 V
	LDO2 OV Threshold	106.00 %	104.5 %	106.00 %	106.00 %	106.00 %	106.00 %
	LDO2 UV Threshold	94.00 %	95.5 %	94.00 %	94.00 %	94.00 %	94.00 %
	LDO2 Degraded UV Monitoring	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV	Normal UV
	VMONLDO2 OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONLDO2 UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
	LDO2 Pin Lift Detection	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled	LDO2 pin lift detection enabled
VMONTRK2	TRK2 Monitoring Voltage	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V	3.3 V
	TRK2 OV Threshold	104.5 %	108.00 %	106 %	106 %	104.50 %	106 %
	TRK2 UV Threshold	95.5 %	92.00 %	94.00 %	94.00 %	95.50 %	94.00 %
	VMONTRK2 OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONTRK2 UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
VMONEXT	External VMON OV Threshold	104.50 %	110.00 %	110.00 %	105.00 %	105.00 %	110.00 %
	External VMON UV Threshold	95.50 %	95.00 %	90 %	95.00 %	95.00 %	90 %
	VMONEXT OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONEXT UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
VMONREF	VREF Monitoring Voltage	5.0 V	3.3 V	5.0 V	5.0 V	3.3 V	3.3 V
	VREF OV Threshold	104.50 %	105.00 %	104.50 %	105.00 %	105.00 %	104.50 %
	VREF UV Threshold	95.50 %	95.00 %	95.50 %	95.00 %	95.00 %	95.50 %

Table 215. OTP configurations*...continued*

	VMONREF OV Deglitch	45 us	45 us	45 us	45 us	45 us	45 us
	VMONREF UV Deglitch	40 us	40 us	40 us	25 us	40 us	40 us
	VREF Pin Lift Detection	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled	VREF pin lift detection enabled
ABIST	ABIST1 On VMONPRE	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled
	ABIST1 On VMONCORE	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled
	ABIST1 On VMONLDO1	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled
	ABIST1 On VMONLDO2	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled
	ABIST1 On VMONTRK1	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled
	ABIST1 On VMONTRK2	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Disabled	ABIST1 Enabled
	ABIST1 On VMONREF	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled
	ABIST1 On VMONEXT	ABIST1 Disabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Enabled	ABIST1 Disabled	ABIST1 Enabled
System Safety Configuration	DFS Entry Mode	Go to DFS when FLT_ERR_ CNT = max	Go to DFS when FLT_ERR_ CNT = max	Go to DFS when FLT_ERR_ CNT = max	Go to DFS when FLT_ERR_ CNT = max	Go to DFS when FLT_ERR_ CNT = max	Go to DFS when FLT_ERR_ CNT = max
	FS1B Assertion Mode	Delayed Assertion Disabled	Delayed Assertion Enabled	Delayed Assertion Enabled	Delayed Assertion Enabled	Delayed Assertion Disabled	Delayed Assertion Enabled
	RSTB Delay From FS0B	0 us	100 us	0 us	100 us	0 us	0 us
	RSTB Low Detection Timer	Timer Disabled	8 Second Timer Enabled	8 Second Timer Enabled	8 Second Timer Enabled	8 Second Timer Enabled	8 Second Timer Enabled
	Watchdog Timer	WD Timer Enable	WD Timer Enable	WD Timer Enable	WD Timer Enable	WD Timer Enable	WD Timer Enable
	Bypass LBIST From Standby	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST	Always perform LBIST
	Main DFS Availability	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available
	Deep Fail-safe State Availability	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available	Deep Fail-safe Available
OTP ID	Program ID High	A	A	A	A	A	D
	Program ID Low	2	3	4	6	B	C
FS Versioning Bits	External Monitor	VMON Disabled	VMON Enabled	VMON Enabled	VMON Enabled	VMON Enabled	VMON Enabled

Table 215. OTP configurations*...continued*

	FCCU Function	FCCU available	FCCU available	FCCU available	FCCU available	FCCU available	FCCU available
	ERRMON Function	ERRMON not available	ERRMON available	ERRMON not available	ERRMON available	ERRMON not available	ERRMON not available

26 Packaging

26.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number.

Table 216. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

26.2 Package outline

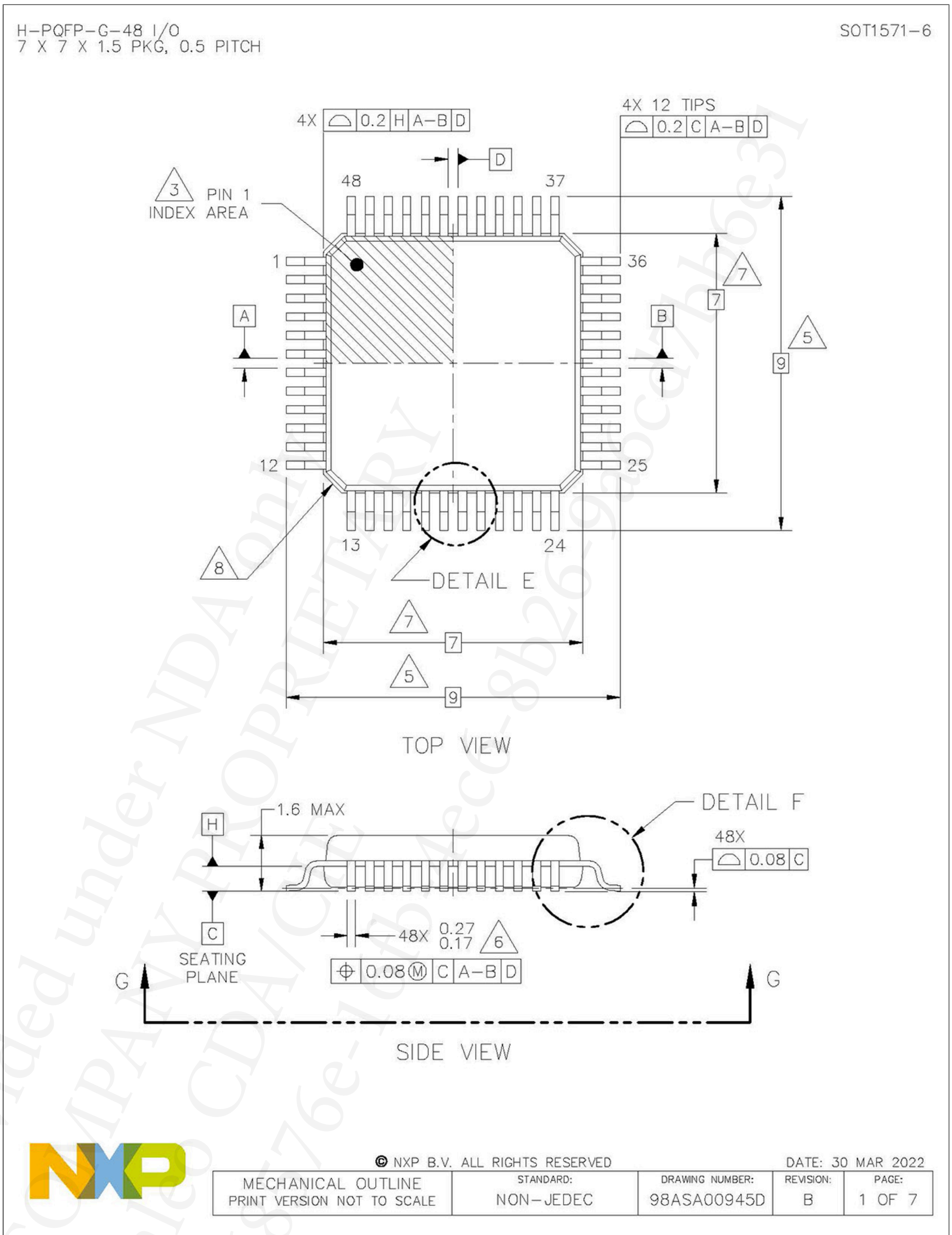


Figure 76. SOT1571-6

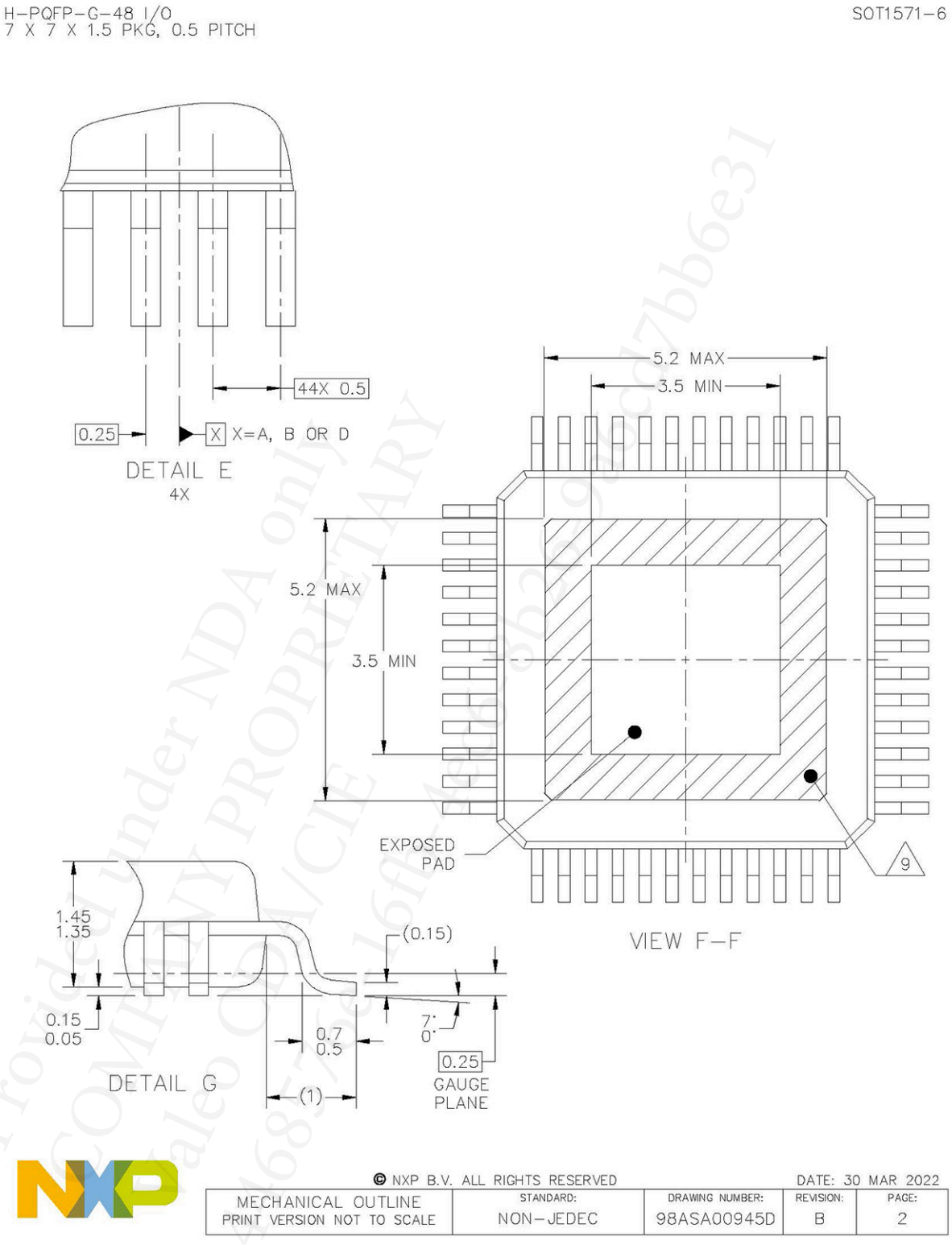


Figure 77. Package outline details (SOT1571-6)

H-PQFP-G-48 I/O
7 X 7 X 1.5 PKG, 0.5 PITCH

SOT1571-6

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
7. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.
10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

DATE: 30 MAR 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA00945D	REVISION: B	PAGE: 6

Figure 78. Package outline notes (SOT1571-6)

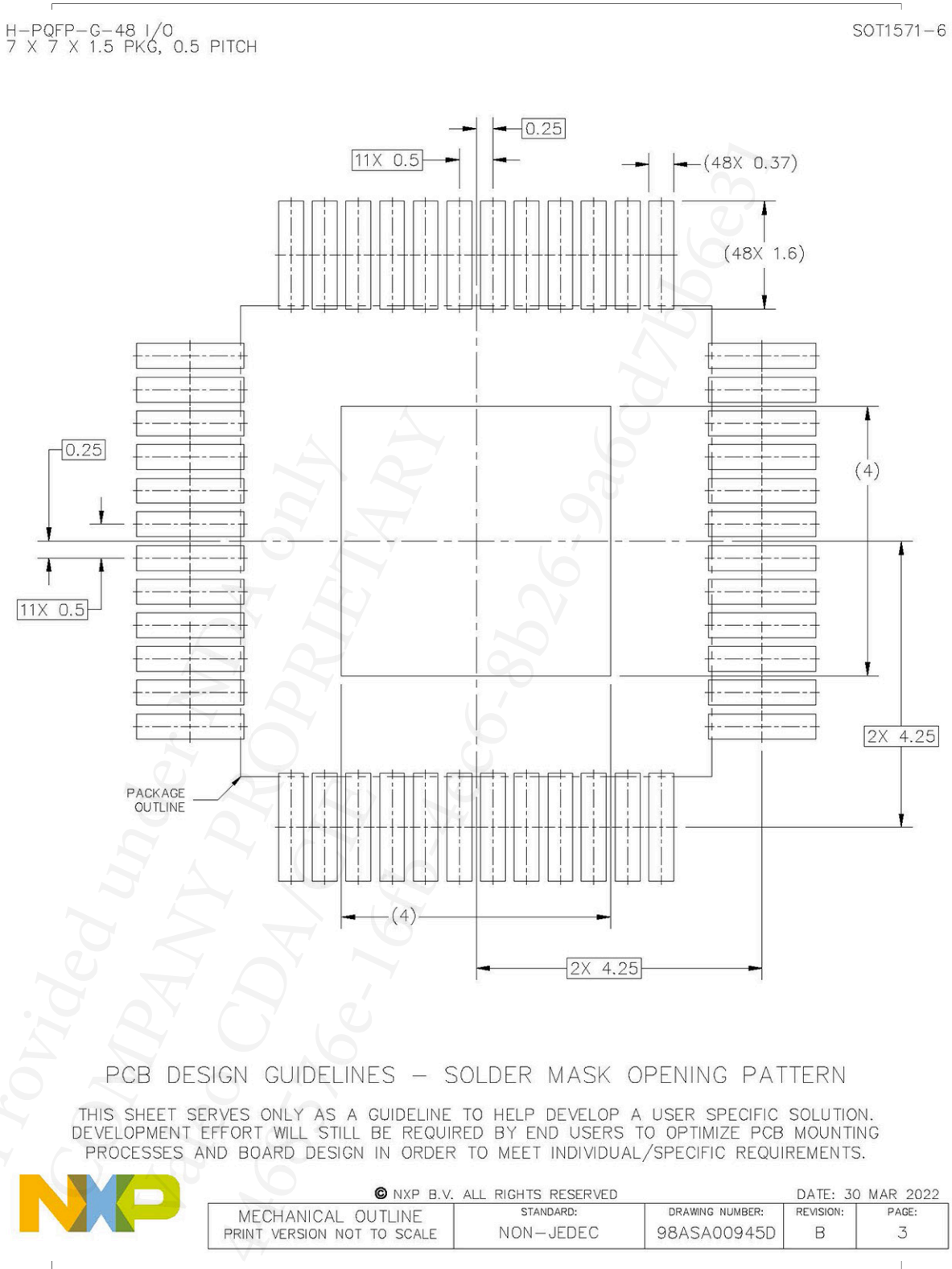
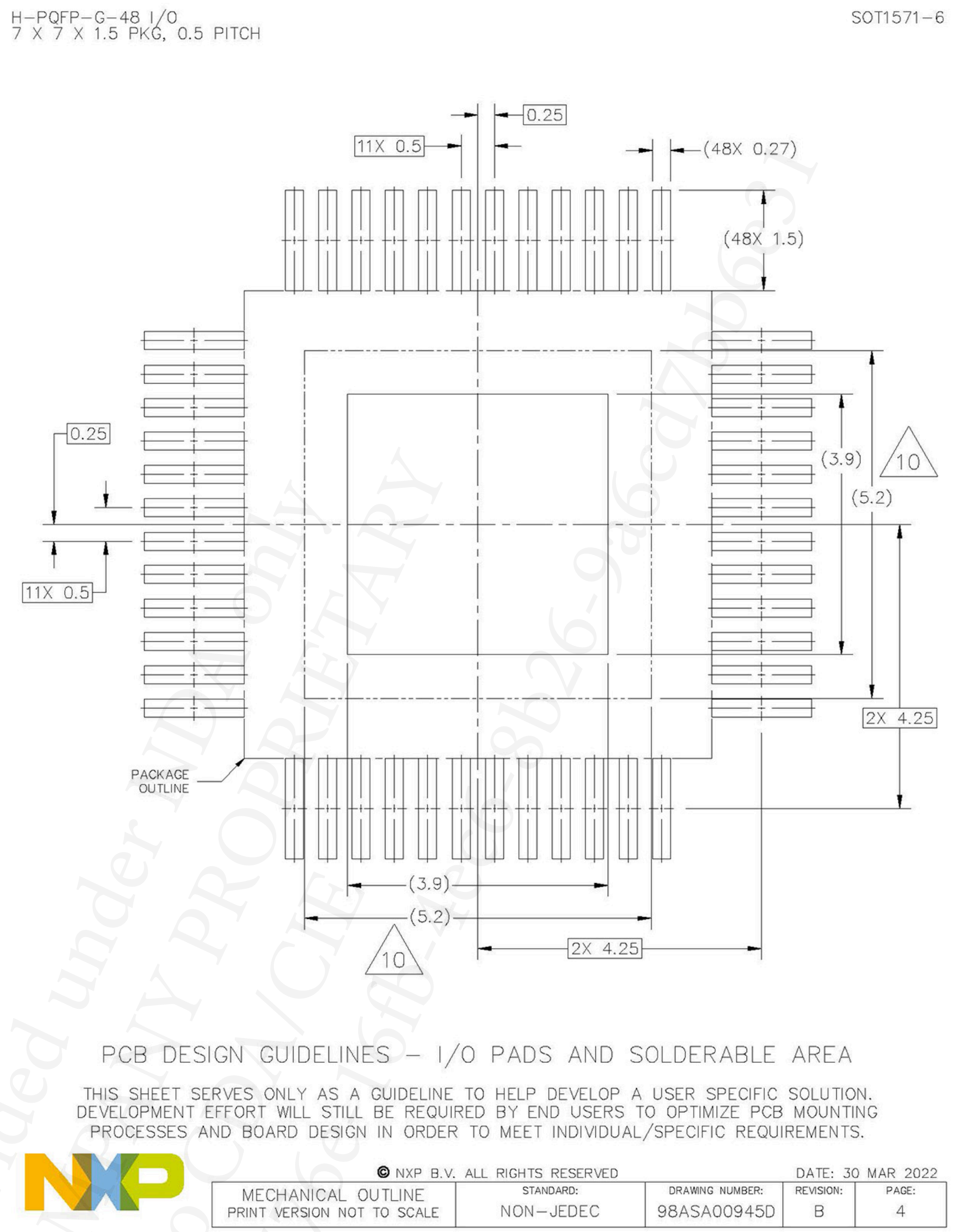


Figure 79. PCB design guidelines - solder mask opening pattern (SOT1571-6)


H-PQFP-G-48 I/O
7 X 7 X 1.5 PKG, 0.5 PITCH
SOT1571-6
0.25
11X 0.5
(48X 0.27)
(48X 1.5)
0.25
11X 0.5
(3.9)
10
(5.2)
2X 4.25
PACKAGE
OUTLINE
(3.9)
(5.2)
10
2X 4.25
PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.
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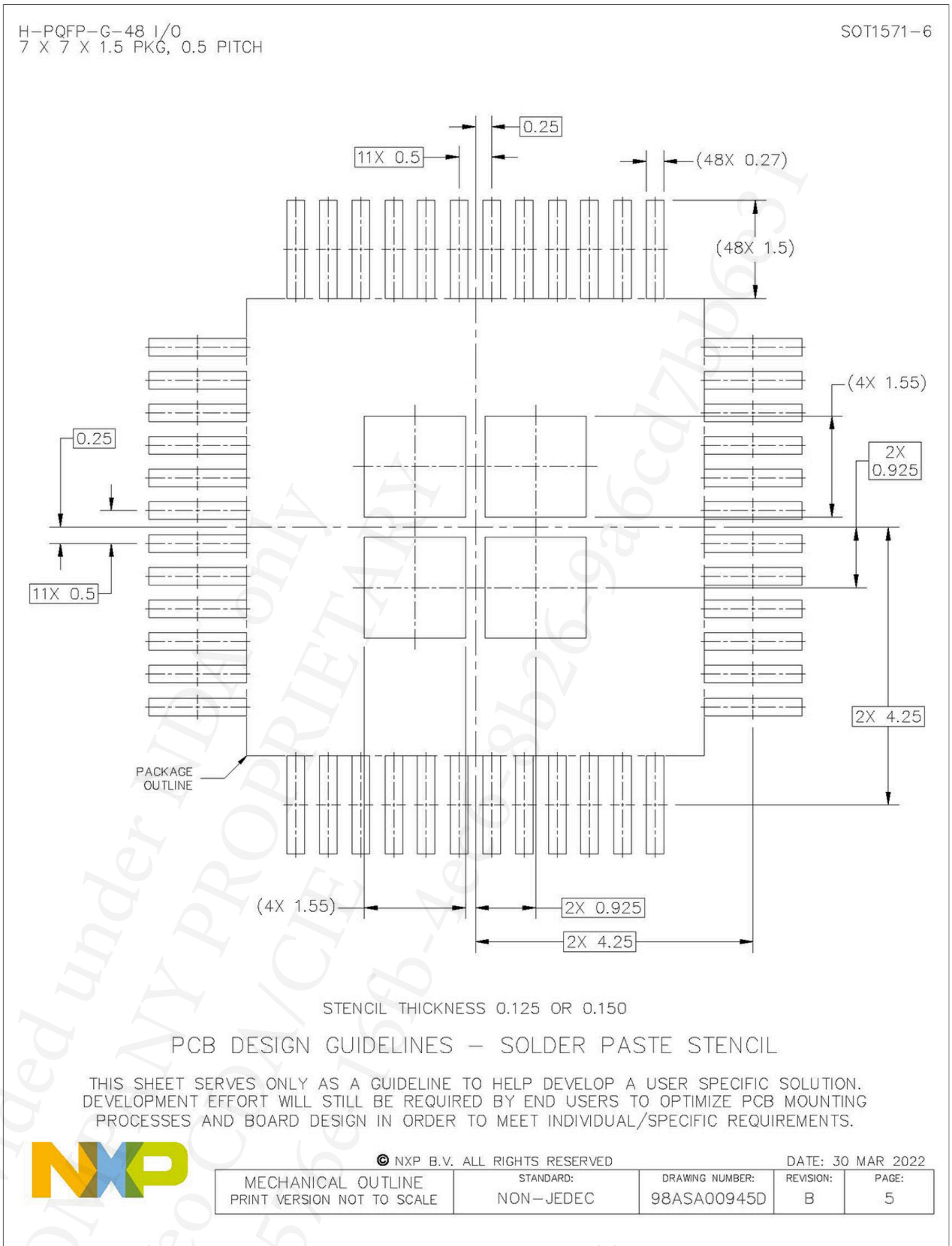
STANDARD:
NON-JEDEC
DRAWING NUMBER:
98ASA00945D
REVISION:
B
PAGE:
4

Figure 80. PCB design guidelines - I/O pads and solderable area (SOT1571-6)


H-PQFP-G-48 I/O
7 X 7 X 1.5 PKG, 0.5 PITCH
SOT1571-6
0.25
11X 0.5
(48X 0.27)
(48X 1.5)
(4X 1.55)
2X 0.925
2X 4.25
PACKAGE OUTLINE
STENCIL THICKNESS 0.125 OR 0.150
PCB DESIGN GUIDELINES — SOLDER PASTE STENCIL
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.
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DATE: 30 MAR 2022
MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE
STANDARD: NON-JEDEC
DRAWING NUMBER: 98ASA00945D
REVISION: B
PAGE: 5

Figure 81. PCB design guidelines - solder paste stencil (SOT1571-6)

27 References

Table 217. References

Documents, Tools, Enablement	URL
FS26 Functional Safety Manual	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Dynamic FMEDA	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
AN12995 - FS26 Product Guidelines	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26_SMPS_Calculator.xls	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 SMPS Simplis models	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Graphical User Interface • To calculate the power dissipation • To create an OTP configuration • To interface an EVB KIT with a computer	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Product Overview	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
KITFS26AEEVM: FS26 Evaluation Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-evaluation-board:KITFS26AEEVM
KITFS26SKTEVM: FS26 Socket Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-programming-socket-board:KITFS26SKTEVM

28 Revision history

Table 218. Revision history

Rev	Date	Description
1	20220329	Initial release.
2	20220414	Update Mechanical Outline data to 98ASA00945D rev. B. Correct figure titles in Section 26.2.
2.1	20220517	• For Table 1, change title from *Orderable parts example* to *Device segmentation* • Correct content of Table 2 • Correct the package outline drawing number in Table 216 • Correct Figure 20 • Add footnotes to Table 122 and change four instances of *VCORE_SS_OTP* to *CORE_SS_OTP* • Correct descriptions in Table 20 • Change approximately 140 bit names from IO* to GPIO*, including instances in Figure 39, Figure 40, Figure 41, Figure 42, Figure 43, and Figure 44 • In Table 130, add tolerance of +/- 0.5 % for AMUX[4:0] = 00001, 0010, and 00011 • In Table 130, add tolerance of +/- 50 mV for AMUX[4:0] = 00100, 00101, and 00110 • In Section 21.3.2, add information about thermal shutdown protection • Correct title of Table 188 by adding *error* • Correct table title from *Error flag for external IC monitoring* to *Acknowledge error detection from MCU* for Table 190 • Add *Quick reference data* disclaimer to *Legal information* section.

Table 218. Revision history*...continued*

Rev	Date	Description
2.2	20221004	• Global corrections to grammar and style throughout • Corrected footnotes throughout • In Section 2, updated VCORE entry under Power Supplies to read: VCORE: synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V. • In Table 1, changed values in column labeled "Core Current Capability" from 1.6 to 1.65 • In Table 3, updated information in "RSTB" row. • In Section 12, updated text. • Corrected Section 14: I_{Q_STBY} Typ values changes from 25, 27 30 to 28, 31, 34 respectively • Corrected Figure 10, Figure 11 and text of Section 14.1, added footnotes • Section 14.2: Corrected Figure 12 • Section 19.4: Removed first three values under 0x12, CFG_OVUV_4_OTP, VMON_PRE_UVTH_OTP[3:0], VPRE UV threshold • Corrected Table 115 • In Table 111: Removed first entry for Hexidecimal Value and Settings, under 0x2A, OTP_VPRE_CFG4, VPRE_PFM_TON_OTP[1:0], VPRE highside minimum on time in PFM (450 kHz / 2.25 MHz) • Corrected Table 114, Table 116, Table 120, Table 122, Table 124, Table 126, Table 131, Table 135 • In Table 116, changed description of $\eta_{PEAK\_VPRE\_PWM}$ from L_{VPRE} = 10 µH with DCR = 60 mΩ to L_{VPRE} = 10 µH with RDCR_LVPRE = 60 mΩ; changed description of $\eta_{PEAK\_VPRE\_PFM}$ from C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{VPRE} = 10 µH with DCR = 60 mΩ, F_{PRE} = 450 kHz to C_{OUT_PRE} = 22 µF with ESR = 2 mΩ, L_{VPRE} = 10 µH with RDCR_LVPRE = 60 mΩ, F_{PRE} = 450 kHz; corrected Typ and Max values for TSD_{VPRE}; corrected Max value for TSD_{VPRE_HYST} • Table 124: Corrected Typ and Max values for $TSDL_{DOx}$; corrected Typ value for TSD_{LDOx_HYS} • Table 126: Corrected Typ and Max values for TSD_{TRKx}; corrected Typ value for TSD_{TRKx_HYS}; updated "Description" of the following entries, V_{TRKx_OFF}, $PSRR_{TRKx\_450KHz}$, and $PSRR_{TRKx\_2.2MHz}$ • Table 135: Corrected Typ and Max values for TSD_{GPIO1}; corrected Typ value for TSD_{GPIO1_HYS} • Corrected text of Section 14.2 • Corrected Section 15.1 • Corrected text of Section 15.2 • Updated text of Section 15.8 • Added text to Table 12 • Replaced image titled "CRC encoder example" in Section 15.8.1 • Corrected text in Table 12 under row for Bit 27 to read "Flags Reporting: WUEVENT, LDT_I, GPIO2_I, GPIO1_I, WK2_I, WK1_I • Corrected text in Section 16 • Added row to Table 51 in Section 17.18 • Updated text in Table 98 in Section 18.15 • Corrected Hexadecimal Value entries in Section 19.4 in rows for 0x1A and 0x1C • Updated, added text in Section 20.2 and Table 116 • Updated "Min" value of $C_{IN\_BST\_BE}$ entry in Table 120 in Section 20.3 • Updated "µF" value of $C_{IN\_BST\_BE}$ entry in Table 121 in Section 20.3.1 • Updated text in Table 122 in Section 20.4 • Updated Table 124 in Section 20.5 • Updated third paragraph in Section 21.3.2 • Corrected Table 136 • Added Figure 60 to Section 22.11.1 • Added Figure 61 to Section 22.11.2 • Repositioned and replaced Figure 62 in Section 22.11.3 • Updated "LBIST Status" for entry 00 in Table 200 in Section 22.12.1 • Updated "Min" values for V_{OTP} and V_{DBG} in Table 214 • Updated Figure 74Section 24.1 • Updated Figure 75Section 24.2 • Added Section 25

Table 218. Revision history...*continued*

Rev	Date	Description
3	20221117	• Global corrections to grammar and style throughout • Updated Table 2 • Updated Table 10 • Updated Section 14.1: – Added list item "L_{VPRE} = 10 µH", updated footnotes – Changed list item "FS0B asserted, FS1B pulled up to a disabled supply in Standby mode" to "FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode." • Updated Section 14.2: – Added list item "L_{VPRE} = 10 µH – Updated list item "LDO1 = 3.3 V, LDO2 = 5 V and VPRE = 5.35 V" to read "V_{LDO1} = 3.3 V, V_{LDO2} = 5 V and V_{PRE} = 5.35 V" – Inserted text after Figure 12 – Changed list item "FS0B asserted, FS1B pulled up to a disabled supply in Standby mode." to "FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode." – Changed list item "FS0B asserted, FS1B pulled up to a disabled supply in Standby mode." to "FS0B = 0 and FS1B = 0, pulled up to a disabled supply in Standby mode." • Updated Section 18.7 • Updated Table 111 • Updated Table 116 • Updated Section 20.3: "In Back-End mode (VBST_CFG_OTP = '1'):" now reads "In Back-End mode or boost not used (VBST_CFG_OTP = '1'):"; inserted text • Updated Table 126 • Updated Section 21.4.1: Changed "448 µs resolution" to "488 µs resolution" • Updated Section 22.4: Inserted text • Updated Table 10: Inserted "L_{VPRE} = 10 µH" in first I_{Q_STBY} entry Description, removed "L_{VPRE} = 10 µH" from second I_{Q_STBY} Description • Updated Table 144 • Updated Table 149 • Updated Table 162 • Updated Table 70: Changed "Flags Reporting: FCCU12, FCCU1, FCCU2, ERRMON to "Flags Reporting: RSTB_DIAG, FS0B_DIAG, FS1B_DIAG" in Bit 13; changed "Source register: FS_DIAG_SAFETY2" to "Source register: FS_SAFE_IOS_1" • Updated Table 109: Changed table title from "FS_LP_REQ register bit description" to "FS_LDT_LPSEL register bit description" • Updated Table 116 – Changed Description of F_{PRE} from "VPRE_FREQ_OTP = 0" and "VPRE_FREQ_OTP = 1" to "VPRE_CLK_OTP = 0" and "VPRE_CLK_OTP = 1", respectively – Changed Description of $t_{PRE\_ON\_MIN\_450K}$ from "VPRE_FREQ_OTP = 0" to "VPRE_CLK_OTP = 0" – Changed Description of $t_{PRE\_OFF\_MIN}$, VPRE_PFM_TOFF_OTP[1:0] = 10 and V_{PREIN} = 12 V switched positions • Updated Table 124 – Removed Symbol I_{Q_LDOx25} – Changed Symbol I_{Q_LDOx85} to I_{Q_LDOx} – Changed I_{Q_LDOx} Description from "$V_{LDOx\_HDR\_STBY}$ = 50mV" to "$V_{LDOx\_HDR\_STBY}$ = 50mV or 350 mV" – Changed Typ value from 21 to 7 • Updated Section 22.10.2: Inserted text • Updated Section 22.11.3: Inserted text • Updated text in Section 23 • Updated Table 215 • Updated: Figure 2, Figure 3, Figure 6, Figure 56, Figure 10, Figure 11, Figure 12, Figure 8, Figure 26, Figure 27 • Updated links in Table 217

29 Legal information

29.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

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