FlexCAN Bit Timing Calculation

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The FlexCAN module supports a variety of means to setup bit timing parameters that are required by the CAN protocol.

This document gives a basic insight into bit timings relationship and provide easy step-by-step guide to calculate bit timing parameters for desired baudrate.

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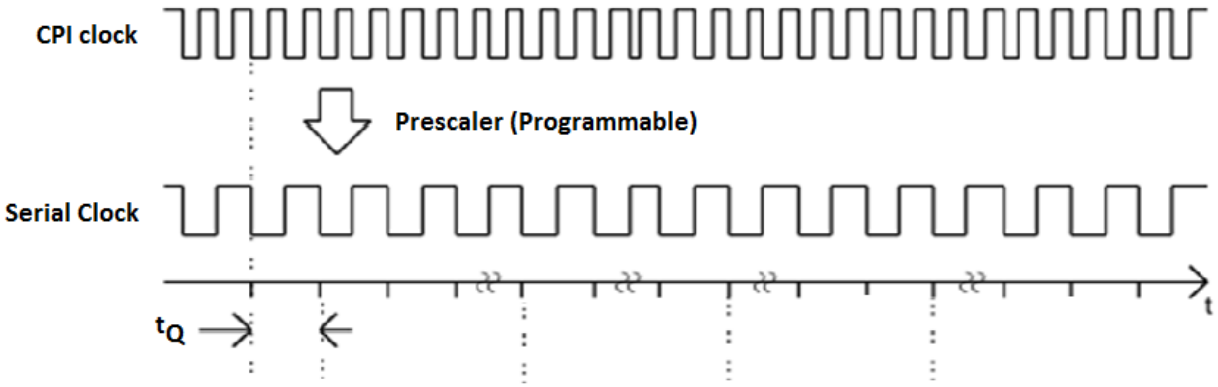
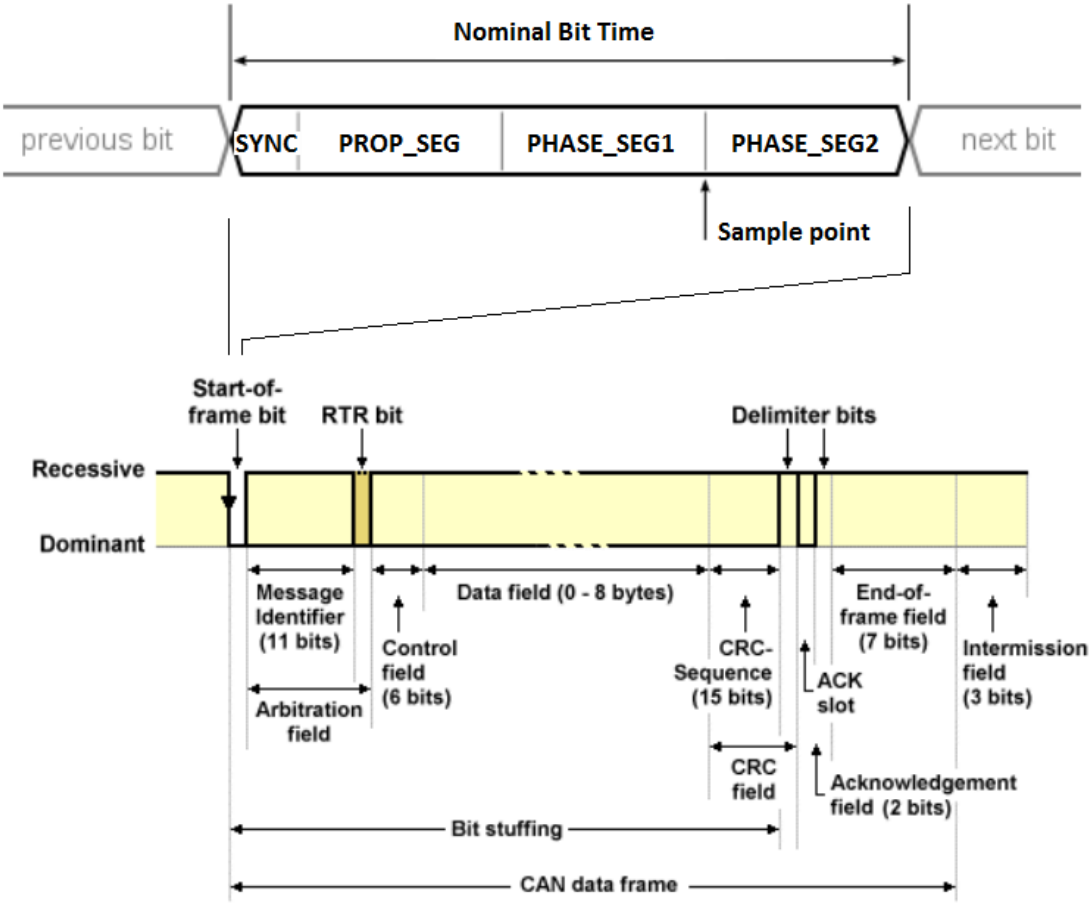
1 Introduction

The clock dependency can be described based on the following figure.





Starting from a data frame transferred on the bus. A desired baudrate tells how many bits are sent on the network per second. The Nominal Bit Rate (baudrate) is uniform throughout the network and is given by:

$$baudrate = 1 / t_{NBT} \quad (1)$$

The t_{NBT} represents a period of the Nominal Bit Time (NBT), i.e. single bit transfered on the bus. The NBT is separated into four non-overlaping segments, SYNC_SEG, PROP_SEG, PHASE_SEG1 and PHASE_SEG2. Each of these segments is an integer multiple of Time Quantum t_Q.

$$t_{NBT} = t_Q + PROP\_SEG * t_Q + PHASE\_SEG1 * t_Q + PHASE\_SEG2 * t_Q = NBT * t_Q \quad (2)$$

The below table summarizes the possible values each segment can be set to.

Segment	Duration
SYNC_SEG	$t_{SYNC\_SEG} = 1\ t_Q$
PROP_SEG	$t_{PROP\_SEG} = 1, 2 \ldots 8\ t_Q$
PHASE_SEG1	$t_{PHASE\_SEG1} = 1, 2 \ldots 8\ t_Q$
PHASE_SEG2	$t_{PHASE\_SEG2} = MAX(IPT, t_{PHASE\_SEG1})$

Note: Tthe function MAX(,) returns the larger of the two arguments.

The duration of the segment PHASE_SEG1 may be between 1 and 8 Time Quanta if one sample per bit is selected and may be between 2 and 8 Time Quanta if three samples per bit are selected. If three samples per bit are chosen, the most frequently sampled value is taken as the bit value.

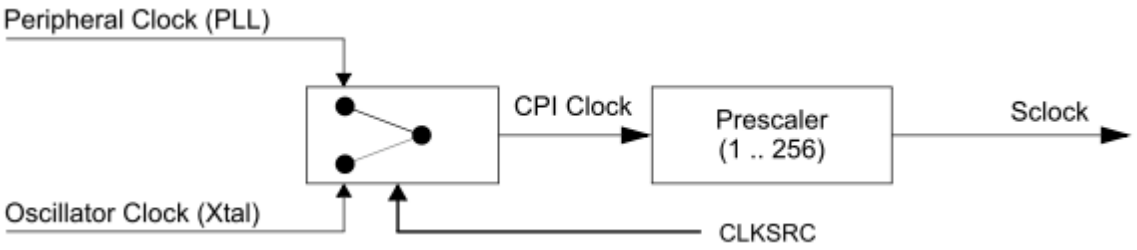
The duration of segment PHASE_SEG2 must be equal to PHASE_SEG1, unless PHASE_SEG1 is less than the Information Processing Time (IPT), in which case PHASE_SEG2 must be equal to the Information Processing Time. The Information Processing Time is equal to 2 Time Quanta

From the table, it would appear that the minimum number of Time Quanta per bit (NBT) is 5. However, many CAN controllers require a minimum of 8 Time Quanta per bit. The maximum number of Time Quanta per bit is 25.

A Time Quantum is the atomic unit of time handled by the CAN engine and it is given by the Serial Clock (Sclock) period as

$$t_Q = 1/Sclock = 1/[CPI\_clock /(PRESDIV+1)]. \quad (3)$$

The CPI_clock is the CAN Protocol Interface clock, can be either the peripheral clock (driven by the FMPLL) or the crystal oscillator clock. The PRESDIV controls a Prescaler that generates the Serial Clock (Sclock)



The clock source selection is done by the CLK_SRC bit of the CTRL register. Moreover this register contains other fields used to control bit timing parameters as was mentioned above: PRESDIV, PROPSEG, PSEG1, PSEG2 and RJW. The SMP specifies if one or three samples per bit is used.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	PRESDIV								RJW		PSEG1			PSEG2		
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	BOFF_MSK	ERR_MSK	CLK_SRC	LPB	TWRN_MSK	RWRN_MSK	0	0	SMP	BOFF_REC	TSYN	LBUF	LOM	PROPSEG		
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

These parameters have to be properly calculated/selected to meet the CAN specification.

The following chapter provides a step-by-step guide for determining the optimum bit timing parameters which satisfy the requirements for proper bit sampling. Besides the desired baudrate and selected CPI clock a physical interface parameters and bus length is also needed to determine propagation segment duration.

2 Step-by-step guide

STEP 1: Determine minimum permissible time for the PROP_SEG segment.

Obtain the maximum propagation delay of the physical interface for both the transmitter and the receiver from the manufacturers data sheet. Calculate the propagation delay of the bus by multiplying the maximum length of the bus by the signal propagation delay of the bus cable. Use these values to calculate t_{PROP_SEG} using equation

$$t_{PROP\_SEG} = 2(t_{BUS} + t_{TX} + t_{RX}) \quad (4)$$

STEP 2: Choose CPI_clock, the Prescaler and NBT.

Determine Prescaler and a Nominal Bit Time (NBT). Basically you can combine equations 1, 2 and 3 into

$$\text{NBT} * \text{Prescaler} = \text{CPI\_clock} / \text{baud rate.} \quad (5)$$

As already mentioned NBT may be integer number in range 8 to 25 and Prescaler in range 1 to 256. Find those combinations of NBT * Prescaler which is equal to CPI_clock /baud rate. There may be a lot of possible combinations. If none can be found choose different CPI_clock.

STEP 3: Calculate PROP_SEG duration.

The number of time quanta required for the PROP_SEG segment are calculated based on chosen Prescaler value

$$\begin{aligned} \text{PROP\_SEG} &= \text{ROUND\_UP}(t_{PROP\_SEG} / t_Q) \\ &= \text{ROUND\_UP}(t_{PROP\_SEG} * \text{CPI\_clock} / \text{Prescaler}) \end{aligned} \quad (6)$$

where the function ROUND_UP( ) returns the argument rounded up to the next integer value.

STEP 4: Determine PHASE_SEG1, PHASE_SEG2

From the number of Time Quanta per bit obtained in Step 2, subtract the PROP_SEG value calculated in Step 3 and subtract 1 t_Q for SYNC_SEG.

If the remaining number is an odd number greater than 3 then add one to the PROP_SEG value and recalculate.

If the remaining number is equal to 3 then PHASE_SEG1 = 1 and PHASE_SEG2 = 2 and only one sample per bit may be chosen. Otherwise divide the remaining number by two and assign the result to PHASE_SEG1 and PHASE_SEG2.

STEP 5: Determine RJW

RJW is chosen as the smaller of 4 and PHASE_SEG1

STEP 6: Calculate required oscillator tolerance

There are two clock tolerance requirements which must be satisfied.

$$(2 * \Delta f) * 10 * t_{NBT} < t_{RJW} \quad (8)$$

$$(2 * \Delta f) * (13 * t_{NBT} - t_{PHASE\_SEG2}) < MIN(t_{PHASE\_SEG1}, t_{PHASE\_SEG2}) \quad (9)$$

where the function MIN(,) returns the smaller of the two arguments.

As the required oscillator tollerance select the smaller of the calculated values.

3 Example

Calculate the bit segments for the following system constraints:

- Bit rate = 500k bit per second
- Bus length = 10m
- Bus propagation delay = 5 x 10-9 s/m
- Physical Interface (PCA82C250) transmitter plus receiver propagation delay = 150ns at 85C
- CPI_clock = 40 MHz

STEP 1:

Physical delay of bus = 10m x 5 ns/m = 50ns
t_{PROP_SEG} = 2(50 + 150) = 400 ns

STEP 2:

NBT * Prescaler = CPI_clock /baud rate = 40 MHz / 500kbps = 80

There can be 4 possibilities:
NBT = 20, Prescaler = 4
NBT = 16, Prescaler = 5
NBT = 10, Prescaler = 8
NBT = 8, Prescaler = 10

Lets choose the first one

STEP 3:

PROP_SEG = ROUND_UP(400ns * 40MHz / 4) = 4

STEP 4:

NBT – 1 – PROP_SEG = 20 – 1 – 4 = 15
As the result is odd increase PROP_SEG and recalculate

20 – 1 – 5 = 14
Divide the number by two and assign the result to PHASE_SEG1 and PHASE_SEG2.

PHASE_SEG1 = 7 and PHASE_SEG2 = 7

STEP 5:

RJW is chosen as the smaller of 4 and PHASE_SEG1, so RJW = 4

STEP 6:

$(2 * \Delta f) * 10 * t_{NBT} < t_{RJW}$
$(2 * \Delta f) * 10 * 20 < 4 \quad => \Delta f < 0.01 = 1\%$

$(2 * \Delta f) * (13 * t_{NBT} – t_{PHASE\_SEG2}) < MIN(t_{PHASE\_SEG1}, t_{PHASE\_SEG2})$
$(2 * \Delta f) * (13 * 20 – 7) < MIN(7, 7) => \Delta f < 0.0138 = 1.38\%$

required oscillator tollerance is 1%

In summary:

Prescaler = 4
Nominal Bit Time = 20
PROP_SEG = 5
PHASE_SEG1 = 7
PHASE_SEG2 = 7
RJW = 4
Oscillator tolerance = 1%

Similarly repeate steps 3-6 for next NBT, Prescaler values given in step 2.
Calculated bit timing parameters are given in following table.

Prescaler [-]	**Sclock [MHz]**	**t_Q [ns]**	**NBT [#t_Q]**	**PROPSEG [# t_Q]**	**PSEG1 [# t_Q]**	**PSEG2 [# t_Q]**	**RJW [# t_Q]**	**Δf[%] [%]**	**sample point [%]**	**CANx_CR** [hex]
4	10	100	20	5	7	7	4	1	65.00	0x03F60004
5	8	125	16	5	5	5	4	1.231527	68.75	0x04E40004
8	5	200	10	3	3	3	3	1.181102	70.00	0x07920002
10	4	250	8	3	2	2	2	0.980392	75.00	0x09490002

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