



e.MMC™ Memory

**MTFC16GAKAECN-4M IT, MTFC16GAKAEJP-4M IT,
MTFC16GAKAENA-4M IT, MTFC32GAKAECN-4M IT,
MTFC32GAKAEJP-4M IT, MTFC32GAKAENA-4M IT,
MTFC64GAKAEEY-4M IT, MTFC64GAKAEYF-4M IT**

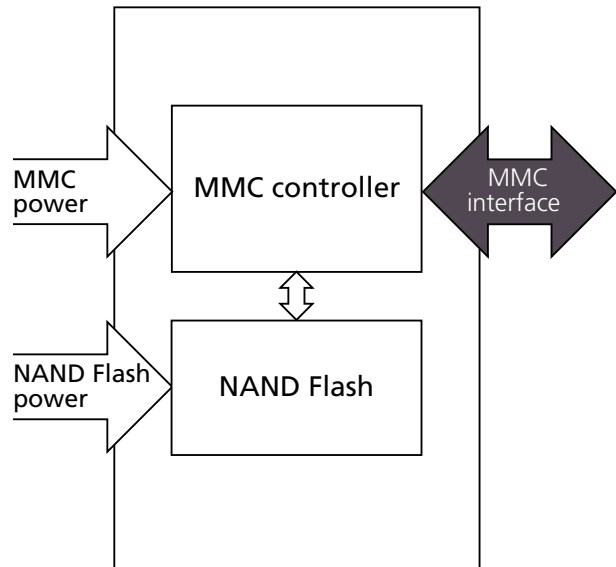
Features

- MultiMediaCard (MMC) controller and NAND Flash
- 153-ball VFBGA (RoHS compliant, "green package")
- 153-ball LFBGA (RoHS compliant, "green package")
- 100-ball TBGA (RoHS compliant, "green package")
- V_{CC} : 2.7–3.6V
- V_{CCQ} (dual voltage): 1.65–1.95V; 2.7–3.6V
- Temperature ranges (ambient)
 - Operating temperature: -40°C to $+85^{\circ}\text{C}$
 - Storage temperature: -40°C to $+85^{\circ}\text{C}$

MMC-Specific Features

- JEDEC/MMC standard version 5.0-compliant (JEDEC Standard No. JESD84-B50)¹
 - Advanced 12-signal interface
 - x1, x4, and x8 I/Os, selectable by host
 - SDR/DDR modes up to 52 MHz clock speed
 - HS200/HS400 modes
 - Real-time clock
 - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
 - Temporary write protection
 - Boot operation (high-speed boot)
 - Sleep mode
 - Replay-protected memory block (RPMB)
 - Secure erase and secure trim
 - Hardware reset signal
 - Multiple partitions with enhanced attribute
 - Permanent and power-on write protection
 - High-priority interrupt (HPI)
 - Background operation
 - Reliable write
 - Discard and sanitize
 - Extended partitioning
 - Context ID

Figure 1: Micron e-MMC Device



MMC-Specific Features (Continued)

- Data TAG
- Packed commands
- Dynamic device capacity
- Backward compatible with previous MMC
- Cache
- Field firmware update (FFU)
- Device health report
- Sleep notification
- Power-off notification
- ECC and block management implemented

Note: 1. The JEDEC specification is available at www.jedec.org/sites/default/files/docs/JESD84-B50.pdf.



e.MMC Performance and Current Consumption by Bus Mode

Table 1: MLC Partition Performance

| Condition ¹ | Typical Values | | | Unit |
|--------------------------|----------------|------|------|------|
| | 16GB | 32GB | 64GB | |
| HS400 | | | | |
| Sequential write | 30 | 40 | 50 | MB/s |
| Sequential read | 250 | 250 | 280 | MB/s |
| Random write (cache on) | 5200 | 5650 | 5800 | IOPS |
| Random write (cache off) | 1130 | 1200 | 1300 | IOPS |
| Random read | 4000 | 4500 | 4700 | IOPS |
| HS200 | | | | |
| Sequential write | 30 | 40 | 40 | MB/s |
| Sequential read | 160 | 160 | 160 | MB/s |
| Random write (cache on) | 5200 | 5650 | 5800 | IOPS |
| Random write (cache off) | 1130 | 1200 | 1300 | IOPS |
| Random read | 4000 | 4500 | 4700 | IOPS |
| DDR52 | | | | |
| Sequential write | 30 | 40 | 40 | MB/s |
| Sequential read | 90 | 90 | 90 | MB/s |
| Random write (cache on) | 5200 | 5650 | 5800 | IOPS |
| Random write (cache off) | 1130 | 1200 | 1300 | IOPS |
| Random read | 3800 | 4000 | 4200 | IOPS |

Note: 1. Bus in x8 I/O mode. Sequential access of 1MB chunk; random access of 4KB chunk over 1GB span. Additional performance data, such as system performance on a specific application board, will be provided in a separate document upon customer request.

Table 2: Current Consumption

| Condition ¹ | Typical Values (I _{CC} /I _{CCQ}) | | | Unit |
|------------------------|---|--------|--------|------|
| | 16GB | 32GB | 64GB | |
| HS400 | | | | |
| Write | 110/25 | 115/25 | 160/30 | mA |
| Read | 125/50 | 140/50 | 155/60 | mA |
| HS200 | | | | |
| Write | 110/25 | 115/25 | 160/30 | mA |
| Read | 125/50 | 135/50 | 120/60 | mA |
| DDR52 | | | | |
| Write | 110/30 | 115/30 | 75/30 | mA |
| Read | 80/35 | 80/35 | 125/35 | mA |
| Idle/Standby | | | | |


Table 2: Current Consumption (Continued)

| Condition ¹ | Typical Values (I_{CC}/I_{CCQ}) | | | Unit |
|------------------------|-------------------------------------|--------|--------|---------------|
| | 16GB | 32GB | 64GB | |
| Sleep | 0/140 | 0/145 | 0/100 | μA |
| Auto standby | 50/140 | 50/145 | 60/100 | μA |

Note: 1. Bus in x8 I/O mode. $V_{CC} = 3.6\text{V}$ and $V_{CCQ} = 1.95\text{V}$. 25°C . Measurements done as average RMS current consumption. I_{CCQ} in READ operation measurements with tester load disconnected.



Part Numbering Information

Micron® e-MMC memory devices are available in different configurations and densities.

Figure 2: e-MMC Part Numbering

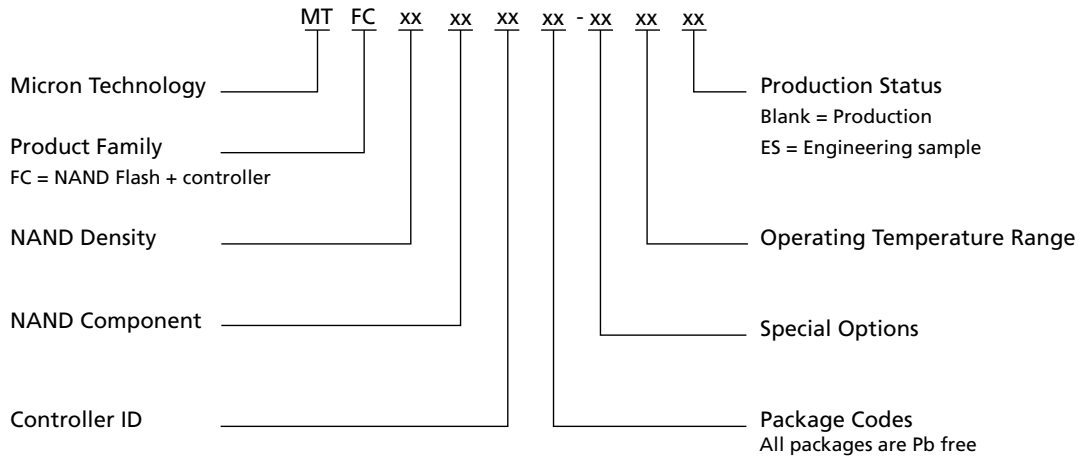


Table 3: Ordering Information

| Base Part Number | Density | Package | Shipping |
|--|---------|--------------------------------------|-----------------------|
| MTFC16GAKAECN-4M IT MTFC16GAKAEJP-4M IT | 16GB | 153-ball VFBGA 11.5mm x 13mm x 1.0mm | Tray Tape and reel |
| MTFC16GAKAENA-4M IT | 16GB | 100-ball TBGA 14mm x 18mm x 1.2mm | Tray Tape and reel |
| MTFC32GAKAECN-4M IT MTFC32GAKAEJP-4M IT | 32GB | 153-ball VFBGA 11.5mm x 13mm x 1.0mm | Tray Tape and reel |
| MTFC32GAKAENA-4M IT | 32GB | 100-ball TBGA 14mm x 18mm x 1.2mm | Tray Tape and reel |
| MTFC64GAKAEEY-4M IT MTFC64GAKAEYF-4M IT | 64GB | 153-ball LFBGA 11.5mm x 13mm x 1.4mm | Tray Tape and reel |

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.



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General Description

Micron *e.MMC* is a communication and mass data storage device that includes a Multi-MediaCard (MMC) interface, a NAND Flash component, and a controller on an advanced 12-signal bus, which is compliant with the MMC system specification. Its cost per bit, small package sizes, and high reliability make it an ideal choice for industrial applications like infrastructure and networking equipment, PC and servers, a variety of other industrial products.

The nonvolatile *e.MMC* draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.



Signal Descriptions

Table 4: Signal Descriptions

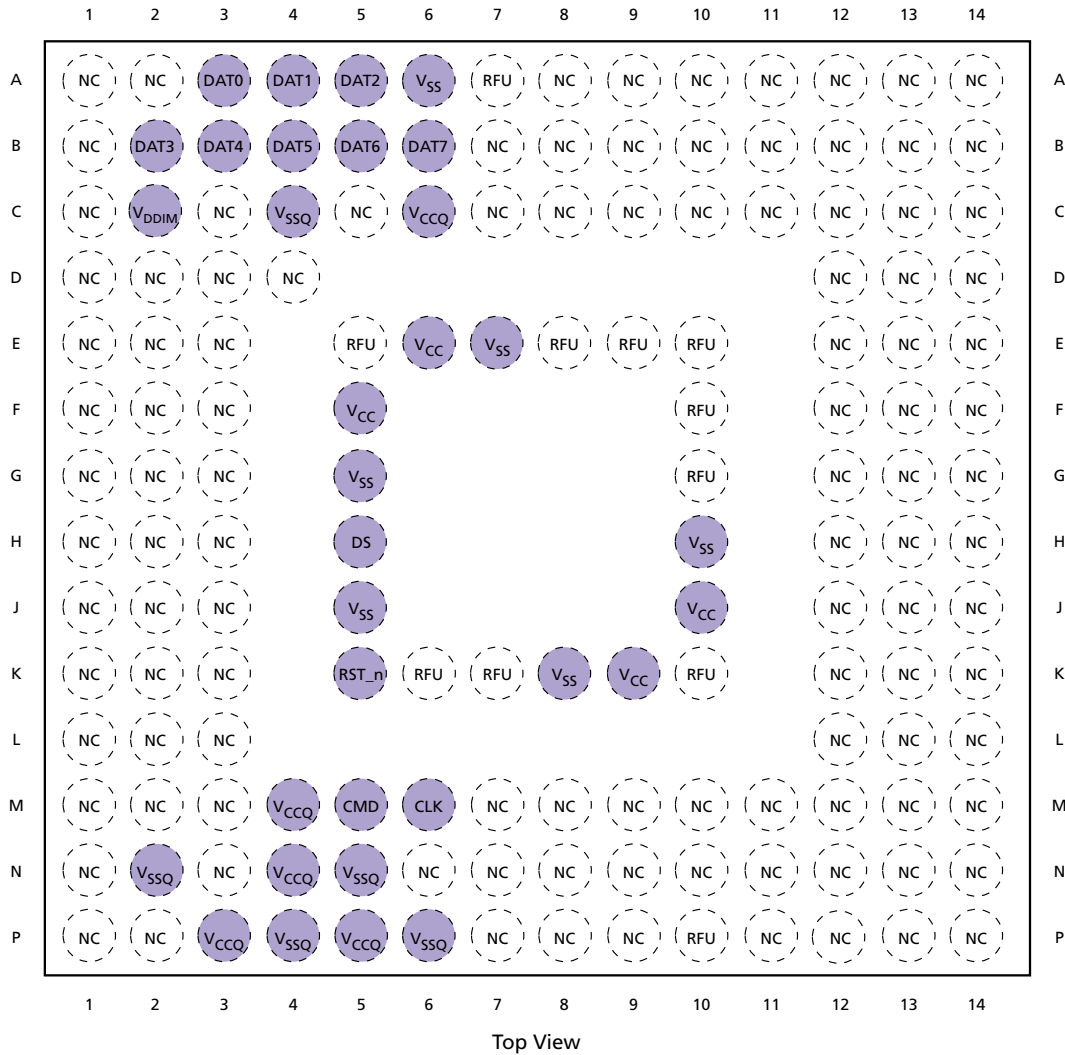
| Symbol | Type | Description |
|-------------------------------|--------|---|
| CLK | Input | Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency. |
| RST_n | Input | Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it. |
| CMD | I/O | Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands are sent from the MMC host to the device, and responses are sent from the device to the host. |
| DAT[7:0] | I/O | Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). The device includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines. |
| DS | Output | Data strobe: Generated by the device and used for data output and CRC status response output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycle of this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the other bit for the negative edge. For CRC status response output, the CRC status is latched on the positive edge only, and is "Don't Care" on the negative edge. |
| V _{CC} | Supply | V _{CC} : NAND interface (I/F) I/O and NAND Flash power supply. |
| V _{CCQ} | Supply | V _{CCQ} : e.MMC controller core and e.MMC I/F I/O power supply. |
| V _{SS} ¹ | Supply | V _{SS} : NAND I/F I/O and NAND Flash ground connection. |
| V _{SSQ} ¹ | Supply | V _{SSQ} : e.MMC controller core and e.MMC I/F ground connection. |
| V _{DDIM} | | Internal voltage node. Do not tie to supply voltage or ground. |
| NC | – | No connect: No internal connection is present. |
| RFU | – | Reserved for future use: No internal connection is present. Leave it floating externally. |

Note: 1. V_{SS} and V_{SSQ} are connected internally.



153-Ball Signal Assignments

Figure 3: 153 Ball (Top View, Ball Down)

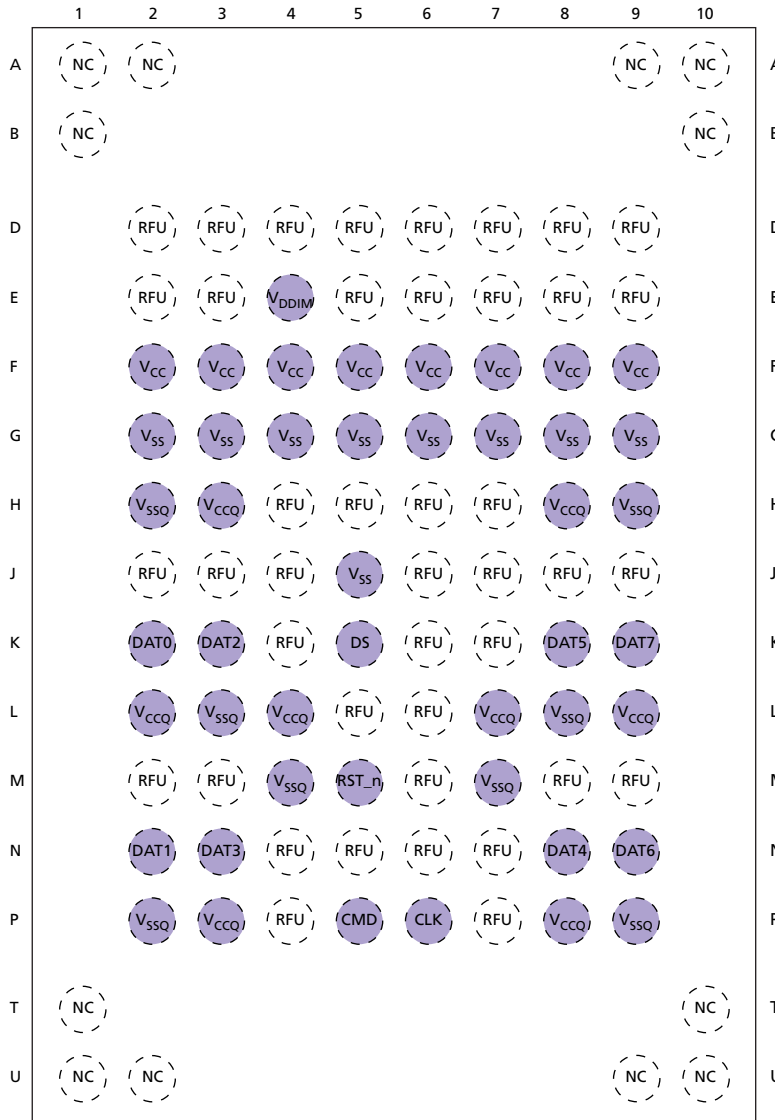


- Notes:
1. Some previous versions of the JEDEC product or mechanical specification had defined reserved for future use (RFU) balls as no connect (NC) balls. NC balls assigned in the previous specifications could have been connected to ground on the system board. To enable new feature introduction, some of these balls are assigned as RFU in the v4.4 mechanical specification. Any new PCB footprint implementations should use the new ball assignments and leave the RFU balls floating on the system board.
 2. VCC, VCCQ, VSS, and VSSQ balls must all be connected on the system board.



100-Ball Signal Assignments

Figure 4: 100 Ball (Top View, Ball Down)

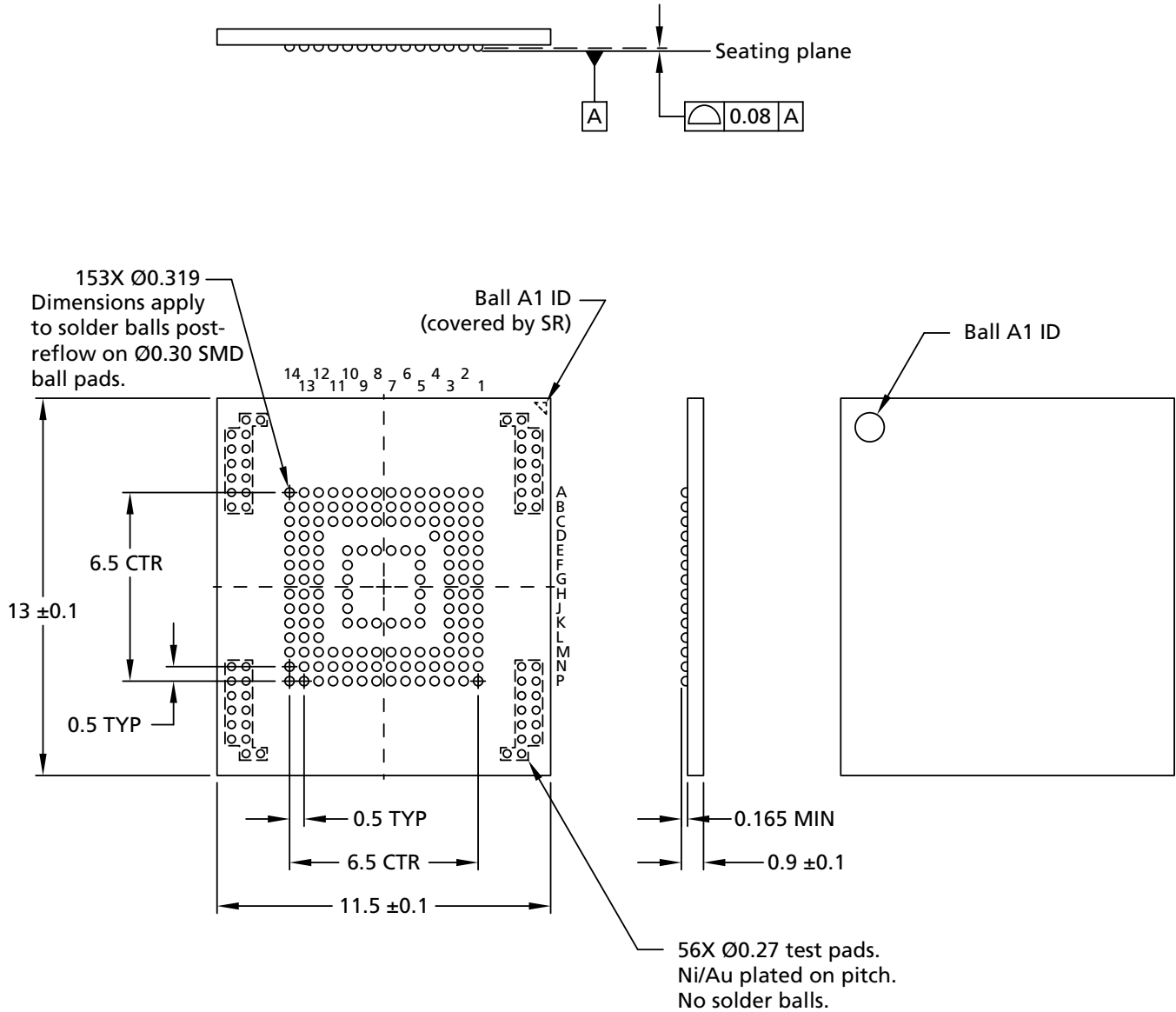


- Notes:
1. Connect a 1 μ F decoupling capacitor from V_{DDIM} to ground.
 2. Some previous versions of the JEDEC product or mechanical specification had defined reserved for future use (RFU) balls as no connect (NC) balls. NC balls assigned in the previous specifications could have been connected to ground on the system board. To enable new feature introduction, some of these balls are assigned as RFU in the v4.4 mechanical specification. Any new PCB footprint implementations should use the new ball assignments and leave the RFU balls floating on the system board.
 3. V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} balls must all be connected on the system board.



Package Dimensions

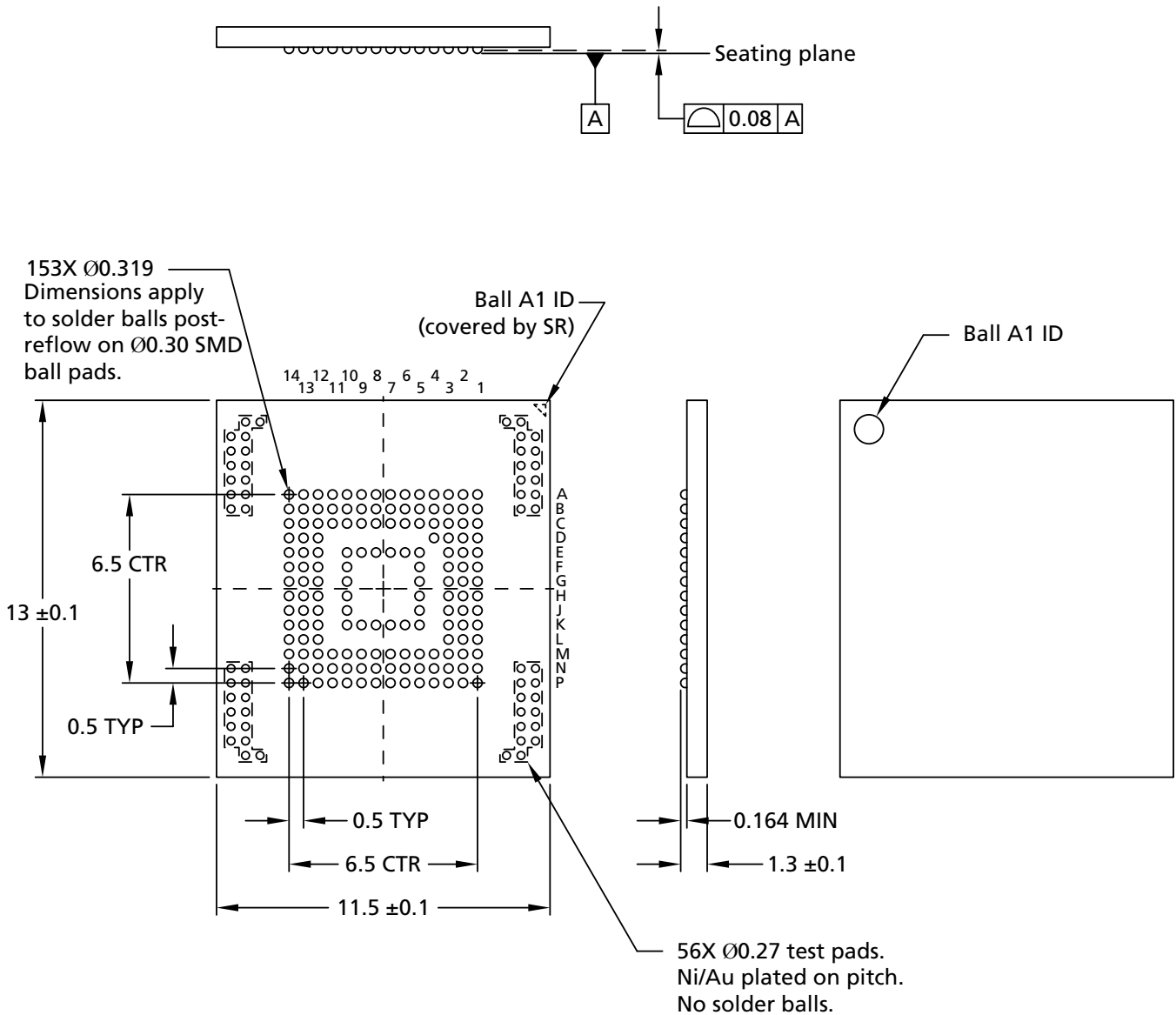
Figure 5: 153-Ball VFBGA – 11.5mm x 13.0mm x 1.0mm (Package Codes: JP, CN)



- Notes: 1. Dimensions are in millimeters
2. SAC302 Solder Ball



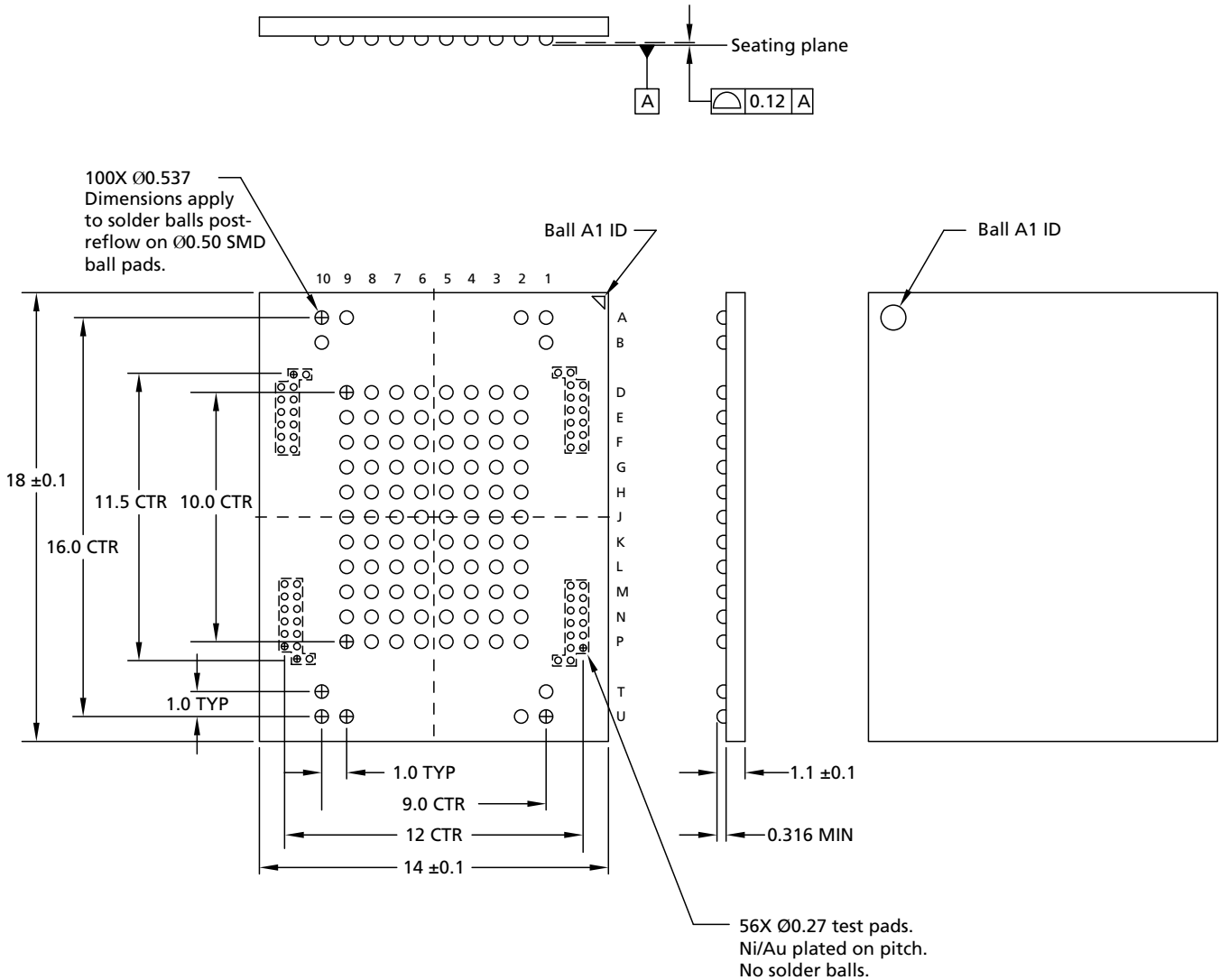
Figure 6: 153-Ball LFBGA – 11.5mm x 13.0mm x 1.4mm (Package Codes: YF, EY)



- Notes: 1. Dimensions are in millimeters
2. SAC302 Solder Ball



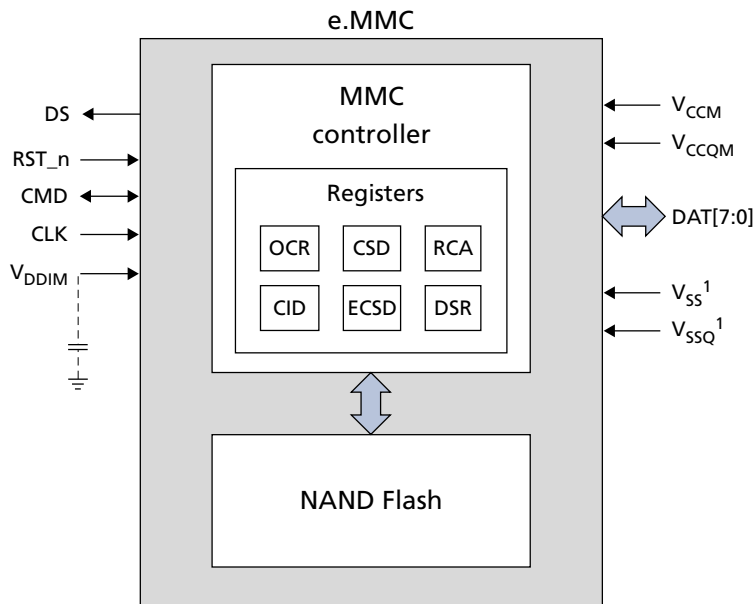
Figure 7: 100-Ball TBGA – 14mm x 18mm x 1.2mm (Package Code: NA)



- Notes: 1. Dimensions are in millimeters
2. SAC302 Solder Ball

Architecture

Figure 8: e.MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND Flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND Flash technology (generation or memory cell type).

The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron e.MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces the defective block with one of the spare blocks. This process is invisible to the host and does not affect data space allocated for the user.

The device also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.

To make the best use of these advanced technologies and ensure proper data loading and storage over the life of the device, the host must exercise the following precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.



OCR Register

The 32-bit operation conditions register (OCR) stores the voltage profile of the card and the access mode indication. In addition, this register includes a status information bit.

Table 5: OCR Parameters

| OCR Bits | OCR Value | Description |
|----------|-----------------------------------|----------------------------|
| [31] | 1b (ready)/0b (busy) ¹ | Device power-on status bit |
| [30:29] | 10b | Sector mode |
| [28:24] | 0 0000b | Reserved |
| [23:15] | 1 1111 1111b | 2.7–3.6V voltage range |
| [14:8] | 000 0000b | 2.0–2.7V voltage range |
| [7] | 1b | 1.70–1.95V voltage range |
| [6:0] | 000 0000b | Reserved |

Note: 1. OCR = C0FF8080h after the device has completed power-up.



CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by e.MMC protocol. Each device is created with a unique identification number.

Table 6: CID Register Field Parameters

| Name | Field | Width | CID Bits | CID Value |
|-----------------------|-------|-------|-----------|-----------|
| Manufacturer ID | MID | 8 | [127:120] | 13h |
| Reserved | – | 6 | [119:114] | – |
| Card/BGA | CBX | 2 | [113:112] | 01h |
| OEM/application ID | OID | 8 | [111:104] | – |
| Product name | PNM | 48 | [103:56] | – |
| Product revision | PRV | 8 | [55:48] | – |
| Product serial number | PSN | 32 | [47:16] | – |
| Manufacturing date | MDT | 8 | [15:8] | – |
| CRC7 checksum | CRC | 7 | [7:1] | – |
| Not used; always 1 | – | 1 | [0] | – |



CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 7: CSD Register Field Parameters

| Name | Field | Size (Bits) | Cell Type ¹ | CSD Bits | CSD Value |
|--|--------------------|-------------|------------------------|-----------|-----------|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 3h |
| System specification version | SPEC_VERS | 4 | R | [125:122] | 4h |
| Reserved ² | – | 2 | – | [121:120] | – |
| Data read access time 1 | TAAC | 8 | R | [119:112] | 4Fh |
| Data read access time 2 in CLK cycles (NSAC × 100) | NSAC | 8 | R | [111:104] | 01h |
| Maximum bus clock frequency | TRAN_SPEED | 8 | R | [103:96] | 32h |
| Card command classes | CCC | 12 | R | [95:84] | 0F5h |
| Maximum read data block length | READ_BL_LEN | 4 | R | [83:80] | 9h |
| Partial blocks for reads supported | READ_BL_PARTIAL | 1 | R | [79] | 0h |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78] | 0h |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77] | 0h |
| DSR implemented | DSR_IMP | 1 | R | [76] | 1h |
| Reserved | – | 2 | – | [75:74] | – |
| Device size | C_SIZE | 12 | R | [73:62] | FFFh |
| Maximum read current at V _{DD,min} | VDD_R_CURR_MIN | 3 | R | [61:59] | 7h |
| Maximum read current at V _{DD,max} | VDD_R_CURR_MAX | 3 | R | [58:56] | 7h |
| Maximum write current at V _{DD,min} | VDD_W_CURR_MIN | 3 | R | [55:53] | 7h |
| Maximum write current at V _{DD,max} | VDD_W_CURR_MAX | 3 | R | [52:50] | 7h |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 7h |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] | 1Fh |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 1Fh |
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] | 0Fh |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31] | 1h |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | 0h |
| Write-speed factor | R2W_FACTOR | 3 | R | [28:26] | 2h |
| Maximum write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 9h |
| Partial blocks for writes supported | WRITE_BL_PARTIAL | 1 | R | [21] | 0h |
| Reserved | – | 4 | – | [20:17] | – |
| Content protection application | CONTENT_PROT_APP | 1 | R | [16] | 0h |
| File-format group | FILE_FORMAT_GRP | 1 | R/W | [15] | 0h |
| Copy flag (OTP) | COPY | 1 | R/W | [14] | 0h |


Table 7: CSD Register Field Parameters (Continued)

| Name | Field | Size (Bits) | Cell Type ¹ | CSD Bits | CSD Value |
|----------------------------|--------------------|-------------|------------------------|----------|-----------|
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | [13] | 0h |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12] | 0h |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | 0h |
| ECC | ECC | 2 | R/W/E | [9:8] | 0h |
| CRC | CRC | 7 | R/W/E | [7:1] | - |
| Reserved | - | 1 | - | [0] | - |

- Notes:
1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
 2. Reserved bits should be read as 0.



ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 8: ECSD Register Field Parameters

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECS1.7D Value |
|---|---|--------------|------------------------|------------|---------------|
| Properties Segment | | | | | |
| Reserved ² | – | 6 | – | [511:506] | – |
| Extended Security Commands Error | EXT_SECURITY_ERR | 1 | R | [505] | 00h |
| Supported command sets | S_CMD_SET | 1 | R | [504] | 01h |
| HPI features | HPI_FEATURES | 1 | R | [503] | 01h |
| Background operations support | BKOPS_SUPPORT | 1 | R | [502] | 01h |
| Max-packed read commands | MAX_PACKED_READS | 1 | R | [501] | 3Fh |
| Max-packed write commands | MAX_PACKED_WRITES | 1 | R | [500] | 3Fh |
| Data tag support | DATA_TAG_SUPPORT | 1 | R | [499] | 01h |
| Tag unit size | TAG_UNIT_SIZE | 1 | R | [498] | 03h |
| Tag resources size | TAG_RES_SIZE | 1 | R | [497] | 00h |
| Context management capabilities | CONTEXT_CAPABILITIES | 1 | R | [496] | 05h |
| Large unit size | LARGE_UNIT_SIZE_M1 | 1 | R | [495] | 07h |
| Extended partitions attribute support | EXT_SUPPORT | 1 | R | [494] | 03h |
| Supported modes | SUPPORTED_MODES | 1 | R | [493] | 03h |
| Field firmware update features | FFU_FEATURES | 1 | R | [492] | 00h |
| Operation code timeout | OPERATION_CODE_TIMEOUT | 1 | R | [491] | 00h |
| Field firmware update arguments | FFU_ARG | 4 | R | [490:487] | 00h |
| Reserved | – | 181 | – | [486:306] | – |
| Number of firmware sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4 | R | [305:302] | 00h |
| Device health report | VENDOR_PROPRIETARY_HEALTH_REPORT | 32 | R | [301:270] | 00h |
| Device life time estimation type B | DEVICE_LIFE_TIME_EST_TYP_B | 1 | R | [269] | 01h |
| Device life time estimation type A | DEVICE_LIFE_TIME_EST_TYP_A | 1 | R | [268] | 01h |
| Pre-end of life information | PRE_EOL_INFO | 1 | R | [267] | 01h |
| Optimal read size | OPTIMAL_READ_SIZE | 1 | R | [266] | 01h |
| Optimal write size | OPTIMAL_WRITE_SIZE | 1 | R | [265] | 08h |
| Optimal trim unit size | OPTIMAL_TRIM_UNIT_SIZE | 1 | R | [264] | 01h |
| Device version | DEVICE_VERSION | 2 | R | [263:262] | 00h |


Table 8: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECS1.7D Value | |
|---|----------------------------|--------------|------------------------|------------|---------------|-----|
| Firmware version ³ | FIRMWARE_VERSION | 8 | R | [261:254] | – | |
| Power class for 200 MHz, DDR at V _{CC} = 3.6V | PWR_CL_DDR_200_360 | 1 | R | [253] | 00h | |
| Cache size | CACHE_SIZE | 4 | R | [252:249] | 00000400h | |
| Generic CMD6 timeout | GENERIC_CMD6_TIME | 1 | R | [248] | 19h | |
| Power-off notification (long) timeout | POWER_OFF_LONG_TIME | 1 | R | [247] | FFh | |
| Background operations status | BKOPS_STATUS | 1 | R | [246] | 00h | |
| Number of correctly programmed sectors | CORRECTLY_PROG_SECTORS_NUM | 4 | R | [245:242] | 00000000h | |
| First initialization time after partitioning (first CMD1 to device ready) | INI_TIMEOUT_AP | 1 | R | [241] | 64h | |
| Reserved | – | 1 | – | [240] | – | |
| Power class for 52 MHz, DDR at 3.6V | PWR_CL_DDR_52_360 | 1 | R | [239] | 00h | |
| Power class for 52 MHz, DDR at 1.95V | PWR_CL_DDR_52_195 | 1 | R | [238] | 00h | |
| Power class for 200 MHz at 1.95V | PWR_CL_200_195 | 1 | R | [237] | 40h | |
| Power class for 200 MHz, at 1.3V | PWR_CL_200_130 | 1 | R | [236] | 00h | |
| Minimum write performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | R | [235] | 00h | |
| Minimum read performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | R | [234] | 00h | |
| Reserved | – | 1 | – | [233] | – | |
| TRIM multiplier | TRIM_MULT | 16GB | 1 | R | [232] | 16h |
| | | 32GB | 1 | R | [232] | 27h |
| | | 64GB | 1 | R | [232] | 16h |
| Secure feature support | SEC_FEATURE_SUPPORT | 1 | R | [231] | 55h | |
| Secure erase multiplier | SEC_ERASE_MULT | 1 | R | [230] | 01h | |
| Secure trim multiplier | SEC_TRIM_MULT | 1 | R | [229] | 01h | |
| Boot information | BOOT_INFO | 1 | R | [228] | 07h | |
| Reserved | – | 1 | – | [227] | – | |
| Boot partition size | BOOT_SIZE_MULT | 1 | R | [226] | 80h | |
| Access size | ACC_SIZE | 16GB | 1 | R | [225] | 08h |
| | | 32GB | 1 | R | [225] | 09h |
| | | 64GB | 1 | R | [225] | 09h |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | 1 | R | [224] | 01h | |
| High-capacity erase timeout | ERASE_TIMEOUT_MULT | 16GB | 1 | R | [223] | 14h |
| | | 32GB | 1 | R | [223] | 1Ah |
| | | 64GB | 1 | R | [223] | 14h |
| Reliable write-sector count | REL_WR_SEC_C | 1 | R | [222] | 01h | |


Table 8: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECS1.7D Value | |
|---|------------------------------------|--------------|------------------------|------------|---------------|-----------|
| High-capacity write protect group size | HC_WP_GRP_SIZE | 1 | R | [221] | 10h | |
| Sleep current (V_{CC}) | S_C_VCC | 1 | R | [220] | 06h | |
| Sleep current (V_{CCQ}) | S_C_VCCQ | 1 | R | [219] | 07h | |
| Production state awareness timeout | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | R | [218] | 14h | |
| Sleep/awake timeout | S_A_TIMEOUT | 1 | R | [217] | 12h | |
| Sleep notification time | SLEEP_NOTIFICATION_TIME | 1 | R | [216] | 0Fh | |
| Sector count | SEC_COUNT | 16GB | 4 | R | [215:212] | 01B80000h |
| | | 32GB | 4 | R | [215:212] | 03700000h |
| | | 64GB | 4 | R | [215:212] | 06E40000h |
| Reserved | – | 1 | – | [211] | – | |
| Minimum write performance for 8-bit at 52 MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 08h | |
| Minimum read performance for 8-bit at 52 MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 08h | |
| Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 08h | |
| Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 08h | |
| Minimum write performance for 4-bit at 26 MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 08h | |
| Minimum read performance for 4-bit at 26 MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 08h | |
| Reserved | – | 1 | – | [204] | – | |
| Power class for 26 MHz at 3.6V | PWR_CL_26_360 | 1 | R | [203] | 00h | |
| Power class for 52 MHz at 3.6V | PWR_CL_52_360 | 1 | R | [202] | 00h | |
| Power class for 26 MHz at 1.95V | PWR_CL_26_195 | 1 | R | [201] | 00h | |
| Power class for 52 MHz at 1.95V | PWR_CL_52_195 | 1 | R | [200] | 00h | |
| Partition switching timing | PARTITION_SWITCH_TIME | 1 | R | [199] | 03h | |
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | 1 | R | [198] | 0Ah | |
| I/O driver strength | DRIVER_STRENGTH | 1 | R | [197] | 1Fh | |
| Card type | CARD_TYPE | 1 | R | [196] | 57h | |
| Reserved | – | 1 | – | [195] | – | |
| CSD structure version | CSD_STRUCTURE | 1 | R | [194] | 02h | |
| Reserved | – | 1 | – | [193] | – | |
| Extended CSD revision | EXT_CSD_REV | 1 | R | [192] | 07h | |
| Modes Segment | | | | | | |
| Command set | CMD_SET | 1 | R/W/E_P | [191] | 00h | |


Table 8: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECS1.7D Value |
|---|----------------------|--------------|-----------------------------|------------|---------------|
| Reserved | – | 1 | – | [190] | – |
| Command set revision | CMD_SET_REV | 1 | R | [189] | 00h |
| Reserved | – | 1 | – | [188] | – |
| Power class | POWER_CLASS | 1 | R/W/E_P | [187] | 00h |
| Reserved | – | 1 | – | [186] | – |
| High-speed interface timing | HS_TIMING | 1 | R/W/E_P | [185] | 00h |
| Reserved | – | 1 | – | [184] | – |
| Bus width mode | BUS_WIDTH | 1 | W/E_P | [183] | 00h |
| Reserved | – | 1 | – | [182] | – |
| Erased memory content | ERASED_MEM_CONT | 1 | R | [181] | 00h |
| Reserved | – | 1 | – | [180] | – |
| Partition configuration | PARTITION_CONFIG | 1 | R/W/E, R/W/E_P | [179] | 00h |
| Boot configuration protection | BOOT_CONFIG_PROT | 1 | R/W, R/W/C_P | [178] | 00h |
| Boot bus width | BOOT_BUS_WIDTH | 1 | R/W/E | [177] | 00h |
| Reserved | – | 1 | – | [176] | – |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W/E_P | [175] | 00h |
| Boot write protection status registers | BOOT_WP_STATUS | 1 | R | [174] | 00h |
| Boot area write protection register | BOOT_WP | 1 | R/W, R/W/C_P | [173] | 00h |
| Reserved | – | 1 | – | [172] | – |
| User write protection register | USER_WP | 1 | R/W, R/W/C_P, R/W/E_P | [171] | 00h |
| Reserved | – | 1 | – | [170] | – |
| Firmware configuration | FW_CONFIG | 1 | R/W | [169] | 00h |
| RPMB size | RPMB_SIZE_MULT | 1 | R | [168] | 01h |
| Write reliability setting register ⁴ | WR_REL_SET | 1 | R/W | [167] | 1Fh |
| Write reliability parameter register | WR_REL_PARAM | 1 | R | [166] | 15h |
| SANITIZE START operation | SANITIZE_START | 1 | W/E_P | [165] | 00h |
| Manually start background operations | BKOPS_START | 1 | W/E_P | [164] | 00h |
| Enable background operations handshake | BKOPS_EN | 1 | R/W | [163] | 00h |
| Hardware reset function | RST_n_FUNCTION | 1 | R/W | [162] | 00h |
| HPI management | HPI_MGMT | 1 | R/W/E_P | [161] | 00h |
| Partitioning support | PARTITIONING_SUPPORT | 1 | R | [160] | 07h |


Table 8: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECS1.7D Value | |
|--|-----------------------------|--------------|------------------------|------------|---------------|---------|
| Maximum enhanced area size | MAX_ENH_SIZE_MULT | 16GB | 3 | R | [159:157] | 000370h |
| | | 32GB | 3 | R | [159:157] | 0006E0h |
| | | 64GB | 3 | R | [159:157] | 000DC8h |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | [156] | 00h | |
| Partitioning setting | PARTITION_SETTING_COMPLETED | 1 | R/W | [155] | 00h | |
| General-purpose partition size | GP_SIZE_MULT_GP3 | 12 | R/W | [154:152] | 000000h | |
| | GP_SIZE_MULT_GP2 | | | [151:149] | 000000h | |
| | GP_SIZE_MULT_GP1 | | | [148:146] | 000000h | |
| | GP_SIZE_MULT_GP0 | | | [145:143] | 000000h | |
| Enhanced user data area size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 000000h | |
| Enhanced user data start address | ENH_START_ADDR | 4 | R/W | [139:136] | 00000000h | |
| Reserved | – | 1 | – | [135] | – | |
| Bad block management mode | SEC_BAD_BLK_MGMNT | 1 | R/W | [134] | 00h | |
| Production state awareness | PRODUCTION_STATE_AWARENESS | 1 | R/W/E | [133] | 00h | |
| Package case temperature is controlled | TCASE_SUPPORT | 1 | W/E_P | [132] | 00h | |
| Periodic wake-up | PERIODIC_WAKEUP | 1 | R/W/E | [131] | 00h | |
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | R | [130] | 01h | |
| Reserved | – | 2 | – | [129:128] | – | |
| Vendor specific fields | VENDOR_SPECIFIC_FIELD | 64 | <vendor specific> | [127:64] | – | |
| Native sector size | NATIVE_SECTOR_SIZE | 1 | R | [63] | 00h | |
| Sector size emulation | USE_NATIVE_SECTOR | 1 | R/W | [62] | 00h | |
| Sector size | DATA_SECTOR_SIZE | 1 | R | [61] | 00h | |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU | 1 | R | [60] | 00h | |
| Class 6 commands control | CLASS_6_CTRL | 1 | R/W/E_P | [59] | 00h | |
| Number of addressed group to be released | DYNCAP_NEEDED | 1 | R | [58] | 00h | |
| Exception events control | EXCEPTION_EVENTS_CTRL | 2 | R/W/E_P | [57:56] | 0000h | |
| Exception events status | EXCEPTION_EVENTS_STATUS | 2 | R | [55:54] | 0000h | |
| Extended partitions attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | R/W | [53:52] | 0000h | |
| Context configuration | CONTEXT_CONF | 15 | R/W/E_P | [51:37] | 00h | |
| Packed command status | PACKED_COMMAND_STATUS | 1 | R | [36] | 00h | |
| Packed command failure index | PACKED_FAILURE_INDEX | 1 | R | [35] | 00h | |
| Power-off notification | POWER_OFF_NOTIFICATION | 1 | R/W/E_P | [34] | 00h | |
| Control to turn the cache on/off | CACHE_CTRL | 1 | R/W/E_P | [33] | 00h | |


Table 8: ECSD Register Field Parameters (Continued)

| Name | Field | Size (Bytes) | Cell Type ¹ | ECSD Bytes | ECS1.7D Value | |
|------------------------------------|------------------------------------|--------------|------------------------|------------|---------------|-----------|
| Flushing of the cache | FLUSH_CACHE | 1 | W/E_P | [32] | 00h | |
| Reserved | – | 1 | – | [31] | – | |
| Mode configuration | MODE_CONFIG | 1 | R/W/E_P | [30] | 00h | |
| Mode operation codes | MODE_OPERATION_CODES | 1 | W/E_P | [29] | 00h | |
| Reserved | – | 2 | – | [28:27] | – | |
| Field firmware update status | FFU_STATUS | 1 | R | [26] | 00h | |
| Pre-loading data size | PRE_LOADING_DATA_SIZE4 | 4 | R/W/E_P | [25:22] | 00h | |
| Maximum pre-loading data size | MAX_PRE_LOADING_DATA_SIZE | 16GB | 4 | R | [21:18] | 00DC0000h |
| | | 32GB | 4 | R | [21:18] | 01B80000h |
| | | 64GB | 4 | R | [21:18] | 03720000h |
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1 | R/W/E, R | [17] | 01h | |
| Secure removal type | SECURE_REMOVAL_TYPE | 1 | R/W/E, R | [16] | 00h | |
| Reserved | – | 16 | – | [15:0] | – | |

- Notes:
1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable;
R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable.
 2. Reserved bits should be read as 0.
 3. Firmware version not populated here for more general document application. For current firmware version, consult Micron local support.
 4. Micron has tested power failure under best-application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition. Micron set this register during factory test and used the one-time programming option.



DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device and its interface voltage; V_{CCQ} is used for the controller and the e.MMC interface voltage.

Figure 9: Device Power Diagram

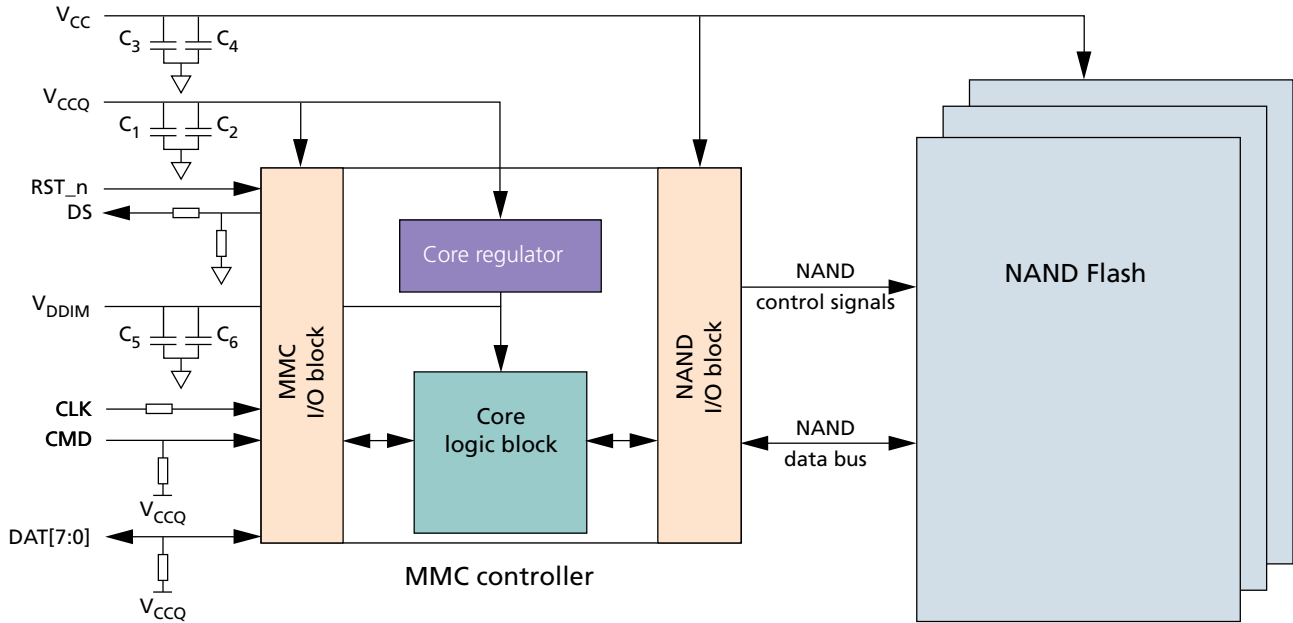


Table 9: Absolute Maximum Ratings

| Parameters | Symbol | Min | Max | Unit |
|---------------------|-----------|------|-----|------|
| Voltage input | V_{IN} | -0.6 | 4.6 | V |
| V_{CC} supply | V_{CC} | -0.6 | 4.6 | V |
| V_{CCQ} supply | V_{CCQ} | -0.6 | 4.6 | V |
| Storage temperature | T_{STG} | -40 | 85 | °C |

Note: 1. Voltage on any pin relative to V_{SS} .


Table 10: Capacitor and Resistance Specifications

| Parameter | Symbol | Min | Max | Typ | Units | Notes |
|---|---------|-----|------|-----|-------|-------|
| Pull-up resistance: CMD | R_CMD | 4.7 | 50 | 10 | kΩ | 1 |
| Pull-up resistance: DAT[7:0] | R_DAT | 10 | 50 | 50 | kΩ | 1 |
| Pull-up resistance: RST_n | R_RST_n | 4.7 | 50 | 50 | kΩ | 2 |
| CLK/CMD/DS/DAT[7:0] impedance | | 45 | 55 | 50 | Ω | 3 |
| Serial resistance on CLK | SR_CLK | 0 | 47 | 22 | Ω | |
| Serial resistance on DS | SR_DS | 0 | 47 | 22 | Ω | 4 |
| Pull-down resistance: DS | R_DS | 10 | 100 | – | kΩ | |
| V _{CCQ} capacitor | C1 | 2.2 | 4.7 | 2.2 | μF | 5 |
| | C2 | 0.1 | 0.22 | 0.1 | | |
| V _{CC} capacitor | C3 | 2.2 | 4.7 | 2.2 | μF | 6 |
| | C4 | 0.1 | 0.22 | 0.1 | | |
| V _{DDIM} capacitor (C _{reg}) | C5 | 1 | 4.7 | 1 | μF | 7 |
| | C6 | 0.1 | 0.1 | 0.1 | | |

- Notes:
- Used to prevent bus floating.
 - If host does not use H/W RESET (RST_n), pull-up resistance is not needed on RST_n line (Extended_CSD[162] = 00h).
 - Impedance match.
 - Recommended in order to compensate eventual impedance mismatch on the PCB.
 - The coupling capacitor should be connected with V_{CCQ} and V_{SSQ} as closely as possible.
 - The coupling capacitor should be connected with V_{CC} and V_{SS} as closely as possible.
 - The coupling capacitor should be connected with V_{DDIM} and V_{SS} as closely as possible.



Revision History

Rev. I – 08/18

- Added Important Notes and Warnings section for further clarification aligning to industry standards
- Corrected typo of package height tolerance in Package Dimensions for Package Codes: JP, CN
- Updated ECSD Register Field Parameters table

Rev. H – 10/17

- New MPNs added

Rev. G – 05/16

- Temperature and Data Strobe clarifications

Rev. F – 03/16

- Status update for 64GB device

Rev. E – 07/15

- Combined 153-ball and 100-ball packages
- Updated registers and performance data

Rev. D – 06/14

- Made package code and part number changes: MTFC16GAKAECN-4M IT, MTFC32GAKAECN-4M IT, and MTFC64GAKAEEY-4M IT

Rev. C – 06/14

- Updated the CID, CSD, and ECSD values
- Added new part numbers to the list on the first page

Rev. B – 04/14

- Added the "Absolute Maximum Ratings" table to the DC Electrical Specifications section

Rev. A – 01/14

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.