

AQRate 5 Gbps and 2.5 Gbps Modes Overview

AQrate™ NBASE-T PHY Transceiver

1. Introduction

The Aquantia 28nm AQrate PHY is a 10GBASE-T PHY transceiver that is compliant to the IEEE 802.3 100BASE-TX, 1000BASE-T, and 10GBASE-T specifications for line-rate operation of 100 Mbps, 1 Gbps, and 10 Gbps respectively. In addition to the IEEE 802.3 standard specifications, the PHY also support IEEE 802.3bz draft specifications for 2.5 Gbps and 5 Gbps line-rates.

The line side operation for the 2.5 Gbps and 5 Gbps modes utilize protocol that complies with the NBASE-T Alliance specification for NBASE-T PHY and IEEE 802.3bz draft specifications. The system side operation for the 2.5 Gbps and 5 Gbps modes run on standard SerDes interfaces and protocols.

This document provides an overview of the AQrate PHY's 2.5 Gbps and 5 Gbps modes of operation.

2. Line-Side Interface

The line-side interface for the PHY is identical to other BASE-T MDI interface with 4 pairs of differential signal to be connected to an RJ-45 connector for data transmission over a compatible twisted-pair copper cable, such as Cat5e, Cat6, and Cat6a UTP cables.

The second generation of Aquantia's AQrate (AQR-Gen2) PHY device family consists of 6 devices in all, including three single-port (AQR107, AQR108, AQR109) and three quad-port PHYs (AQR407, AQR408, AQR409). All devices in each family are pin-compatible allowing a single design to be leveraged across multiple applications. The following operational data speeds are supported in each series:

- AQRxx7 100M, 1G, 2.5G, 5G, 10G
- AQRxx8 100M, 1G, 2.5G, 5G
- AQRxx9 100M, 1G, 2.5G

3. System-side Interface

The AQR-Gen2 PHY device family supports the following SerDes modes.

Table 1 – System Interface SerDes Modes

Speed	USX	KR	XFI	2500BASE-X	SGMII	1000BASE-X
10 Gbps	x	x	x			
5 Gbps	x	+	+			
2.5 Gbps	x	+	+	x		
1 Gbps	x	+	+	+	x	x
100 Mbps	x	+	+	+	x	

The options marked with 'x' or light green color cells are native rates. The options marked with '+' or light orange cells operate within IEEE 802.3x Flow-Control and port-based pause frame rate adaptation mode over one of the native SerDes modes.

3.1 Interoperability

The PHY can interoperate, in any of the supported speeds, with any MAC IC that supports the SerDes modes listed in Table 1 and is capable of processing and responding to Pause frame request.

3.2 Rate Adaptation

When the PHY is operating in the AQrate mode, for any non-10 Gbps speed over XFI including 1 Gbps and 100 Mbps, the SerDes interface electrically operates in its native mode at 10 Gbps rate. Similarly, when operating in 2500Base-X mode, the line-side can operate in 1G or 100M rate while the system interface remains in 2500Base-X.

The traffic management can be done at the system level by rate limiting the traffic so that the MAC does not transmit packets at rates that exceed the established line rate. For example, if the line rate is at 5 Gbps, the total traffic rate from the MAC to the PHY should be limited to a maximum of 50% payload. Appropriate rate limiting should be applied for other non-native speeds.

The other method of AQrate mode rate adaptation is through the IEEE 802.3x Flow Control and PHY's port-based pause (XON/XOFF) frame generation. The MAC interface has to be enabled to respond to the Pause frame request from the PHY. As the MAC sends packets to the PHY, the FIFO buffer at the PHY's SerDes RX starts to fill up. If the buffer level crosses the XOFF threshold, the PHY sends pause requests to the MAC and MAC has to respond by suppressing packet transmission until the requested wait time (Pause Quanta) has expired and no XOFF Pause frames are received by the MAC.

The XON-XOFF thresholds, Pause quanta, and time delay between PHY pause frames are user programmable.

The default configuration for AQrate mode rate adaptation is through Pause frame mechanism.

4. History

Rev.	Date	Description
1.0	4/1/2016	First release

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