QorIQ LX2160A Reference Design Board Reference Manual

Supports LX2160ARDB Revision B

Document Number: LX2160ARDBRM
Rev. 0, 09/2018

Contents

Section number **Title** **Page**

Chapter 1
LX2160ARDB Overview

Chapter 2
LX2160ARDB Functional Description

Chapter 3
Qixis Programming Model

Chapter 1
LX2160ARDB Overview

The QorIQ® LX2160A reference design board (RDB) provides a comprehensive platform that enables design and evaluation of the QorIQ LX2160A processor. The LX2160ARDB comes pre-loaded with a board support package (BSP) based on a standard Linux kernel. The board comes in a 1U rackmount chassis form factor. It is lead-free and RoHS-compliant.

The board:

- Enables network intelligence with the next generation Datapath (DPPA2) which provides differentiated offload and a rich set of input/output, including 10/25/40 Gigabit Ethernet and PCIe Gen 4
- Delivers unprecedented efficiency and new virtualized networks
- Supports designs in 5G packet processing, network function virtualization, storage controller, white box switching, network interface cards, and mobile edge computing
- Supports all three LX2 family members (16-core LX2160A, 12-core LX2120A, and 8-core LX2080A)

This document provides detailed information about LX2160ARDB interfaces, power supplies, clocks, DIP switches, LEDs, and CPLD system controller.

1.1 Acronyms and abbreviations

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1-1. Acronyms and abbreviations

Term	Description
ATX	Advanced Technology eXtended
CAN	Controller area network
CCI	Cache coherency interconnect
CCS	CodeWarrior connection server
CPLD	Complex programmable logic device

Table continues on the next page...

Table 1-1. Acronyms and abbreviations (continued)

Term	Description
CTS	Clear to send
DCM	Development system control monitor
DDR SDRAM	Double data rate synchronous dynamic random-access memory
DIMM	Dual inline memory module
DIP	Dual inline package
DPAA	Data path acceleration architecture
DUT	Device under test
EC	Ethernet controller
ECC	Error correcting code
ECID	Electronic chip identification
EDINK	e500 core demonstrative interactive nanokernel
EMI	Ethernet management interface
eMMC	Embedded multimedia card
eSDHC	Enhanced secure digital host controller
FET	Field-effect transistor
FlexSPI	Flexible serial peripheral interface
FPGA	Field-programmable gate array
GbE	Gigabit Ethernet
GPIO	General purpose input/output
HDLC	High-level data link control
HSSI	High-speed serial interface
I2C	Inter-integrated circuit
JTAG	Joint Test Action Group (IEEE® Standard 1149.1™)
LOS	Loss of signal
MDIO	Management data input/output
OCM	Offline configuration manager
OTG	On-The-Go
PBL	Pre-boot loader
PLL	Phase-locked loop
POR	Power-on reset
PSU	Power supply unit
PTP	Precision time protocol
PWM	Pulse width modulation
QSPI	Quad serial peripheral interface
RCW	Reset configuration word
RDIMM	Registered dual inline memory module
RTC	Real time clock
RTS	Request to send
SATA	Serial advanced technology attachment

Table continues on the next page...

Table 1-1. Acronyms and abbreviations (continued)

Term	Description
SDRAM	Synchronous dynamic random-access memory
SerDes	Serializer/deserializer
SGMII	Serial gigabit media independent interface
SPD	Serial presence detect
SPI	Serial peripheral interface
SS	Spread spectrum
SSC	Spread spectrum clocking
TCXO	Temperature compensated crystal (Xtal) oscillator
UART	Universal asynchronous receiver/transmitter
UDIMM	Unbuffered dual inline memory module
UFT	Universal frequency translator
USB	Universal serial bus
USXGMII	Universal serial 10 gigabit media independent interface
XGT	10GBase-T
XSPI	Octal serial peripheral interface

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on the LX2160ARDB.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 1-2. Related documentation

Document	Description	Location / how to access
QorIQ LX2160A Reference Design Board Getting Started Guide	Explains the LX2160ARDB settings and physical connections needed to boot the board	QorIQ LX2160A Reference Design Board Getting Started Guide
QorIQ LX2160A Reference Design Board Errata	Describes known errata and workarounds for the LX2160ARDB	QorIQ LX2160A Reference Design Board Errata
QorIQ LX2160A Product Brief	Provides a brief overview of the LX2160A processor	QorIQ LX2160A Product Brief
QorIQ LX2160A Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	Contact FAE / sales representative
QorIQ LX2160A Family Reference Manual	Provides a detailed description about the LX2160A QorIQ multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information	Contact FAE / sales representative

Table continues on the next page...

Table 1-2. Related documentation (continued)

Document	Description	Location / how to access
QorIQ LX2160A Chip Errata	Lists the details of all known silicon errata for the LX2160A	Contact FAE / sales representative
QorIQ LX2160A Design Checklist, AN5407	This document provides recommendations for new designs based on the LX2160A. This document can also be used to debug newly designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.	Contact FAE / sales representative
Layerscape LX2160A BSP	This document explains how to use the QorIQ LX2160A BSP, which is a Linux-based development kit, to evaluate and explore the features of the LX2160A SoC.	Contact FAE / sales representative
CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual	This manual explains how to use the CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA product.	CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual
CodeWarrior TAP Probe User Guide	Provides details of CodeWarrior® TAP, which enables target system debugging through a standard debug port (usually JTAG) while connected to a developer workstation through Ethernet or USB	CodeWarrior TAP Probe User Guide

1.3 Block diagrams

This section provides block diagrams showing major functional units of the LX2160A processor and LX2160ARDB.

The figure below shows the LX2160A processor block diagram.

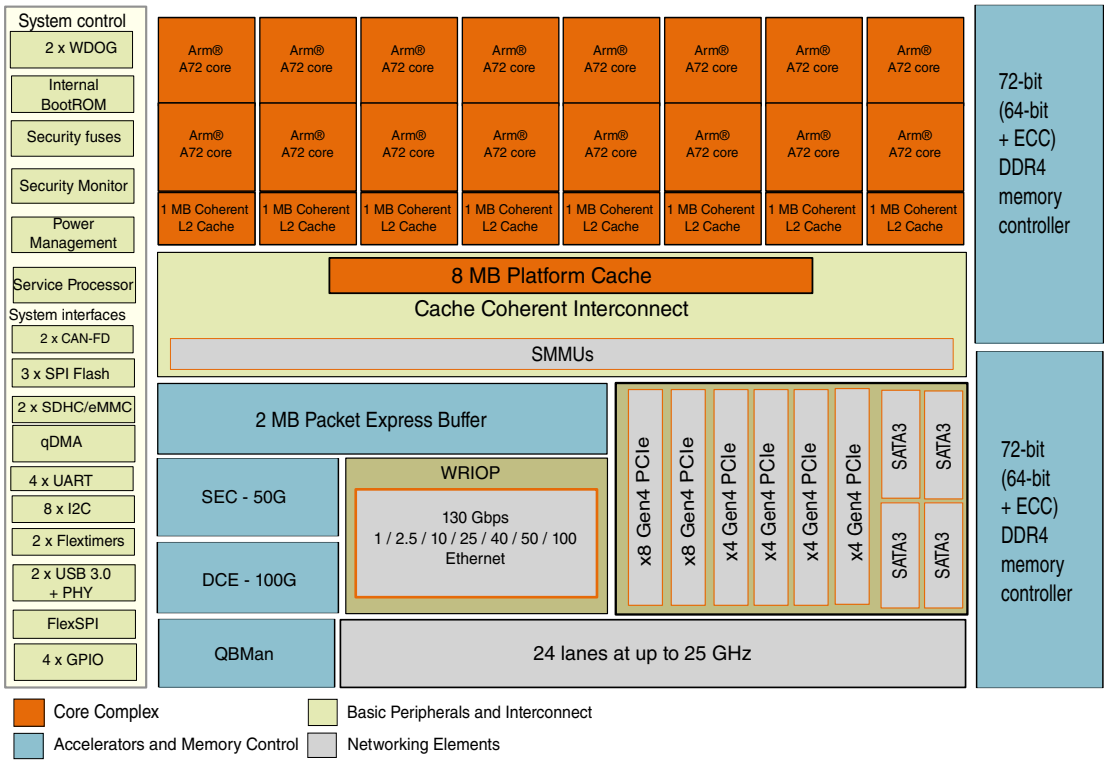


Figure 1-1. LX2160A block diagram

The figure below shows the LX2160ARDB block diagram.

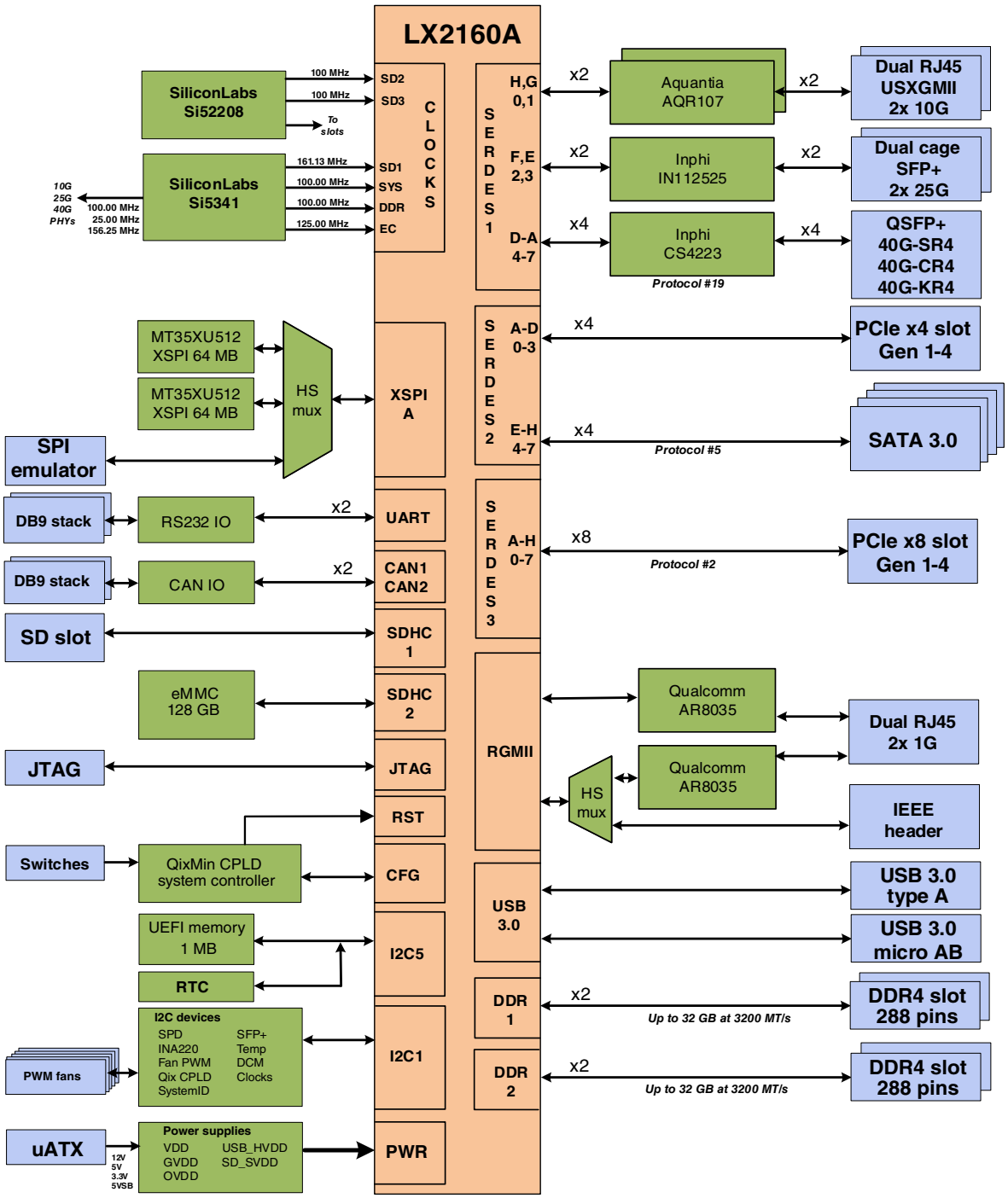


Figure 1-2. LX2160ARDB block diagram

1.4 Board features

The table below lists the features of the LX2160ARDB.

Table 1-3. LX2160ARDB features

LX2160ARDB feature	Specification	Description
Processor	16-core processor	16 Arm® Cortex®-A72 processor cores based on 32-/64-bit Armv8 architecture, supporting speeds of up to 2.2 GHz **NOTE:** For more details on the LX2160A processor, see *QorIQ LX2160A Family Reference Manual*.
DDR memory	Two 72-bit DDR4 ports (64-bit data, 8-bit ECC)	Each DDR4 port supports: • Two 288-pin DIMM connectors • Four chip selects • Single-/dual-rank, unbuffered/registered DDR4 memory modules • 64-bit data bus • x4, x8, and x16 data width memory • Data rates of up to 3.2 GigaTransfers/second (GT/s) • Double-bit error detection and single-bit error correction ECC (8-bit check word across 64-bit data)

High-speed serial ports (SerDes)	Three SerDes controllers (24 lanes)	• SerDes1:
		  • Lanes 0-1: Supports two 10 GbE RJ45 USXGMII connectors, each connected through an Aquantia AQR107 PHY
		  • Lanes 2-3: Supports two 25 GbE SFP+ modules, connected through an Inphi IN112525 PHY
		  • Lanes 4-7: Supports one 40 GbE (40G-SR4, 40G-CR4, or 40G-KR4) QSFP+ module, connected through an Inphi CS4223 PHY
		• SerDes2:
		  • Lanes 0-3: Supports one PCIe x4 (Gen 1/2/3/4) connector
		  • Lanes 4-7: Supports four SATA 3.0 connectors
		• SerDes3:
		  • Lanes 0-7: Supports one PCIe x8 (Gen 1/2/3/4) connector
		• Each SerDes lane supports speeds of up to 25 GHz

eSDHC	eSDHC1	Supports a secure digital (SD) connector (J42) for connecting an SD card
	eSDHC2	Supports 128 GB Micron MTFC128GAJAECE-IT embedded multimedia card (eMMC), supporting HS-400 high-speed transfer mode
Octal SPI (XSPI)	One XSPI controller (XSPI_A)	• Supports two 64 MB onboard octal SPI flash memories • Supports a QSPI emulator for offboard QSPI emulation
I2C	Six I2C controllers (I2C1, I2C2, I2C3, I2C4, I2C5, and I2C6)	• Most system devices (other than UEFI) are accessed via I2C1, which is multiplexed to isolate address conflicts and reduce capacitive load • I2C1 is translated to 3V3_SB, allowing programming access to devices, such as power controllers, clocks, and memories, while the system is off • I2C2 is only used for SDHC1_CD_B and SDHC1_WP • I2C3 is only used for CAN1 input/output • I2C4 is only used for CAN2 input/output • I2C5 is used for UEFI support (memory and RTC) • I2C6 is used for optional AQR107 PHY access
Serial ports	Two UART ports (UART1 and UART2)	A dual-stack DB9 male connector providing two UART connectors, each connected through an RS-232 transceiver
USB 3.0	Two high-speed USB 3.0 ports with integrated PHYs	• Supports super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations • USB#1 3.0 port is connected to a Type A host connector • USB#2 3.0 port is configured as On-The-Go (OTG) with a Micro-AB connector

Table continues on the next page...

Table 1-3. LX2160ARDB features (continued)

LX2160ARDB feature	Specification	Description
Ethernet	Two tri-speed RGMII interfaces	• 10 Mb / 100 Mb / 1 Gb Ethernet is supported • An RJ45 connector with link and activity status is used with each RGMII interface • IEEE 1588™ precision time protocol (PTP) is supported through an onboard header (J29)
Clocks	System clock (SYSCLK) and DDR clock (DDRCLK)	• 100 MHz differential clock to DIFF_SYSCLK • 100 MHz single-ended clock to DDRCLK
	SerDes clocks	• 161.1328125 MHz clock to SerDes1 PLL 1 and PLL 2 • 100 MHz clock to SerDes2 PLL 1 and PLL 2 • 100 MHz clock to SerDes3 PLL 1 and PLL 2 • 100 MHz clock to AQR107 10 GbE PHY 1 and 2 • 25 MHz clock to IN112525 25 GbE PHY • 156.25 MHz clock to CS4223 40 GbE PHY • 100 MHz clock to x4 and x8 PCIe slots
	Ethernet clocks	125 MHz clocks to Ethernet controllers and IEEE 1588 port
Power supplies		• 12 V, 5 V, 3.3 V, and 5 V (standby) ATX power supplies • 0.8 V (VDD) for the LX2160A core • 1.2 V (G1VDD and G2VDD) for DDR4 • 0.92 V (SD_SVDD) for SerDes cores • 1.8 V (SD_OVDD) for SerDes I/O drivers • 0.9 V (SD_AVDD) for SerDes PLLs • 1.8 V (OVDD) for general I/O • 1.8 V (standby) and 3.3 V (standby) for CPLD core and I/O • 0.8 V for USB_SVDD and USB_SDVDD • 3.3 V for USB_HVDD • 0.8 V (TA_BB_VDD) for the LX2160A secure monitor • 1.8 V for TA_PROG_SFP and PROG_MTR
Debug features		Arm Cortex 10-pin JTAG connector
Package		• Package type is 40 mm x 40 mm, 1517 Flip Chip, Plastic-ball, Grid Array (FC-PBGA) • Socket and heat sink are included

System logic	CPLD	• Manages the following:
		  • System power sequencing
		  • System reset sequencing
		  • System and SerDes clock speed selections
		  • SoC POR configuration at reset
		• Implements registers for system control and monitoring
		• General fault monitoring and logging

1.5 Board top view

The figure below shows the top-side view of the LX2160ARDB.

Figure 1-3. LX2160ARDB top view

Chapter 2
LX2160ARDB Functional Description

The LX2160ARDB architecture is primarily determined by the LX2160A processor, with the need to evaluate the LX2160A processor features and to deliver an easily usable, off-the-shelf software development platform.

This chapter explains all major functional components of the LX2160ARDB. The chapter is divided into the following sections:

- Power supplies
- Clocks
- DDR interface
- SerDes interface
- Ethernet controller interface
- Ethernet management interface
- eSDHC interface
- XSPI interface
- USB interface
- I2C interface
- UART interface
- CAN interface
- JTAG port
- Interrupt controller
- GPIO access
- Temperature measurement
- LEDs
- DIP switches
- System controller

2.1 Power supplies

The LX2160ARDB provides all the voltages necessary for the correct operation of the LX2160A processor, DDR4 UDIMM, PHYs, and numerous other peripherals. All power is derived from an external power supply, which supplies bulk +12 V, +5 V, +3.3 V, as well as +5 V standby power.

The ATX-compatible supply is managed by the system controller CPLD and drives the power supplies shown in the figures below.

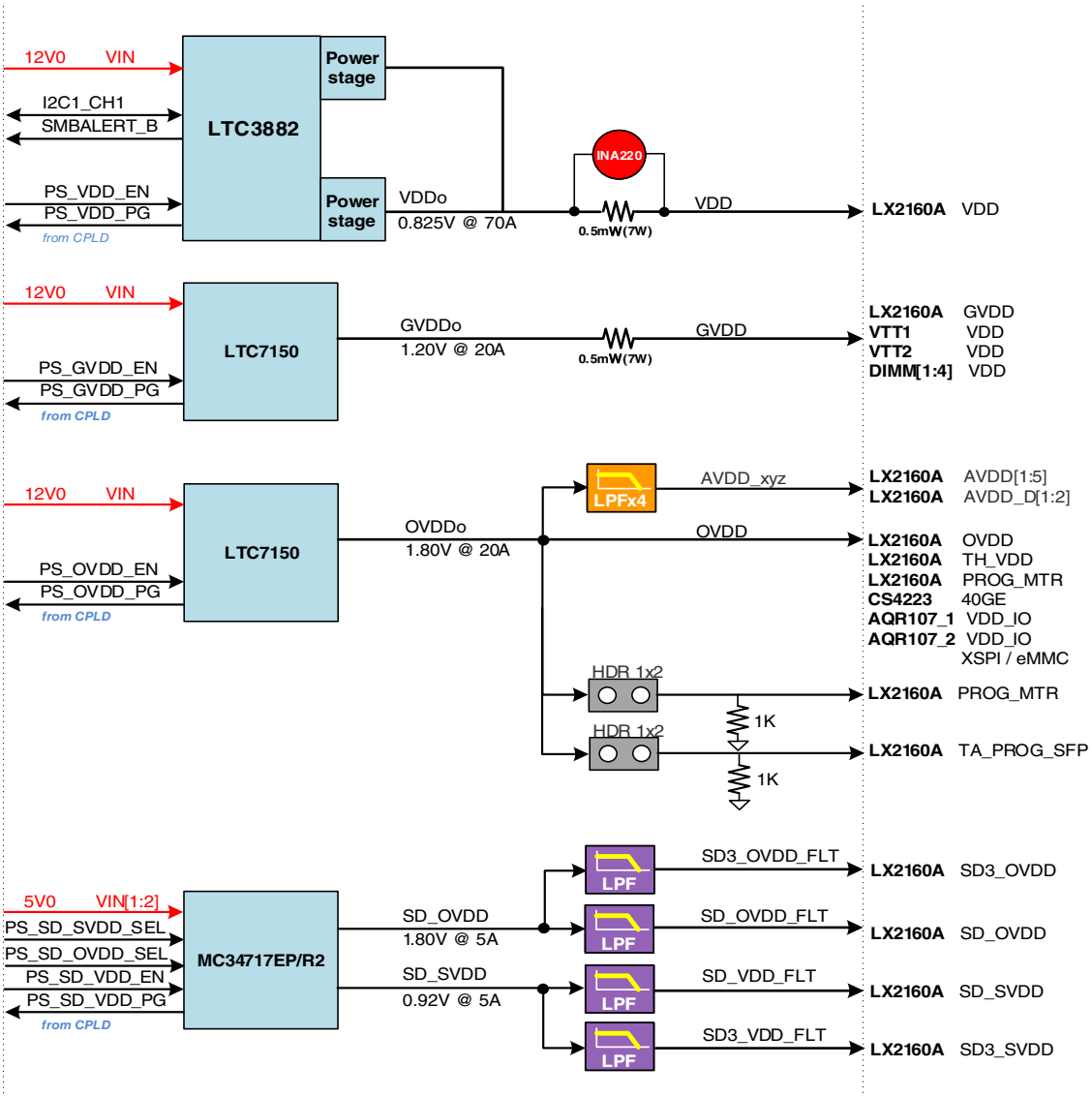


Figure 2-1. Power supplies - Part 1

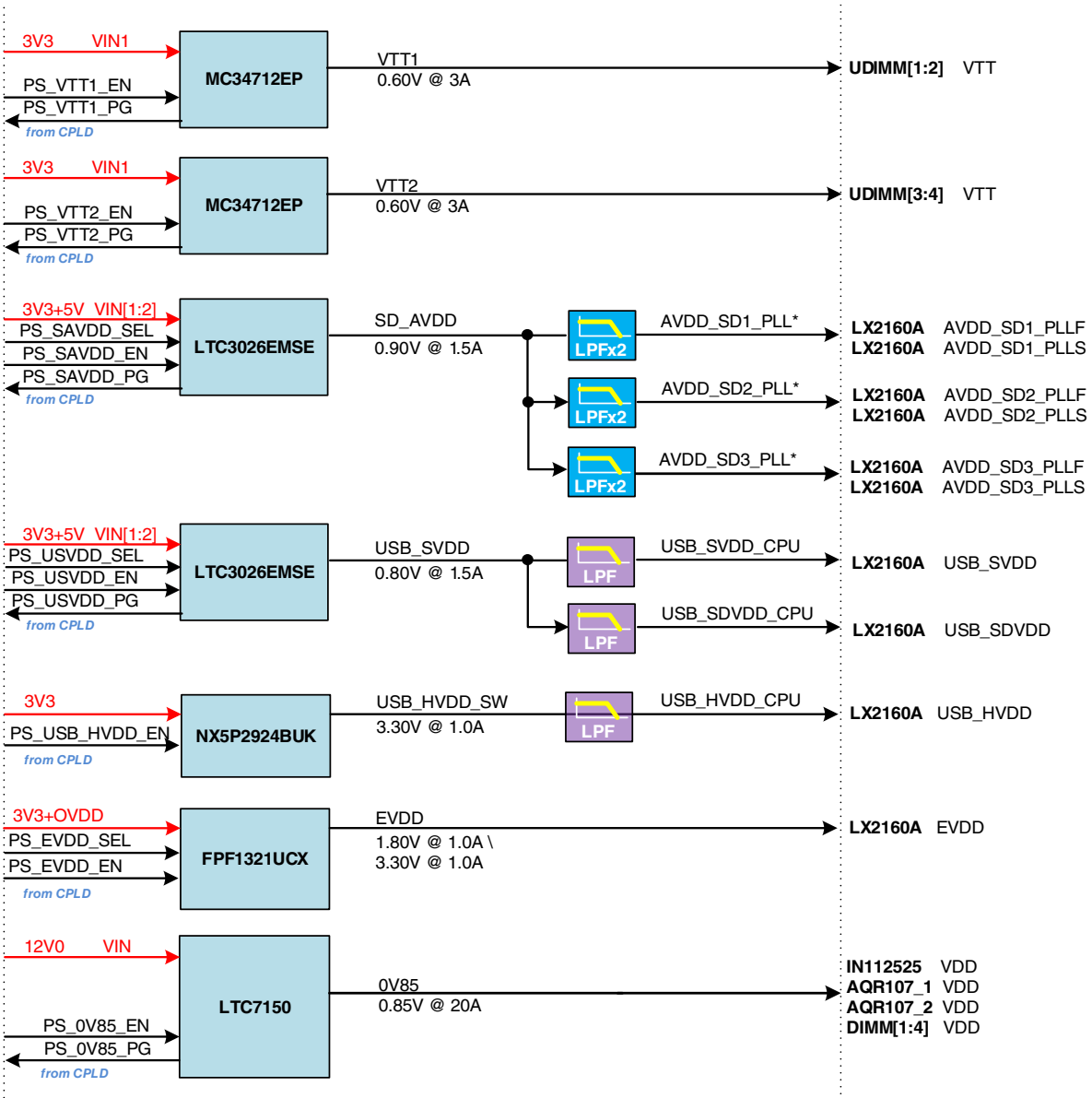


Figure 2-2. Power supplies - Part 2

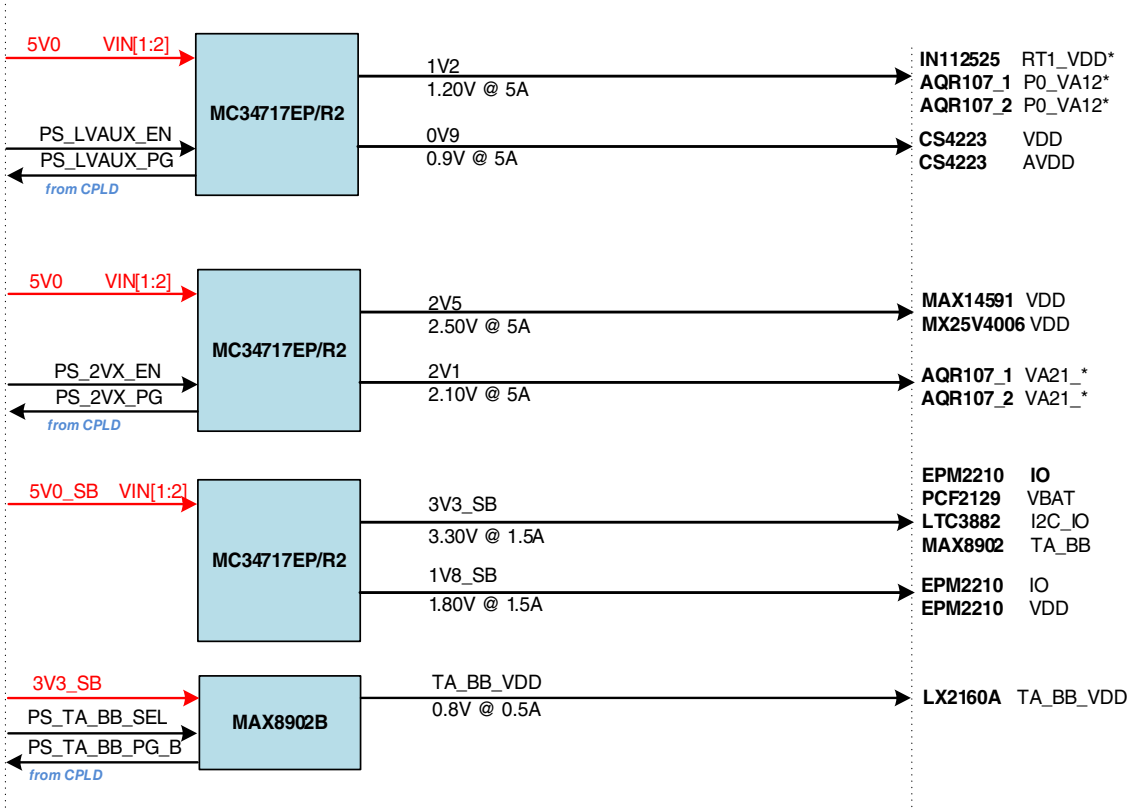


Figure 2-3. Power supplies - Part 3

Note that several power supplies have onboard low-pass filters, to prevent board switching noise from coupling into sensitive analog supplies. The figure below shows the filters used.

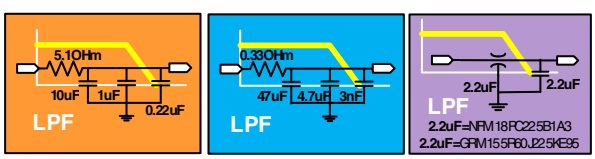


Figure 2-4. Passive low pass filters

2.1.1 Primary power supply

The primary power supply for the LX2160ARDB is an external 300 W ATX12V/ EPS12V power supply. The following tables show its main features.

Table 2-1. Primary power supply

Power supply	Description	
External ATX 12 V power supply	Vin	90 - 264 Vac
	Fin frequency	50 - 60 Hz

Table continues on the next page...

Table 2-1. Primary power supply (continued)

Power supply	Description	
	Iin	< 8.5 A at 100 Vac, 4 A at 240 Vac
	Power good	Power-on delay time of 100 ~ 500 ms
	Operating temperature range	0 ~ 50 °C on full load
	Relative humidity	20~ 80%

Table 2-2. ATX12V/EPS12V power supply characteristics

Group	Outputs					Unit
Voltage	+3.3	+5	+12	-12	+5 (SB)	V
Maximum load	10	14	25	0.3	2.0	A
Minimum load	0.5	1	2	0	0.1	A
Regulation	±5	±5	±5	±10	±5	%
Ripple and noise	60	60	120	120	50	mV
Capacitive loads	10000	10000	10000	330	10000	µF

2.1.2 Secondary power supplies

The table below lists the secondary power supplies for the LX2160ARDB. These supplies are derived from the ATX power supply unit and they are used to power various onboard devices. A few are on all the time, while most others are enabled and disabled in a particular order, as controlled by the CPLD system controller.

Table 2-3. Secondary power supplies

Part identifier	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
U12	LTC3882	Linear Technology	VDD	0.825 V at 70 A with ±3% accuracy	Supplies power to the LX2160A cores
U16	LTC7150	Linear Technology	GVDD	1.2 V at 20 A with ±3% accuracy	Supplies power to the LX2160A DDR controllers, DDR memories, and DDR memory termination power supplies (VTT1 and VTT2)
U15	LTC7150	Linear Technology	OVDD	1.8 V at 20 A with ±3% accuracy	Supplies power to the LX2160A general I/O drivers. OVDD also supplies power to the PROG_MTR and TA_PROG_SFP pins, through J8 and J9 jumpers, respectively,

Table continues on the next page...

Table 2-3. Secondary power supplies (continued)

Part identifier	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
					which are normally open (unmounted). **NOTE:** Filtered OVDD power is also supplied to the core CPU PLLs (AVDD[1:5] and AVDD_D[1:2]).
U17	MC34717EP/R2	NXP Semiconductors	SD_OVDD	1.8 V at 5 A ±3% accuracy	Supplies power to the LX2160A SerDes I/O drivers
			SD_SVDD	0.92 V at 5 A ±3% accuracy	Supplies power to the LX2160A SerDes cores
U20	MC34712EP	NXP Semiconductors	VTT1	0.6 V at 3 A	Supplies power to the DDR#1 UDIMM memory termination power
U21	MC34712EP	NXP Semiconductors	VTT2	0.6 V at 3 A	Supplies power to the DDR#2 UDIMM memory termination power
U24	LTC3026EMSE	Linear Technology	SD_AVDD	0.9 V at 1.5 A	Supplies power to the LX2160A SerDes PLLs. **NOTE:** Filtered SD_AVDD power is supplied to SerDes1, SerDes2 and SerDes3 PLLs (AVDD_SD[1:3]_PLLF and AVDD_SD[1:3]_PLLS).
U22	LTC3026EMSE	Linear Technology	USB_SVDD	0.8 V at 1.5 A	Supplies power to the LX2160A USB PHY super speed (SS) and high speed (HS) power supplies
U34	NX5P2924BUK	NXP Semiconductors	USB_HVDD_SW	3.3 V at 1 A	Supplies power to the 3.3 V USB PHY HS power supply
U33	FPF1321UCX	ON Semiconductor	EVDD	1.8 V or 3.3 V at 1 A	eSDHC I/O power. **NOTE:** EVDD can change between 1.8 V and 3.3 V on command of the SDHC IP block for certain board configurations. **NOTE:** FPF1321UCX is a power switch, not a power supply.

Table continues on the next page...

Table 2-3. Secondary power supplies (continued)

Part identifier	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
					OVDD is the source of the 1.8 V power.
U29	LTC7150	Linear Technology	0V85	0.85 V at 20 A with ±3% accuracy	Supplies power to the Aquantia AQR107 PHYs, Inphi IN112525 PHY, and DDR memories
U30	MC34717EP/R2	NXP Semiconductors	1V2	1.2 V at 5 A with ±3% accuracy	Supplies power to the Aquantia AQR107 PHYs and Inphi IN112525 PHY
			0V9	0.9 V at 5 A with ±3% accuracy	Supplies power to the Inphi CS4223 PHY
U31	MC34717EP/R2	NXP Semiconductors	2V5	2.5 V at 5 A with ±3% accuracy	Supplies power to DDR4 DIMM connectors
			2V1	2.1 V at 5 A with ±3% accuracy	Supplies power to the Aquantia AQR107 PHYs
U3	MC34717EP/R2	NXP Semiconductors	3V3_SB	3.3 V at 1.5 A	Standby (“hot”) power for the CPLD core
			1V8_SB	1.8 V at 1.5 A	Standby (“hot”) power for the CPLD core and I/O
U27	MAX8902B	Maxim Integrated	TA_BB_VDD	0.8 V at 0.5 A	Supplies power to the LX2160A secure monitor

2.1.3 Power supply sequence

The external ATX power supply provides 5V_SB voltage when connected to an AC power outlet. This is an independent 5V power supply that is always active. This voltage is used to generate the 3V3_SB and 1V8_SB standby power supplies, which are used to power the CPLD.

With power available, CPLD can manage the orderly power-up of the rest of the system on an appropriate event (one of the following):

- The power switch (push button) is pressed
- The SW_AUTO_ON switch (SW4[2]) is set to '1'

On receipt of a power event signal, the CPLD power sequencer block manages the orderly enable of the remaining power supplies, as shown in the figure below.

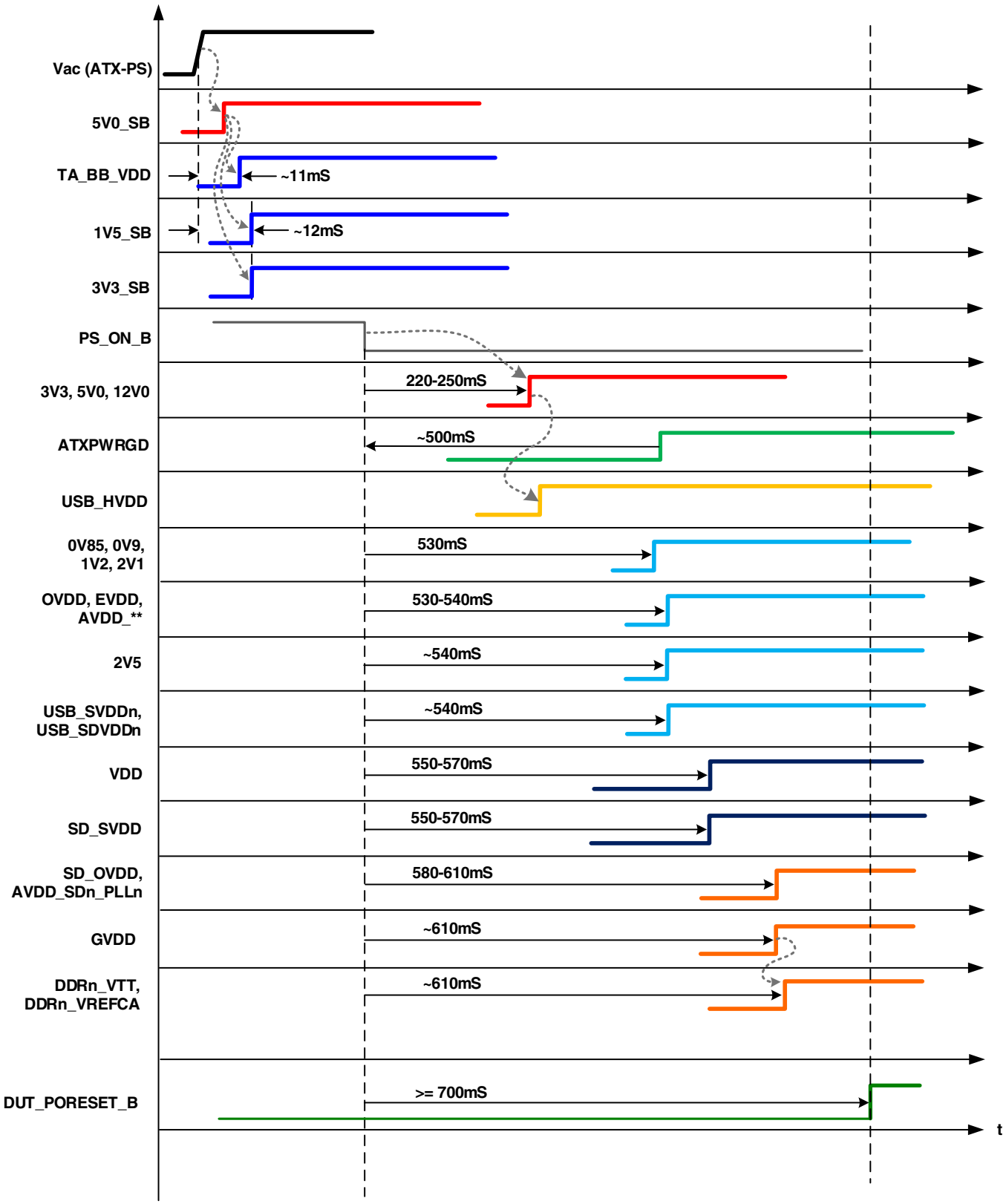


Figure 2-5. Power up voltage sequence

The LX2160ARDB follows the power supply sequencing requirements as detailed in *QorIQ LX2160A Data Sheet*.

2.1.4 Current and power measurement

The LX2160ARDB implements onboard current and power measurements only for the VDD supply. For selected other supplies, monitoring resistors are available. The table below lists all measurable supplies.

Table 2-4. Power monitoring

Power	Measurement device	Shunt resistor value	Notes
VDD	LTC3882	–	Standard PMBus commands, for example, READ_IOUT
	INA220	0.0005	
GVDD	External meter	0.0005	

Power supplies not listed in the above table are considered as low-current/incidental supplies and are not instrumented for power measurement.

2.2 Clocks

The LX2160ARDB provides all the clocks required for the processor and peripheral interfaces. The figure below shows the LX2160ARDB clock architecture.

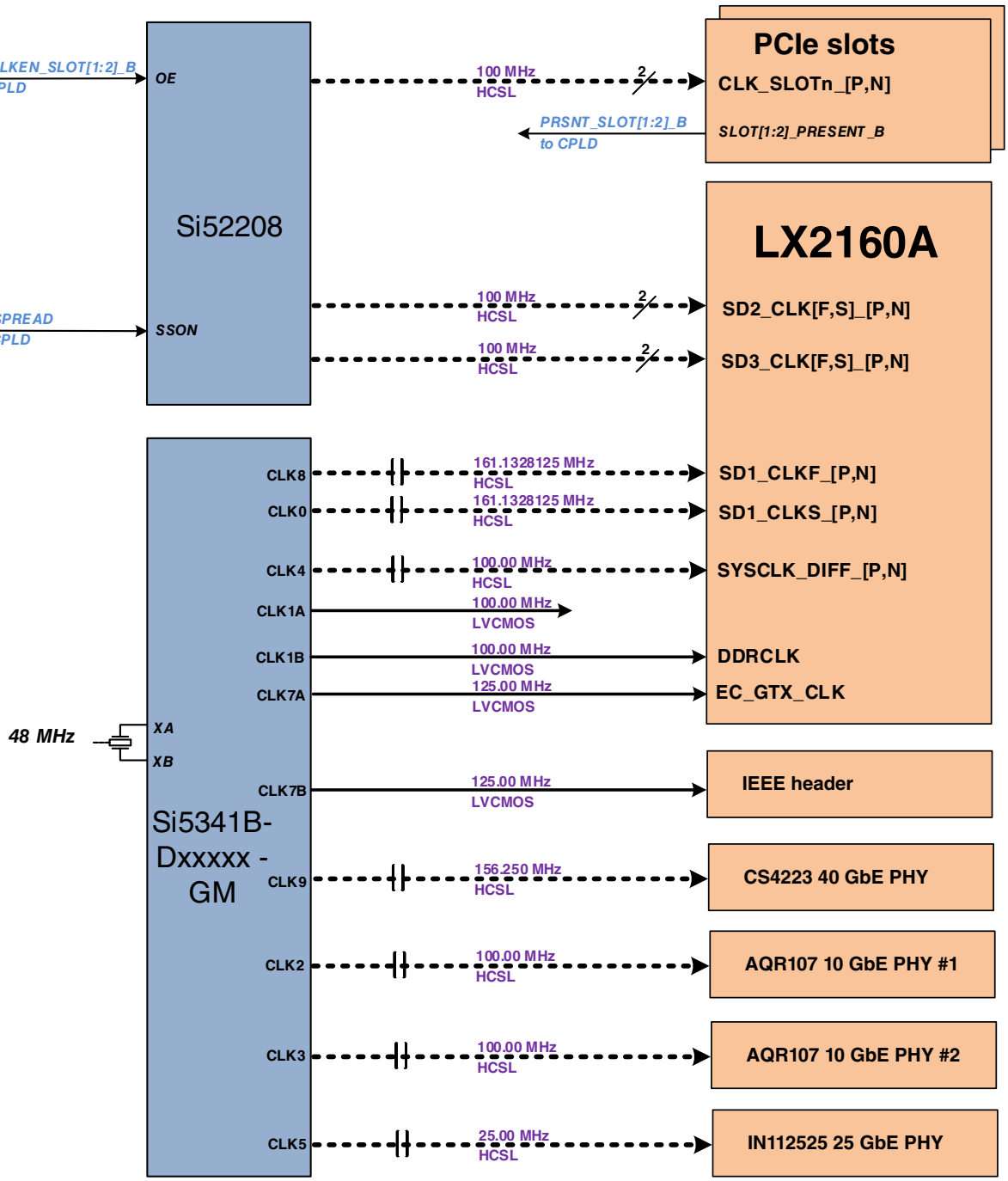


Figure 2-6. LX2160ARDB clock architecture

All the clocks are fixed frequency, and most are produced by the Si5341B or Si52208. The following table summarizes the specifications of each clock and the component that provides it.

Table 2-5. LX2160ARDB clocks

Part identifier	Clock generator	Clock	Specifications	Destination
Y1	Hot-powered crystal oscillator	HOT_CLK	• Frequency: 25 MHz • Output type: CMOS	CPLD
U130	Si5341B-D08333-GM	OUT0: CLK_SD1_S_[P, N]	• Frequency: 161.1328125 MHz • Output type: HCSL • Operating voltage: 1.8 V	SerDes1 controller PLL 2
		OUT1B: DDRCLK_SE	• Frequency: 100 MHz • Output type: LVCMOS • Operating voltage: 1.8 V	DDRCLK
		OUT2: CLK_10GE_PHY1_[P, N]	• Frequency: 100 MHz • Output type: LVDS • Operating voltage: 1.8 V	10 GbE PHY 1 (AQR107)
		OUT3: CLK_10GE_B_[P, N]	• Frequency: 100 MHz • Output type: LVDS • Operating voltage: 1.8 V	10 GbE PHY 2 (AQR107)
		OUT4: SYSCLK_DIFF_[P, N]	• Frequency: 100 MHz • Output type: HCSL • Operating voltage: 1.8 V	DIFF_SYSCLK
		OUT5: CLK_25GE_REF_[P, N]	• Frequency: 25 MHz • Output type: HCSL • Operating voltage: 1.8 V	25 GbE PHY (IN112525)
		OUT7: EC_CLK125 / CLK_1588_CGEN	• Frequency: 125 MHz • Output type: LVCMOS • Operating voltage: 1.8 V	Ethernet controller / IEEE 1588 port
		OUT8: CLK_SD1_F_[P, N]	• Frequency: 161.1328125 MHz • Output type: HCSL • Operating voltage: 1.8 V	SerDes1 controller PLL 1

Table continues on the next page...

Table 2-5. LX2160ARDB clocks (continued)

Part identifier	Clock generator	Clock	Specifications	Destination
		OUT9: CLK_PHY_40GE_[P, N]	• Frequency: 156.25 MHz • Output type: HCSL • Operating voltage: 1.8 V	40 GbE PHY (CS4223)
U117	Si52208-A01AGM	DIFF0_[P, N]: CLK_SD2_F_[P, N]	• Frequency: 100 MHz (spread-spectrum capable) • Output type: HCSL	SerDes2 controller PLL 1
		DIFF1_[P, N]: CLK_SD2_S_[P, N]		SerDes2 controller PLL 2
		DIFF2_[P, N]: CLK_SLOT1_[P, N]		PCIe x4 slot
		DIFF3_[P, N]: CLK_SLOT2_[P, N]		PCIe x8 slot
		DIFF4_[P, N]: CLK_SD3_F_[P, N]		SerDes3 controller PLL 1
		DIFF5_[P, N]: CLK_SD3_S_[P, N]		SerDes3 controller PLL 2

2.3 DDR interface

The LX2160ARDB supports two high-speed DDR4 memory ports: DDR#1 and DDR#2.

The figure below shows the architecture of the DDR#1 memory port.

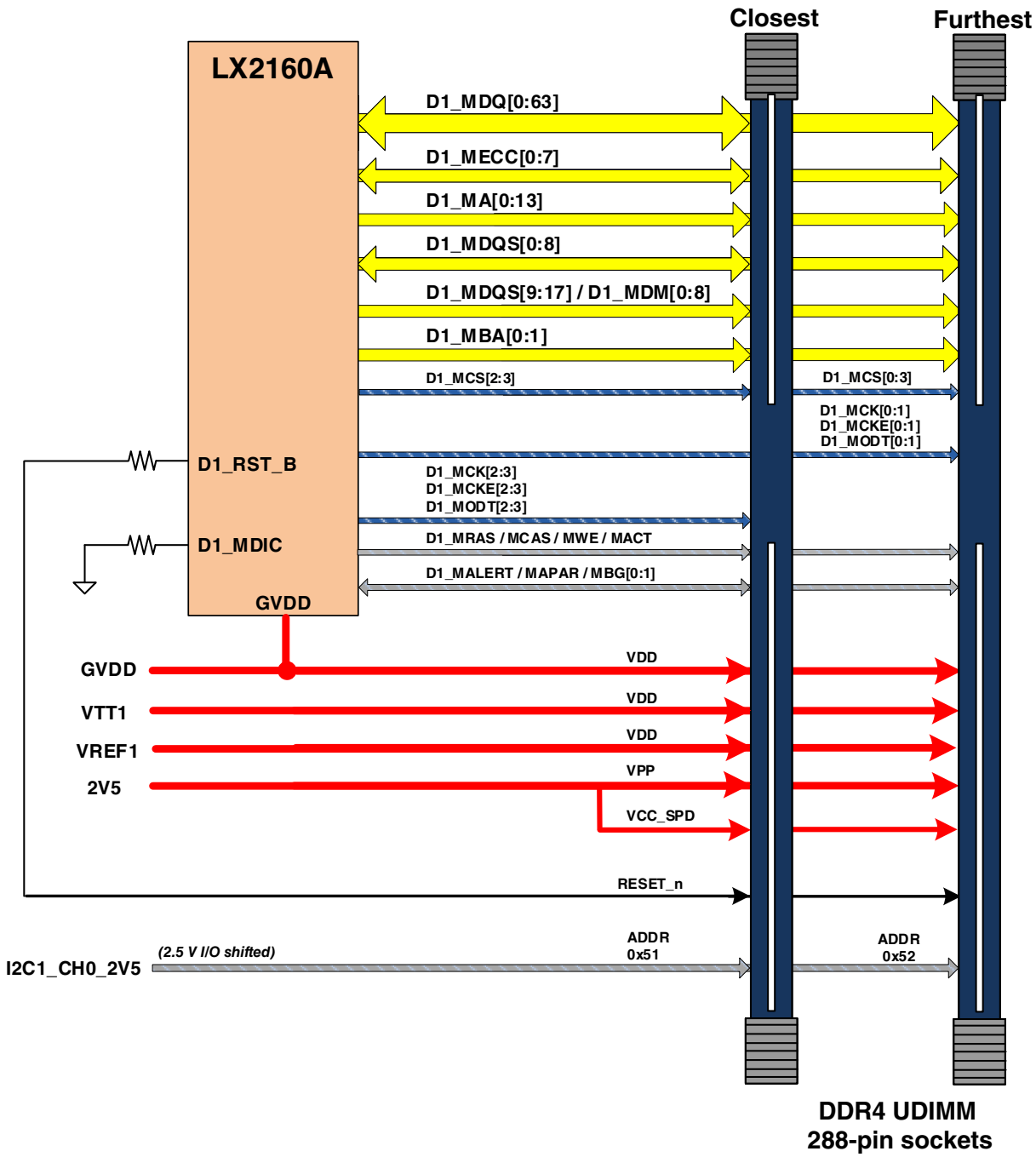


Figure 2-7. DDR#1 memory port architecture

The figure below shows the architecture of the DDR#2 memory port.

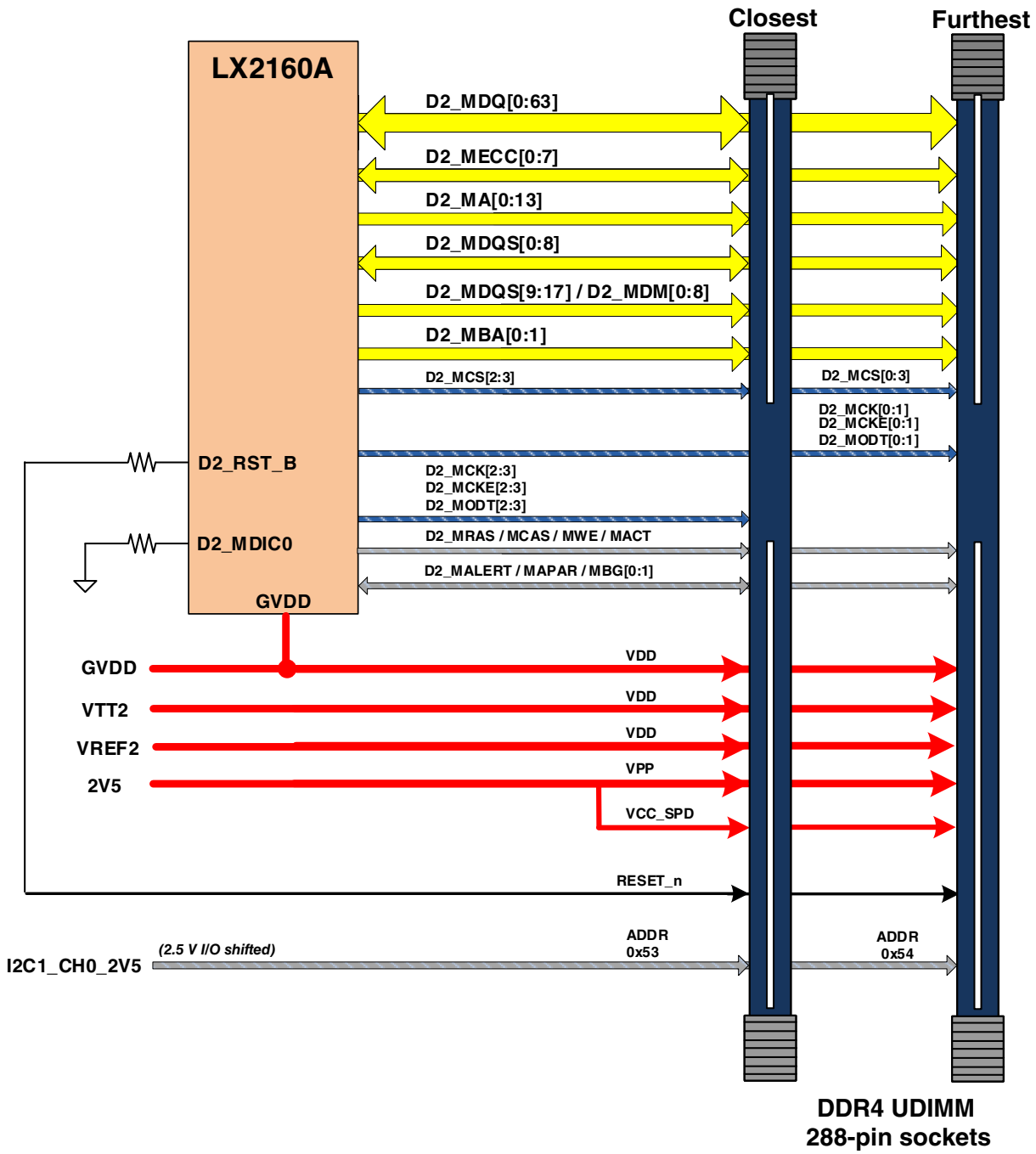


Figure 2-8. DDR#2 memory port architecture

Following are the characteristics of each DDR4 port available on the LX2160ARDB:

- Provides two DIMM connectors each supporting an industry-standard, 288-pin, JEDEC-compliant DDR4 UDIMM or RDIMM module:
  - DIMM#1 (J14/J15) supports four chip selects (D1_MCS_B[0:3] / D2_MCS_B[0:3]) for single-, dual-, and quad-rank DDR4 memory modules
  - DIMM#2 (J16/J17) supports two chip selects (D1_MCS_B[2:3] / D2_MCS_B[2:3]) for single- and dual-rank DDR4 memory modules

- Supports only DDR4 memory
- Supports DDR4 memory devices with data widths of 8/16 bits
- Supports 4-bit memory devices with minor board modification to remove pull-down resistors that are mounted on the D1 or D2 MDQS[9:17]_N traces.
- Supports 64-bit data and 8-bit ECC
- Operates at up to 3.2 GigaTransfers/second (GT/s)
- Memory interface includes all necessary termination and I/O power
- Memory signals are routed in a way to achieve maximum performance on the bus

By default, one of the two DIMM sockects of each LX2160ARDB DDR port has a DIMM installed. It is a 288-pin, dual-rank, 16 GB DDR4 SDRAM UDIMM (MTA18ADF2G72AZ-3G2E1), which supports 64-bit data with 8-bit ECC and operates at up to 3.2 GT/s (0.62 ns frequency at column access strobe (CAS) latency = 22).

NOTE

The LX2160ARDB DDR interface can work with any JEDEC-compliant, 288-pin, DDR4 UDIMM or RDIMM module. The DIMM used in the board is a representative DIMM.

2.3.1 DDR power

The LX2160ARDB power supplies provide the voltages shown in the table below specifically for the DDR4 subsystem (see Power supplies for further details).

Table 2-6. DDR power supplies

Voltage name	Voltage	Current	Description
GVDD	1.2 V	<= 20 A	DDR and processor I/O power
VTT1	0.6 V	<= 3 A	DDR#1 termination supply
VTT2	0.6 V	<= 3 A	DDR#2 termination supply

2.4 SerDes interface

The LX2160A processor supports three SerDes modules (SerDes1, SerDes2, and SerDes3), each having eight high-speed serial communication lanes. Each SerDes lane supports speeds of up to 25 GHz.

The figure below shows the LX2160ARDB SerDes architecture.

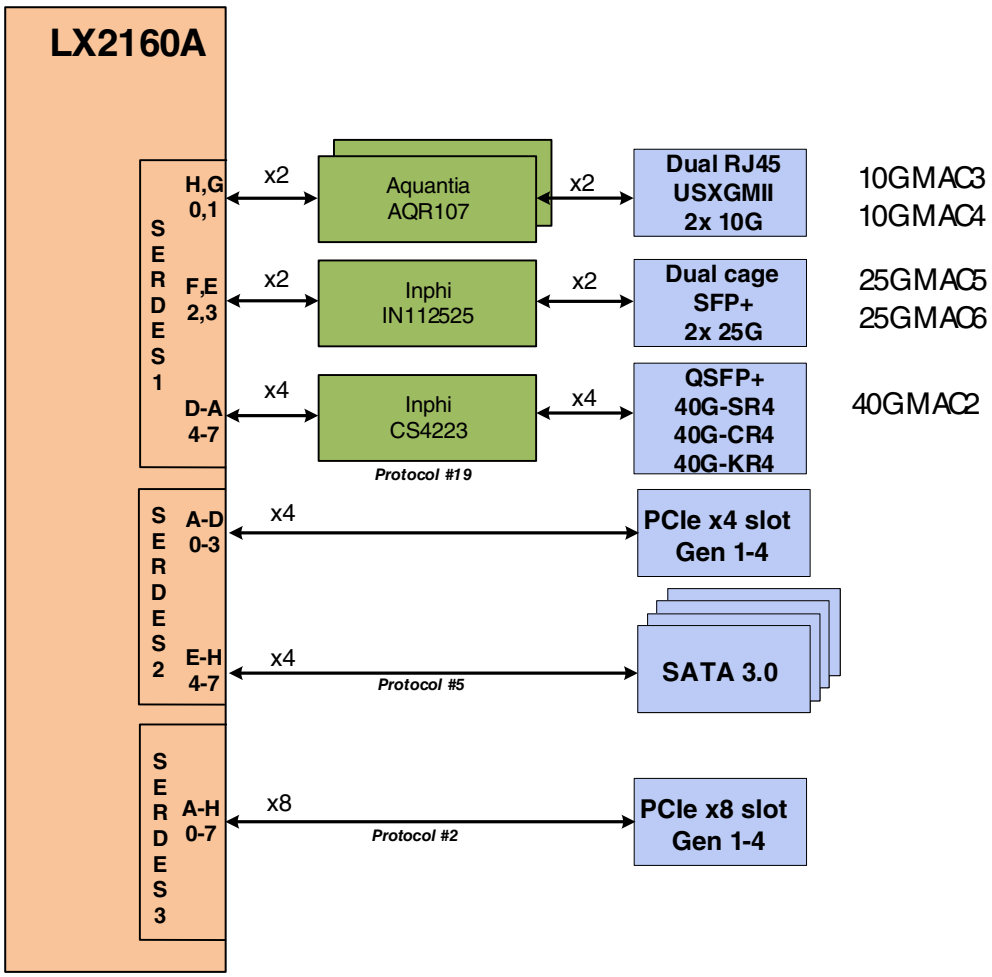


Figure 2-9. SerDes architecture

The figure below shows the possible SerDes protocol combinations that can be used on the LX2160ARDB with the LX2160A processor.

LX2160A	SerDes 1 : x8 : Front Side							
Lanes	0/H	1/G	2/G	3/E	4/D	5/C	6/B	7/A
Protocol 19	XFI.3	XFI.4	25GE.5	25GE.6	40GE.2			
Clocks	161.1328125 MHz		161.1328125 MHz		161.1328125 MHz			

LX2160A	SerDes 2 : x8 : Front Side							
Lanes	0/A	1/B	2/C	3/D	4/E	5/F	6/G	7/H
Protocol 5	PCIe.3 x4				SATA.3	SATA.4	SATA.1	SATA.2
Clocks	100.00 MHz				100.00 MHz			

LX2160A	SerDes 3 : x8 : Back Side							
Lanes	0/A	1/B	2/C	3/D	4/E	5/F	6/G	7/H
Protocol 2	PCIe.5 x8							
Clocks	100.00 MHz							

Figure 2-10. SerDes protocol combinations

The table below shows the LX2160ARDB SerDes assignments when the LX2160A processor is used.

Table 2-7. SerDes assignments for LX2160A processor

SerDes module	Lane	Connectivity	Port
1	H / 0	Aquantia AQR107 10 GbE PHY #1	2x 10 GbE RJ45 USXGMII magnetic jacks (10G MAC3/4)
	G / 1	Aquantia AQR107 10 GbE PHY #2	
	F-E / 2-3	Inphi IN112525 25 GbE PHY	2x 25 GbE SFP+ fiber transceiver cages (25G MAC5/6)
	D-A / 4-7	Inphi CS4223 40 GbE PHY	40 GbE QSFP+ fiber transceiver cage (40G MAC2)
2	A-D / 0-3	PCI Express (Gen 1/2/3/4)	PCI Express x4 connector (slot 1)[1]
	E / 4	SATA	SATA header 1
	F / 5	SATA	SATA header 2
	G / 6	SATA	SATA header 3
	H / 7	SATA	SATA header 4
3	A-H / 0-7	PCI Express (Gen 1/2/3/4)	PCI Express x8 connector (slot 2)

1. A right-angle adapter is required to connect a PCIe Gen 1/2/3 connector. No adapter is required when using a PCIe Gen 4 connector.

NOTE

No muxes or other configuration is required for SerDes operation.

2.5 Ethernet controller interface

The LX2160A processor supports two Ethernet controllers, EC1 and EC2, supporting the RGMII protocol. On the LX2160ARDB, each Ethernet controller is connected to a 1 GbE RGMII Ethernet PHY (Qualcomm AR8035), which is connected to an RJ45 jack coupled with magnetics. The two RJ45 jacks are stacked on the board such that jack for EC1 is at the bottom and jack for EC2 is at the top.

The figure below shows the architecture of the Ethernet controller interface.

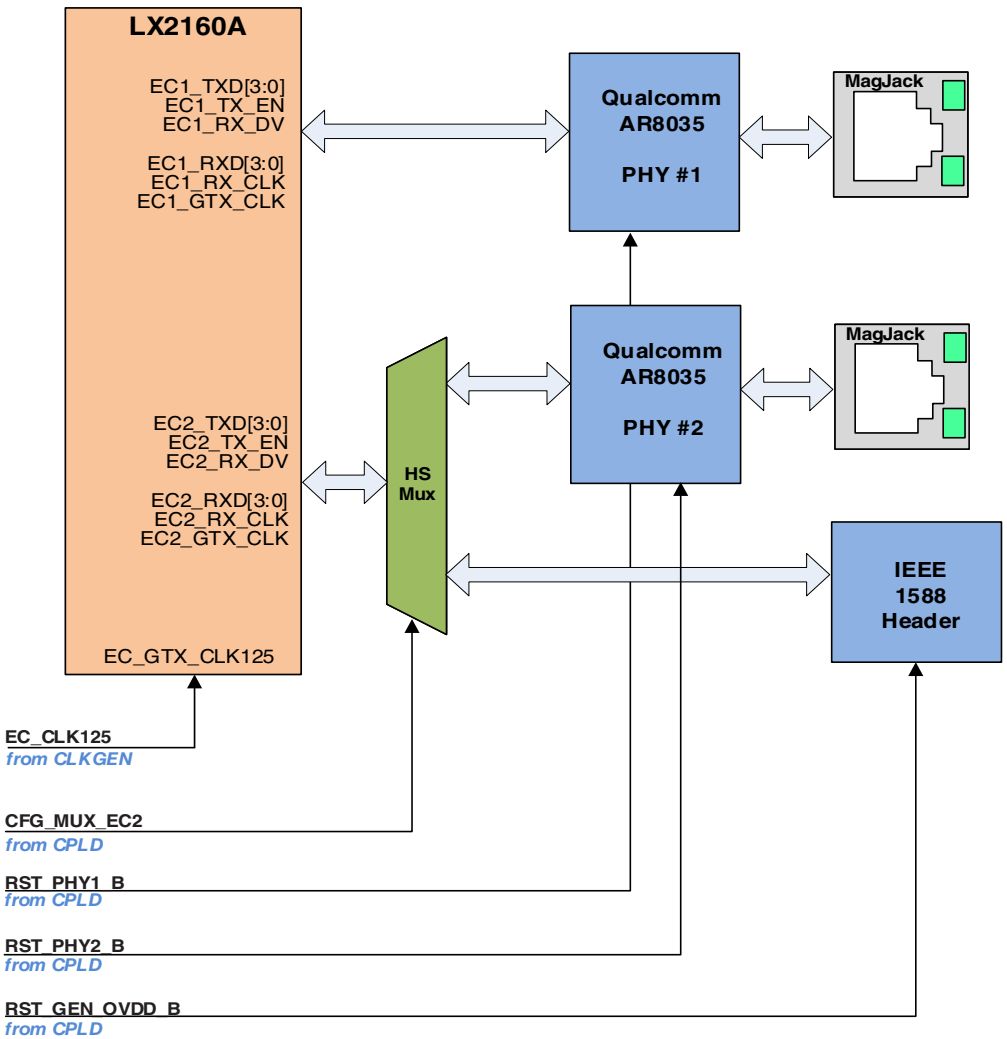


Figure 2-11. Ethernet controller architecture

2.5.1 IEEE 1588 interface

The LX2160A processor provides support for the IEEE 1588™ precision time protocol (PTP), which works in tandem with the Ethernet controllers to time-stamp the incoming packets. A 12-pin header is provided on the board to allow access to the IEEE 1588 system (see figure below).

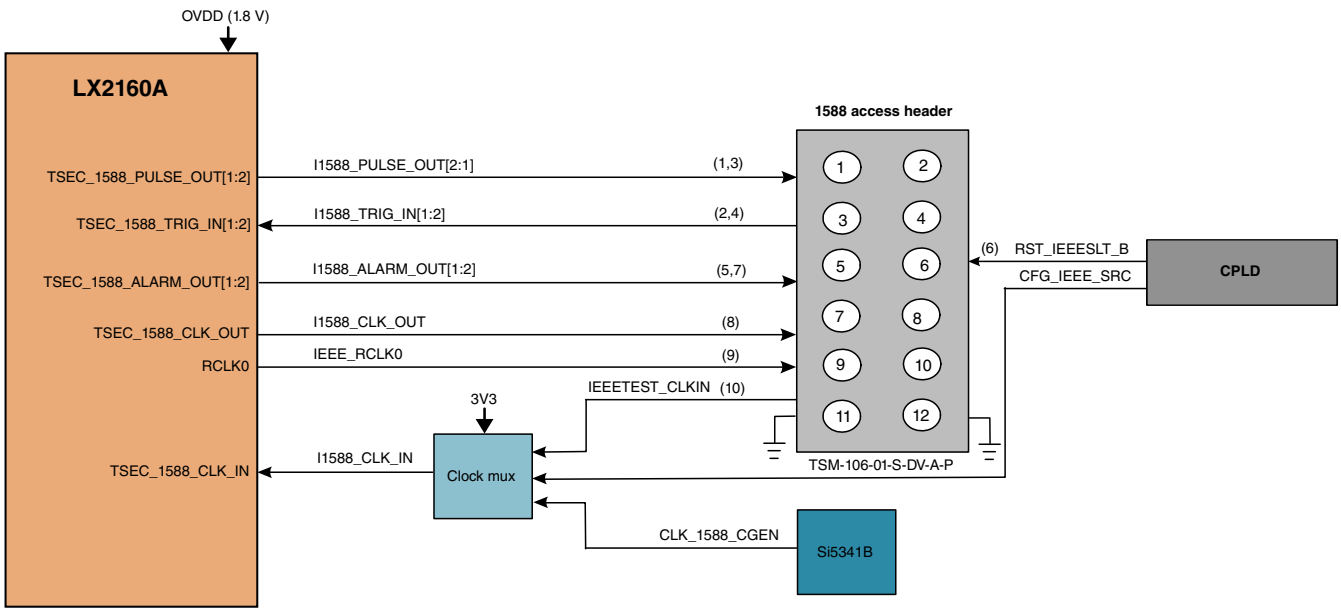


Figure 2-12. IEEE 1588 architecture

The table below lists the testing options provided by the IEEE 1588 test header.

Table 2-8. IEEE 1588 port

IEEE 1588 feature	Specifications	Description
Clocks	Input clock	Ethernet reference clock (to processor) is driven from an onboard 125 MHz oscillator source. Under software configuration, it may be clocked from the IEEE 1588 header instead.
	Output clock	Ethernet output clock is driven to the IEEE 1588 header
Signals	Other related signals	All remaining IEEE 1588 signals are connected to the dedicated header pins

2.6 Ethernet management interface

The LX2160ARDB has two Ethernet management interfaces, EMI1 and EMI2, for controlling PHY transceivers. The figure below shows the PHY device connections.

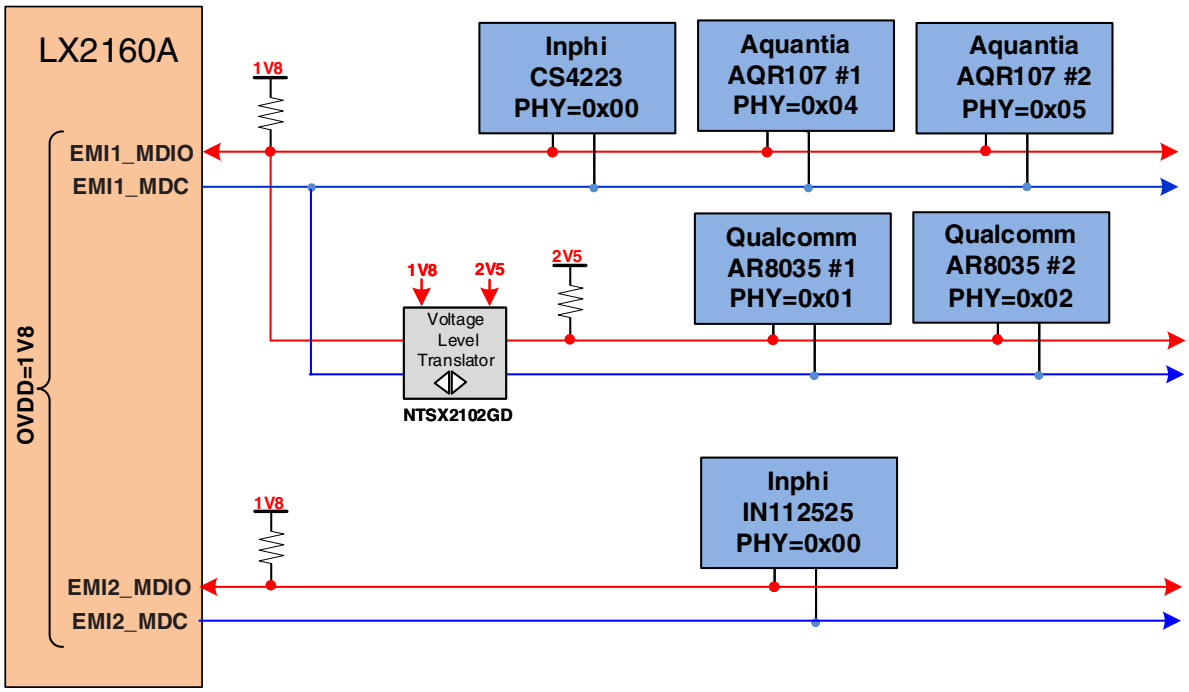


Figure 2-13. EMI routing architecture

Both EMI1 and EMI2 operate at OVDD (1.8 V) levels. For devices not operating at 1.8 V, EMI signals are bi-directionally shifted to the compatible voltage using voltage level translators.

NOTE

In the LX2160ARDB, no multiplexer routing is needed for EMI connections.

The table below summarizes the EMI connections.

Table 2-9. EMI connections

EMI bus	MDIO address	Device connected
EMI1	0x00	Inphi CS4223 40 GbE PHY
	0x01	Qualcomm AR8035 1 GbE PHY #1
	0x02	Qualcomm AR8035 1 GbE PHY #2
	0x04	Aquantia AQR107 10 GbE PHY #1
	0x05	Aquantia AQR107 10 GbE PHY #2
EMI2	0x00	Inphi IN112525 25 GbE PHY

2.7 eSDHC interface

The LX2160A processor supports two enhanced secured digital host controllers (eSDHC): eSDHC1 and eSDHC2.

The LX2160ARDB eSDHC1 interface provides a secure digital (SD) connector (J42) for connecting an SD card to the board. Because the LX2160A processor supports dynamic EVDD (selectable 1.8 V / 3.3 V), SDHC1_VSEL automatically changes the input/output voltage to follow the SD card. I2C2 must be programmed in the RCW to serve as the card detect (CD_B) and write protect (WP) pins for eSDHC1 interface. This happens automatically when the SD card slot is selected as the boot device.

The figure below shows the eSDHC1 connections in the LX2160ARDB.

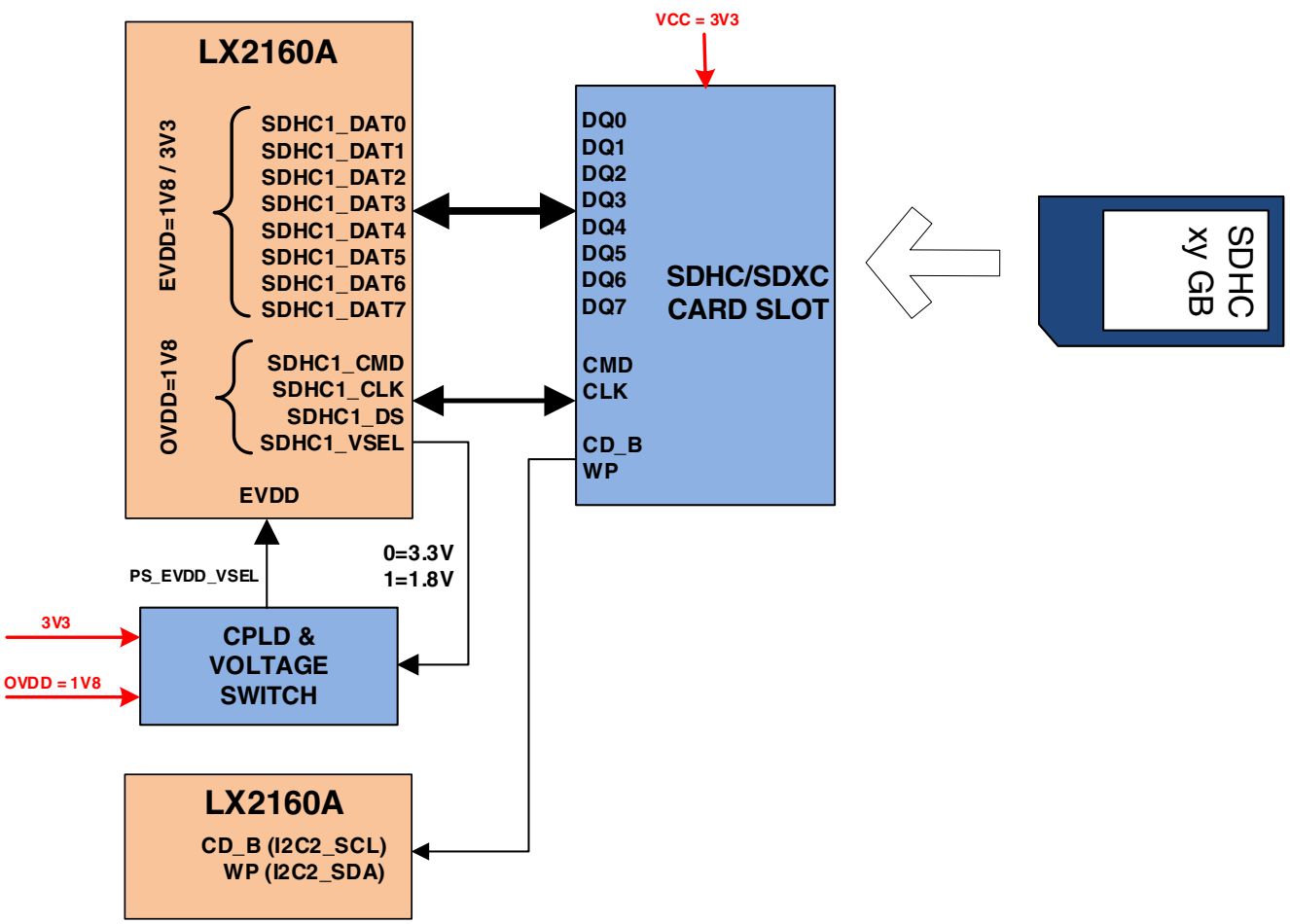


Figure 2-14. eSDHC1 architecture

The LX2160ARDB eSDHC2 interface is connected to an eMMC device on the board. It supports either an FBGA169 device or an FBGA153 device. By default, an FBGA169 eMMC device is supported. The table below shows the devices supported by the eSDHC2 interface.

Table 2-10. Supported eMMC devices

Part number	Manufacturer	Memory size	Notes
MTFC128GAJAECE-IT	Micron	128 GB	Supported by default
SDINADF4-128G	Sandisk	128 GB	

The figure below shows the eSDHC2 connections in the LX2160ARDB.

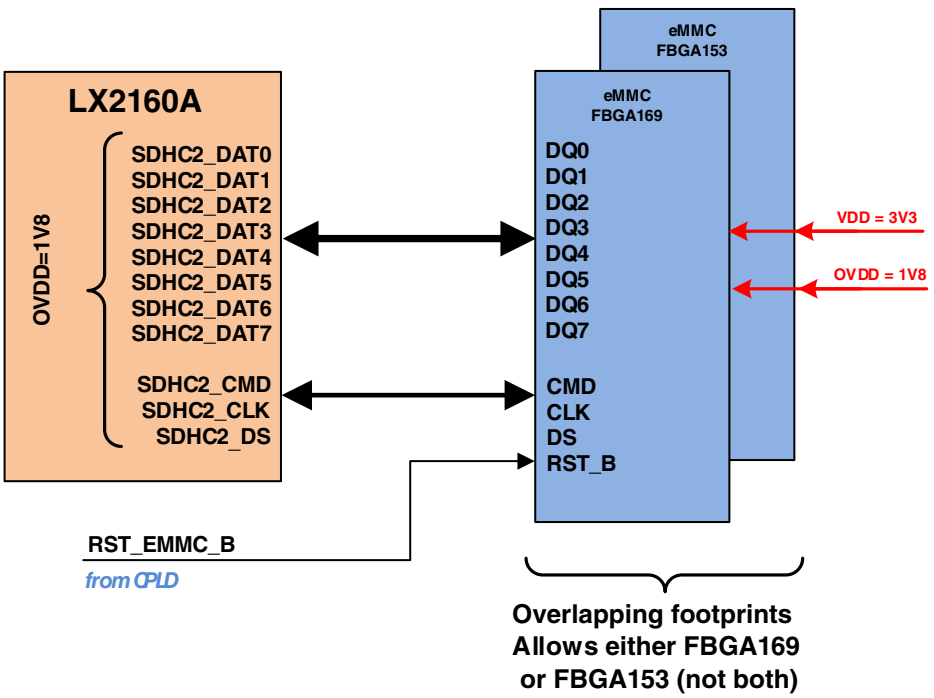


Figure 2-15. eSDHC2 architecture

2.8 XSPI interface

The LX2160ARDB octal serial peripheral interface (XSPI) supports two onboard XSPI flash memories for boot image and one QSPI emulator for offboard QSPI emulation. The XSPI chip-select signals from the processor are driven to the XSPI memories or the QSPI emulator through two high-speed multiplexers. The XSPI interface supports Single/Dual/Quad/Octal mode data transfer (1/2/4/8 bidirectional data lines).

The figure below shows the LX2160ARDB XSPI connections.

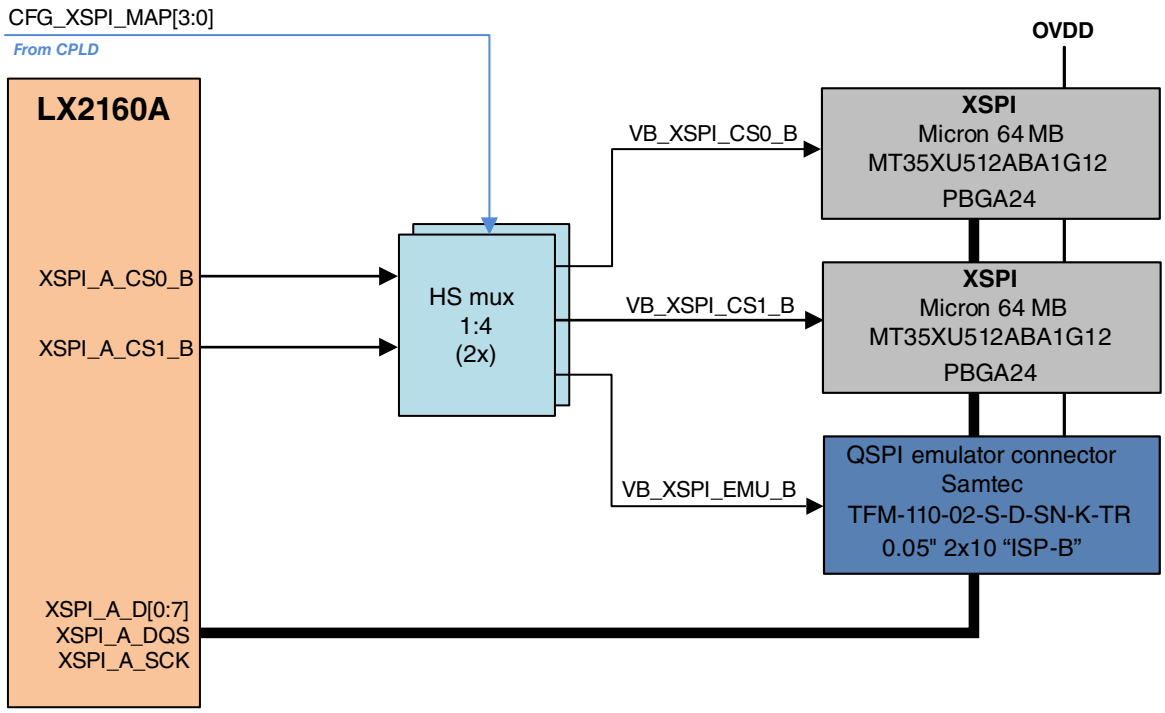


Figure 2-16. XSPI architecture

The table below shows the devices attached to the LX2160ARDB XSPI interface.

Table 2-11. Devices attached to XSPI interface

Part identifier	Part number	Manufacturer	Description
U112	MT35XU512ABA1G12	Micron	64 MB, PBGA24 octal SPI serial flash memory
U115			
J13	TFM-110-02-S-D-SN-K-TR	Samtec	A 2x10-pin connector that connects to an external QSPI flash emulator (DediProg EM100Pro) through an ISP-ADP-intel-B cable adapter. The EM100Pro emulator uses 1.8 V as the input/output voltage.

The table below describes the XSPI routing configuration.

Table 2-12. XSPI configuration

Configuration signal	DIP switch	CPLD register	Description

Bit value	XSPI_A_CS0	XSPI_A_CS1	Description
000 (default setting)	Dev #0	Dev #1	Boot from default flash memory
001	Dev #1	Dev #0	Boot from alternative flash memory

Table 2-12. XSPI configuration

Configuration signal	DIP switch	CPLD register	Description			
			Bit value	XSPI_A_CS0	XSPI_A_CS1	Description
			010	QSPI emulator	Dev #0	Boot from QSPI emulator, program default flash memory
			011	QSPI emulator	Dev #1	Boot from QSPI emulator, program alternative flash memory
			100	Dev #0	QSPI emulator	Emulator access

2.9 USB interface

The LX2160ARDB supports two universal serial bus (USB) 3.0 controllers, with each port connected to a different type of USB connector for maximum flexibility. The table below describes the USB ports.

Table 2-13. USB ports

USB port	Connector type	Location	Supported modes
USB1	Type A	Front panel	• Host mode: Jumper J31 is shorted (default mode) • Device mode: Jumper J31 is open
USB2	Micro-AB	Front panel	• Host mode: Jumper J33 is shorted • OTG mode: Jumper J33 is open (default mode)

As described in the table above, operating modes for USB1 and USB2 ports are controlled through the J31 and J33 jumpers, respectively.

The figure below shows the architecture of the LX2160ARDB USB interface.

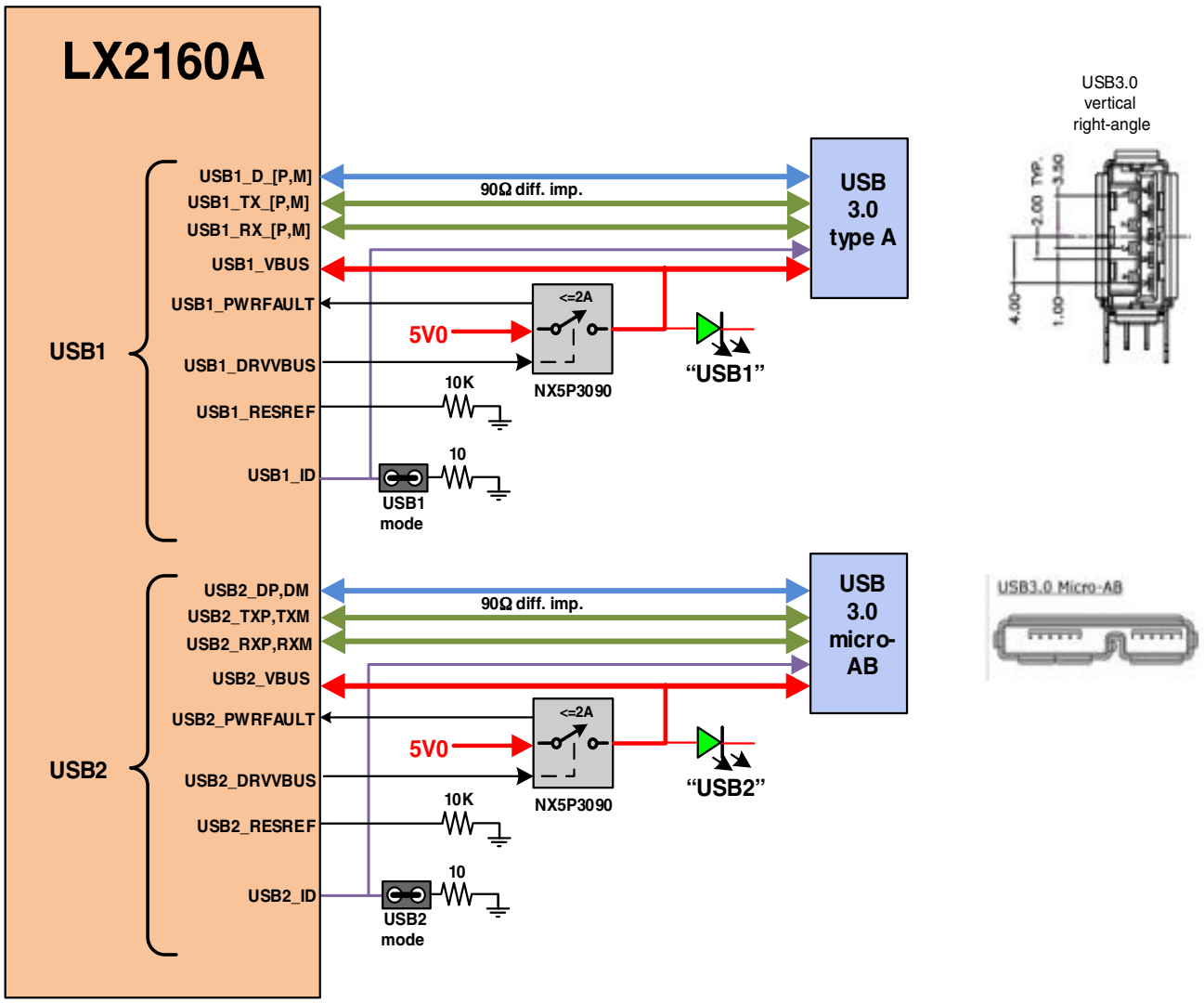


Figure 2-17. USB architecture

The USBx_DRVVBUS and USBx_PWRFAULT pins of each USB controller are connected to a programmable-current USB switch, NX5P3090UK (from NXP), for individual port management. The USB switch is powered from +5 V USB power supply. The USB1_DRVVBUS/USB2_DRVVBUS signal controls the VBUS drive for USB1/ USB2 port. The USB1_PWRFAULT/USB2_PWRFAULT signal gets power fault indications through the USB switch. The maximum allowed current consumption of a USB connected device is 2 A per channel.

Each USB connector has an LED nearby, USB1_5V and USB2_5V, which are active when the +5 V USB power supply is enabled.

2.10 I2C interface

The LX2160A processor supports up to six I2C buses. Most system devices (other than UEFI) are accessed via I2C1 port, which is connected to a PCA9547PW I2C multiplexer to isolate address conflicts and effectively manage the large number of I2C devices. The I2C1 port is translated to 3V3_SB to provide programming access to power controllers, clocks, memories, and so on, when the system is powered off.

The figure below shows the I2C bus architecture.

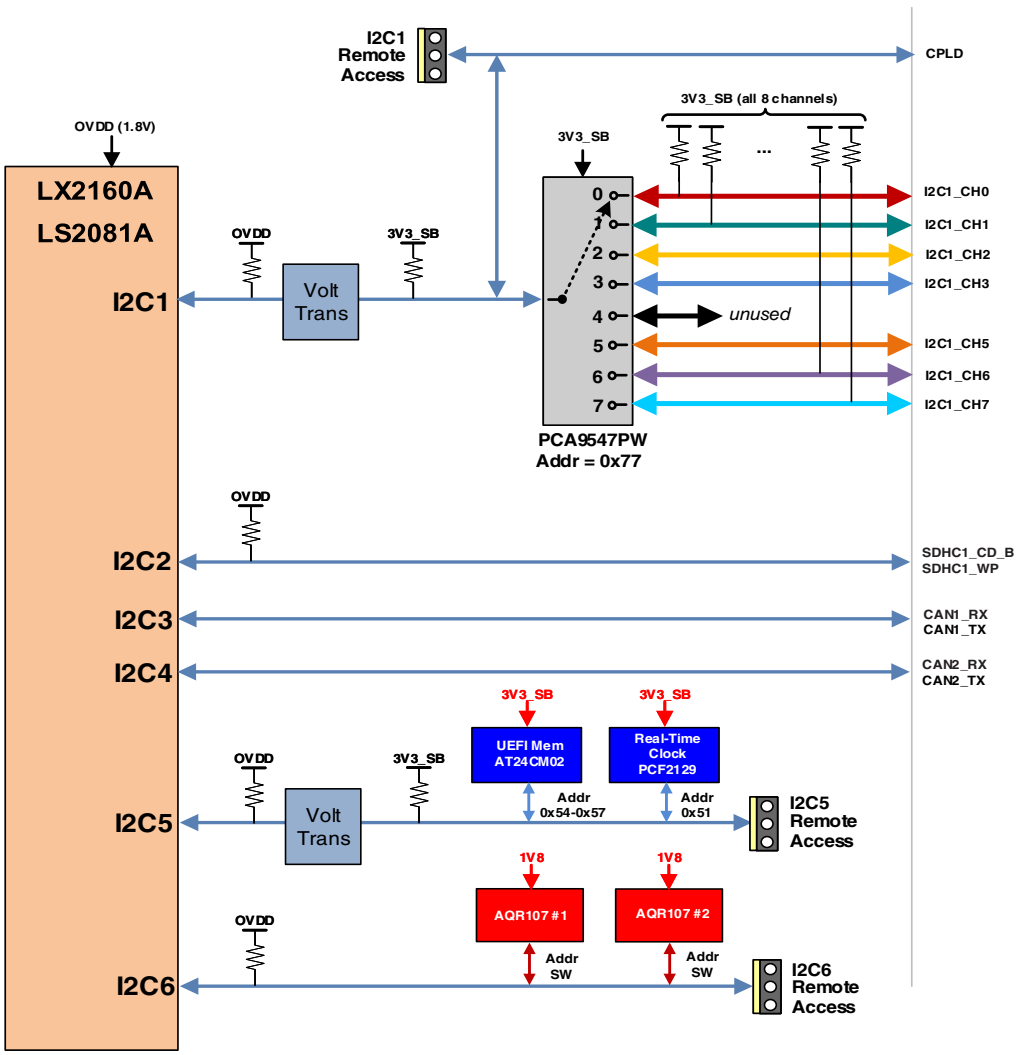


Figure 2-18. I2C bus architecture

The multiplexer used for the I2C1 bus partitions the bus into eight sub-buses, called "channels." Software must program the multiplexer to access one of the eight I2C1 channels. All boot-software-dependent devices are placed on channel 0, or "I2C1_CH0" as it is named. Channel 0 is the default selection upon reset so that software has immediate access to critical resources.

The I2C devices indirectly available on the I2C1 bus are shown in the figure below.

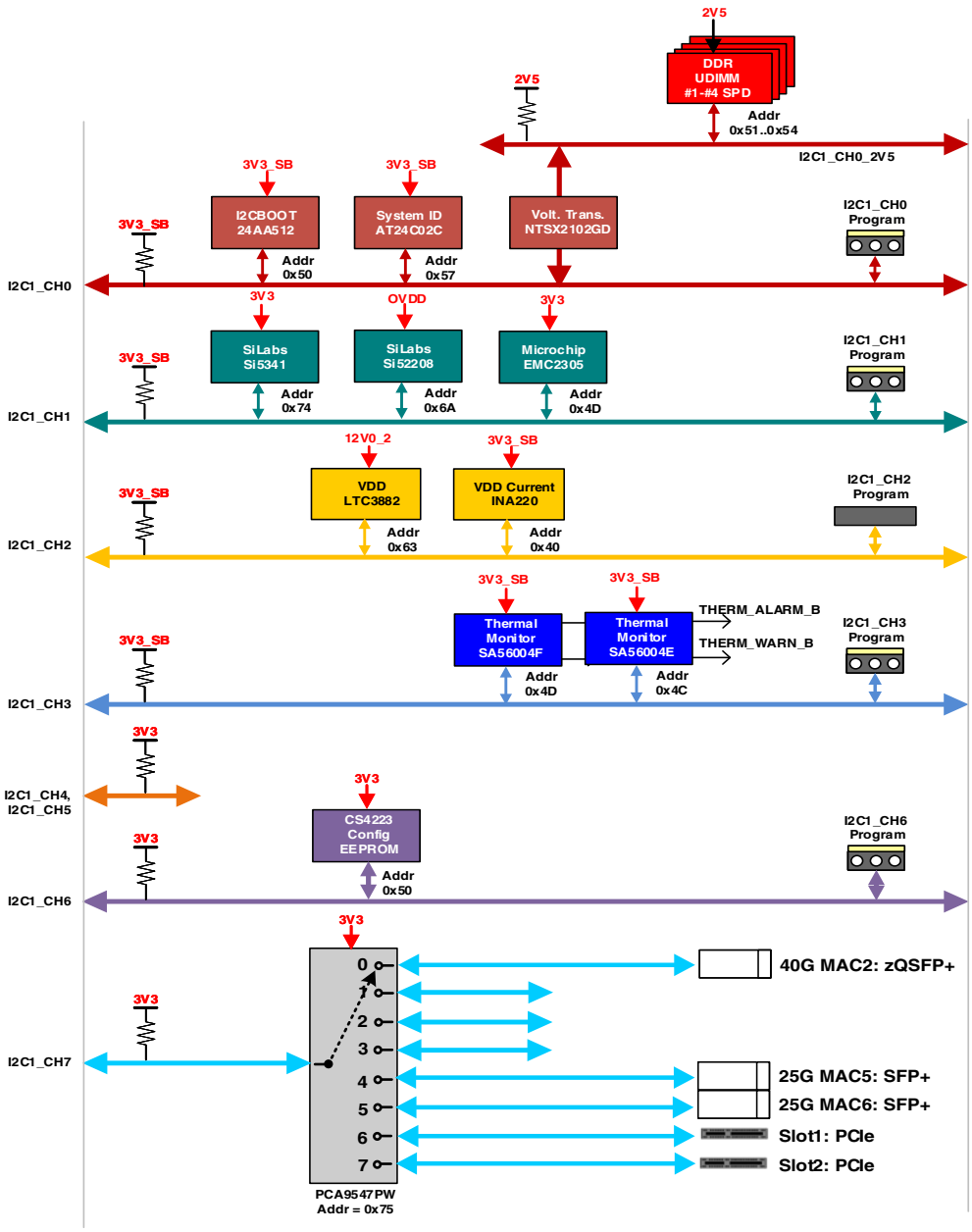


Figure 2-19. I2C channels

The following table describes all major devices available on I2C bus.

Table 2-14. I2C bus device map

I2C bus	7-bit address	Device	Description	Notes
(All)	-	I2C master	LX2160ARDB	
	0x66	I2C slave	CPLD	I2C access to CPLD BCSRs (registers).

Table continues on the next page...

Table 2-14. I2C bus device map (continued)

I2C bus	7-bit address	Device	Description	Notes
	0x77	NXP PCA9547PW	I2C bus multiplexer (primary)	Converts I2C1 bus into eight channels
I2C1_CH0	0x50	Microchip 24AA512-I/SN	I2C boot memory	Provides I2C booting option
	0x51	256-byte EEPROM	SPD data	Stores SPD and temperature data for DDR#1 UDIMM connector 1
	0x52	256-byte EEPROM	SPD data	Stores SPD and temperature data for DDR#1 UDIMM connector 2
	0x53	256-byte EEPROM	SPD data	Stores SPD and temperature data for DDR#2 UDIMM connector 1
	0x54	256-byte EEPROM	SPD data	Stores SPD and temperature data for DDR#2 UDIMM connector 2
	0x57	Microchip AT24C02C-XHM-B: 256-byte EEPROM	System ID	Stores board-specific data, such as MAC addresses and serial number/errata. Write protectable.
I2C1_CH1	0x4D	Microchip EMC2305	5-channel PWM fan controller	
	0x6A	Silicon Labs Si52208-A01AGM	PCIe clock generator	
	0x74	Silicon Labs Si5341B-D08333-GM	Clock synthesizer	Provides SYSCLK and non-PCIe SerDes clocks
I2C1_CH2	0x40	Texas Instruments INA220	VDD voltage/current/power monitor	Reports voltage, current, and power data for VDD
	0x63	Linear Technology LTC3882	VDD power regulator	Supplies power to the core voltage rail (VDD)
I2C1_CH3	0x4C	NXP SA56004ED	Thermal monitor 1	Monitors processor thermal diode 1
	0x4D	NXP SA56004FD	Thermal monitor 2	Monitors processor thermal diode 2
I2C1_CH4	Unused			
I2C1_CH5	Unused			
I2C1_CH6	0x50	Microchip 24AA512-I/SN	Memory for booting 40 GbE CS4223	
I2C1_CH7	0x75	NXP PCA9547PW	I2C bus multiplexer (secondary)	Converts I2C1_CH7 channel into eight sub-channels
I2C1_CH7_CH0	0x50	Quad SFP+ cage	40G MAC2 QSFP+ port	

Table continues on the next page...

Table 2-14. I2C bus device map (continued)

I2C bus	7-bit address	Device	Description	Notes
I2C1_CH7_CH1	Unused			
I2C1_CH7_CH2	Unused			
I2C1_CH7_CH3	Unused			
I2C1_CH7_CH4	0x50	SFP+ cage (#1)	25G MAC5 SFP port	
I2C1_CH7_CH5	0x50	SFP+ cage (#2)	25G MAC6 SFP port	
I2C1_CH7_CH6	-	PCIe slot 1	PCIe slot 1	
I2C1_CH7_CH7	-	PCIe slot 2	PCIe slot 2	
I2C2	Unused			
I2C3	Unused			
I2C4	Unused			
I2C5	0x51	NXP PCF2129AT	Real-time clock	Provides real-time clock
	0x54 - 0x57	Microchip AT24CM02-SSHM-B: 256 KB EEPROM	UEFI storage	Provides UEFI variable storage in four logical devices
I2C6	-	Aquantia AQR107 PHY (#1)	10 Gbit Ethernet PHY 1	Optional, software-defined address
	-	Aquantia AQR107 PHY (#2)	10 Gbit Ethernet PHY 2	Optional, software-defined address

NOTE

A 7-bit address does not include the read/write (R/W) bit as an address member, though some datasheets might do so. For consistency, all I2C addresses above are of 7 bits only.

NOTE

To access I2C devices on the secondary I2C mux, the primary I2C mux needs to be programmed at address 0x77 and the secondary I2C mux at address 0x75.

2.11 UART interface

The LX2160A processor provides two UART blocks, which support two full serial ports with hardware flow control, or four serial ports with no flow control. On the LX2160ARDB, the UART ports are available for external connection through a dual-port stacked DB9 male connector. Two RS-232 transceivers (Linear Technology LTC2804-1) translate the signals to RS-232 levels. The figure below shows the UART architecture.

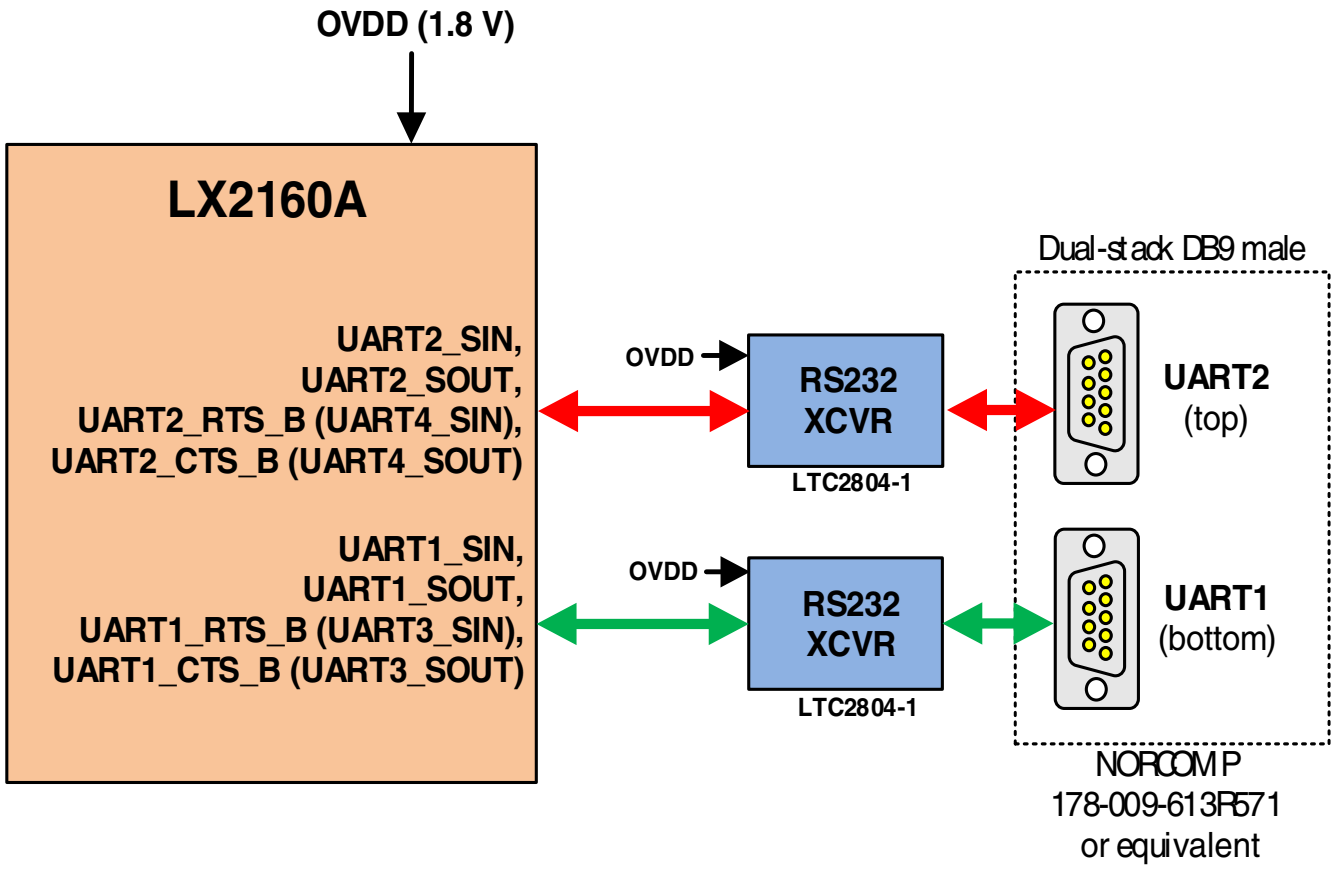


Figure 2-20. UART architecture

2.11.1 Quad serial port support

The serial ports support converting each 4-wire serial port into two independent 2-wire serial ports (for a total of four). When enabled, the UART1_RTS_B/UART2_RTS_B signal becomes UART3_SIN/UART4_SIN and the UART1_CTS_B/UART2_CTS_B signal becomes UART3_SOUT/UART4_SOUT. To evaluate UART3 and/or UART4, a custom DB9 interface cable must be created, as shown in the following figure.

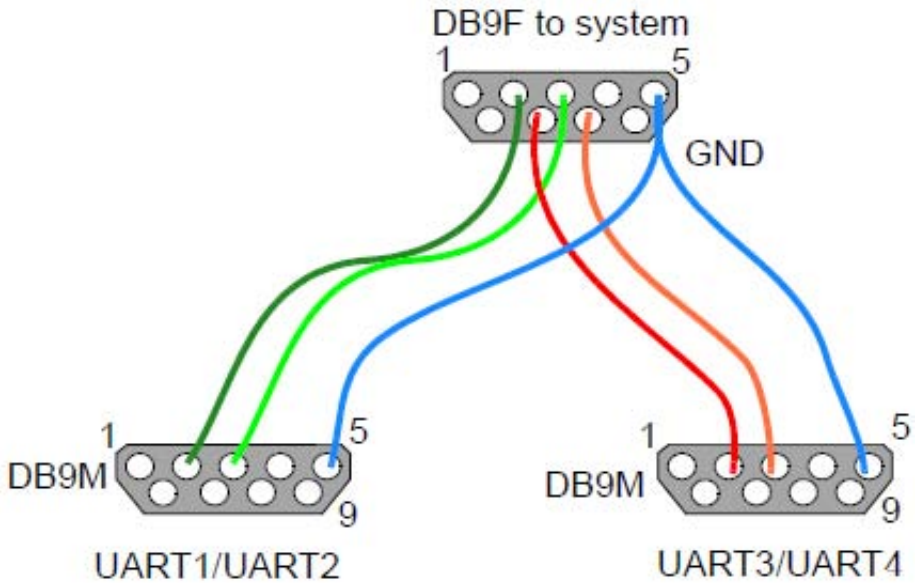


Figure 2-21. 4-wire to 2-wire UART adapter

NOTE

NXP does not make or supply this adapter cable.

2.12 CAN interface

The LX2160A processor supports two controller area network (CAN) modules, CAN1 and CAN2. On the LX2160ARDB, the CAN ports are available for external connection through a dual-port stacked DB9 male connector. Two high-speed CAN transceivers (NXP TJA1051T/3) provide an interface for the CAN ports to send and receive CAN signals to and from the processor. The figure below shows the CAN architecture.

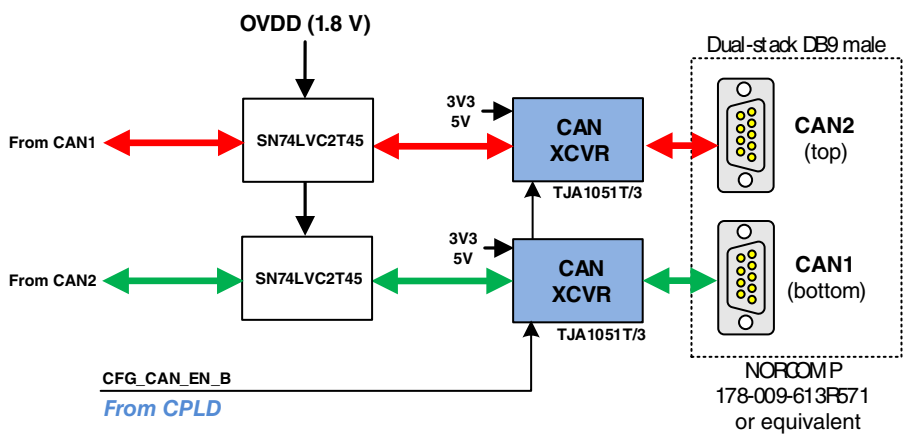


Figure 2-22. CAN architecture

2.13 JTAG port

The JTAG port provides access to the processor using a standard 10-pin Arm Cortex JTAG connector for debugging purposes. The following figure shows the LX2160ARDB JTAG architecture.

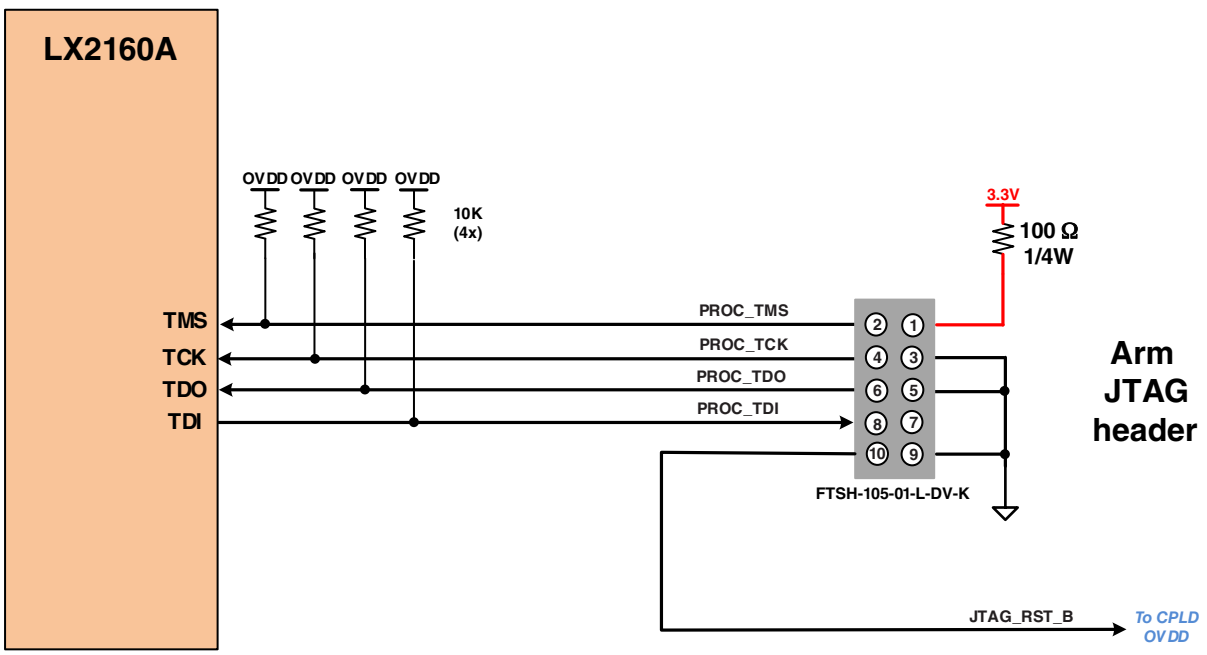


Figure 2-23. JTAG architecture

2.14 Interrupt controller

Some of the LX2160A generic interrupt controller (GIC) pins are reserved for use with RTC and different Ethernet PHYs. The remaining pins are used to merge various board-related interrupt sources for handling by the processor, or for general GPIO use. The interrupts are connected as shown in the figure below.

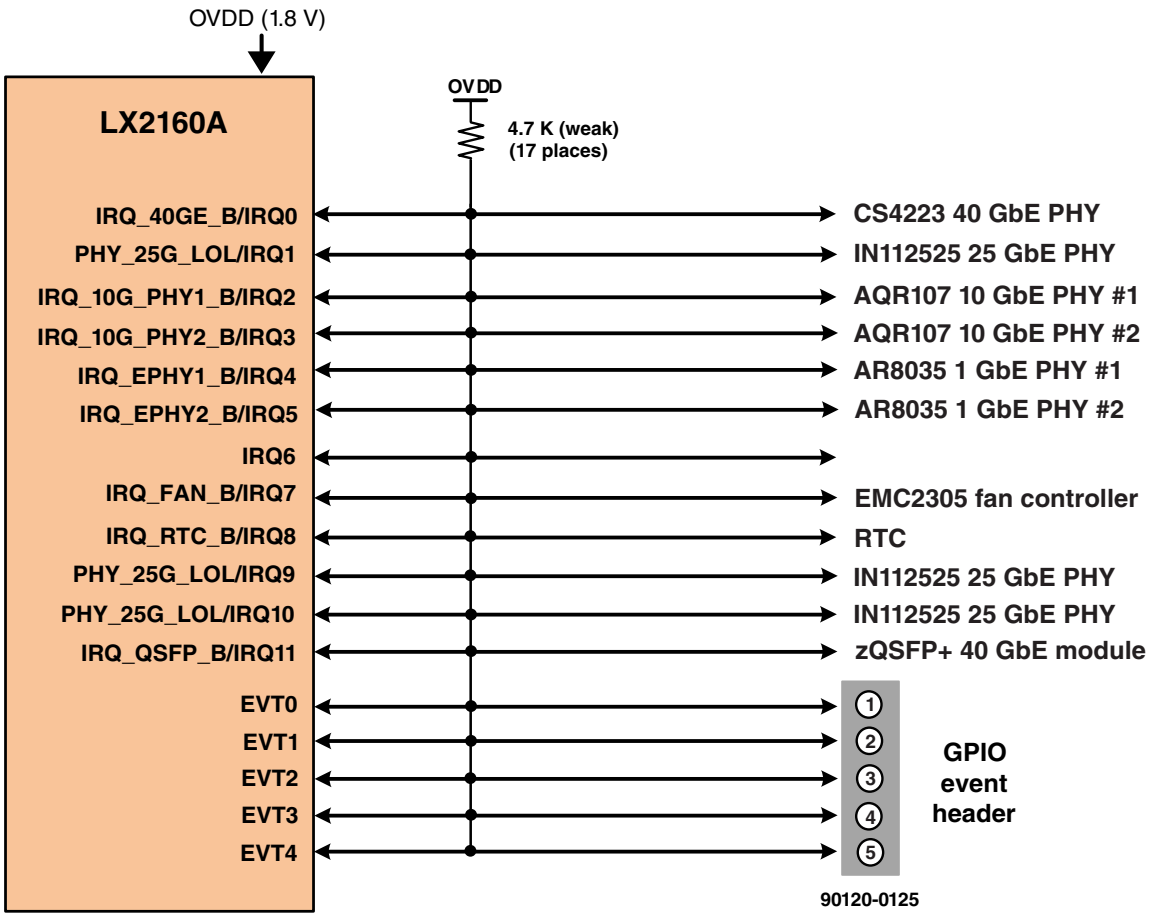


Figure 2-24. Interrupt architecture

The table below summarizes the interrupt assignments used.

Table 2-15. LX2160ARDB interrupt assignments

Interrupt signal	Supported function	Description
IRQ0_B	IRQ_40GE_B	40 GbE PHY (CS4223) interrupt
IRQ1_B	PHY_25G_LOL	25 GbE PHY (IN112525) loss-of-lock interrupt
IRQ2_B	IRQ_10G_PHY1_B	10 GbE PHY #1 (AQR107) interrupt
IRQ3_B	IRQ_10G_PHY2_B	10 GbE PHY #2 (AQR107) interrupt
IRQ4_B	IRQ_EPHY1_B	1 GbE PHY #1 (AR8035) interrupt
IRQ5_B	IRQ_EPHY2_B	1 GbE PHY #2 (AR8035) interrupt
IRQ6_B	Unassigned	
IRQ7_B	IRQ_FAN_B	EMC2305 fan controller interrupt
IRQ8_B	IRQ_RTC_B	RTC interrupt
IRQ9_B	PHY_25G_LOL (if SFP2_MOD_ABS is low)	SFP2 transceiver loss-of-lock interrupt
IRQ10_B	PHY_25G_LOL (if SFP3_MOD_ABS is low)	SFP3 transceiver loss-of-lock interrupt
IRQ11_B	IRQ_QSFP_B	zQSFP+ transceiver (40 GbE PHY) interrupt

2.15 GPIO access

The LX2160A processor has no dedicated general-purpose input/output (GPIO) pins. Instead, GPIO functions are multiplexed internally onto other signals, which must be disabled before using the GPIO functions. For the LX2160ARDB, GPIO access is provided through the IRQ pins IRQ[0:11] and EVT pins EVT[0:4] but only when those pins are not used for IRQ or other purposes. The following figure shows the GPIO access header.

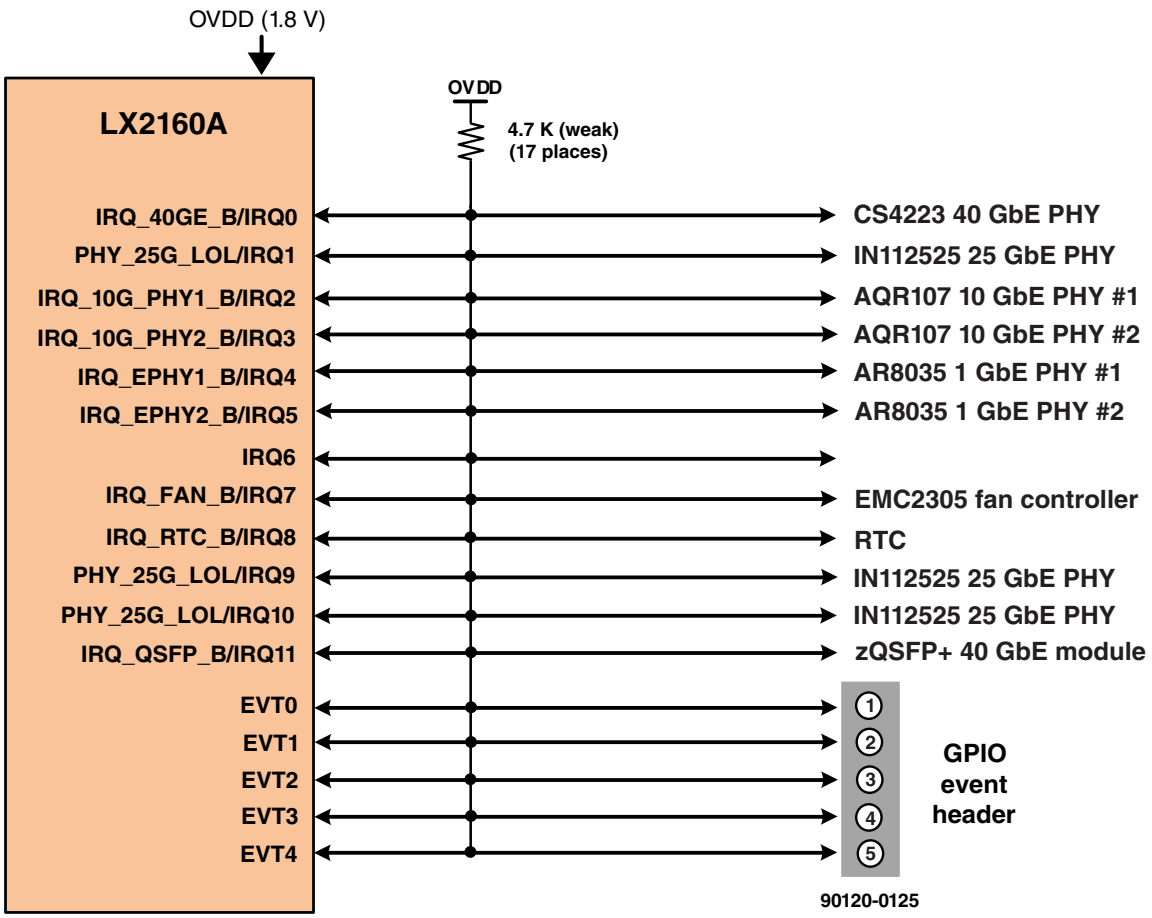


Figure 2-25. GPIO interface

By programming the RCW "IRQ_EXT" field properly, an unused IRQ pin can be reassigned to GPIO purposes. Event signals from EVT pins EVT[0:4] flow through a 5-pin GPIO header.

The table below shows the GPIO mapping in the LX2160ARDB.

Table 2-16. GPIO mapping

LX2160A pin	LX2160A GPIO function	LX2160A primary function
IRQ0	GPIO3[0]	IRQ_40GE_B
IRQ1	GPIO3[1]	PHY_25G_LOL
IRQ2	GPIO3[2]	IRQ_10G_PHY1_B
IRQ3	GPIO3[3]	IRQ_10G_PHY2_B
IRQ4	GPIO3[4]	IRQ_EPHY1_B
IRQ5	GPIO3[5]	IRQ_EPHY2_B
IRQ6	GPIO3[6]	
IRQ7	GPIO3[7]	IRQ_FAN_B
IRQ8	GPIO3[8]	IRQ_RTC_B
IRQ9	GPIO3[9]	PHY_25G_LOL (if SFP2_MOD_ABS is low)
IRQ10	GPIO3[10]	PHY_25G_LOL (if SFP3_MOD_ABS is low)
IRQ11	GPIO3[11]	IRQ_QSFP_B
EVT0_B	GPIO3[12]	
EVT1_B	GPIO3[13]	
EVT2_B	GPIO3[14]	
EVT3_B	GPIO3[15]	
EVT4_B	GPIO3[16]	

NOTE

Because all IRQ signals have a pull-up, GPIO pins programmed to input mode default to “1”.

2.16 Temperature measurement

The LX2160A processor has two thermal monitoring diodes, which can be measured on the LX2160ARDB by two thermal monitor devices, SA56004ED and SA56004FD, from NXP. Software can perform direct die temperature readings with an accuracy of ±1 °C. See I2C interface for addressing information.

In addition to monitoring, the SA56004ED and SA56004FD devices can also trigger alarms upon detecting thermal problems. To do this, the thermal warning and thermal alert signals from these devices are connected to the system controller (CPLD), as well as to status LEDs. The CPLD uses these signals to power down the system, to protect the processor from over-temperature damage.

The LX2160ARDB thermal management scheme is shown in the figure below.

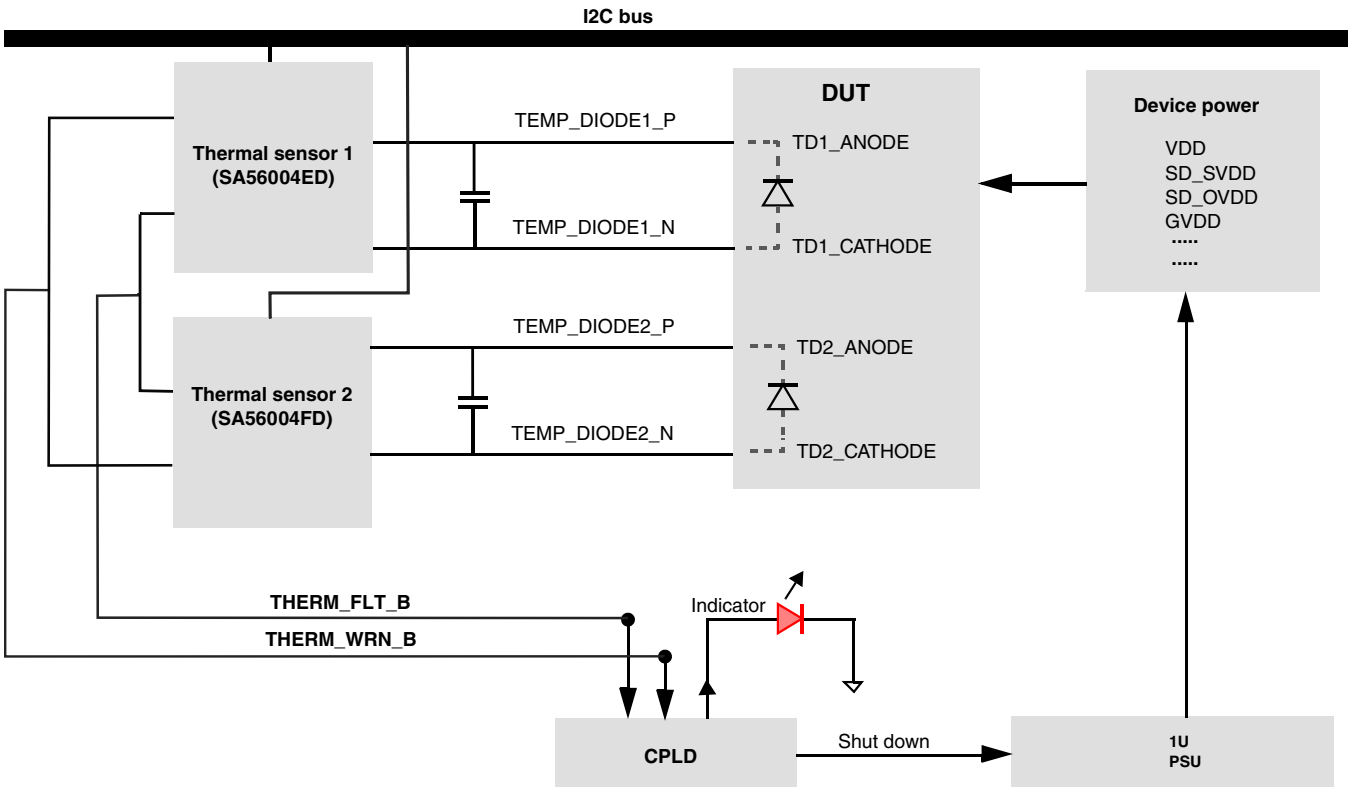


Figure 2-26. Thermal management scheme

Thermal monitoring happens with no programming involved. However, if the thermal limit, by default set as 85 °C, is higher than desired, it will need to be re-programmed. To change the thermal trip point, issue the I2C writes listed in the table below.

Table 2-17. Thermal monitor configuration

I2C write	Description
0x77 0x0B 0x0B	Program primary I2C bus multiplexer (PCA9547PW) to get access to I2C1_CH3 (I2C sub-channel for SA56004ED/SA56004FD)
0x4C 0x19 <TLIMIT> (thermal monitor 1) 0x4D 0x19 <TLIMIT> (thermal monitor 2)	Program the thermal limit of SA56004ED/SA56004FD external measurement (the processor). <TLIMIT> can be any user-defined value, for example, decimal 50.

NOTE

The SW_BYPASS_B switch (SW4[1]) disables thermal monitoring. This may be necessary if operating the board without a processor installed, as an open thermal diode connection will measure as 127 °C.

2.17 LEDs

The LX2160ARDB has numerous onboard light-emitting diodes (LEDs), which can be used to monitor various system functions, such as power on, reset, board faults, and so on. The information collected from LEDs can be used for debugging purposes. The table below lists all the LEDs present on the LX2160ARDB.

Table 2-18. LX2160ARDB LEDs

Reference designator	LED color	LED name	Description (when LED is ON)
D1	Yellow	PRELOAD	The PSU-loading FET is active; it may be hot during power-up or shortly afterward. Avoid touching this area.
D18	Blue	PASS	The CPLD has completed power and reset sequencing and no errors are detected
D19	Yellow	ASLEEP	The processor has not exited Sleep mode, which generally indicates: • Improper RCW source selection • Boot memory does not contain a valid RCW/PBL • PLL multipliers in the RCW data are not compatible with the fixed SYSCLK, DDRCLK, or SDCLK values
D20	Red	FAIL	One of the following has happened: • A thermal over-temperature fault has occurred • One or more power supplies have not started • Software has set the register CTL[0] (FAIL) to indicate a software fault
D21	Red	PORST	The CPLD is asserting PORESET_B to the processor and is in the process of restarting the system
D22	Red	RST REQ	The processor is asserting RESET_REQ_B. This is typically due to the reasons described for the ASLEEP LED.
D23	Red	THERM	Thermal monitors have detected a thermal fault and have shut down the system **NOTE:** Unless reprogrammed by user software, the thermal trip point is 85 °C.
D41	Red	ROTERR	The processor has been installed in the socket rotated 90, 180, or 270 degrees from the pin 1 orientation. The system and device power supplies have been shut down to protect the device.
D24	Green	M7	General status. See Multi-status LEDs for details.
D25	Green	M6	
D26	Green	M5	
D27	Green	M4	
D42	Green	M3	
D43	Green	M2	
D45	Green	M1	
D44	Green	M0	

Table continues on the next page...

Table 2-18. LX2160ARDB LEDs (continued)

Reference designator	LED color	LED name	Description (when LED is ON)
D28	Green	3VSB	The ATX power supply is supplying 3.3 V “standby power” to the system. The system cannot power up unless this supply is provided.
D29	Green	3V3	3V3 ATX power supply is operating correctly
D30	Green	VDD	VDD (processor core) power supply is operating correctly
D31	Green	GVDD	GVDD (DDR4) power supply is operating correctly
D32	Green	SDAV	SD_AVDD power supply is operating correctly
D33	Green	USBV	USB_SVDD power supply is operating correctly
D34	Green	OVDD	OVDD power supply is operating correctly
D35	Green	0V85	0V85 power supply is operating correctly
D36	Green	VTT1	VTT1 power supply is operating correctly
D37	Green	SDV	SD_VDD power supply is operating correctly
D38	Green	2Vx	2V1 and 2V5 power supplies are operating correctly
D39	Green	LVX	0V9 and 1V2 power supplies are operating correctly
D5	Green	QSFP	A QSFP module is installed in the QSFP port
D9	Green	25GMAC5	An SFP module is installed in 25G MAC5 SFP port
D10	Green	25GMAC6	An SFP module is installed in 25G MAC6 SFP port
D11	Green	USB1_5V	5 V power is supplied to the USB #1 connector for external devices
D13	Green	USB2_5V	5 V power is supplied to the USB #2 connector for external devices

2.17.1 Multi-status LEDs

The board includes eight multi-status LEDs that indicate hardware activity; however, software can override these LEDs to use them for debugging purposes. The table below describes the functions of the multi-status LED arrays.

Table 2-19. LED array functions

LED	Startup (from power on to power-up complete + 2 seconds)	Normal (after 2 seconds)	User-defined (if register CTL[1] (LED) = 1)
M7	Power Sequencer state (see Table 2-20)	"Idle" pattern, a pattern shown to indicate that the FPGA has completed all startup activities	M[7:0] reflect contents of the LED register
M6			
M5			
M4		Off always	
M3	Reset Sequencer state (see Table 2-21)	Live I2C1_SCL activity	
M2		Live I2C remote activity	
M1		Same as M[3:2], except that short pulses are stretched to 500 ms for easier detection	
M0			

NOTE

The LX2160ARDB power up voltage sequence diagram (LX2160ARDB Reference Manual) lists the power supplies assigned to each tier.

Table 2-20. Power Sequencer state

State	LED: M[7:4]	Description
IDLE	1110 = 0xE	Waiting for power-on events (for example, switch)
WAIT_ATX	0000 = 0x0	Waiting for ATX PSU to report stable
EN_TIER1	0001 = 0x1	Enable tier 1 PSUs, wait for tier 1 power-good reports
EN_TIER2	0010 = 0x2	Enable tier 2 PSUs, wait for tier 2 power-good reports
EN_TIER3	0011 = 0x3	Enable tier 3 PSUs, wait for tier 3 power-good reports
EN_TIER4	0100 = 0x4	Enable tier 4 PSUs, wait for tier 4 power-good reports
WAIT_ALL	0110 = 0x6	Wait for all unmanaged PSUs to report power-good
PG_FAIL	0111 = 0x7	All power supplies were not stable within 1800*30 ns after the last power was enabled
STABLE	1000 = 0x8	Power sequencing complete. Wait for power-off events.
DISABLE	1101 = 0xD	Disable tiers 4..1 PSUs, in that order, with 1 ms delay
FAULT	1111 = 0xF	Fault occurred. Power supplies were shut down due to thermal faults or die rotation errors.

Table 2-21. Reset Sequencer state

State	LED: M[3:0]	Description
IDLE	0000 = 0x0	Waiting for initial reset events
RECONFIG	0010 = 0x2	Update configuration from registers
CLOCK_LOCK	0101 = 0x5	Wait for clock PLLs to stabilize
RELEASE_ALL	0110 = 0x6	Release all hardware resets except DUT
RELEASE_DUT	0111 = 0x7	Release DUT from reset
STABLE	1000 = 0x8	Reset sequencing complete. Wait for reset events.
RESET_REQ	1001 = 0x9	Start reset due to DUT RESET_REQ_B
PORESET	1010 = 0xA	Start reset due to JTAG_RST_B
RST_WATCH	1011 = 0xB	Start reset due to watchdog timeout
RST_BY_REG	1100 = 0xC	Start reset due to setting register bit RST_CTL[RST] = 1
RST_BY_SW	1101 = 0xD	Start reset due to pushbutton switch
RECONFIG	1110 = 0xE	Start reset due to reconfig request via RCFG[GO] = 1
POST_RST	1111 = 0xF	Wait for reset requests to clear

2.18 DIP switches

The LX2160ARDB provides dual inline package (DIP) switches to allow easy configuration of the system for the most popular board options. These switches are stored in BRDCFG and DUTCFG registers by CPLD before being used, allowing software (either local or remote) to reconfigure the system as needed.

The table below explains the DIP switches available in the LX2160ARDB. For each DIP switch:

- If the switch is up (on), the value is 1
- If the switch is down (off), the value is 0

Table 2-22. Switch settings

<table>
<tr><th>Switch</th><th>Supported function</th><th>Description</th></tr>
<tr><td>SW1[1:4]</td><td>RCW fetch location
CFG_RCW_SRC[3:0]</td><td>SW_RCW_SRC[3:0]
0000: Hard-coded RCW
1000: SDHC1: SD card
1001: SDHC2: eMMC
1010: I2C boot EEPROM
1100: XSPI sNAND, 2 KB pages
1101: XSPI sNAND, 4 KB pages
1111: XSPI serial NOR, 24-bit address (default setting)</td></tr>
<tr><td>SW1[5]</td><td>Reset mode
RESET_REQ_B</td><td>SW_RST_MODE
0: Ignore RESET_REQ_B
1: Trigger system reset on assertion of RESET_REQ_B (default setting)</td></tr>
<tr><td>SW1[6:8]</td><td>XSPI_A device mapping
CFG_XSPI_MAP[3:0]</td><td>SW_XMAP[2:0]: Controls how XSPI_A chip-selects are connected to devices/peripherals.
<table>
<tr><th>Bit value</th><th>XSPI_A_CS0</th><th>XSPI_A_CS1</th><th>Description</th></tr>
<tr><td>000 (default setting)</td><td>DEV#0</td><td>DEV#1</td><td>Boot from default flash memory</td></tr>
<tr><td>001</td><td>DEV#1</td><td>DEV#0</td><td>Boot from alternative flash memory</td></tr>
<tr><td>010</td><td>QSPI emulator</td><td>DEV#0</td><td>Boot from QSPI emulator, program default flash memory</td></tr>
<tr><td>011</td><td>QSPI emulator</td><td>DEV#1</td><td>Boot from QSPI emulator, program alternative flash memory</td></tr>
<tr><td>100</td><td>DEV#0</td><td>QSPI emulator</td><td>Emulator access</td></tr>
</table></td></tr>
<tr><td>SW2[1]</td><td>PCIe Spread-Spectrum enable</td><td>SW_SPREAD</td></tr>
</table>

Table continues on the next page...

Table 2-22. Switch settings (continued)

Switch	Supported function	Description
	CFG_SPREAD	• 0: 100 MHz clocks for PCIe slots are fixed (default setting) • 1: 100 MHz clocks for PCIe slots are spread-spectrum modulated
SW2[2]	CS4223 configuration CFG_40GE_ROM	SW_P40IN • 0: CS4223 40 GbE PHY is not self-configured (default setting) • 1: CS4223 40 GbE PHY is self-configured on reset
SW2[3]	PCIe slot clock enable CFG_CLKEN_SLOT[1:2]_B	SW_SLOTCLK • 0: PCIe slots are clocked only when a card is installed (default setting) • 1: PCIe slots are clocked always
SW2[4]	CS4223 MDC clock generation	SW_MDC40G_EN • 0: CS4223 does not receive clock during PORESET_B (default setting) • 1: CS4223 receives ~1 MHz clock during PORESET_B
SW2[5]	SDHC voltage control	SW_SDHC_VCTL • 0: EVDD switches between 1.8 V and 3.3 V as required (default setting) • 1: EVDD locked to 1.8 V only. Only low-voltage (LV) SDHC cards are supported in this mode.
SW2[6]	Unused CFG_ENG_USE0	SW_ENGUSE0 Reserved with 1 as the default setting
SW2[7]	Unused CFG_ENG_USE1	SW_ENGUSE1 Reserved with 1 as the default setting
SW2[8]	DDR clock source selection CFG_ENG_USE2	SW_ENGUSE2 • 0: DDR clocked from DDRCLK pin (default setting) • 1: DDR clocked from differential SYSCLK
SW3[1:3]	Device type selection TEST_SEL_B, CFG_SVR[0:1]	SW_TESTSEL_B + SW_SVR[0:1] • 011: LX2120A/E • 101: LX2080C/E • 111: LX2160A/E (default setting) • All other values are reserved
SW3[4]	SoC use CFG_SOC_USE	SW_SOCUSE • 1: Normal mode (default setting) **NOTE:** Do not change the default setting of this switch.
SW3[5:6]	CPU device override	SW_CPU_SEL • 00: Override to LS2-family device • 01: Override to LX2-family device • 10: Reserved • 11: Reserved (default setting) **NOTE:** This switch's settings are ignored if SW3[7] is set to 0.
SW3[7]	Force CPU selection	SW_CPU_FORCE • 0: Normal mode (default setting) • 1: Use SW_CPU_SEL instead of CPU_ID **NOTE:** Do not change the default setting of this switch.
SW3[8]	Unused	Reserved with 0 as the default setting
SW4[1]	Bypass mode	SW_BYPASS_B

Table continues on the next page...

Table 2-22. Switch settings (continued)

Switch	Supported function	Description
		• 0: Disable thermal monitors and other alarms • 1: Normal operation (default setting)
SW4[2]	Automatic power on	SW_AUTO_ON • 0: Normal power on/off (default setting) • 1: Always power up
SW4[3]	System configuration write protect CFG_MEM_WP	SW_CFG_WP • 0: Allow writes to SYSID and I2C flash • 1: Write-protect SYSID and I2C flash (default setting)
SW4[4]	JTAG Scan mode TBSCAN_EN_B	SW_TBSCAN • 0: Boundary Scan mode • 1: Debugging mode (default setting)
SW4[5]	Boot Box mode	SW_BOOTBOX_B • 0: Enable Boot Box mode • 1: Normal operating mode (default setting)
SW4[6]	VDD power enable	SW_VDD_DIS • 0: Enable VDD power supply (default setting) • 1: Disable VDD power supply
SW4[7:8]	General purpose CFG_GPIN[7:6]	SW_GPIN[7:6] • 00: Software or end-user defined (default setting)

The table below summarizes the default switch settings of the LX2160ARDB DIP switches.

Table 2-23. Default switch settings

DIP switch	Default setting
SW1	1111_1000
SW2	0000_0110
SW3	1111_1100
SW4	1011_1000

2.19 System controller

The LX2160ARDB system controller (or “CPLD” for short) controls the operation of the system, including:

- AC power supply control
- Onboard regulator control and sequencing
- Reset assertion to processor and devices
- Processor and system configuration

- Interrupt management
- System alert monitoring and status display
- Remapping of system boot devices
- Handling of board control and status registers

The following two figures show the system controller architectural details.

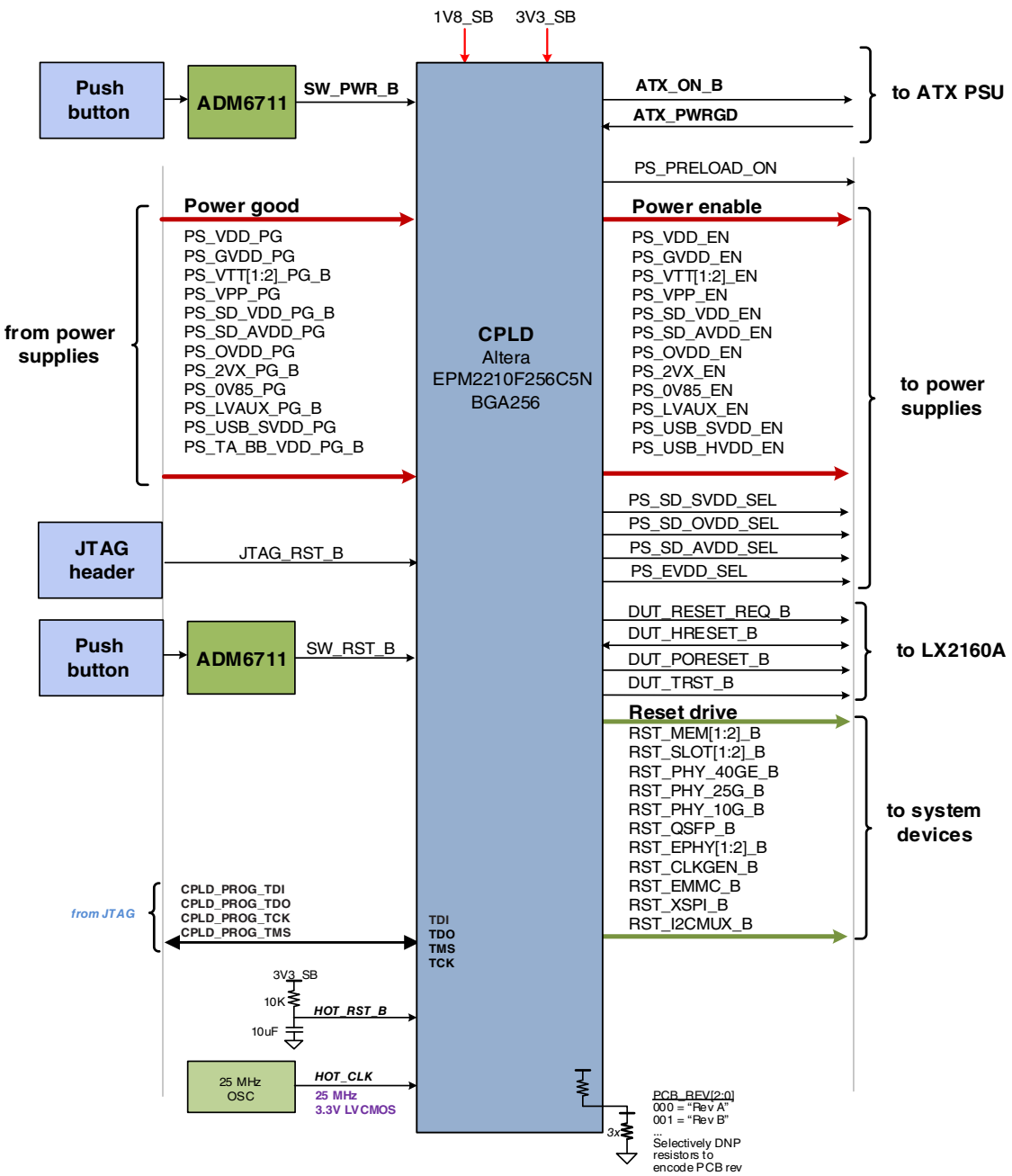


Figure 2-27. System controller architecture

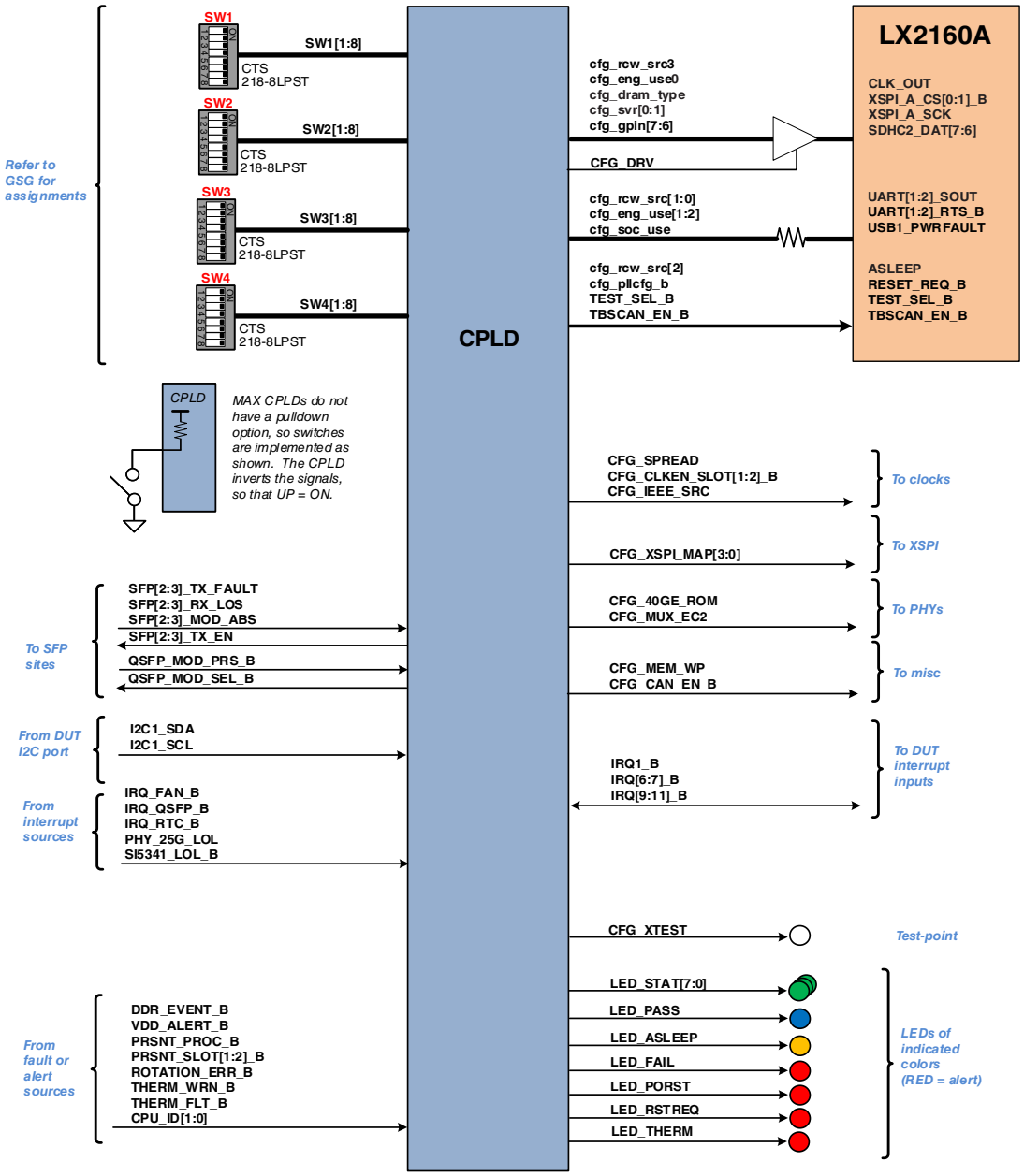


Figure 2-28. System controller architecture (continued)

The system controller is implemented in a 256-ball micro-BGA Altera CPLD, EPM2210F256C5N.

The system controller is powered continuously using the 3.3 V and 1.8 V regulators, powered from the ATX PSU +5 V standby power. This allows it to control all aspects of board bring-up, including initial power sequencing.

2.19.1 System configuration

The system controller uses switches to configure the target system into various modes. Switches are sampled and stored in BRDCFG and DUTCFG registers. BRDCFG registers are always active, and software may change them to result in immediate changes to the system configuration. DUTCFG registers are used to control processor configuration pins that are only sampled during PORESET_B, such as RCW_SRC in DUTCFG0. Changes to DUTCFG registers only take effect on the next reset or reconfiguration event. The following figure shows the configuration hardware arrangement.

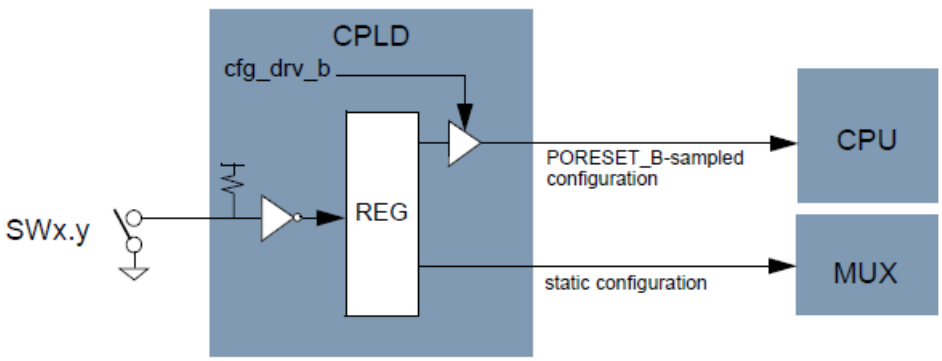


Figure 2-29. Configuration sampling

Note that switches cause a short to ground when closed. To make it easier to set and read switches, values are inverted in the CPLD, so that when a switch is on, the value used is 1.

All switches can be read from software to easily determine the system configuration for reporting purposes (see the "Core Management Space Registers" section of the "CPLD Programming Model" chapter).

The table below describes the LX2160A reset configuration signals.

Table 2-24. Processor configuration settings

Configuration signal	LX2160A primary signal	DIP switch	CPLD register	Description
CFG_RCW_SRC3	CLK_OUT	SW1[1:4]	DUTCFG0[3:0]	Specifies RCW fetch location
CFG_RCW_SRC2	ASLEEP			
CFG_RCW_SRC1	UART1_SOUT			
CFG_RCW_SRC0	UART2_SOUT			
CFG_SVR[0:1]	XSPI1_A_CS[0:1]_B	SW3[2:3]	DUTCFG2[2:1]	Silicon variations
TEST_SEL_B[1]	TEST_SEL_B	SW3[1]	DUTCFG2[0]	Silicon variations
CFG_ENG_USE0	XSPI1_A_SCK	SW2[6]	DUTCFG11[7]	Specifies whether single ended or differential clock is used in the SoC

Table continues on the next page...

Table 2-24. Processor configuration settings (continued)

Configuration signal	LX2160A primary signal	DIP switch	CPLD register	Description
CFG_ENG_USE1	UART1_RTS_B	SW2[7]	DUTCFG11[6]	Undefined option
CFG_ENG_USE2	UART2_RTS_B	SW2[8]	DUTCFG11[5]	Specifies whether DDRCLK pin or differential SYSCLK is used to clock DDR
CFG_SOC_USE	USB1_DRVVBUS	SW3[4]	DUTCFG6[0]	Undefined option
CFG_GPIN[7:6]	SDHC2_DAT[3:2]	SW4[7:8]	DUTCFG12[7:6]	User defined
TBSCAN_EN_B	TBSCAN_EN_B	SW4[4]	CTL[7]	Controls whether the JTAG operates in Boundary Scan or Debug mode

1. TEST_SEL_B is a static signal (constantly driven), unlike most other processor configuration signals.

All other configuration signals are static and unrelated to the processor. The following table summarizes these configuration signals.

Table 2-25. Non-processor configuration settings

Configuration signal	DIP switch	CPLD register	Description
CFG_XSPI_MAP[0:3]	SW1[6:8]	BRDCFG0[7:5]	Controls how XSPI_A chip-selects are connected to devices/peripherals
CFG_MUX_EC2	-	BRDCFG4[7]	Controls the configuration of Ethernet controller 2
CFG_IEEE_SRC	-	BRDCFG4[6]	Selects the source for IEEE clock
CFG_CAN_EN_B	-	BRDCFG4[5]	Enables/disables CAN transceivers
CFG_40GE_ROM	SW2[2]	BRDCFG4[4]	Controls the configuration of the CS4223 40 GbE PHY
CFG_SPREAD	SW2[1]	BRDCFG4[0]	Controls whether clocks for PCIe slots are spread-spectrum modulated or fixed
CFG_MEM_WP	SW4[3]	CTL[3]	Allows/prevents write to SYSID and I2C flash

2.19.2 System startup

The system controller manages the orderly startup of the system by managing power enables and reset assertion (including device configuration), in the order shown in the table below.

Table 2-26. Startup sequence

Controller	Step	Action	Description
Power sequencer	1	Wait for power-on event.	Triggered by the SW_PWR_B signal, or by setting switch SW_AUTO_ON=1.
	2	Enable ATX power supply.	Enable ATX PSU, wait for it to report “power good”. LX2160A PORESET_B is asserted during power-up.

Table continues on the next page...

Table 2-26. Startup sequence (continued)

Controller	Step	Action	Description
	3	Apply power to group 1 power supplies.	Enable group 1 power supplies, wait for all members to report “power good” (if supported): • 0V85 • 0V9 • 1V2 • 2V1 • 2V5 • OVDD • EVDD • USB_SVDD
	4	Apply power to group 2 power supplies.	Enable group 2 power supplies, wait for all members to report “power good” (if supported): • VDD • SD_SVDD
	5	Apply power to group 3 power supplies.	Enable group 3 power supplies, wait for all members to report “power good” (if supported): • SD_OVDD • GVDD • VTT1 • VTT2
	6	Complete power sequencer; trigger reset sequencer.	Control transfers from power to reset handlers. The power sequencer watches for power switch events and will restart at power sequencer step 1 if any are detected.
Reset sequencer	1	Assert all resets.	LX2160A PORESET_B is asserted if not already asserted. Device resets are asserted: • RST_PHY_40GE_B • RST_PHY_25G_B • RST_PHY_10G_B • RST_EPHY[1:2]_B • RST_SLOT[1:2]_B • RST_MEM[1:2]_B • RST_QSFP_B • RST_XSPI_B • RST_EMMC_B • RST_IEEESLT_B • RST_I2CMUX_B The LX2160A processor asserts ASLEEP and HRESET_B in response. ASLEEP is monitored with an LED, otherwise the signals are ignored.
	2	Wait for reset clear.	Wait for reset assertion to be released. The reset sequencer will stall as long as any reset input is asserted: • JTAG_RST_B • SW_RST_B
	3	Sample switches.	Internal registers are reset to default values. Registers that default to switch values are set now.

Table continues on the next page...

Table 2-26. Startup sequence (continued)

Controller	Step	Action	Description
	4	Drive configuration values.	Reset-sampled configuration signals are driven: • CFG_RCW_SRC[3:0] • CFG_SVR[0:1] • CFG_ENG_USE[0:2] • CFG_SOC_USE • CFG_GPIN[7:6] Static (constant) configuration signals are driven: • CFG_XSPI_MAP[0:3] • CFG_MUX_EC2 • CFG_IEEE_SRC • CFG_CAN_EN_B • CFG_40GE_ROM • CFG_SPREAD • CFG_MEM_WP • CFG_CLKEN_SLOT[1:2] The CFG_DRV_B signal is asserted now, to help with the few configuration signals that cannot be driven by the CPLD.
	5	Release resets.	Release all resets shown in reset sequencer step 1. The processor samples reset pins at this time.
	6	Tristate reset-sampled pins.	Three SYSCLK periods after step 5: De-assert CFG_DRV_B. Tristate configuration signals drive outputs. This ensures proper configuration hold time. The CPLD is no longer involved in reset activity.
	7	Processor reset.	The LX2160A processor begins loading RCW data from the specified RCW source location. When RCW loading is complete, the LX2160A processor de-asserts HRESET_B and ASLEEP. If RCW data is correct, then the system will start running the code. If there is an error, then RESET_REQ_B is asserted and the system halts.
	8	Reset sequence complete.	The CPLD has finished reset management. The reset sequencer watches for reset switch events and will restart at reset sequencer step 1 if any are detected.

Chapter 3
Qixis Programming Model

The system controller CPLD contains many registers which may be used to monitor and control both the processor and hardware on the RDB. A 3-pin header on the system allows remote monitoring/control of the system, or the processor can access these registers itself using I2C port 1, using the standard address of 0x66. This address and the register layout adheres to the QixMin (minimal Qixis) standards, allowing easier code reuse across platforms. This chapter explains each of the registers in the register block.

This table shows the register memory map for Qixis.

Table 3-1. Qixis Register Memory Map

Offset	Register	Width (In bits)	Access	Reset value
000h	Identification (ID)	8	RO	01000010b
001h	Board Version (VER)	8	RO	11b
002h	Qixis Version (QVER)	8	RO	00000001b
003h	Programming Model (MODEL)	8	RO	01000000b
004h	Minor Revision (MINOR)	8	RW	00000101b
005h	General Control (CTL)	8	RW	00000x00b
006h	Auxiliary (AUX)	8	RW	00000000b
009h	System Status (STAT_SYS)	8	RO	000x0000b
00Ah	Alarm (ALARM)	8	RO	10000010b
00Bh	Presence Detect 1 (STAT_PRES1)	8	RO	0xx0xxxxb
00Ch	Presence Detect 2 (STAT_PRES2)	8	RO	xxxxxx11b
00Eh	LED Control (LED)	8	RW	00000000b
010h	Reconfiguration Control (RCFG)	8	RW	0010x00xb
018h	SFP CSR 1 (SFP1)	8	RW	10000000b
019h	SFP CSR 2 (SFP2)	8	RW	10110000b
01Ah	SFP CSR 3 (SFP3)	8	RW	10110000b
01Dh	LOS Status (LOS)	8	RO	00000000b
01Fh	Watchdog (WATCH)	8	RW	xxxxxxxb
021h	Power Control 2 (PWR_CTL2)	8	RW	00000000b
022h	Power Event Trace (PWR_EVENT)	8	RO	00000000b

Table continues on the next page...

Table 3-1. Qixis Register Memory Map (continued)

Offset	Register	Width (In bits)	Access	Reset value
024h	Power Status 0 (PWR_MSTAT)	8	RO	110010xxb
025h	Power Status 1 (PWR_STAT1)	8	RO	11111111b
026h	Power Status 2 (PWR_STAT2)	8	RO	1xx11111b
030h	Clock Speed 1 (CLK_SPD1)	8	RO	00000000b
033h	Clock ID/Status (CLK_ID)	8	RO	00000000b
040h	Reset Control (RST_CTL)	8	RW	00xx0000b
041h	Reset Status (RST_STAT)	8	RO	00000000b
042h	Reset Event Trace (RST_REASON)	8	RO	xxxx0000b
043h	Reset Force 1 (RST_FORCE1)	8	RW	00000000b
044h	Reset Force 2 (RST_FORCE2)	8	RW	00000000b
045h	Reset Force 3 (RST_FORCE3)	8	RW	00000000b
04Bh	Reset Mask 1 (RST_MASK1)	8	RW	00000000b
04Ch	Reset Mask 2 (RST_MASK2)	8	RW	00000000b
04Dh	Reset Mask 2 (RST_MASK3)	8	RW	00000000b
050h	Board Configuration 0 (BRDCFG0)	8	RW	xxx00000b
051h	Board Configuration 1 (BRDCFG1)	8	RO	00000000b
052h	Board Configuration 2 (BRDCFG2)	8	RO	xxxx0000b
053h	Board Configuration 3 (BRDCFG3)	8	RO	00000000b
054h	Board Configuration 4 (BRDCFG4)	8	RW	000x0x0xb
060h	DUT Configuration 0 (DUTCFG0)	8	RW	0000xxxxb
061h	DUT Configuration 1 (DUTCFG1)	8	RW	xxxxxxxb
062h	DUT Configuration 2 (DUTCFG2)	8	RW	xxxxxxx1b
066h	DUT Configuration 6 (DUTCFG6)	8	RW	1xxxxxxxb
06Bh	DUT Configuration 11 (DUTCFG11)	8	RW	xxxxxxxxb
06Ch	DUT Configuration 12 (DUTCFG12)	8	RW	xxxxxxxxb
090h	Interrupt Status 0 (IRQSTAT0)	8	RO	11xxxx11b
091h	Interrupt Status 1 (IRQSTAT1)	8	RO	111111xxb
094h	Interrupt Control 0 (IRQCTL0)	8	RW	00000000b
096h	Interrupt Control 2 (IRQCTL2)	8	RW	00000000b
098h	Interrupt Drive 0 (IRQDRV0)	8	RW	00000000b
099h	Interrupt Drive 1 (IRQDRV1)	8	RW	00000000b
09Ah	Interrupt Drive 2 (IRQDRV2)	8	RW	00000000b
09Dh	Interrupt Drive 5 (IRQDRV5)	8	RW	00000000b
0D8h	Core Management Address (CMSA)	8	RW	00000000b
0D9h	Core Management Data (CMSD)	8	RW	00000000b
0DCh	Switch Control (SWS_CTL)	8	RW	00000101b
0DDh	Switch Sample Status (SWS_STAT)	8	RO	10000000b

3.1 Register Conventions

An undefined register address does not have any defined register value. Reads and writes to such addresses should be avoided. If you attempt to read such addresses, undefined data is returned. Undefined register addresses may be defined in the future.

For registers which do not define all bits, reserved bits behave as follows:

3.1.1 Reserved Bits

Register	Recommended Actions
DUTCFG	Read as 1. Write ones to unused bits.
others	Read as 0. Write zeroes to unused bits.

Future definitions of reserved bits will maintain backward compatibility with the above rules.

3.2 Resets

The reset values for registers are defined as follows:

3.2.1 Reset Actions

Term	Reset Action
NONE	Register cannot be reset. Applies to read-only registers.
ARST	Auxiliary Reset: registers are reset when the system powers up with standby power, and is never altered by hardware again. Software writes are preserved.
CRST	Control Reset: registers are not reset except under exceptional situations, such as power cycles or watchdog timeout.
RRST	Reconfig Reset: configuration registers are reset as with CRST unless a reconfiguration reset has been requested.
GRST	General Reset: always reset, for any reason.

Generally, a register is wholly affected by only one reset source, however there are exceptions and these are shown with separate reset lines for each reset source.

3.3 Identification Registers

The ID block of registers contain values which identify the board, including major revisions to the board and/or system controller FPGA or CPLD.

3.4 Identification (ID)

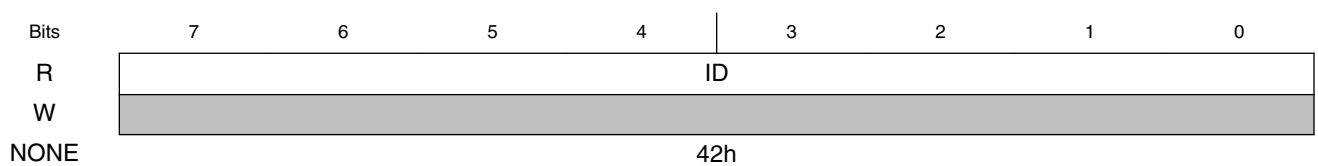
3.4.1 Address

Register	Offset
ID	000h

3.4.2 Function

The ID register contains a unique classification number. This ID number is used by system software to identify board types. The ID number remains same for all board revisions.

3.4.3 Diagram



3.4.4 Fields

Field	Function
7-0 ID	The board-specific identifier for the system. 42h= LX2160ARDB

3.5 Board Version (VER)

3.5.1 Address

Register	Offset
VER	001h

3.5.2 Function

The VER register records version information for the PCB board as well the board architecture. The PCB board version can change without impacting the board architecture version, and vice versa.

3.5.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	ARCH				BRD			
W								
NONE	1				1			

3.5.4 Fields

Field	Function
7-4 ARCH	Board architecture version: 1= V1 2= V2 (etc.) The ARCH field starts at 1 and is only changed if major software-impacting architectural changes to the board occur: changes to PHY vendors, memory devices, etc.
3-0 BRD	PCB board version: 1= Rev A (or pre-release) 2= Rev B (etc.)

Field	Function
	The BRD field reports physical updates to the boards, often incorporating errata fixes or improvements, which may or may not affect software. Software often uses this field to print board version identification, such as: `printf("Board Version: %c", (get_pixis( VER ) & 0Fh) + 'A' - 1 );`

3.6 Qixis Version (QVER)

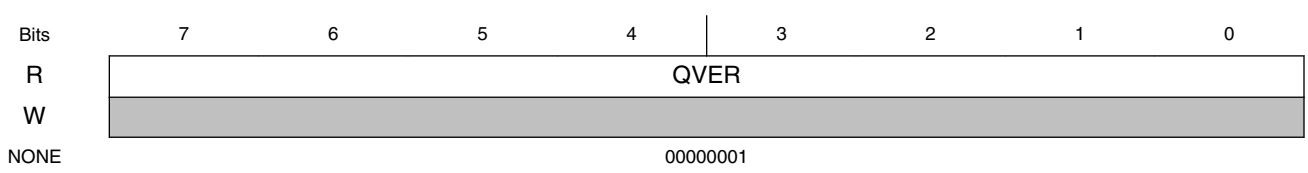
3.6.1 Address

Register	Offset
QVER	002h

3.6.2 Function

The QVER register contains the major version information of the Qixis system controller. Minor revision information may be found in the MINOR register.

3.6.3 Diagram



3.6.4 Fields

Field	Function
7-0 QVER	Qixis version as a decimal value: 1= Version 1 2= Version 2

3.7 Programming Model (MODEL)

3.7.1 Address

Register	Offset
MODEL	003h

3.7.2 Function

The MODEL register contains information about the software programming model version and PCB Bill Of Materials (BOM) information.

3.7.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	MIN	BOM			MODEL			
W								
NONE	0	1	00		0000			

3.7.4 Fields

Field	Function
7 MIN	Programming Model Type: 0= Normal Qixis register set. 1= Subset Qixis register set (QixMin).
6 BOM	Model Register Encoding: 0= Lower 4 bits contain programming model revision (MODEL). 1= reserved.
5-4 -	Reserved.
3-0 MODEL	Model (BOM Version) Information: 0000= No revision: PCB version is 'A', 'B', etc.

Field	Function
	0001= Revision 1 : PCB version is 'A1', 'B1', etc. 0010= Revision 2 : PCB version is 'A2', 'B2', etc. and so forth. Note that this field should be appended to the VER.PCB information only if non-zero.

3.8 Minor Revision (MINOR)

3.8.1 Address

Register	Offset
MINOR	004h

3.8.2 Function

The MINOR (or MINTAG) register can be used to obtain CPLD build information from software. The register returns a subset of the Qixis QTAG facility but more than the limited MINOR facility on other RDBs.

Writes to MINOR select various pieces of information for subsequent read. On reset, the 'minor revision' field is returned, for backward-compatiblity.

Concatenated with the QVER register, it forms the full revision information for the CPLD device. This is typically reported as:

```
qver = get_pixis( QVER );
minor = get_pixis( MINOR );
printf("FPGA: V%d", qver );
if (minor != 0) {
  printf(".%d", minor );
}
```

Note: setting the MINOR/MINTAG register to 5h before reading is optional, as on every reset 05h is the default.

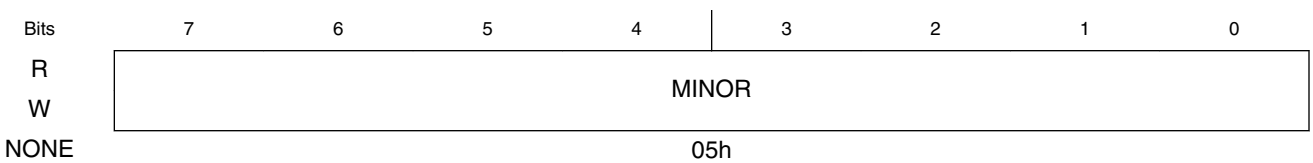
Note: for harmonization with QDS-supporting code (e.g. uboot), if MINOR is zero, do not print it.

Other information can be obtained by writing the corresponding address and reading the register. Reserved fields are found only in QDS QTAG but are present for compatibility. Contents are as follows:

3.8.2 MINTAG Definition

Address Range	Name	Definition
0x00-0x03	TAG	not implemented.
0x05-0x06	MINOR	Minor build version: u16 value in little-endian order.
0x08-0x0B	DATE	Date/time stamp: u32 Unix GMT time value in big-endian order.
0x0C	RELEASE	Released flag: 0=unreleased, non-zero=released.
0x10-0x2F	NAME	not implemented.
0x30-7F	reserved	reserved

3.8.4 Diagram



3.8.5 Fields

Field	Function
7-0 MINOR	Read: Data to read from MINOR/MINTAG. Write: Address of data to read.

3.9 Control and Status Registers

This block of registers control the operation of Qixis itself (or other operations which do not constitute controlling the board or the DUT, which are managed with BRDCFG/ DUTCFG registers) or monitor the status of various things.

3.10 General Control (CTL)

3.10.1 Address

Register	Offset
CTL	005h

3.10.2 Function

The CTL register is used to control various aspects of the target system.

3.10.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	SWLED		AMASK	XTEST		BBOX	LED	FAIL
CRST	00		0	0	0	SW_BOOTBOX_B	0	0

3.10.4 Fields

Field	Function
7-6 SWLED	Controls front-panel power-switch LEDs: when CTL.LED is set
5 AMASK	Alarm Mask Mode: 0= ALARM register reads return alarm status (normal). 1= ALARM register reads return the alarm mask.
4 XTEST	This bit directly drives the XTEST signal, typically driving an SMA connector. The function is user-defined.

Table continues on the next page...

Field	Function
3 -	Reserved.
2 BBOX	Boot-Box Mode: 0= PASS/FAIL LEDs operate normally. 1= Both PASS and FAIL are off. Software can clear this bit to report completion of pass/fail testing (both off indicates testing in progress).
1 LED	Software Diagnostic LED Enable: 0= Diagnostic LEDs operate normally. 1= Software can directly control the M7:M0 monitoring LEDs using the LED register.
0 FAIL	Software Failure Diagnostic LED: 0= FAIL LED is not asserted due to software (it might still be on due to hardware failures). 1= FAIL LED is forced on. Generally, this indicates a software-diagnosed error.

3.11 Auxiliary (AUX)

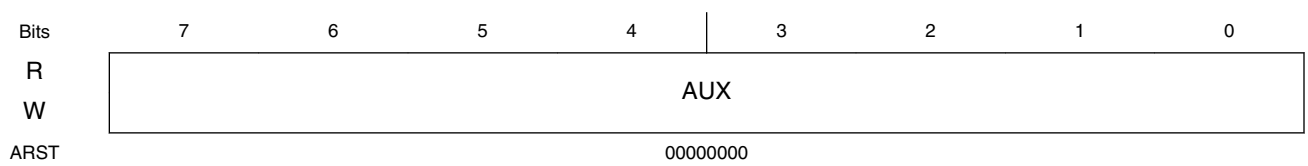
3.11.1 Address

Register	Offset
AUX	006h

3.11.2 Function

The AUX register may be used by software to store information. The AUX register is initialized to zero when the system is powered-up, and never altered by hardware again.

3.11.3 Diagram



3.11.4 Fields

Field	Function
7-0 AUX	User-defined value.

3.12 System Status (STAT_SYS)

3.12.1 Address

Register	Offset
STAT_SYS	009h

3.12.2 Function

The STAT_SYS register reports general system status.

3.12.3 Diagram

Bits	7	6	5	4	3	2	1	0
R				BBOX	ALARMED	ALTERED	ASLEEP	
W								
NONE	000			~SW_BBOX	0	0	0	0

3.12.4 Fields

Field	Function
7-5 -	Reserved.
4 BBOX	BootBox Mode Selected: 0= The system operates normally.

Table continues on the next page...

Field	Function
	1= The system operates in the special BootBox mode. The PASS and FAIL LEDs can be controlled independently, and the watchdog defaults to enabled and 2 seconds.
3 ALARMED	Alarm Status: 0= The system has no active alarms. 1= The system has an active alarms and is asserting FAIL.
2 ALTERED	Reconfiguration Active: 0= The system has been configured as normal. 1= The system has been reconfigured by software.
1 ASLEEP	ASLEEP Reporting: 0= At least one core is actively operating. 1= All cores are in sleep mode.
0 -	Reserved.

3.13 Alarm (ALARM)

3.13.1 Address

Register	Offset
ALARM	00Ah

3.13.2 Function

The ALARM register detects and reports any alarms raised in the QIXIS system.

Write 1 to an ALARM register bit to prevent Qixis from recognizing that alarm condition. By default, all alarms are handled.

3.13.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	FAN	PSEQ	CTL	VTOFF	ORIENT	VDD	TWARN	TALERT
W								
ARST	1	0	0	0	0	0	1	0

3.13.4 Fields

Field	Function
7 FAN	Fan Controller Alert: 0= Fan controller operating normally. 1= Fan controller signalling IRQ. NOTE: This alarm is masked by default.
6 PSEQ	Power Sequencer Fault: 0= Power sequencer operating normally. 1= Power sequencer was unable to power one or more supplies.
5 CTL	Software Fault (CTL[FAIL] was set).
4 VTOFF	VCC Power Supply Temp Off Fault 0= The system is powered normally. 1= The system powers off due to overtemperature of the supply monitored by VT (see bit 5).
3 ORIENT	Processor Orientation Fault: 0= The processor is correctly installed. 1= The processor is installed incorrectly, and the power is turned off forcibly.
2 VDD	VDD Power Supply Temperature Warning: 0= The VDD power supply temperature is within normal limits. 1= The VDD power supply temperature has exceeded warning limits.
1 TWARN	Temperature Fault: 0= The temperature is within normal limits. 1= The temperature has exceeded warning limits. NOTE: This signal may be asserted by either SA56004 thermal monitor. The temperature limits depend upon software programming.
0 TALERT	Temperature Alert: 0= The temperature is within normal limits. 1= The temperature has exceeded fault limits. NOTE: This signal may be asserted by either SA56004 thermal monitor. The temperature limits depend upon software programming.

3.14 Presence Detect 1 (STAT_PRES1)

3.14.1 Address

Register	Offset
STAT_PRES1	00Bh

3.14.2 Function

The STAT_PRES1 register detects the presence and type of processor installed.

3.14.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	DUT	EFFID		FORCED			CPUID	
W								
NONE	0	XX		0	11		XX	

3.14.4 Fields

Field	Function
7 DUT	Processor Present: 0= A processor is detected (soldered-in or socketed). 1= No device detected.
6-5 EFFID	Effective Processor ID: 00= (reserved) 01= LX2160A installed. 10= (reserved) 11= LX2168A installed.
4 FORCED	Processor Override: 0= Processor type (EFFID) is based on device. 1= Processor type (EFFID) was overridden using SW_CPU_FORCE.
3-2 -	Reserved.
1-0 CPUID	Normal Processor ID: Same values as EFFID, but unaltered by SW_CPU_FORCE.

3.15 Presence Detect 2 (STAT_PRES2)

3.15.1 Address

Register	Offset
STAT_PRES2	00Ch

3.15.2 Function

The STAT_PRES2 register detects the installation of cards in various PCI Express or SGMII slots.

3.15.3 Diagram

Bits	7	6	5	4	3	2	1	0
R							SLOT2	SLOT1
W								
NONE	111111						1	1

3.15.4 Fields

Field	Function
7-2 -	Reserved.
1 SLOT2	(same as SLOT1)
0 SLOT1	0= a card is installed. 1= no card is installed.

3.16 LED Control (LED)

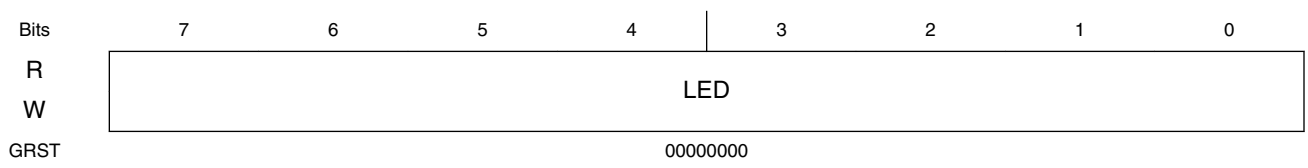
3.16.1 Address

Register	Offset
LED	00Eh

3.16.2 Function

The LED register can be used to directly control the monitoring LEDs (M7-M0) for software debugging or other purposes. Direct control of the LEDs is possible only when CTL[LED] is set to 1; otherwise they are used to display general system activity.

3.16.3 Diagram



3.16.4 Fields

Field	Function
7-0 LED	LED Status Control: 0= LED M[bitno] is off. 1= LED M[bitno] is on.

3.17 Reconfiguration Registers

This block of registers controls the operation of the reconfiguration system, which is used to alter the configuration of the board or processor into different voltages, SYSCLK frequencies, boot device selections, or any other configuration controlled by a BRDCFG or DUTCFG register.

3.18 Reconfiguration Control (RCFG)

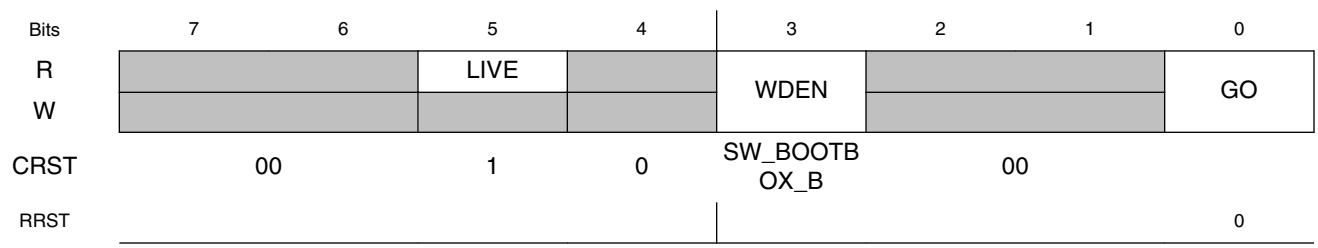
3.18.1 Address

Register	Offset
RCFG	010h

3.18.2 Function

The RCFG register is used to control the reconfiguration sequencer.

3.18.3 Diagram



3.18.4 Fields

Field	Function
7-6 -	Reserved.
5 LIVE	Immediate changes for BRDCFG registers: 1= BRDCFG registers outputs occur immediately. For QixMin, LIVE is always 1.
4	Reserved.

Table continues on the next page...

Field	Function
-	
3 WDEN	Watchdog Enable: 0= The watchdog is not enabled during reconfiguration. 1= The watchdog is enabled during reconfiguration. If not disabled within 2^29 clock cycles (> 8 minutes), the system is reset. NOTE: This is not a highly-secure watchdog; software can reset this bit at any time and disable the watchdog.
2-1 -	Reserved.
0 GO	Reconfiguration Start: 0= Reconfiguration sequencer is idle. 1= On the 0-to-1 transition, the reconfiguration process begins.

3.19 SFP CSR 1 (SFP1)

3.19.1 Address

Register	Offset
SFP1	018h

3.19.2 Function

The SFP1 register controls and monitors the zQSFP+ cage used with the 40GE PHY (40G MAC2).

3.19.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	PRS						LPMODE	SEL
W	PRS							
CRST	1	0	0	0	0	0	0	0

3.19.4 Fields

Field	Function
7 PRS	QSFP_MOD_PRS_B Status: 0= A QSFP module is installed in the QSFP cage. 1= No QSFP module is detected.
6-4 -	Reserved.
3-2 -	Reserved.
1 LPMODE	QSFP_LPMODE Control: 0= QSFP module is in normal power mode. 1= QSFP module is in low-power mode.
0 SEL	QSFP_MOD_SEL_B Control: 0= QSFP module is enabled. 1= QSFP module is disabled.

3.20 SFP CSR 2 (SFP2)

3.20.1 Address

Register	Offset
SFP2	019h

3.20.2 Function

The SFP2 register controls and monitors the SFP+ cage used with the 25G PHY #1 (25G MAC5).

3.20.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	PRS_B		TXFLT	RXLOS				TXEN_B
W	PRS_B		TXFLT	RXLOS				
CRST	1	0	1	1	000			0

3.20.4 Fields

Field	Function
7 PRS_B	SFP2_MOD_ABS Status: 0= An SFP module is installed in the SFP cage. 1= No SFP module is detected.
6 -	Reserved.
5 TXFLT	SFP2_TX_FAULT Status: 0= SFP module reports no transmit errors. 1= SFP module reports transmit fault.
4 RXLOS	SFP2_RX_LOS Status: 0= SFP module reports no receive errors. 1= SFP module reports receive loss-of-signal.
3-1 -	Reserved.
0 TXEN_B	SFP2_TX_EN Control: 0= SFP module transmitter is enabled. 1= SFP module transmitter is disabled.

3.21 SFP CSR 3 (SFP3)

3.21.1 Address

Register	Offset
SFP3	01Ah

3.21.2 Function

The SFP3 register controls and monitors the SFP+ cage used with the 25G PHY #1 (25G MAC6).

3.21.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	PRS_B		TXFLT	RXLOS				TXEN_B
W	PRS_B		TXFLT	RXLOS				
CRST	1	0	1	1	000			0

3.21.4 Fields

Field	Function
7 PRS_B	SFP3_MOD_ABS Status: 0= An SFP module is installed in the SFP cage. 1= No SFP module is detected.
6 -	Reserved.
5 TXFLT	SFP3_TX_FAULT Status: 0= SFP module reports no transmit errors. 1= SFP module reports transmit fault.
4 RXLOS	SFP3_RX_LOS Status: 0= SFP module reports no receive errors. 1= SFP module reports receive loss-of-signal.
3-1 -	Reserved.
0 TXEN_B	SFP3_TX_EN Control: 0= SFP module transmitter is enabled. 1= SFP module transmitter is disabled.

3.22 LOS Status (LOS)

3.22.1 Address

Register	Offset
LOS	01Dh

3.22.2 Function

The LOS register reports LOS (Loss Of Signal) or LOL (Loss of Lock) for various interfaces.

3.22.3 Diagram

Bits	7	6	5	4	3	2	1	0
R							CKLOL	RT25G
W								
NONE	000000						0	0

3.22.4 Fields

Field	Function
7-2 -	Reserved.
1 CKLOL	SI5341 Loss of Lock: 0= SI5341 clock synthesize locked. 1= SI5341 clock synthesize has lost lock on outputs.
0 RT25G	Retimer 25G PHY Loss of Lock: 0= Retimer has lock on all lanes. 1= Retimer has lost lock on one or more lanes. Note: Since the 25G retimer services a pair of independent lanes, the global lock reporting is less useful.

3.23 Watchdog (WATCH)

3.23.1 Address

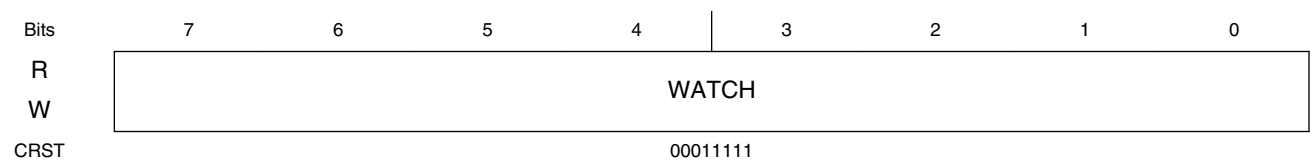
Register	Offset
WATCH	01Fh

3.23.2 Function

The WATCH register selects the watchdog timer value used during the reconfiguration processes. When RCFG[WDEN] enables the watchdog timer, a count down timer begins. If the DUT software does not disable or restart the watchdog timer within the specified limits, the system restarts.

Note that the watchdog timer is not dependent upon a reconfiguration sequence being active. While it is typically enabled along with RCFG[GO] as part of a reconfiguration sequence; in fact, it is independent and can be enabled for any reason.

3.23.3 Diagram



3.23.4 Fields

Field	Function

7-0
WATCH
	Watchdog timer value, as determined by the formula:
	`time-out = [ WATCH * (2.0sec) ] + 2.0sec`
	Examples:
	`11111111=  8 min`
	`00111111=  2 min`
	`00001111=  32 sec`

Field	Function
	00000011= 8 sec 00000000= 2 sec

3.24 Power Control/Status Registers

The power registers provide the ability to monitor general power status, as well as individual power status (for those supplies that have reporting capability). Other registers provide limited power control features (most power control is through the PMBus/I2C interface).

3.25 Power Control 2 (PWR_CTL2)

3.25.1 Address

Register	Offset
PWR_CTL2	021h

3.25.2 Function

The PWR_CTL2 register is used to control system power-on/power-off events.

3.25.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	PWR							
W								
CRST	0	0000000						

3.25.4 Fields

Field	Function
7 PWR	Toggle System Power 0= No action. 1= On the 0-to-1 transition, toggle the system power supply. The bit must be reset to zero before additional power cycles can occur. Qixis interfaces which are powered from system power (as opposed to standby power) cannot power-up the system.
6-0 -	Reserved.

3.26 Power Event Trace (PWR_EVENT)

3.26.1 Address

Register	Offset
PWR_EVENT	022h

3.26.2 Function

The PWR_EVENT register records which events caused power-on or -off events.

3.26.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	PPEVENT				PEVENT			
W								
NONE	0000				0000			

3.26.4 Fields

Field	Function
7-4 PPEVENT	Previous Power Event: This field contains the previous value stored in the PEVENT field.
3-0 PEVENT	Power Event: The field will contain one of the following codes, indicating the event which caused the power change: 0000= No history. 0001= Forced power-off (fault, temp, etc). 0010= Automatic power-up (SW_AUTO_ON is set). 0011= POWER switch used to power on. 0110= ATX PSU dropped power (external event). 0111= POWER switch used to power off. 1010= Thermal fault forced power off. 1111= Unknown.

3.27 Power Status 0 (PWR_MSTAT)

3.27.1 Address

Register	Offset
PWR_MSTAT	024h

3.27.2 Function

The PWR_MSTAT register monitors the overall power status of the board, including that of the main (ATX or other) power supply used to power all other rails.

3.27.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	ATXON	ATXGD		FAULT	PWROK		SSTATE	
W								
NONE	1	1	0	0	1	0	11	

3.27.4 Fields

Field	Function
7 ATXON	Main Power Supply Control Status: 0= Power supply is set to off. 1= Power supply is set to on.
6 ATXGD	Main Power Supply Status: 0= Power supply is off or not yet stable. 1= Power supply is on and stable.
5 -	Reserved.
4 FAULT	Faulted: 0= Power supply system operating normally. 1= Power supply system was shutdown for some reason. Check the ALARM register for details.
3 PWROK	General Power Status: 0= One or more power supplies are off or not yet stable. 1= All power supplies are on and stable.
2 -	Reserved.
1-0 SSTATE	Reports the current power savings level, for those devices which support it. 11= S3 - completely on Note: If a device does not support hardware (i.e external) power savings modes, S3 is always reported.

3.28 Power Status 1 (PWR_STAT1)

3.28.1 Address

Register	Offset
PWR_STAT1	025h

3.28.2 Function

The PWR_STATn registers are used to monitor the status of individual power supplies. If a bit is set to '1', the respective power supply is operating correctly.

Note that unassigned bits default to one, allowing power failure detection to be easily performed (if the value is not FFh, at least one supply is not operating).

Due to the high variability of the hardware devices used, PWR_STATn register bits are not assigned any universally fixed values. For more details, see the target platform documentation.

3.28.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	0V85	2VX	LVAUX	SD_AVDD	SD_VDD		USB	VDD
W								
NONE	1	1	1	1	1	1	1	1

3.28.4 Fields

Field	Function
7 0V85	VCC_0V85 Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
6 2VX	2.1V and 2.5V Power Supply Status: 0= One or both power supplies are disabled or faulted. 1= Power supplies are operating.
5 LVAUX	LVAUX Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.

Table continues on the next page...

Field	Function
4 SD_AVDD	SD_AVDD Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
3 SD_VDD	SD_SVDD and SD_OVDD Power Supply Status: 0= One or both power supplies are disabled or faulted. 1= Power supplies are operating.
2 -	Reserved.
1 USB	USB_sVDD Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
0 VDD	VDD Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.

3.29 Power Status 2 (PWR_STAT2)

3.29.1 Address

Register	Offset
PWR_STAT2	026h

3.29.2 Function

Monitors various power statuses; see PWR_STAT1 for details.

3.29.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	TA_BB			OVDD		VTT2	VTT1	GVDD
W								
NONE	1	11		1	1	1	1	1

3.29.4 Fields

Field	Function
7 TA_BB	TA_BB Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
6-5 -	Reserved.
4 OVDD	OVDD (1.8V) Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
3 -	Reserved.
2 VTT2	VTT2 (DDR block #2) Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
1 VTT1	VTT1 (DDR block #1) Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
0 GVDD	GVDD (1.2V) Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.

3.30 Clock Control Registers

The clock control registers control programmable clock synthesizers used to supply clocks to the processor and associated peripherals.

3.31 Clock Speed 1 (CLK_SPD1)

3.31.1 Address

Register	Offset
CLK_SPD1	030h

3.31.2 Function

The CLK_SPD1 register is used to report the user-selectable speed settings (typically from switches) for the SYSCLK and DDRCLK clocks.

Values in the CLK_SPD1 register are used by boot software accurately initialize timing-dependent parameters, such as for UART baud rates, I2C clock rates, and DDR memory timing.

3.31.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	DDRCLK				SYSCLK			
W								
NONE	0000				0000			

3.31.4 Fields

Field	Function
7-4 DDRCLK	DDRCLK Rate Selection: 0000= 100.00 MHz (fixed) Other values are Reserved.
3-0 SYSCLK	SYSCLK Rate Selection: 0000= 100.00 MHz (fixed) Other values are Reserved.

3.32 Clock ID/Status (CLK_ID)

3.32.1 Address

Register	Offset
CLK_ID	033h

3.32.2 Function

The CLK_ID register is used to identify the arrangement of the clock control registers. Software should check CLK_ID register before attempting to interpret/control the clock control registers.

3.32.3 Diagram

Bits	7	6	5	4	3	2	1	0
R					ID			
W								
NONE	0000				0000			

3.32.4 Fields

Field	Function
7-4 -	Reserved.
3-0 ID	System Clock ID = 0000 (NONE) CLK0= SYSCLK is fixed on this system.

3.33 Reset Control Registers

The reset control register group handles reset behavior configuration and general monitoring of resets.

3.34 Reset Control (RST_CTL)

3.34.1 Address

Register	Offset
RST_CTL	040h

3.34.2 Function

The RST_CTL register is used configure or trigger reset actions.

3.34.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W			REQMD					RST
CRST	00		SW_RST_MODE		000			0

3.34.4 Fields

Field	Function
7-6 -	Reserved.
5-4 REQMD	00= Disabled - do nothing. 01= reserved 10= reserved 11= Normal - assert PORESET_B to DUT to begin normal reset sequence.
3-1 -	Reserved.
0	Reset:

Field	Function
RST	0= Reset sequencer operates normally. 1= Upon transition from 0 to 1, restart the reset sequence.

3.35 Reset Status (RST_STAT)

3.35.1 Address

Register	Offset
RST_STAT	041h

3.35.2 Function

The RST_STAT register reports the current status of various reset-related signals.

3.35.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	WAIT	SYSRST				HRST	PORST	RREQ
W								
NONE	0	0	0	0	0	0	0	0

3.35.4 Fields

Field	Function
7 WAIT	Reset Waiting: 0= Reset sequencer is operating normally. 1= Reset sequencer is in RMT-WAIT state, waiting for permission to proceed.
6 SYSRST	System Reset: 0= System is operating normally. 1= System is in reset.

Table continues on the next page...

Field	Function
5-3 -	Reserved.
2 HRST	HRESET_B status: 0= HRESET_B is not asserted. 1= HRESET_B is asserted.
1 PORST	PORESET_B status: 0= PORESET_B is not asserted. 1= PORESET_B is asserted.
0 RREQ	RESET_REQ_B status: 0= RESET_REQ_B is not asserted. 1= RESET_REQ_B is asserted.

3.36 Reset Event Trace (RST_REASON)

3.36.1 Address

Register	Offset
RST_REASON	042h

3.36.2 Function

The RST_REASON register is used to report the cause of the most-recent reset cycle.

3.36.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	PREV				REASON			
W								
NONE	1111				0000			

3.36.4 Fields

Field	Function
7-4 PREV	Previous reset reason: (see REASON field codes)
3-0 REASON	Reset Reason: 0000= Power-on reset 0001= JTAG_RST_B asserted 0010= (reserved) 0011= RST_CTL[RST] asserted 0100= SW_RST_B switch (chassis or on-board) was pushed. 0101= RCFG[GO] asserted (reconfiguration reset). 0110= RESET_REQ_B assertion (from processor). 1111= No event recorded yet.

3.37 Reset Force 1 (RST_FORCE1)

3.37.1 Address

Register	Offset
RST_FORCE1	043h

3.37.2 Function

The RST_FORCEn registers are used to force reset to a particular device, independent of the general reset sequencer. As long as a bit is set to 1, the reset signal to grouped devices will be asserted.

Resetting a resource while in used by the bootloader or OS will typically cause crashes, etc. Use carefully.

3.37.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	CLK	XSPI	QSFP	I2CMUX	EMMC	MEM3	MEM2	MEM1
GRST	0	0	0	0	0	0	0	0

3.37.4 Fields

Field	Function
7 CLK	1= Assert RST_CLKGEN_B.
6 XSPI	1= Assert RST_XSPI_B.
5 QSFP	1= Assert RST_QSFP_B.
4 I2CMUX	1= Assert RST_I2CMUX_B.
3 EMMC	1= Assert RST_EMMC _B
2 MEM3	Reset DIMMs on DDR port #3 (LX2168A only). 1= Assert RST_MEM3_B
1 MEM2	Reset DIMMs on DDR port #3 1= Assert RST_MEM2_B
0 MEM1	Reset DIMMs on DDR port #1 1= Assert RST_MEM1_B

3.38 Reset Force 2 (RST_FORCE2)

3.38.1 Address

Register	Offset
RST_FORCE2	044h

3.38.2 Function

Asserts selected reset sources. See RST_FORCE1 for details.

3.38.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	EPHY2	EPHY1	PHY10	PHY25	PHY40	TRST	HRST	PORST
GRST	0	0	0	0	0	0	0	0

3.38.4 Fields

Field	Function
7 EPHY2	1= Assert RST_EPHY2_B for the RealTek PHY #2.
6 EPHY1	1= Assert RST_EPHY1_B for the RealTek PHY #1.
5 PHY10	1= Assert RST_PHY_10G_B to the Aquantia AQR107 10Gbps PHY.
4 PHY25	1= Assert RST_PHY_25G_B to the 25Gbps retimer.
3 PHY40	1= Assert RST_PHY_40G_B to the CS4223 40GE PHY.
2 TRST	1= Assert DUT_TRST_B.
1 HRST	1= Assert DUT_HRESET_B. NOTE: This bit only asserts the signal to the DUT; it is not intended to be used as a general system reset.
0 PORST	1= Assert DUT_PORESET_B. NOTE: This bit only asserts the signal to the DUT; it is not intended to be used as a general system reset.

3.39 Reset Force 3 (RST_FORCE3)

3.39.1 Address

Register	Offset
RST_FORCE3	045h

3.39.2 Function

Asserts selected reset sources. See RST_FORCE1 for details.

3.39.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	SLOT1	SLOT2						IEEE
GRST	0	0	00000					0

3.39.4 Fields

Field	Function
7 SLOT1	1= Assert RST_SLOT1_B.
6 SLOT2	1= Assert RST_SLOT2_B.
5-1 -	Reserved.
0 IEEE	1= Force RST_IEEESLT_B.

3.40 Reset Mask 1 (RST_MASK1)

3.40.1 Address

Register	Offset
RST_MASK1	04Bh

3.40.2 Function

The RST_MASKn registers are used to block reset to a particular device, independent of the general reset sequencer. As long as a bit is set to 1, the reset signal to that device or devices will be blocked.

RST_MASKn bits have the same bit definition as their counterparts in RST_FORCEn; refer to Table 5-53 for details.

Note that RST_MASK bits are cleared on AUX reset, and so are usually only cleared by software. This is very different from the RST_FORCE registers.

3.40.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	CLK	XSPI	QSFP	I2CMUX	EMMC	MEM3	MEM2	MEM1
ARST	0	0	0	0	0	0	0	0

3.40.4 Fields

Field	Function
7 CLK	1= Mask RST_CLKGEN_B.
6 XSPI	1= Mask RST_XSPI_B.
5 QSFP	1= Mask RST_QSFP_B.
4 I2CMUX	1= Mask RST_I2CMUX_B.
3	1= Mask RST_EMMC _B

Table continues on the next page...

Field	Function
EMMC	
2 MEM3	Reset DIMMs on DDR port #3 (LX2168A only). 1= Mask RST_MEM3_B
1 MEM2	Reset DIMMs on DDR port #3 1= Mask RST_MEM2_B
0 MEM1	Reset DIMMs on DDR port #1 1= Mask RST_MEM1_B

3.41 Reset Mask 2 (RST_MASK2)

3.41.1 Address

Register	Offset
RST_MASK2	04Ch

3.41.2 Function

Masks selected reset sources. See RST_FORCE1 for details.

3.41.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	EPHY2	EPHY1	PHY10	PHY25	PHY40	TRST	HRST	PORST
ARST	0	0	0	0	0	0	0	0

3.41.4 Fields

Field	Function
7 EPHY2	1= Mask RST_EPHY2_B for the RealTek PHY #2.

Table continues on the next page...

Field	Function
6 EPHY1	1= Mask RST_EPHY1_B for the RealTek PHY #1.
5 PHY10	1= Mask RST_PHY_10G_B to the Aquantia AQR107 10Gbps PHY.
4 PHY25	1= Mask RST_PHY_25G_B to the 25Gbps retimer.
3 PHY40	1= Mask RST_PHY_40G_B to the CS4223 40GE PHY.
2 TRST	1= Mask DUT_TRST_B.
1 HRST	1= Mask DUT_HRESET_B.
0 PORST	1= Mask DUT_PORESET_B.

3.42 Reset Mask 2 (RST_MASK3)

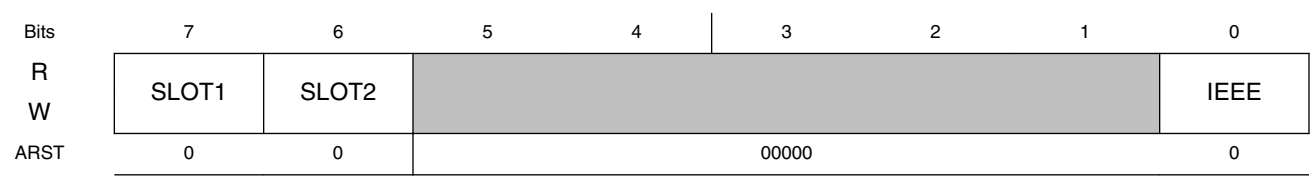
3.42.1 Address

Register	Offset
RST_MASK3	04Dh

3.42.2 Function

Masks selected reset sources. See RST_FORCE1 for details.

3.42.3 Diagram



3.42.4 Fields

Field	Function
7 SLOT1	1= Mask RST_SLOT1_B.
6 SLOT2	1= Mask RST_SLOT2_B.
5-1 -	Reserved.
0 IEEE	1= Mask RST_IEEESLT_B.

3.43 Board Configuration Registers

This block of registers control the configuration of the board. BRDCFG registers are always static, driven at all times power is available. There are up to 16 registers providing up to 128 control options; however, not every platform implements all the registers.

3.44 Board Configuration 0 (BRDCFG0)

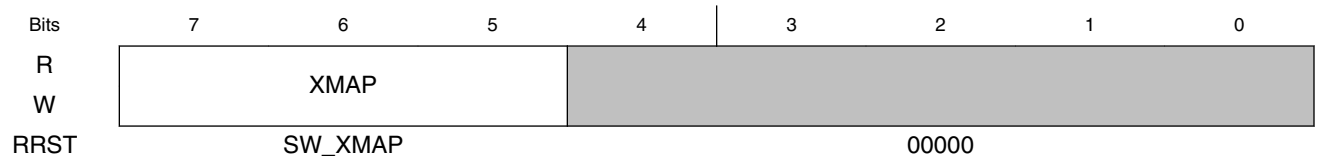
3.44.1 Address

Register	Offset
BRDCFG0	050h

3.44.2 Function

The BRDCFG0 register is commonly used to select IFC and QSPI boot devices.

3.44.3 Diagram



3.44.4 Fields

Field	Function
7-5 XMAP	XMAP controls how XSPI_A chip-selects are connected to devices/peripherals. XSPI_A_CS0 XSPI_A_CS1 ========== ========== 000= DEV #0 DEV #1 001= DEV #1 DEV #0 010= EMU DEV #0 011= EMU DEV #1 100= DEV #0 EMU
4-0 -	Reserved.

3.45 Board Configuration 1 (BRDCFG1)

3.45.1 Address

Register	Offset
BRDCFG1	051h

3.45.2 Function

The BRDCFG1 register shows/controls SYSCLK and DDRCLK speeds.

3.45.3 Diagram

Bits	7	6	5	4	3	2	1	0
R			DDRCLK				SYSCLK	
W								
RRST	00		00		00		00	

3.45.4 Fields

Field	Function
7-6 -	Reserved.
5-4 DDRCLK	DDRCLK Frequency Selection: 00= 100.00 MHz (fixed) All other values are reserved.
3-2 -	Reserved.
1-0 SYSCLK	SYSCLK Frequency Selection: 00= 100.00 MHz (fixed) All other values are reserved.

3.46 Board Configuration 2 (BRDCFG2)

3.46.1 Address

Register	Offset
BRDCFG2	052h

3.46.2 Function

The BRDCFG2 register reporst SerDes clock speeds for SerDes blocks 1 and 2. PCIe clocks may be fixed or spread-spectrum enabled, as selected by BRDCFG4.SPREAD.

3.46.3 Diagram

Bits	7 6	5 4	3 2	1 0
R	SD1CK1	SD1CK2	SD2CK1	SD2CK2
W				
RRST	CPU_ID	11	00	00

3.46.4 Fields

Field	Function
7-6 SD1CK1	SerDes1 Clock #1 (F) Rate: 11= 161.1328125 MHz (fixed)
5-4 SD1CK2	SerDes1 Clock #2 (S) Rate: 11= 161.1328125 MHz (fixed)
3-2 SD2CK1	SerDes2 Clock #1 (F) Rate: 00= 100.0000000 MHz (fixed)
1-0 SD2CK2	SerDes2 Clock #2 (S) Rate: 00= 100.0000000 MHz (fixed)

3.47 Board Configuration 3 (BRDCFG3)

3.47.1 Address

Register	Offset
BRDCFG3	053h

3.47.2 Function

The BRDCFG3 register reports SerDes clock speeds for SerDes block 3. PCIe clocks may be fixed or spread-spectrum enabled, as selected by BRDCFG4.SPREAD.

3.47.3 Diagram

Bits	7	6	5	4	3	2	1	0
R	SD3CK1		SD3CK2					
W								
RRST	00		00		0000			

3.47.4 Fields

Field	Function
7-6 SD3CK1	SerDes3 Clock #1 (F) Rate: 00= 100.0000000 MHz (fixed)
5-4 SD3CK2	SerDes3 Clock #2 (S) Rate: 00= 100.0000000 MHz (fixed)
3-0 -	Reserved.

3.48 Board Configuration 4 (BRDCFG4)

3.48.1 Address

Register	Offset
BRDCFG4	054h

3.48.2 Function

The BRDCFG4 register controls general board configuration.

3.48.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	EC2	IEEECLK	CAN_EN	ROM40G	I2C40G	SLOTCLK	SPRLVL	SPREAD
RRST	0	0	0	SW_P40IN	0	SW_SLOTCLK	0	SW_SPREAD

3.48.4 Fields

Field	Function
7 EC2	Ethernet2 Configuration (net CFG_MUX_EC2): 0= Processor EC2 pins connect to Ethernet PHY #2. 1= Processor EC2 pins connect IEEE slot (alternate function).
6 IEEECLK	IEEE Clock Source Configuration (net CFG_IEEE_SRC): 0= IEEE clock provided by on-board 125.00 MHz reference. 1= IEEE clock provided by IEEE slot pin 10.
5 CAN_EN	CAN I/O Enable (net CFG_CAN_EN_B): 0= CAN transceivers are disabled. 1= CAN transceivers are enabled.
4 ROM40G	40GE PHY ROM Configuration Enable: 0= CS4223 40GE PHY should power up unconfigured. 1= CS4223 40GE PHY should use its configuration EEPROM for initial settings and DSP software load.
3 I2C40G	CS4223 40G PHY I2C Enable ((new CFG_CS4223_I2C_EN): Grants access to the private I2C bus/boot memory used by the CS4223. 0= I2C bus inaccessible. 1= I2C bus accessible.
2 SLOTCLK	SLOTCLK controls whether PCIe slot clocks are enabled always, or only when a device is installed. This may be useful when installing a larger PCIe device in a smaller slot (i.e. an x16 in an x8 slot). 0= Slot clocks enabled only when device installed. 1= Slot clocks enabled always.
1 SPRLVL	PCI Express Spread-Spectrum Spread Level: 0= -0.25% spread. 1= -0.50% spread. Valid for Rev B or later boards only.
0	PCI Express Spread-Spectrum Enable (net CFG_SPREAD):

Field	Function
SPREAD	0= Disabled: PCI-Express 100 MHz clocks (all) are locked. 1= Enabled: PCI-Express 100 MHz clocks (all) are spread-spectrum modulated.

3.49 DUT Configuration Registers

This block of registers control the configuration of the DUT (Device Under Test). DUTCFG registers, unlike BRDCFG registers, are not always driven - they are driven only during the reset configuration sampling interval (PORESET_B assertion), and remain tri-stated thereafter. Refer to the device hardware specification for hardware pin-sampled timing parameters.

3.50 DUT Configuration 0 (DUTCFG0)

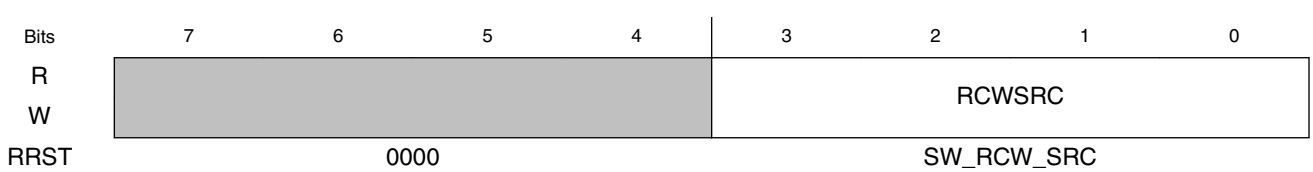
3.50.1 Address

Register	Offset
DUTCFG0	060h

3.50.2 Function

The DUTCFG0 register is used to select the boot device used upon reset (cfg_rcw_src).

3.50.3 Diagram



3.50.4 Fields

Field	Function
7-4 -	Reserved.
3-0 RCWSRC	RCW Source Location (cfg_rcw_src): 0nnn= Hard-coded RCW 1000= SDHC1: SD Card 1001= SDHC2: eMMC 1010= I2C Boot EEPROM 1100= XSPI sNAND, 2KB pages 1101= XSPI sNAND, 4KB pages 1111= XSPI serial NOR, 24bit address

3.51 DUT Configuration 1 (DUTCFG1)

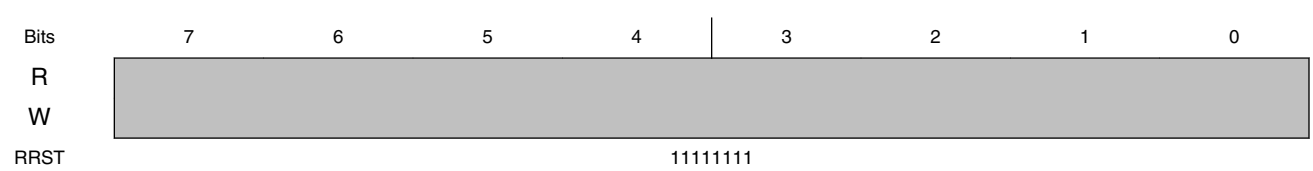
3.51.1 Address

Register	Offset
DUTCFG1	061h

3.51.2 Function

The DUTCFG1 register holds the LSB of cfg_rcw_src values when they are larger than 8 bits. For the LX2160ARDB, this register is ignored.

3.51.3 Diagram



3.51.4 Fields

Field	Function
7-0 -	Reserved.

3.52 DUT Configuration 2 (DUTCFG2)

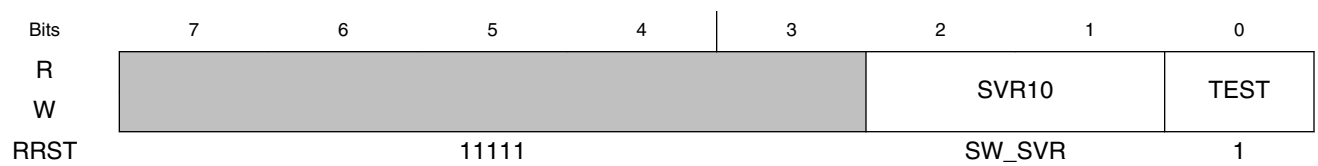
3.52.1 Address

Register	Offset
DUTCFG2	062h

3.52.2 Function

The DUTCFG2 register manages processor device selection (SVR) and internal-only device test features.

3.52.3 Diagram



3.52.4 Fields

Field	Function
7-3	Reserved.

Table continues on the next page...

Field	Function
-	
2-1 SVR10	Controls System Version (config cfg_svr[1:0]): XX= Selected processor variant (refer to the device Reference Manual). NOTE: SVR settings must match installed device.
0 TEST	Controls Test Select (config TEST_SEL_B): X= Test-mode selection. NOTE: Unlike all other DUTCFG bits, TEST_SEL_B is always driven.

3.53 DUT Configuration 6 (DUTCFG6)

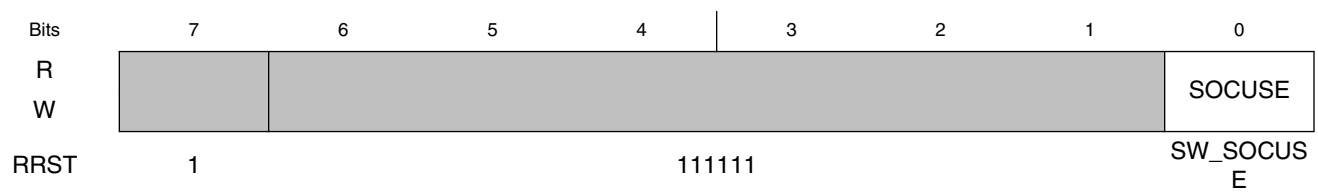
3.53.1 Address

Register	Offset
DUTCFG6	066h

3.53.2 Function

The DUTCFG6 register is used to sample device-specific test modes.

3.53.3 Diagram



3.53.4 Fields

Field	Function
7	Reserved.

Table continues on the next page...

Field	Function
-	
6-1 -	Reserved.
0 SOCUSE	Controls cfg_soc_use. 1= Default.

3.54 DUT Configuration 11 (DUTCFG11)

3.54.1 Address

Register	Offset
DUTCFG11	06Bh

3.54.2 Function

The DUTCFG11 register is used to control the CFG_ENG_USE signals. The function of these bits are defined by silicon engineers for special use.

3.54.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	ENGUSE0	ENGUSE1	ENGUSE2					
RRST	SW_ENGUSE0	SW_ENGUSE1	SW_ENGUSE2			11111		

3.54.4 Fields

Field	Function
7 ENGUSE0	ENG_USE0: Differential Clock Mode (cfg_enguse0): 0= Processor uses differential SYSCLK_P/SYSCLK_N input.

Table continues on the next page...

Field	Function
	1= Processor uses single-ended SYSCLK input.
6 ENGUSE1	ENG_USE1: Reserved (cfg_enguse1): 1= Default value for reserved pins.
5 ENGUSE2	ENG_USE2: DDR Clock Source Select (cfg_enguse2): 0= DDR clocked from DDRCLK pin (default). 1= DDR clocked from differential SYSCLK.
4-0 -	Reserved.

3.55 DUT Configuration 12 (DUTCFG12)

3.55.1 Address

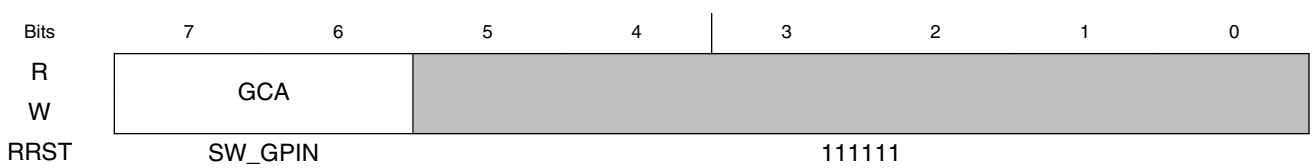
Register	Offset
DUTCFG12	06Ch

3.55.2 Function

The DUTCFG12 register is used to provide the general-purpose GPCFG signals.

These settings are sampled by the processor for customers to use as desired, but have no hardware effects.

3.55.3 Diagram



3.55.4 Fields

Field	Function
7-6 GCA	General Purpose Configuration Inputs (cfg_gpin): XX= Value for cfg_gpin[7:6].
5-0 -	Reserved.

3.56 IRQ Management Registers

The IRQ control and status registers may be used to monitor and control the behavior of various interrupt (IRQ, EVT, and TMPDET) signals.

IRQSTATn registers show the real-time status of connected interrupt pins. Interrupts have device-defined polarities, so no interpretation is made as to whether a signal is considered asserted or deasserted.

IRQCTLn registers allow control of interrupt drive options of level-sensitive or edge-sensitive, with active-high or -low assertion. Not all interrupts have this facility.

IRQDRVn registers allows forcing interrupt pins to a high or low state. The IRQDRV settings take priority over interrupt sources, so these registers may optionally be used to implement interrupt masks.

3.56.1 Interrupt Assignments

Interrupt	Assignment	Has CTL
IRQ1	IN112525 PHY LOL	Y
IRQ6	(none)	N
IRQ7	Fan interrupt (from EMC2305)	N
IRQ9	IN112525 PHY LOL if SFP2 MOD_ABS low	Y
IRQ10	IN112525 PHY LOL if SFP3 MOD_ABS low	Y
IRQ11	zQSFP+ transceiver (40G PHY) interrupt	N
TMPDETB	TMP_DETECT_B	N

3.57 Interrupt Status 0 (IRQSTAT0)

3.57.1 Address

Register	Offset
IRQSTAT0	090h

3.57.2 Function

The IRQ_STAT0 register reports the current level of the IRQ0..IRQ7 signals, if both existing and connected.

3.57.3 Diagram

Bits	7	6	5	4	3	2	1	0
R		IRQ1					IRQ6	IRQ7
W								
NONE	1	1	1111				1	1

3.57.4 Fields

Field	Function
7 -	Reserved.
6 IRQ1	1= IRQ1_B signal is high.
5-2 -	Reserved.
1 IRQ6	1= IRQ6_B signal is high.
0 IRQ7	1= IRQ7_B signal is high.

3.58 Interrupt Status 1 (IRQSTAT1)

3.58.1 Address

Register	Offset
IRQSTAT1	091h

3.58.2 Function

The IRQ_STAT1 register reports the current level of the IRQ8..IRQ12 signals and TA_TMP_DETECT_B, if both existing and connected.

3.58.3 Diagram

Bits	7	6	5	4	3	2	1	0
R		IRQ9	IRQ10	IRQ11		TATMPDET		
W								
NONE	1	1	1	1	1	1	11	

3.58.4 Fields

Field	Function
7 -	Reserved.
6 IRQ9	1= IRQ9_B signal is high.
5 IRQ10	1= IRQ10_B signal is high.
4 IRQ11	1= IRQ11_B signal is high.
3 -	Reserved.

Table continues on the next page...

Field	Function
2 TATMPDET	1= TA_TMP_DETECT_B signal is high.
1-0 -	Reserved.

3.59 Interrupt Control 0 (IRQCTL0)

3.59.1 Address

Register	Offset
IRQCTL0	094h

3.59.2 Function

The IRQCTL0 register allows defining interrupt output modes for IRQ[0:3], where relevant to the target system.

3.59.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W			IRQ1					
CRST	00		00		00		00	

3.59.4 Fields

Field	Function
7-6 -	Reserved.
5-4	Sets mode of IRQ1 output:

Table continues on the next page...

Field	Function
IRQ1	00= Level-sensitive: drive IRQ1 low on interrupt input == 1. 01= Level-sensitive: drive IRQ1 high on interrupt input == 1. 10= Edge-triggered: drive IRQ1 low on a 0-to-1 edge. 11= Edge-triggered: drive IRQ1 high on a 0-to-1 edge. Edge-triggered interrupts are cleared by reading the IRQCTL0 register.
3-2 -	Reserved.
1-0 -	Reserved.

3.60 Interrupt Control 2 (IRQCTL2)

3.60.1 Address

Register	Offset
IRQCTL2	096h

3.60.2 Function

The IRQCTL2 register allows defining interrupt output modes for IRQ[8:11], where relevant to the target system.

3.60.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W			IRQ9		IRQ10			
CRST	00		00		00		00	

3.60.4 Fields

Field	Function
7-6 -	Reserved.
5-4 IRQ9	Sets mode of IRQ9 output: 00= Level-sensitive: drive IRQ9 low on interrupt input == 1. 01= Level-sensitive: drive IRQ9 high on interrupt input == 1. 10= Edge-triggered: drive IRQ9 low on a 0-to-1 edge. 11= Edge-triggered: drive IRQ9 high on a 0-to-1 edge. Edge-triggered interrupts are cleared by reading the IRQCTL2 register.
3-2 IRQ10	Sets mode of IRQ10 output: (same as IRQ9).
1-0 -	Reserved.

3.61 Interrupt Drive 0 (IRQDRV0)

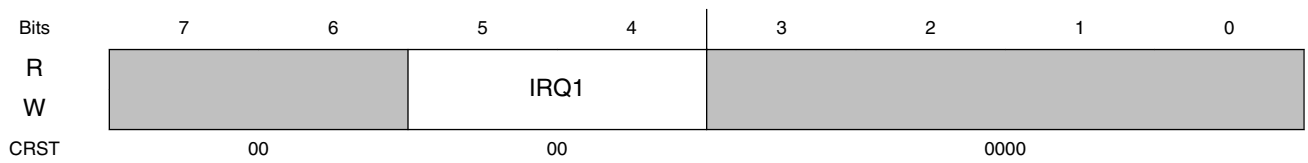
3.61.1 Address

Register	Offset
IRQDRV0	098h

3.61.2 Function

The IRQDRV0 register allows control of selected interrupt pins.

3.61.3 Diagram



3.61.4 Fields

Field	Function
7-6 -	Reserved.
5-4 IRQ1	Allows control of the IRQ1_B pin. 0X= Undriven (Z). 10= Drive IRQ1_B low. 11= Drive IRQ1_B high. The status of IRQ1_B can be monitored with the IRQSTAT registers.
3-0 -	Reserved.

3.62 Interrupt Drive 1 (IRQDRV1)

3.62.1 Address

Register	Offset
IRQDRV1	099h

3.62.2 Function

The IRQDRV1 register allows control of selected interrupt pins.

3.62.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W					IRQ6		IRQ7	
CRST	0000				00		00	

3.62.4 Fields

Field	Function
7-4 -	Reserved.
3-2 IRQ6	Allows control of the IRQ6_B pin. 0X= Undriven (Z). 10= Drive IRQ6_B low. 11= Drive IRQ6_B high. The status of IRQ6_B can be monitored with the IRQSTAT registers.
1-0 IRQ7	Allows control of the IRQ7_B pin. 0X= Undriven (Z). 10= Drive IRQ7_B low. 11= Drive IRQ7_B high. The status of IRQ7_B can be monitored with the IRQSTAT registers.

3.63 Interrupt Drive 2 (IRQDRV2)

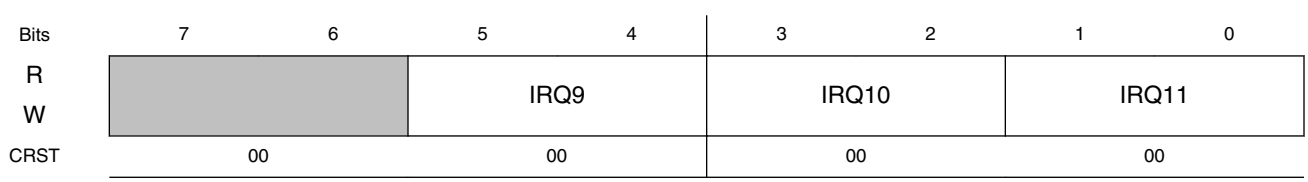
3.63.1 Address

Register	Offset
IRQDRV2	09Ah

3.63.2 Function

The IRQDRV2 register allows control of selected interrupt pins.

3.63.3 Diagram



3.63.4 Fields

Field	Function
7-6 -	Reserved.
5-4 IRQ9	Allows control of the IRQ9_B pin. 0X= Undriven (Z). 10= Drive IRQ9_B low. 11= Drive IRQ9_B high. The status of IRQ9_B can be monitored with the IRQSTAT registers.
3-2 IRQ10	Allows control of the IRQ10_B pin. 0X= Undriven (Z). 10= Drive IRQ10_B low. 11= Drive IRQ10_B high. The status of IRQ10_B can be monitored with the IRQSTAT registers.
1-0 IRQ11	Allows control of the IRQ11_B pin. 0X= Undriven (Z). 10= Drive IRQ11_B low. 11= Drive IRQ11_B high. The status of IRQ11_B can be monitored with the IRQSTAT registers.

3.64 Interrupt Drive 5 (IRQDRV5)

3.64.1 Address

Register	Offset
IRQDRV5	09Dh

3.64.2 Function

The IRQDRV5 register allows control of selected interrupt pins.

3.64.3 Diagram

Bits	7	6	5	4	3	2	1	0
R W	TMP_CTL							
CRST	00		000000					

3.64.4 Fields

Field	Function
7-6 TMP_CTL	Allows control of the TA_TMP_DETECT_B pin. 0X= Undriven (Z). 10= Drive TA_TMP_DETECT_B low. 11= Drive TA_TMP_DETECT_B high. The status of TA_TMP_DETECT_B can be monitored with the IRQSTAT registers.
5-0 -	Reserved.

3.65 Core Management Space Registers

The core management address/data registers allow access to internal Qixis control registers, primarily the direct switch access registers which allow easy reporting of board configuration.

For RDB systems, only the following are defined:

3.65.1 CMS Registers

Address	Name	Definition
00	SW#	Number of configuration switches.
01..0F	SWn	Image of configuration switch #n.

Ranges not listed are reserved.

A standard use of the CMSA/CMSD port is to read the state of configuration switches, for example:

```
Qixis_Set_Reg( CMS_A, 00h );

nr = Qixis_Get_Reg( CMS_D );

for (i = 1; i <= nr; i++) {

   Qixis_Set_Reg( CMS_A, i );

   printf("SW%1d = %02X\\ n", i, Qixis_Get_Reg( CMS_D ));

}
```

3.66 Core Management Address (CMSA)

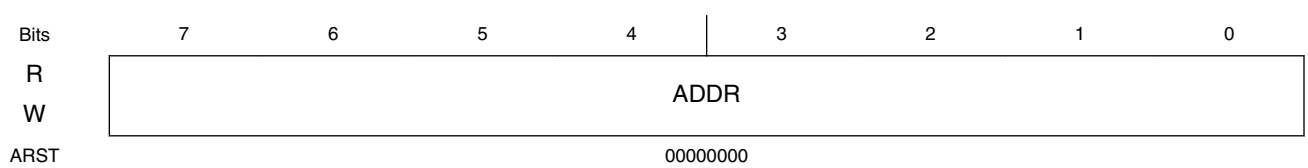
3.66.1 Address

Register	Offset
CMSA	0D8h

3.66.2 Function

The CMSA register selects one of the internal core management registers within Qixis for subsequent read- or write-access via the CMSD register.

3.66.3 Diagram



3.66.4 Fields

Field	Function
7-0	Select internal CMS register for read/write via CMSD.

Field	Function
ADDR	

3.67 Core Management Data (CMSD)

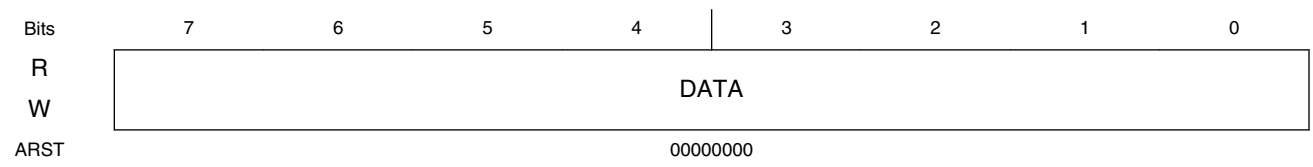
3.67.1 Address

Register	Offset
CMSD	0D9h

3.67.2 Function

CMSD contains the value of a CMS register selected by CMSA. See CMSA for details.

3.67.3 Diagram



3.67.4 Fields

Field	Function
7-0 DATA	Read/write internal CMS registers selected with CMSA.

3.68 Switch Manager Registers

For systems which have serially-sampled switches (as opposed to direct connection), the SWS_* registers control/monitor the IP which manges the sampling and virtualization of the switches.

For the LX2160ARDB, a limited subset of the QDS switch management system is provided to allow software to override all switches.

3.69 Switch Control (SWS_CTL)

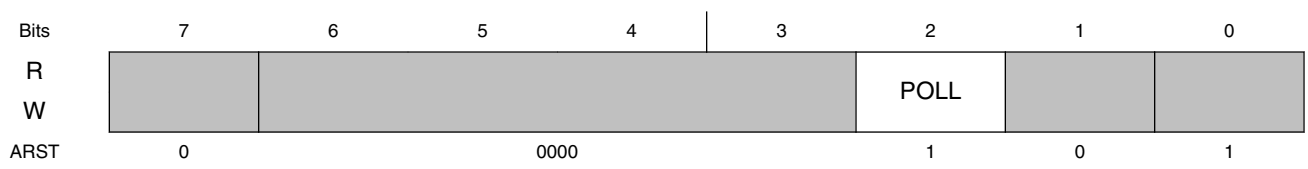
3.69.1 Address

Register	Offset
SWS_CTL	0DCh

3.69.2 Function

The SWS_CTL register manages the switch sampler.

3.69.3 Diagram



3.69.4 Fields

Field	Function
7 -	Reserved.
6-3 -	Reserved.
2	Poll Switches:

Table continues on the next page...

Field	Function
POLL	0= Polling is disabled. 1= Polling is enabled; the switches are sampled continually.
1 -	Reserved.
0 -	Reserved.

3.70 Switch Sample Status (SWS_STAT)

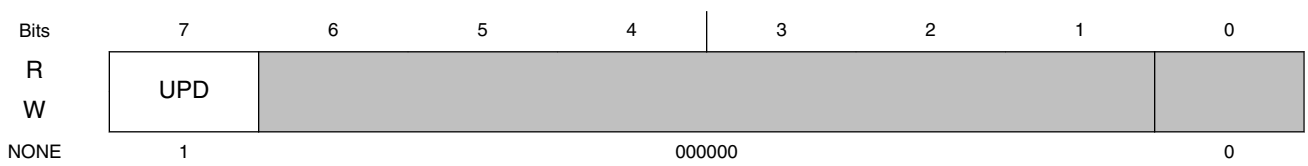
3.70.1 Address

Register	Offset
SWS_STAT	0DDh

3.70.2 Function

SWS_STAT reports on update activity from the serial switch sampler.

3.70.3 Diagram



3.70.4 Fields

Field	Function
7 UPD	Updated: 0= (reserved)

Table continues on the next page...

Switch Sample Status (SWS_STAT)

Field	Function
	1= The switches were updated.
6-1 -	Reserved.
0 -	Reserved.

Appendix A
Revision History

The table below summarizes the revisions to this document.

Table A-1. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 0	09/2018		Initial public release

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “ typicals ,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer’s applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Document Number LX2160ARDBRM
Revision 0, 09/2018