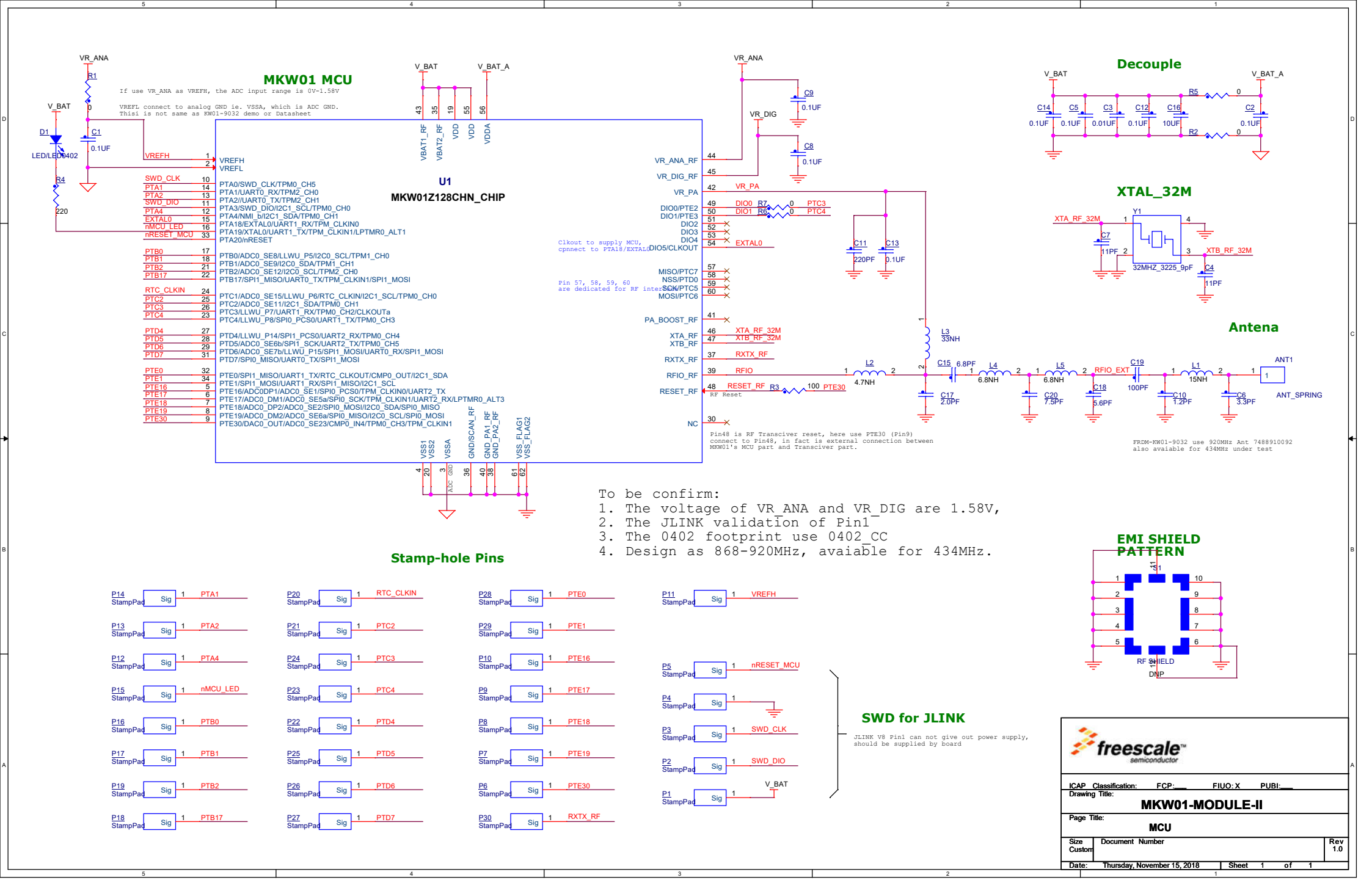
MKW01 MCU
If use VR_ANA as VREFH, the ADC input range is 0V~1.58V
VREFL connect to analog GND ie. VSSA, which is ADC GND.
Thisi is not same as KW01-9032 demo or Datasheet
U1
MKW01Z128CHN_CHIP
Clkout to supply MCU, cpnnect to PTA18/EXTALO
Pin 57, 58, 59, 60 are dedicated for RF interface
Pin48 is RF Transciver reset, here use PTE30 (Pin9) connect to Pin48, in fact is external connection between MKW01's MCU part and Transciver part.
Decouple
XTAL_32M
Antena
FRDM-KW01-9032 use 920MHz Ant 7488910092 also avaiable for 434MHz under test
To be confirm:
1. The voltage of VR_ANA and VR_DIG are 1.58V,
2. The JLINK validation of Pin1
3. The 0402 footprint use 0402_CC
4. Design as 868-920MHz, avaiable for 434MHz.
Stamp-hole Pins
EMI SHIELD PATTERN
SWD for JLINK
JLINK V8 Pin1 can not give out power supply, should be supplied by board
freescale semiconductor
ICAP Classification: FCP:__ FIUO: X PUBI:__
Drawing Title: MKW01-MODULE-II
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Document Number
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