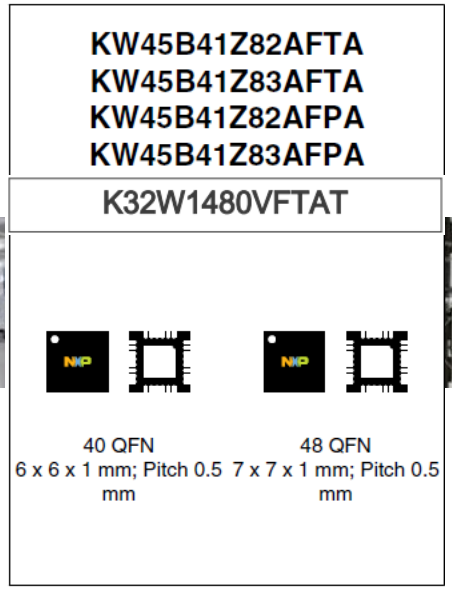
KW45 & K32W1 MINIMUM BOM

MINIMUM COMPONENTS NEEDED TO USE KW45 OR K32W1 PRODUCTS AND DCDC CONFIGURATIONS

SE TEAM

APRIL 2024



CONFIDENTIAL AND PROPRIETARY

SECURE CONNECTIONS FOR A SMARTER WORLD

KW45 & K32W148
HVQFN48 – 7X7

BYPASS

Power config diagram – DCDC Bypass

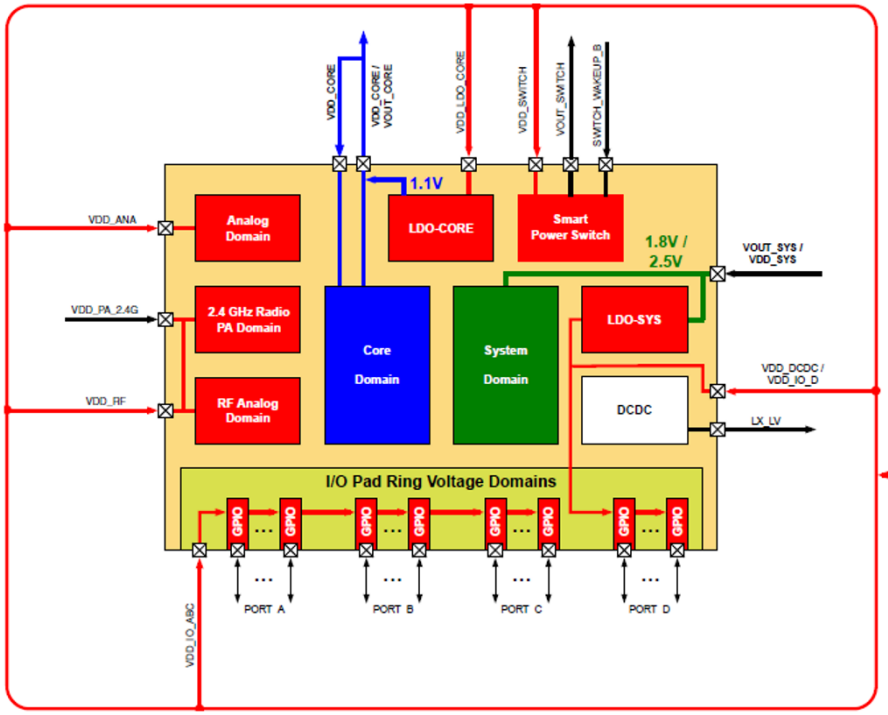
Configuration

- Bypass DCDC
- External 3.3 V for LDO-CORE, LDO-SYS, VDD_IO
- Generate VPA_2PGHZ internally from VDD_RF

Regulator	Output	Input voltage range
DCDC	**1.8V to 2.5 V**	**1.8V to 2.5 V**
LDO-SYS	1.8 / 2.5 V	1.8~3.6 V
LDO-CORE	1.05 / 1.1 / 1.15 V	1.71~3.6 V (Enable); 0.84~1.21 V (Bypass)

VPA_2P4GHZ	Tx Output Power	VPA source	VDD_RF
0.9 V	+1.8 dBm	External or internal	1.175 ~3.6 V
1.525 V	+7 dBm		1.8 ~ 3.6 V
2.2 V	+10 dBm		2.475~3.6 V

Note: VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally.

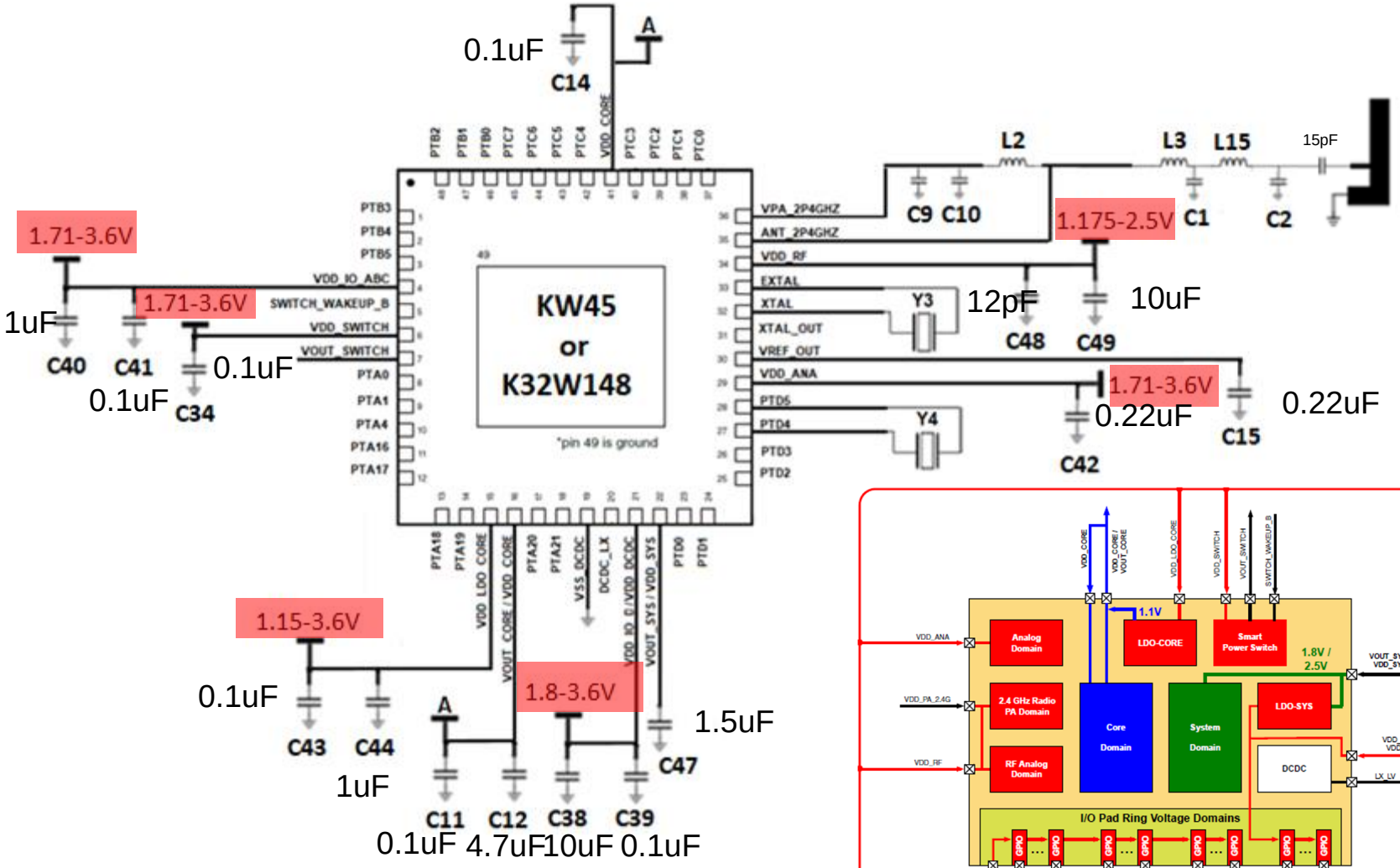


VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally.
For internal generation, VDD_RF voltage must be equal to or exceed VPA + 275 mV.

Warning: Do not connect the pin VDD_SYS (internal connection)

DCDC Bypass Schematic HVQFN48 – 7x7

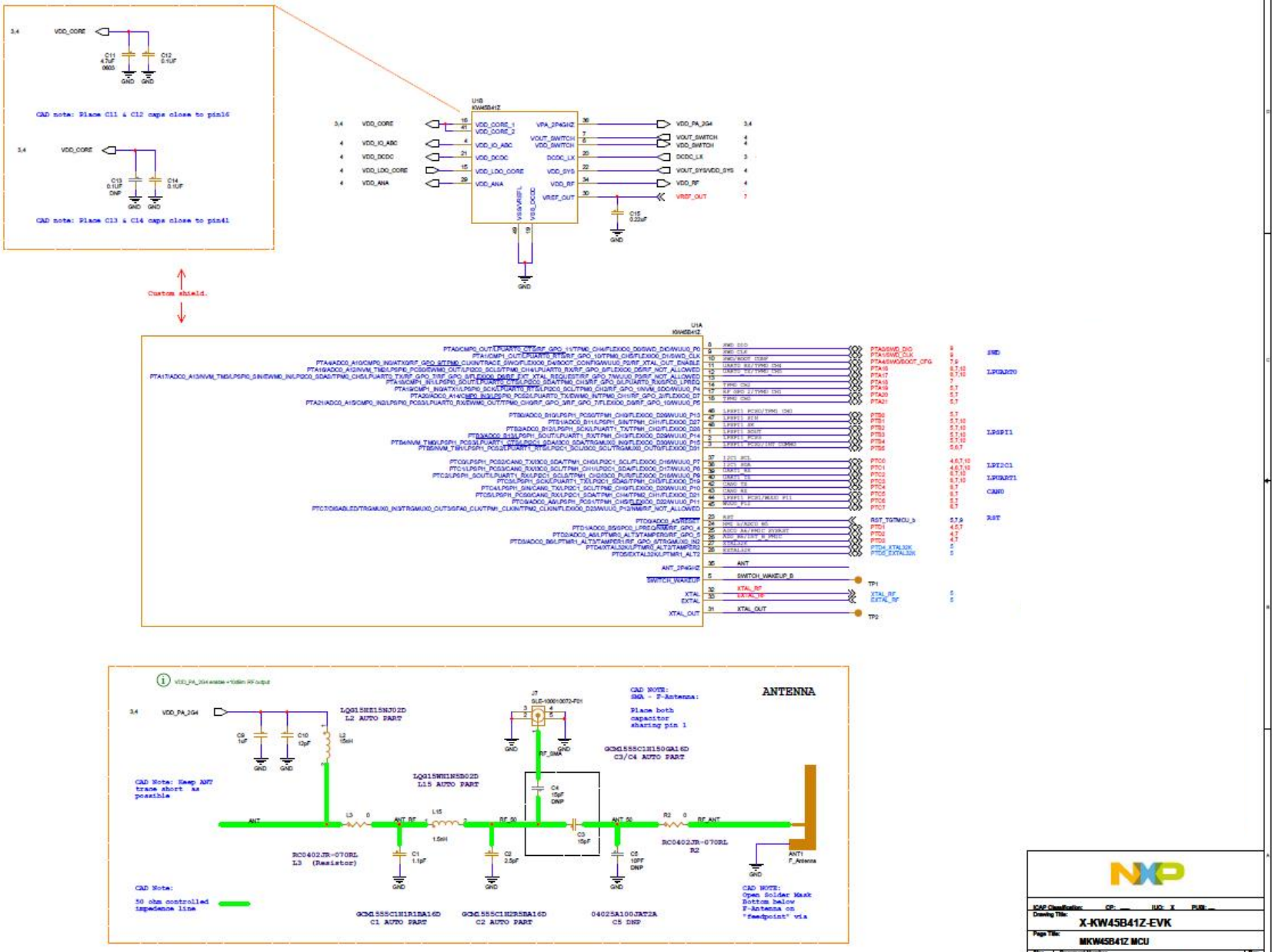
DCDC bypass mode with the possibility of Bluetooth LE Low Power mode active.



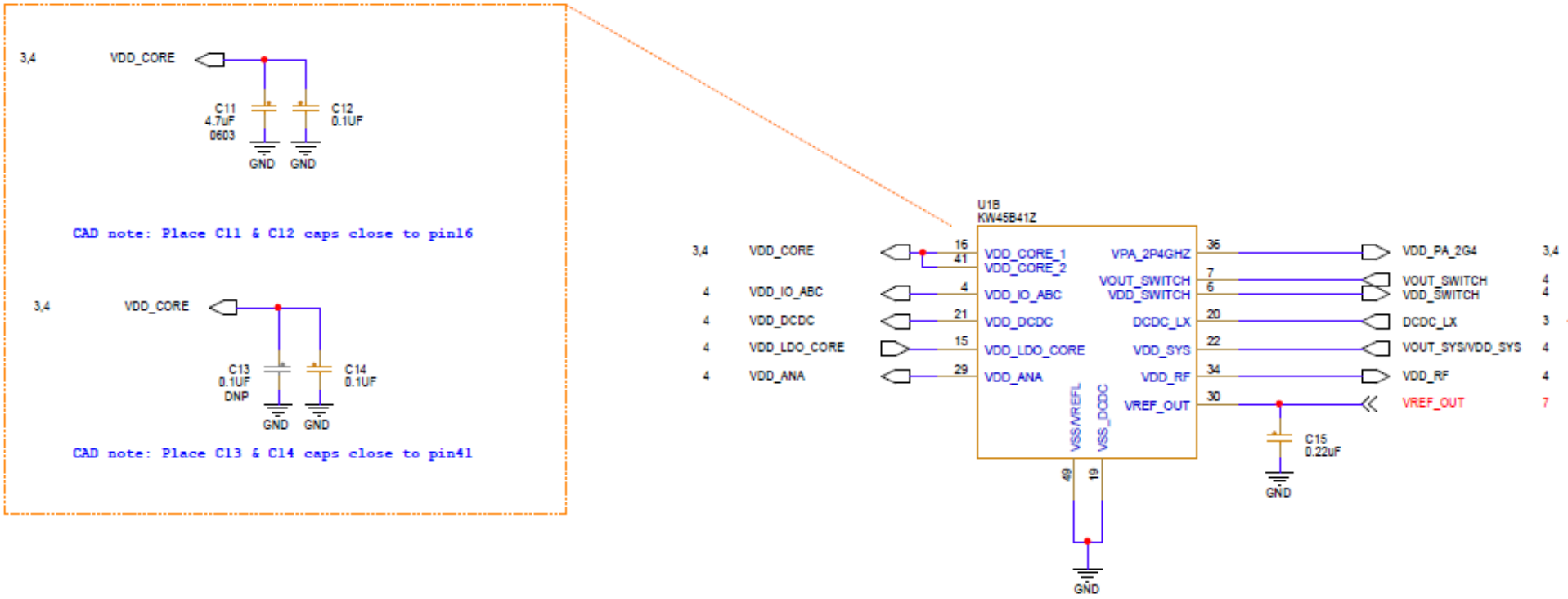
CONFIDENTIAL AND PROPRIETARY

Product in Bypass Mode

HVQFN48 – 7x7

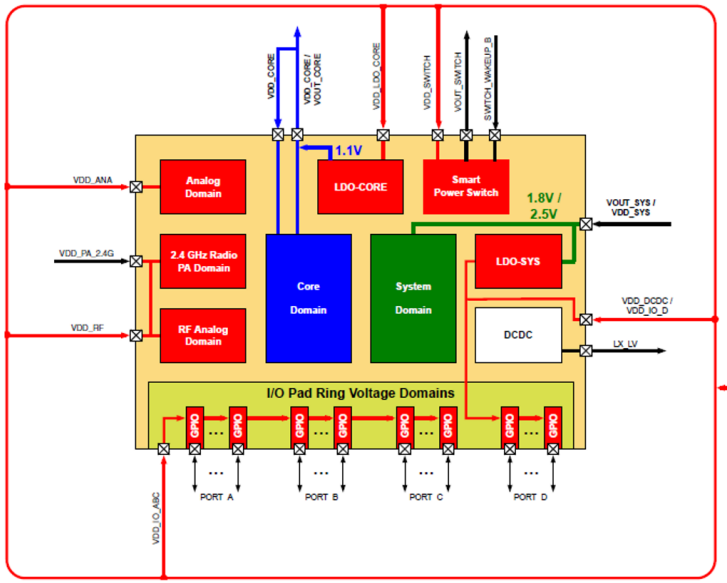


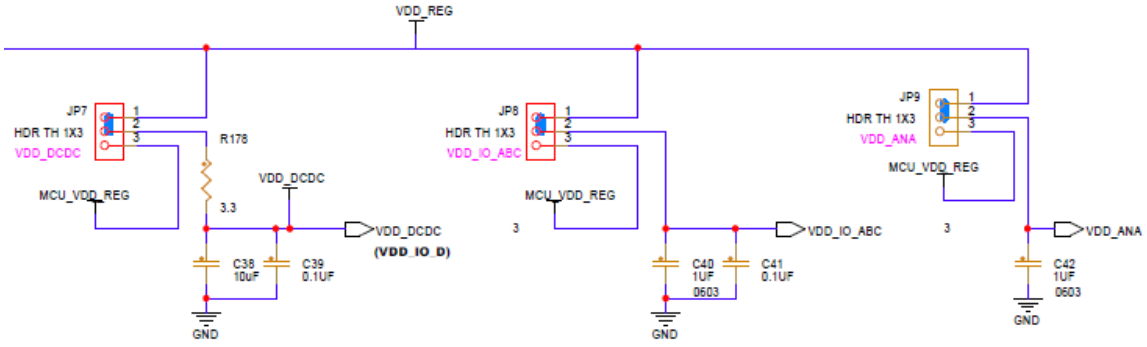
Evaluation board – Recommendation - Bypass

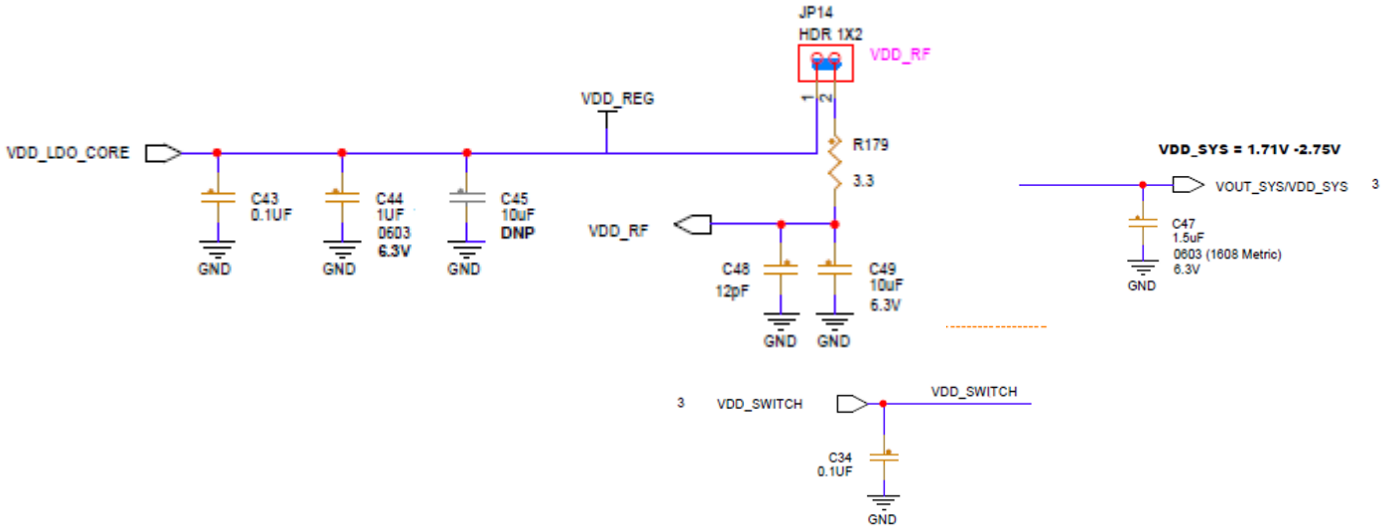


CONFIDENTIAL AND PROPRIETARY

Evaluation board – Recommendation - Bypass







Warning: During Fuse programing, the Vout_sys must be set to 2.5V.

➔ Do not connect the pin VDD_SYS (pin)

➔ It's done internaly on the IC

DCDC Bypass BOM HVQFN48 – 7x7

Bluetooth LE Low Power mode option available (32kHz populated)

Reference	Value
C11,C14,C34,C39,C41,C43	0.1uF
C40,C44	1uF
C12	4.7uF
C15,C42	0.22uF
C48	12pF
C47	1.5uF (or 1uF acceptable)
C38,C49	10uF
Printed IFA antenna	2.4GHZ
U1	KW45B41Z Or K32W148
Y3	32MHz
Y4	32.768 kHz
RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(LQG15HZ15NJ02D)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

CONFIDENTIAL AND PROPRIETARY

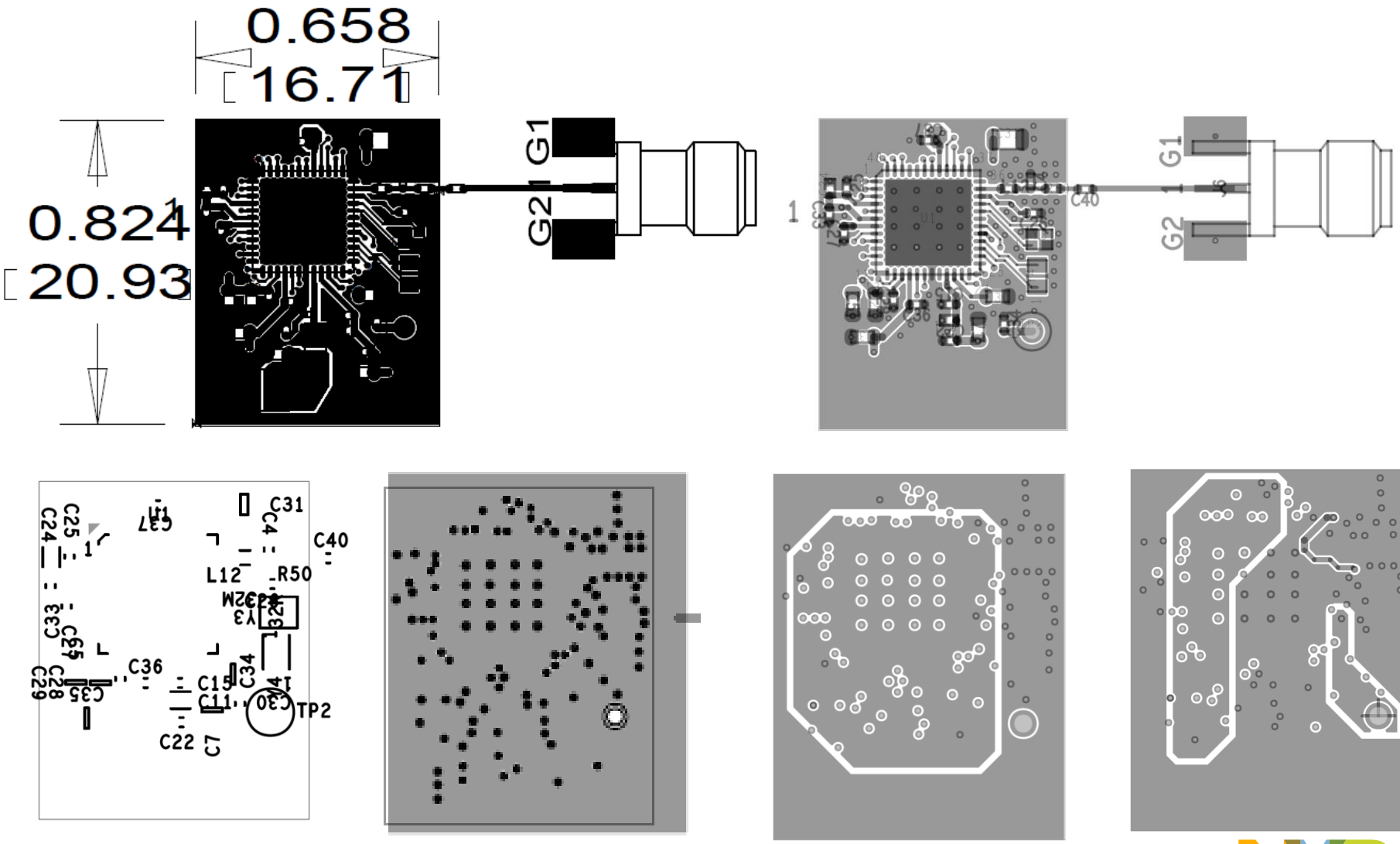
DCDC Bypass Pin configuration HVQFN48 – 7x7

Pin Number	Pin Name	Bypass connection
4	VDD_IO_ABC	1.71-3.6V
6	VDD_SWITCH	1.71-3.6V
7	VOUT_SWITCH	Floating (when not used)
15	VDD_LDO_CORE	1.15-3.6V
16	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
20	DCDC_LX	Floating (not used)
21	VDD_DCDC	1.8-3.6V
22	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
29	VDD_ANA	1.71-3.6V
30	VREF_OUT	Floating (except the decoupling capacitor)
34	VDD_RF	1.175-2.5V
36	VPA_2P4GHZ	0.9-2.4V
41	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
49	VSS	GND
19	VSS_DCDC	GND

Warning: ➔ Do not connect the pin VDD_SYS (internal connection)

Bluetooth LE Low Power mode option available (32kHz populated)

Layout example on bypass mode HVQFN48WF – 7x7



CONFIDENTIAL AND PROPRIETARY

BUCK

EVK – Power config diagram – DCDC Buck

Configuration

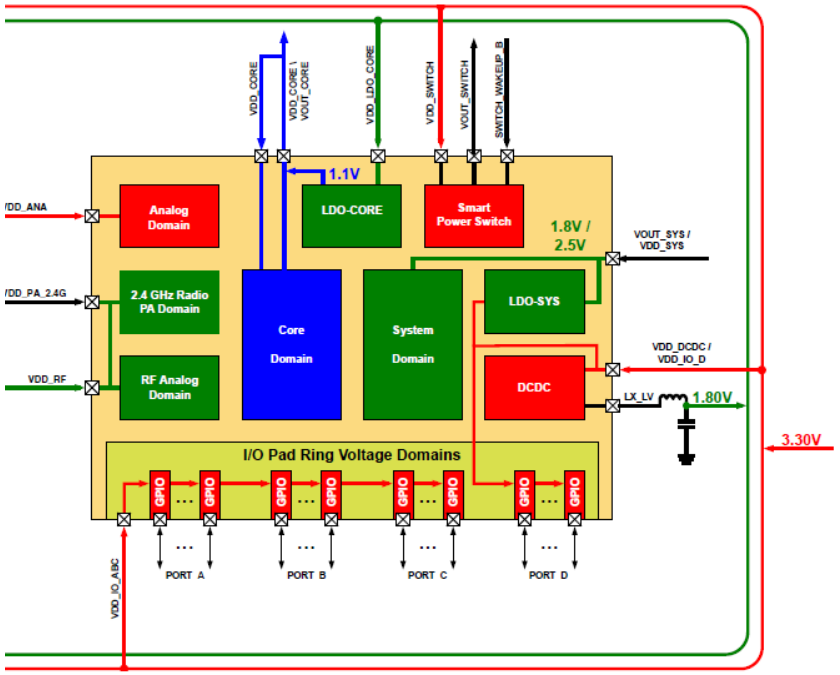
- Bypass DCDC
- External 3.3 V for LDO-CORE, LDO-SYS, VDD_IO
- Generate VPA_2PGHZ internally from VDD_RF

Regulator	Output	Input voltage range
DCDC	1.25 / 1.35 / 1.8 / 2.5 V	1.71~3.6 V; >= output + 500 mV
LDO-SYS	1.8 / 2.5 V	1.8~3.6 V
LDO-CORE	1.05 / 1.1 / 1.15 V	1.71~3.6 V (Enable); 0.84~1.21 V (Bypass)

VPA_2P4GHZ	Tx Output Power	VPA source	VDD_RF
0.9 V	+1.8 dBm	External or internal	1.175 ~3.6 V
1.525 V	+7 dBm		1.8 ~ 3.6 V
2.2 V	+10 dBm		2.475~3.6 V

Note: VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally. For internal generation, it can support up to +7 dBm and VDD_RF voltage must meet specific voltage range.

VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally. For internal generation, VDD_RF voltage must be equal to or exceed VPA + 275 mV.

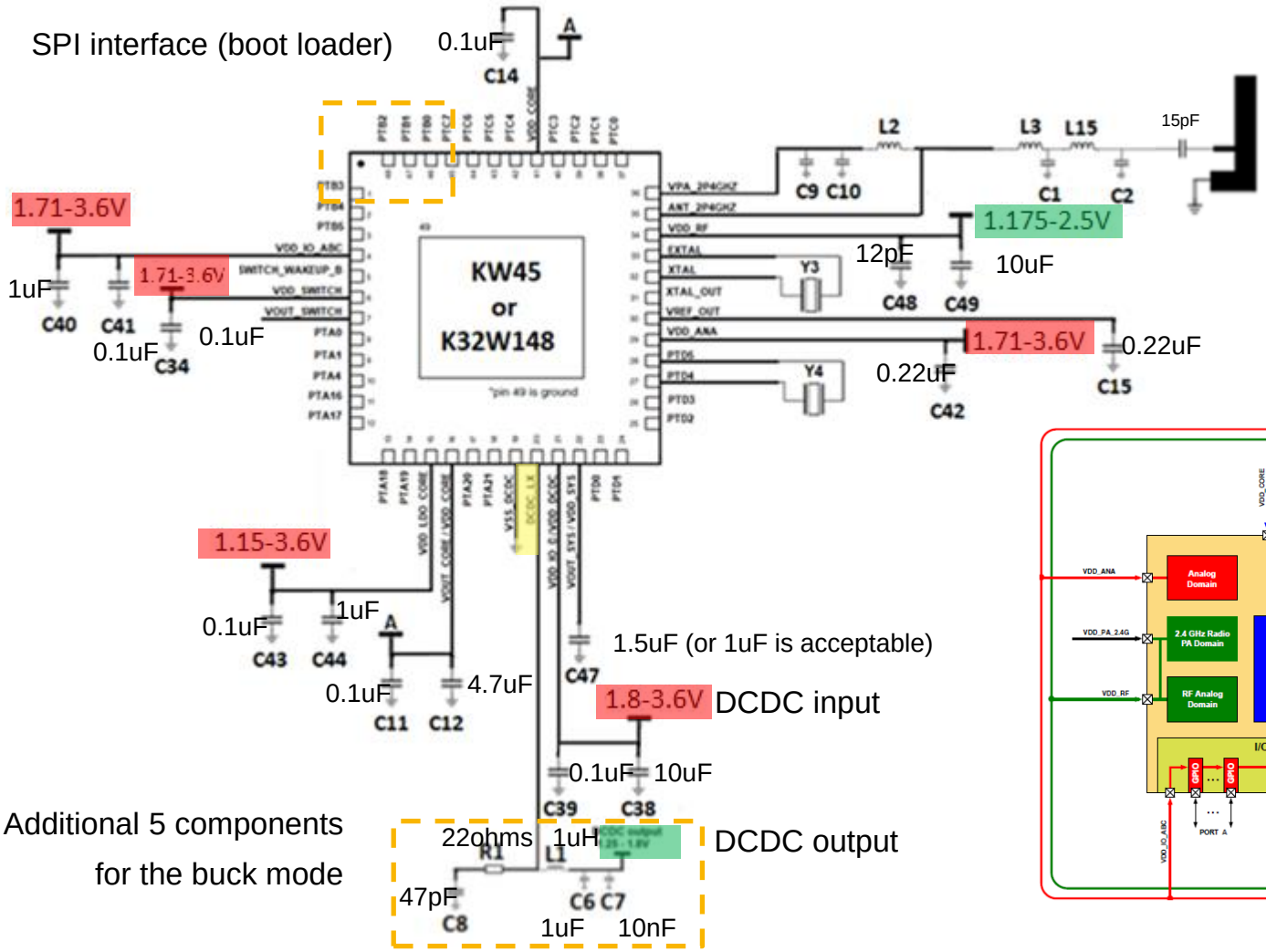


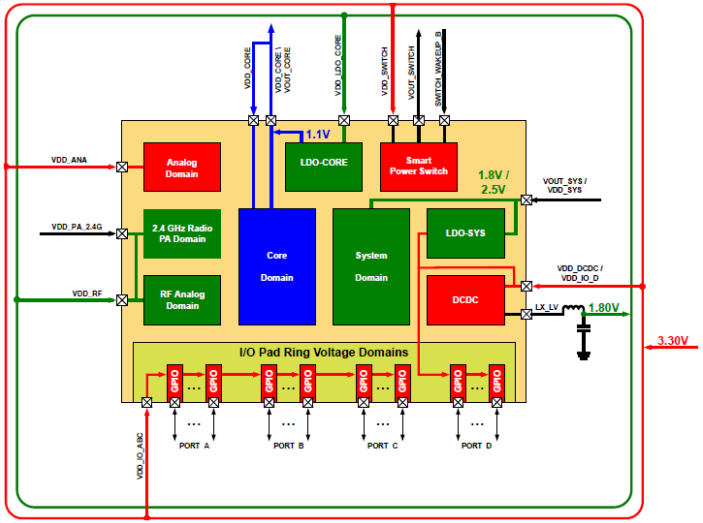
Warning: During Fuse programing, the Vout sys must be set to 2.5V.
➔ Do not connect the pin VDD_SYS (internal connection)

Product in Buck Mode

HVQFN48 – 7x7

Possibility of Bluetooth LE Low Power mode active in case 32kHz is populated.

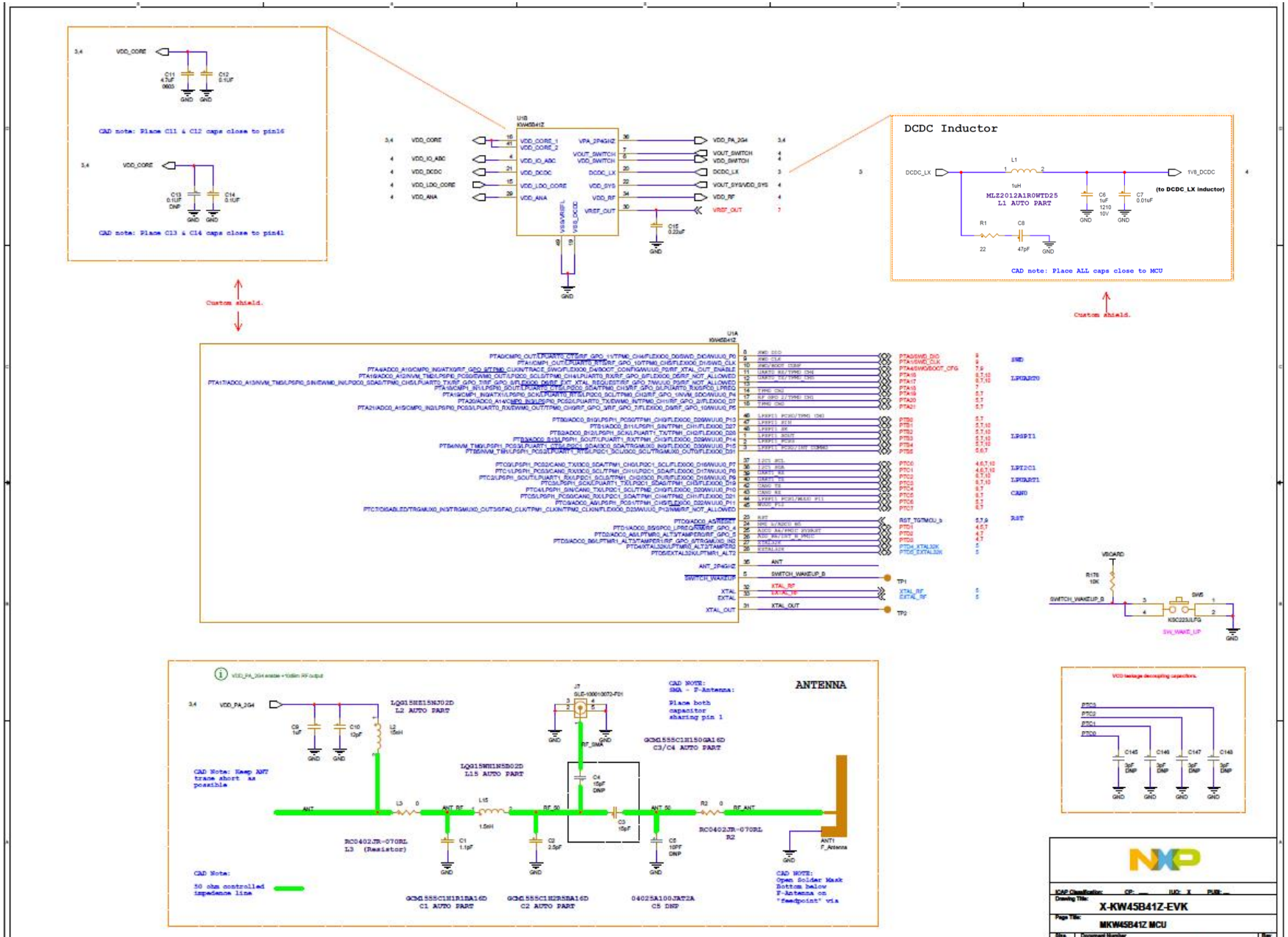




CONFIDENTIAL AND PROPRIETARY

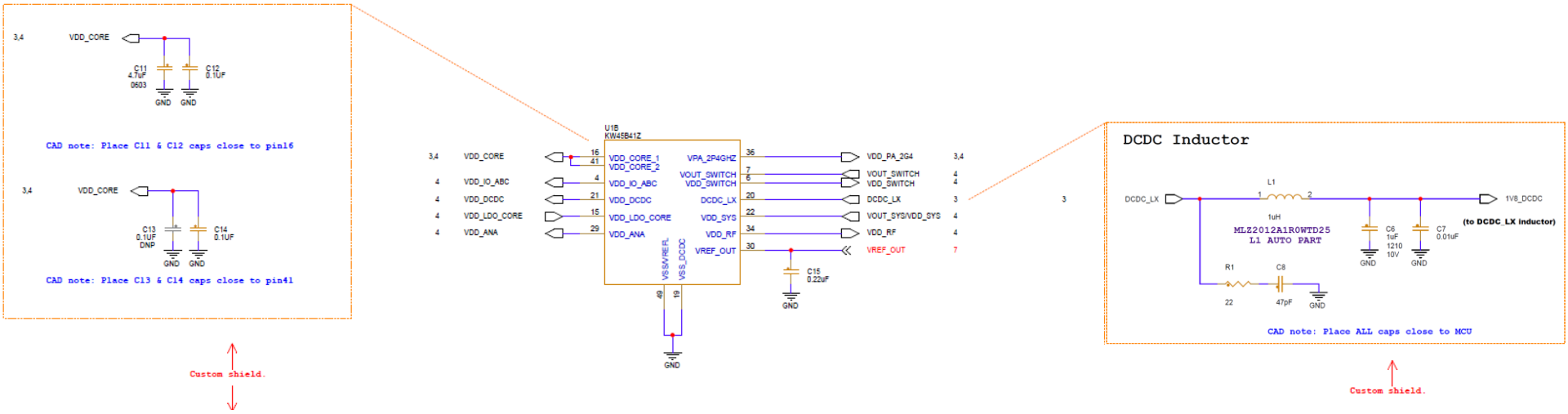
Product in Buck Mode

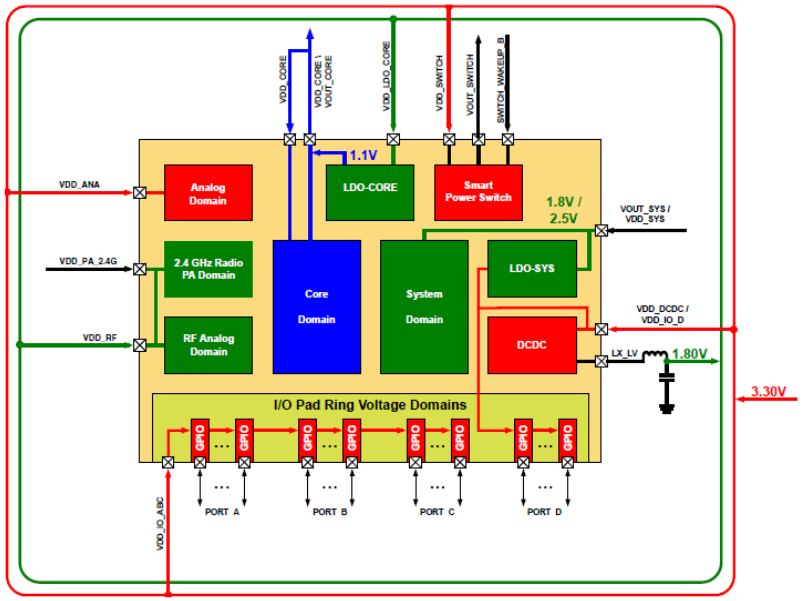
HVQFN48 – 7x7



Evaluation board – Recommendation

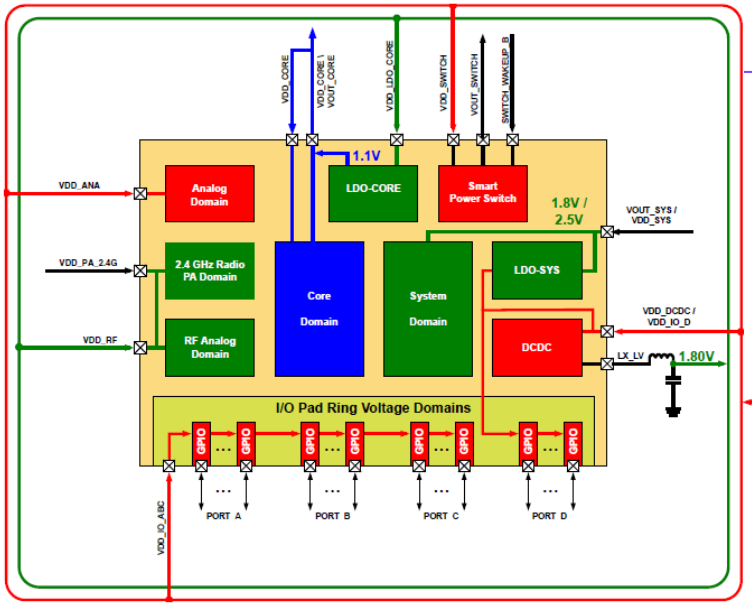
Recommanded DCDC inductor (L1): MLZ2012A1R0WTD25

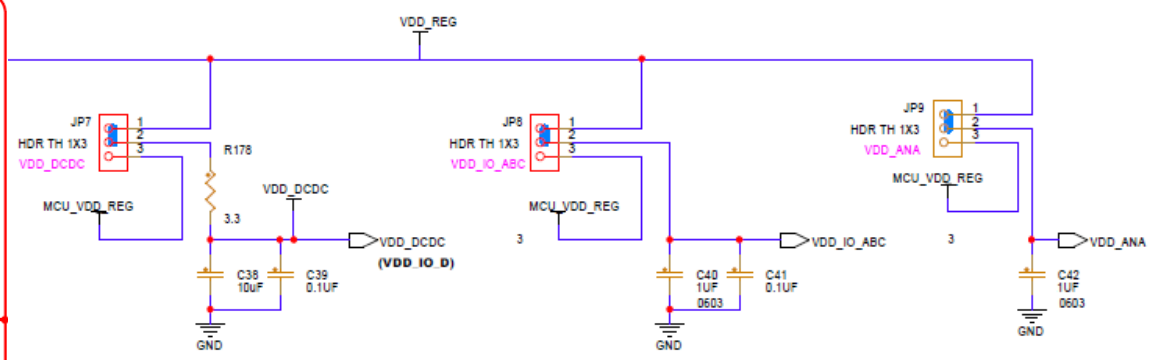


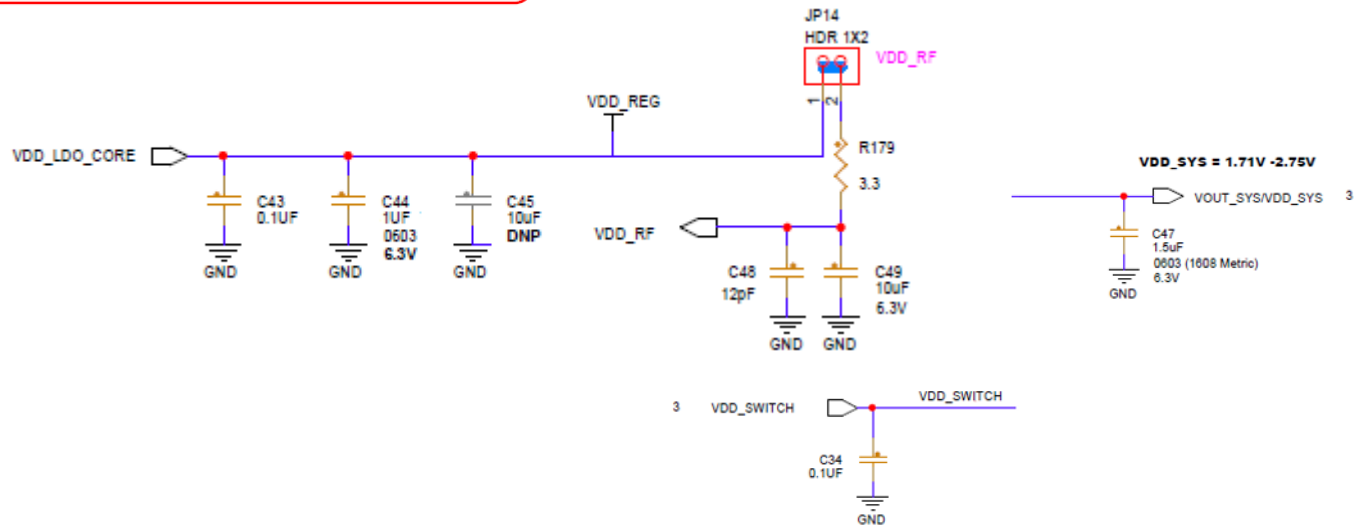


CONFIDENTIAL AND PROPRIETARY

Evaluation board – Recommendation - Buck







Warning: During fuse programing, the Vout_sys must be set to 2.5V.

➔ Do not connect the pin VDD_SYS (pin)

➔ It's done internaly on the IC

DCDC Buck BOM HVQFN48 – 7x7

Bluetooth LE Low Power mode option available (32kHz populated)

Reference	Value
C38,C49	10uF
C6,C40,C44	1uF
C11,C14,C34,C39,C41,C43	0.1uF
C12	4.7uF
C15,C42	0.22uF
C7	10nF
C8	47pF
C48	12pF
C47	1.5uF (or 1uF)
Printed IFA antenna	2.4GHZ
R1	22 ohms
L1 (MLZ2012A1R0WTD25)	1uH
U1	KW45B41Z Or K32W148
Y3	32MHz
Y4	32.768 kHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(*LQG15HZ15NJ02D*)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

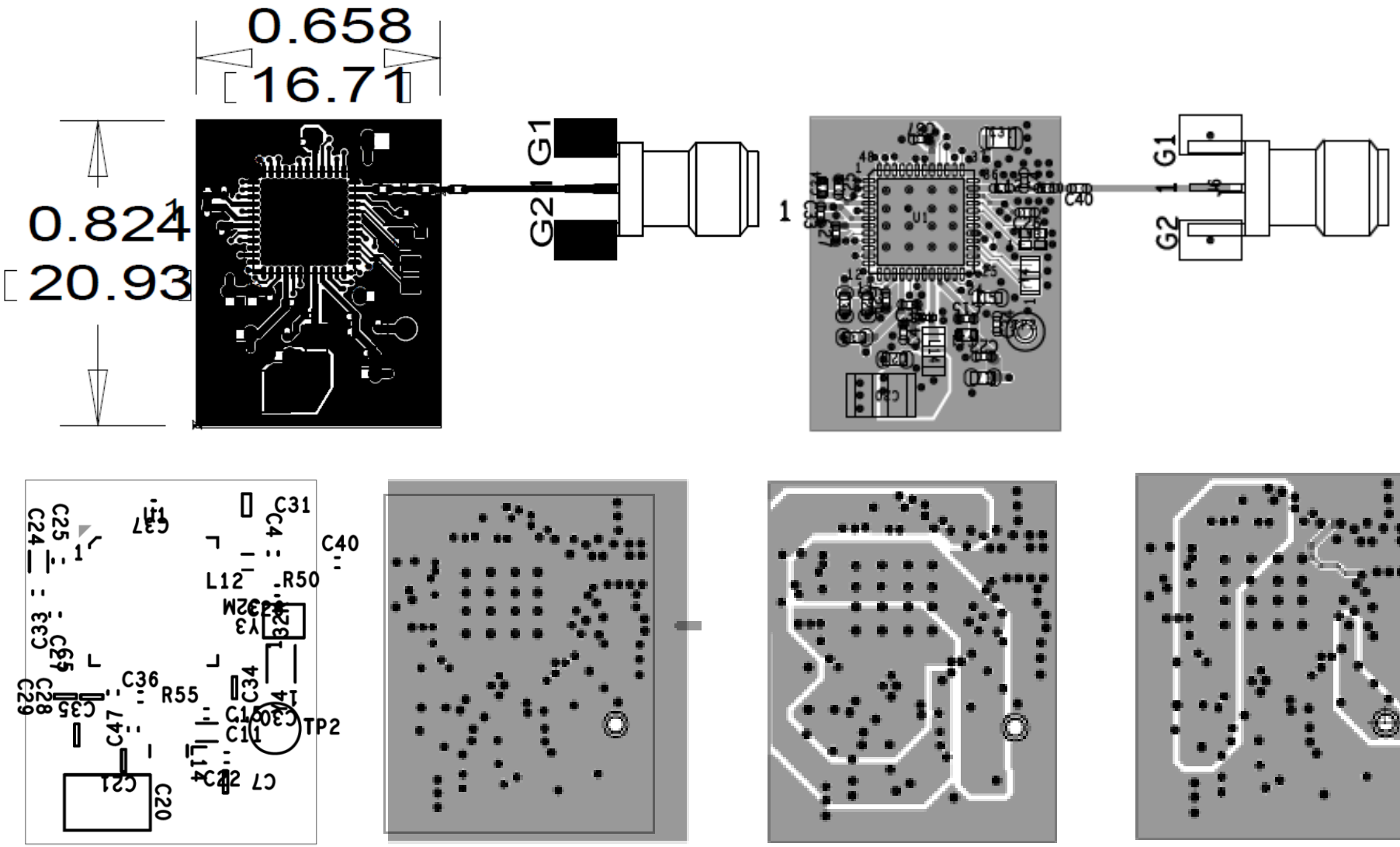
DCDC Buck Pin configuration HVQFN48 – 7x7

Pin Number	Pin Name	Buck connection
4	VDD_IO_ABC	1.71-3.6V
6	VDD_SWITCH	1.71-3.6V
7	VOUT_SWITCH	Floating (when not used)
15	VDD_LDO_CORE	1.15-3.6V
16	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
20	DCDC_LX	1.71-3.6V
21	VDD_DCDC	1.8-3.6V
22	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
29	VDD_ANA	1.71-3.6V
30	VREF_OUT	Floating (except the decoupling capacitor)
34	VDD_RF	1.175-2.5V
36	VPA_2P4GHZ	0.9-2.4V
41	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
49	VSS	GND
19	VSS_DCDC	GND

Warning: ➔ Do not connect the pin VDD_SYS (internal connection)

Bluetooth LE Low Power mode option available (32kHz populated)

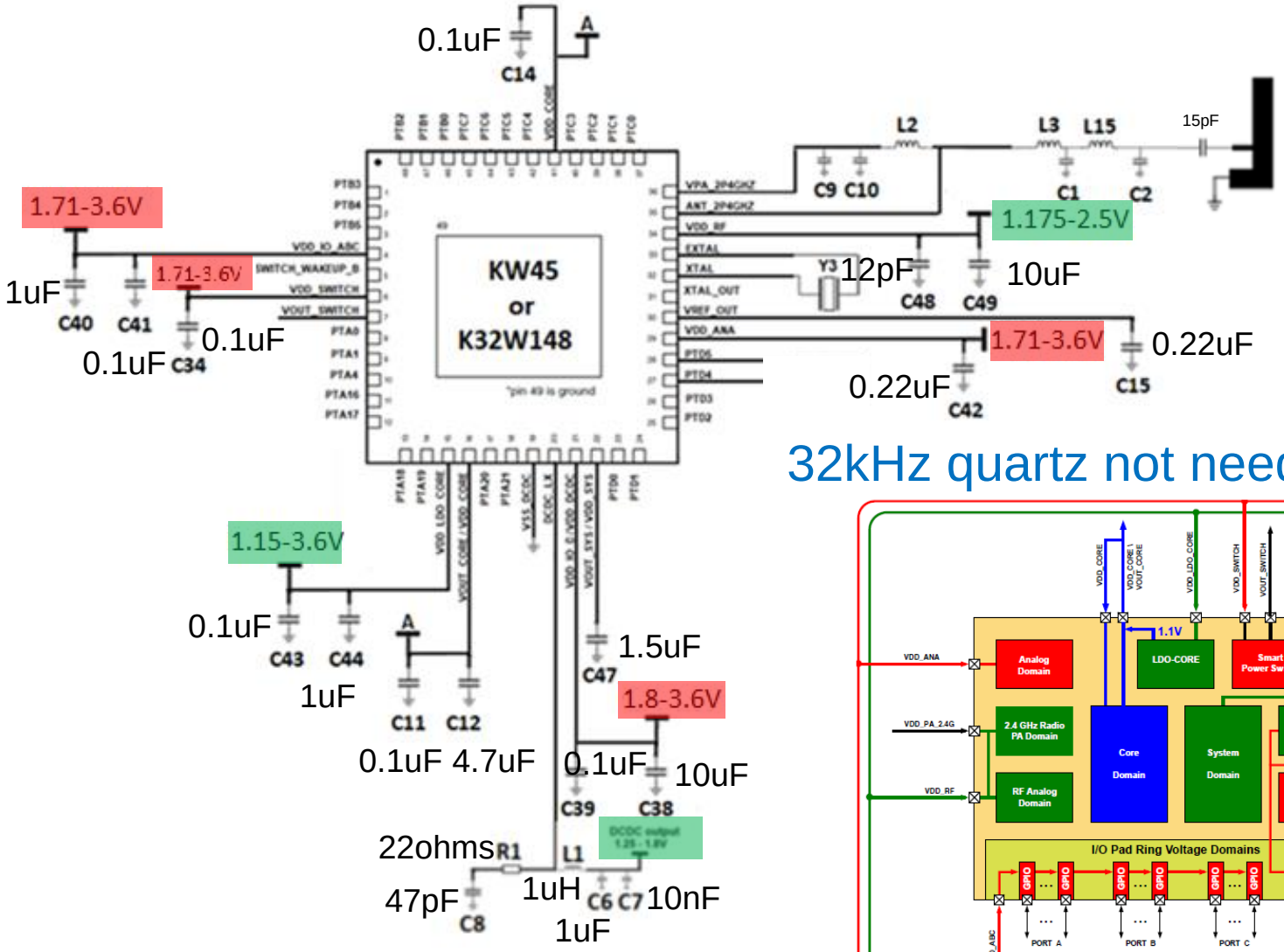
Layout example on buck mode HVQFN48 – 7x7



BUCK MODE
NO BLUETOOTH LE
LOW POWER MODE

Product in Buck Mode

HVQFN48 – 7x7



32kHz quartz not needed

CONFIDENTIAL AND PROPRIETARY

DCDC Buck BOM

HVQFN48 – 7x7

No Bluetooth LE Low Power mode.

Reference	Value
C38,C49	10uF
C6,C40,C44	1uF
C11,C14,C34,C39,C41,C43	0.1uF
C12	4.7uF
C15,C42	0.22uF
C7	10nF
C8	47pF
C48	12pF
C47	1.5uF (or 1uF)
Printed IFA antenna	2.4GHZ
R1	22 ohms
L1 (MLZ2012A1R0WTD25)	1uH
U1	KW45B41Z Or K32W148
Y3	32MHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(LQG15HZ15NJ02D)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

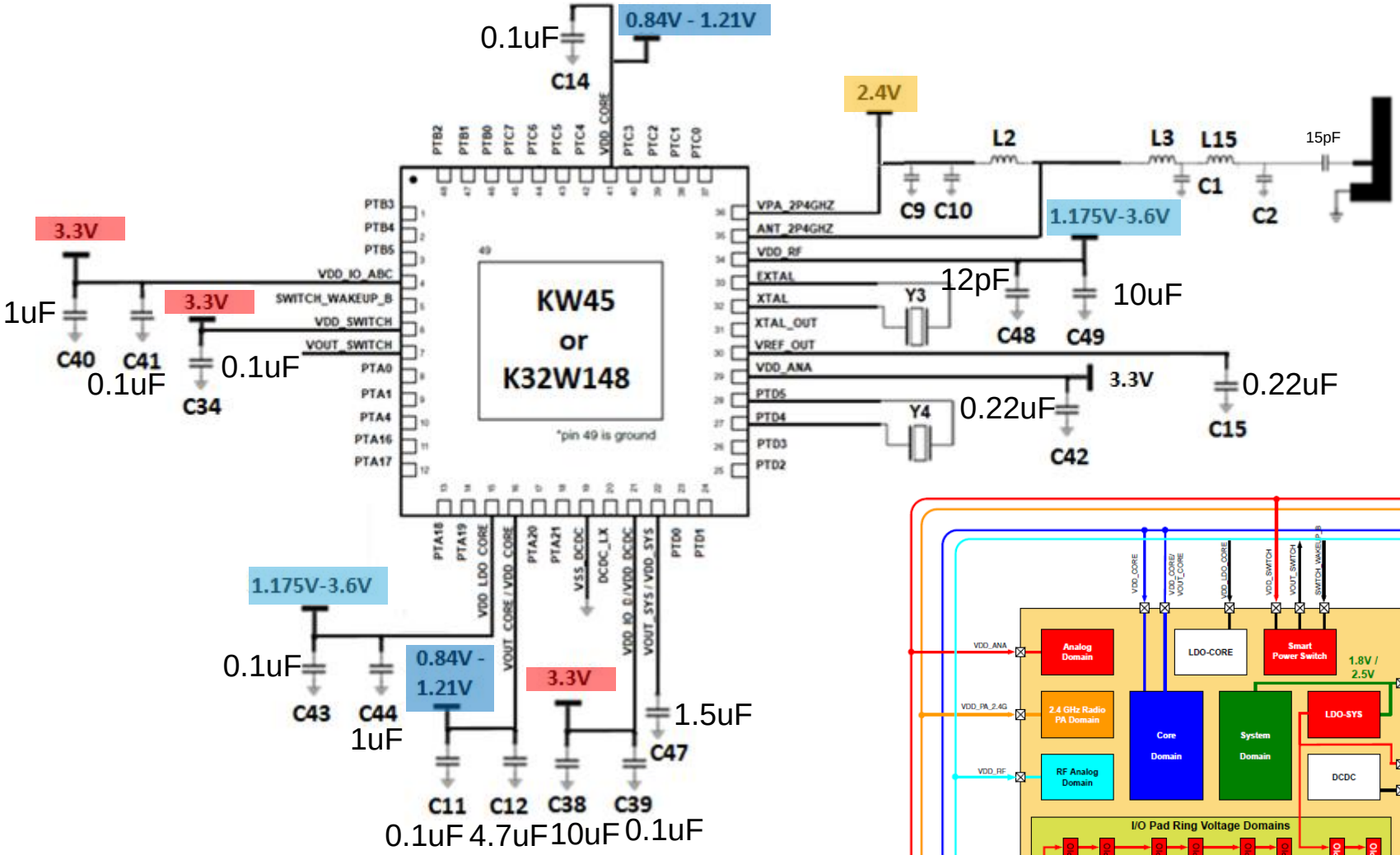
Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

PMIC SUPPLY

KW45 – PMIC supply

HVQFN48 – 7x7

Possibility of Bluetooth LE Low Power mode active.



CONFIDENTIAL AND PROPRIETARY

POWER SWITCH

KW45-EVK – Power config diagram – Power Switch

SMART POWER SWITCH LOW POWER USE CASE

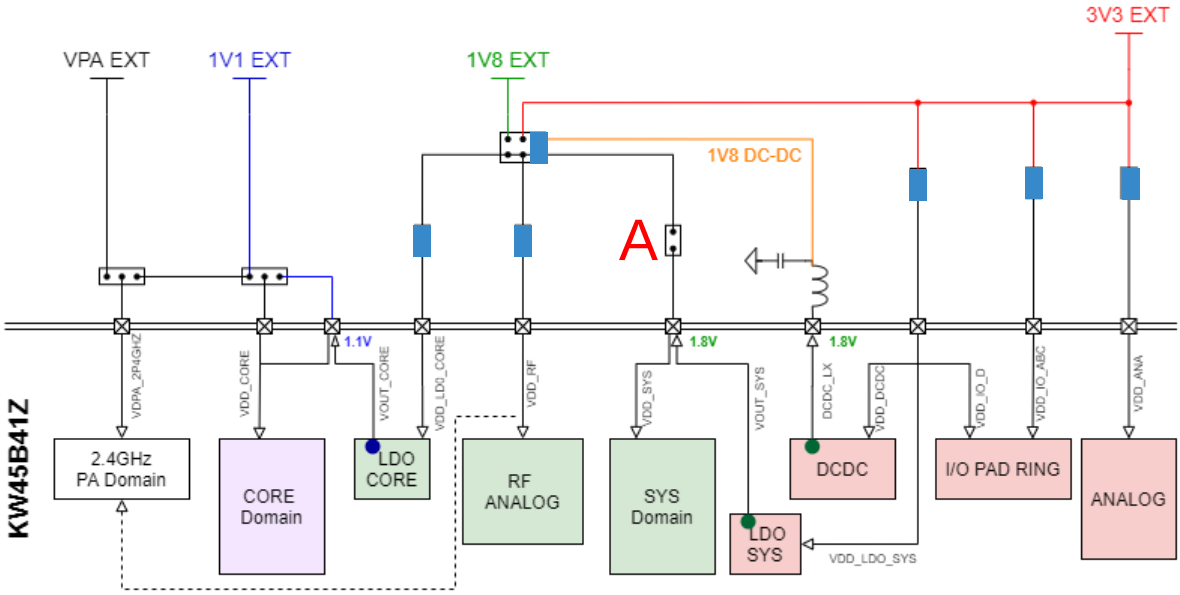
<100 NA TOTAL LEAKAGE CURRENT

Configuration

- External 3.3 V supply to Smart Power Switch
- Power switch output connected to
  - DCDC, LDO-SYS, VDD_ANA and VDD_IO
- DCDC output connected to
  - LDO-CORE, VDD_RF

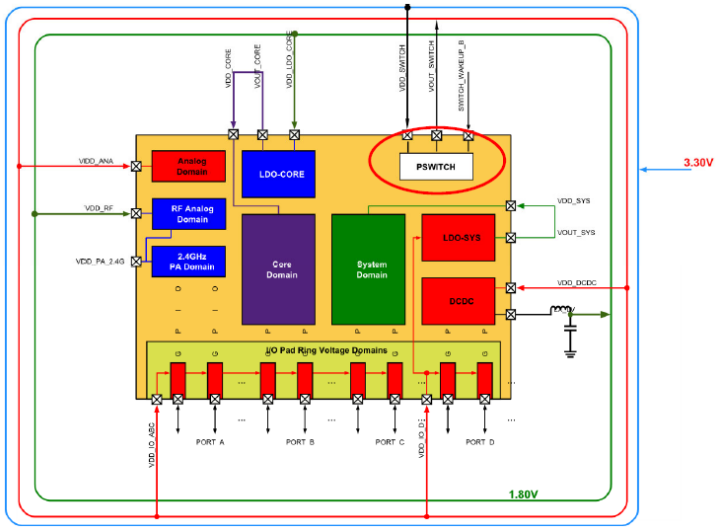
Usage

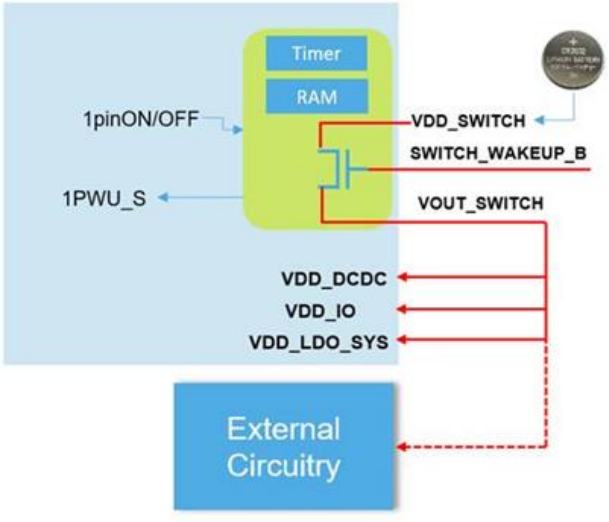
- Software can disable smart power switch in Deep Power Down modes
- Reenable Switch from:
  - External wakeup pin
  - Internal timer with FRO16K
- Standby RAM regulator support 8KB RAM retention
- Can configure to disable during manufacturing process that disconnects battery from device in order to maximize battery life



Warning: During fuse programing, the Vout sys must be set to 2.5V.

➔ Do not connect the pin VDD_SYS (pin) jumper on A





SMART POWER SWITCH

ULTRA LOW POWER & FLEXIBLE

Performance

- <100 nA (typ) leakage current when OFF (no RAM retention, timer disabled)
- <700 nA (typ) leakage current when OFF (8KB RAM retention + timer)
- 40 mA active output current capability

Flexible

- Can be used to power partial or entire chip supply
- Can be used to power external circuits saving BOM costs

Configurable power control

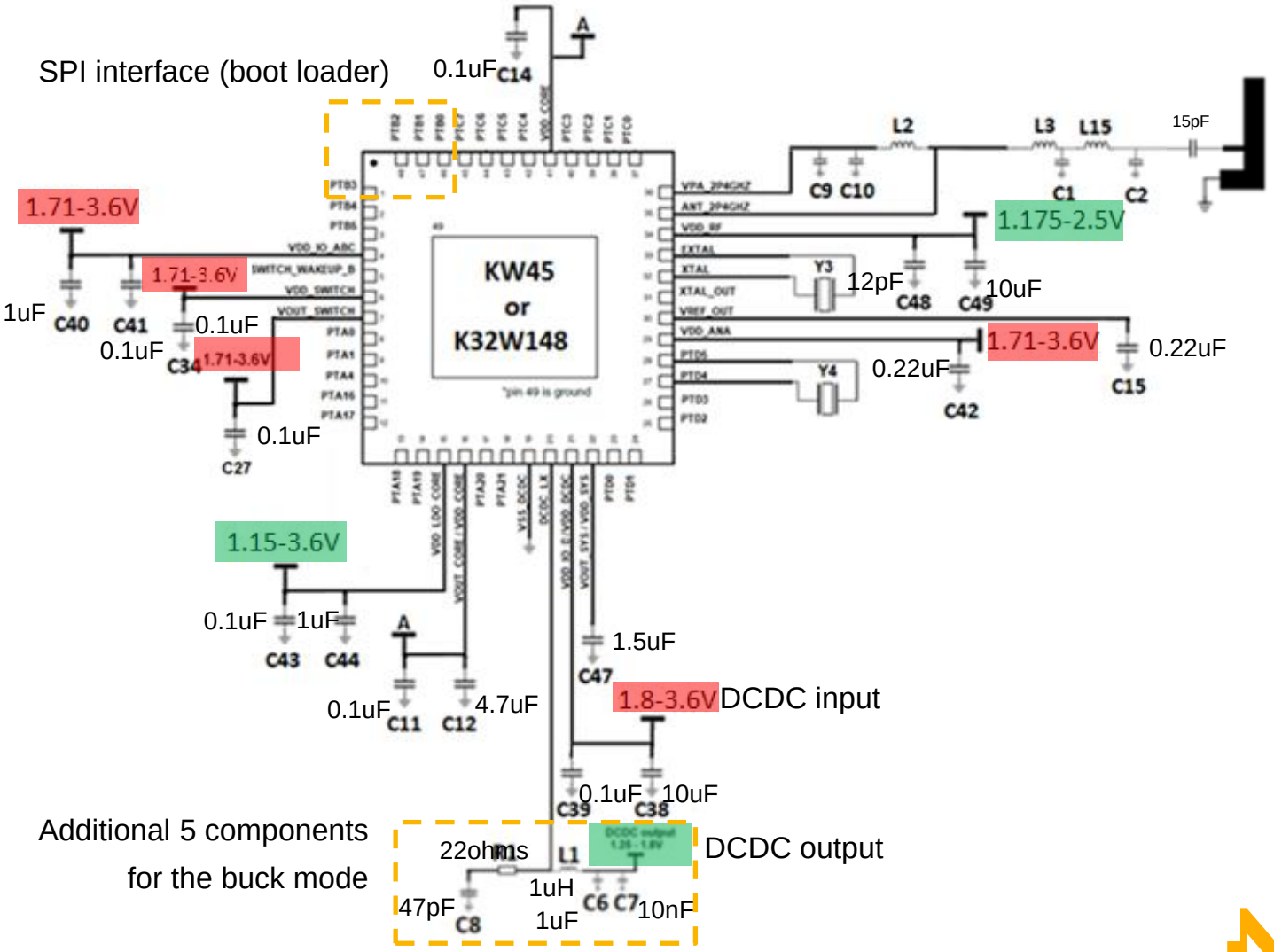
- One external wakeup pin (SWITCH_WAKEUP_B) to enable power switch
- Internal Timer timeout (from 7.8125ms to 1s) to enable power switch
- Dedicated register bits to control power switch in Low Power mode / Active mode

Data storage

- Support up to 8KB RAM retention

Power switch schematic HVQFN48 – 7x7

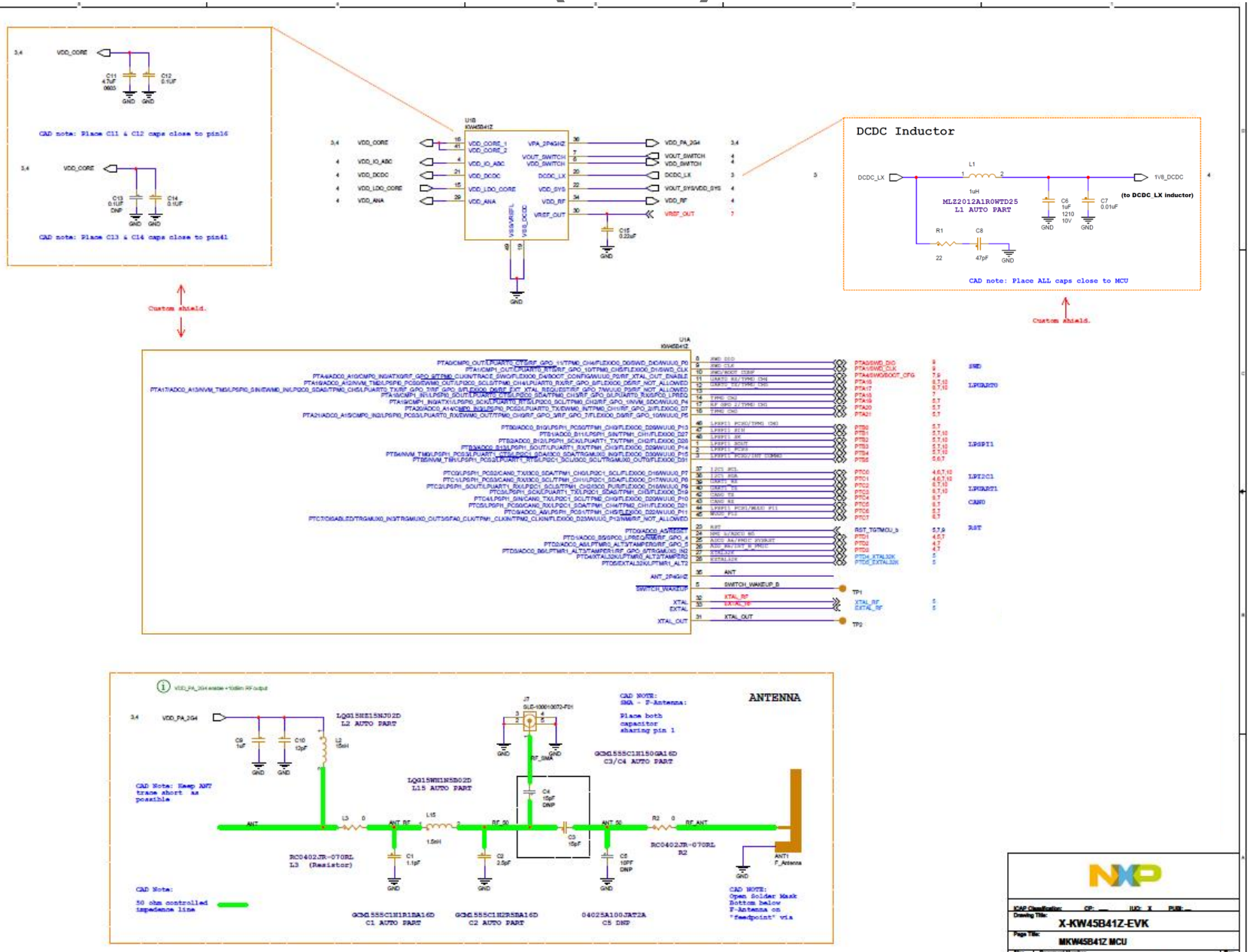
DCDC buck mode with the possibility of Bluetooth LE Low Power mode active.



CONFIDENTIAL AND PROPRIETARY

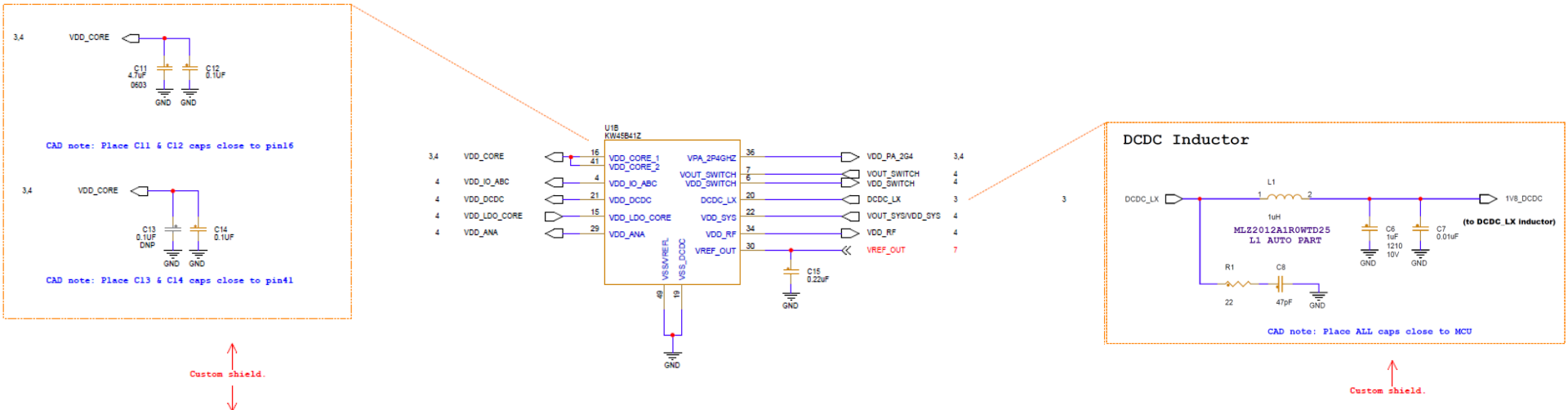
Product in Power Switch (Buck)

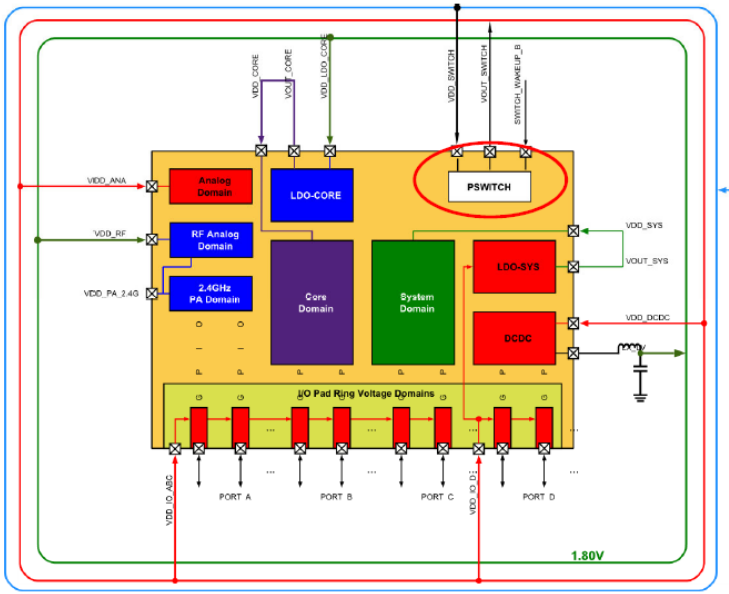
HVQFN48 – 7x7



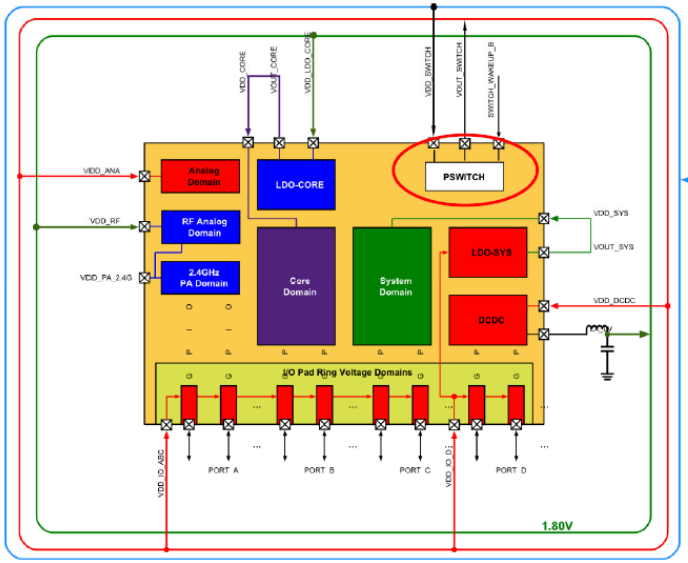
Evaluation board – Recommendation

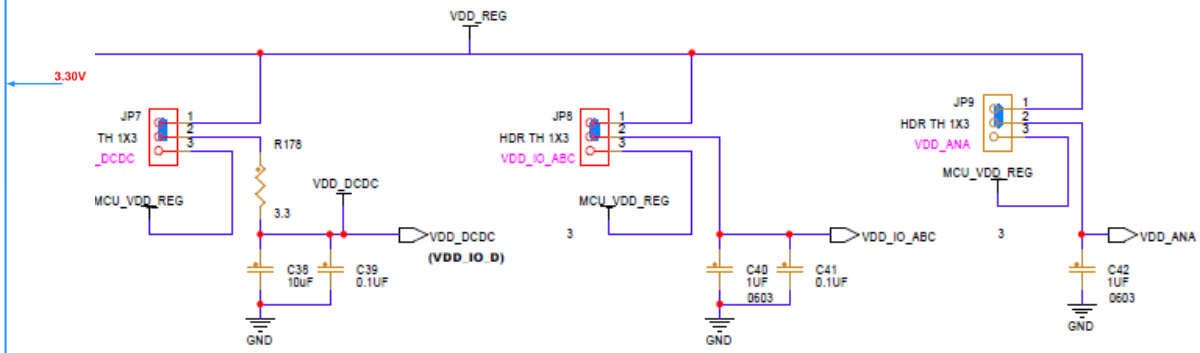
Recommanded DCDC inductor (L1): MLZ2012A1R0WTD25

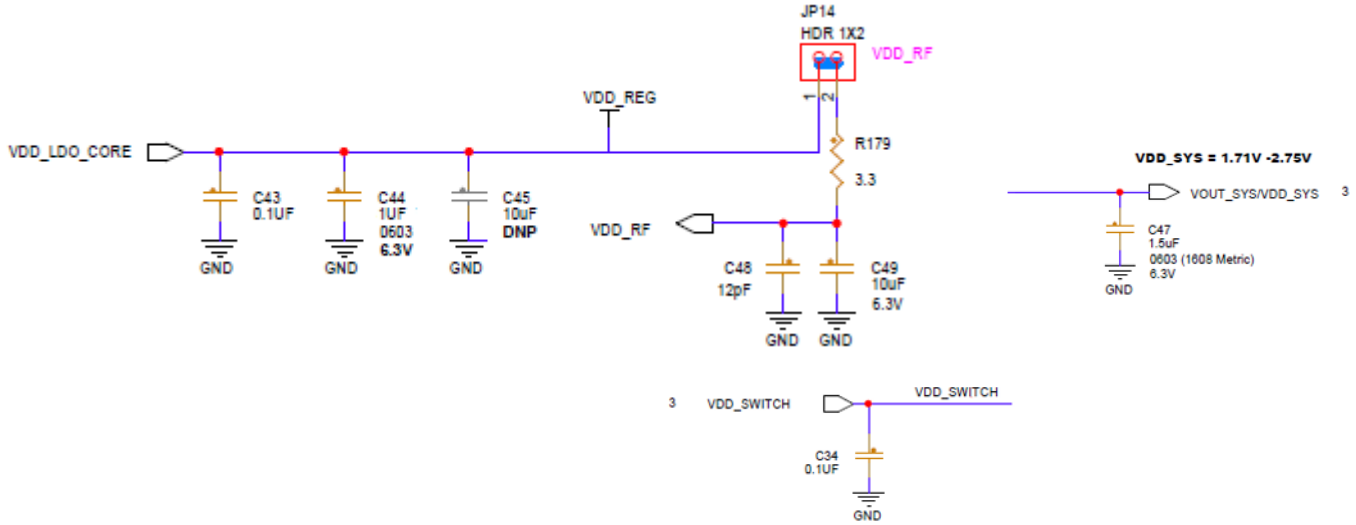




Evaluation board – Recommendation - Buck







Warning: During fuse programing, the Vout_sys must be set to 2.5V.

- ➔ Do not connect the pin VDD_SYS (pin)
- ➔ It's done internaly on the IC

Power Switch (DCDC Buck) BOM HVQFN48 – 7x7

Bluetooth LE Low Power mode option available (32kHz populated)

Reference	Value
C38,C49	10uF
C6,C40,C44	1uF
C11,C14,C27,C34,C36,C39,C41,C43	0.1uF
C12	4.7uF
C15,C42	0.22uF
C7	10nF
C8	47pF
C48	12pF
C47	1.5uF (or 1uF)
Printed IFA antenna	2.4GHZ
R1	22 ohms
L1 (MLZ2012A1R0WTD25)	1uH
U1	KW45B41Z Or K32W148
Y3	32MHz
Y4	32.768 kHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(LQG15HZ15NJ02D)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

Power Switch (DCDC buck) Pin configuration

HVQFN48WF – 7x7

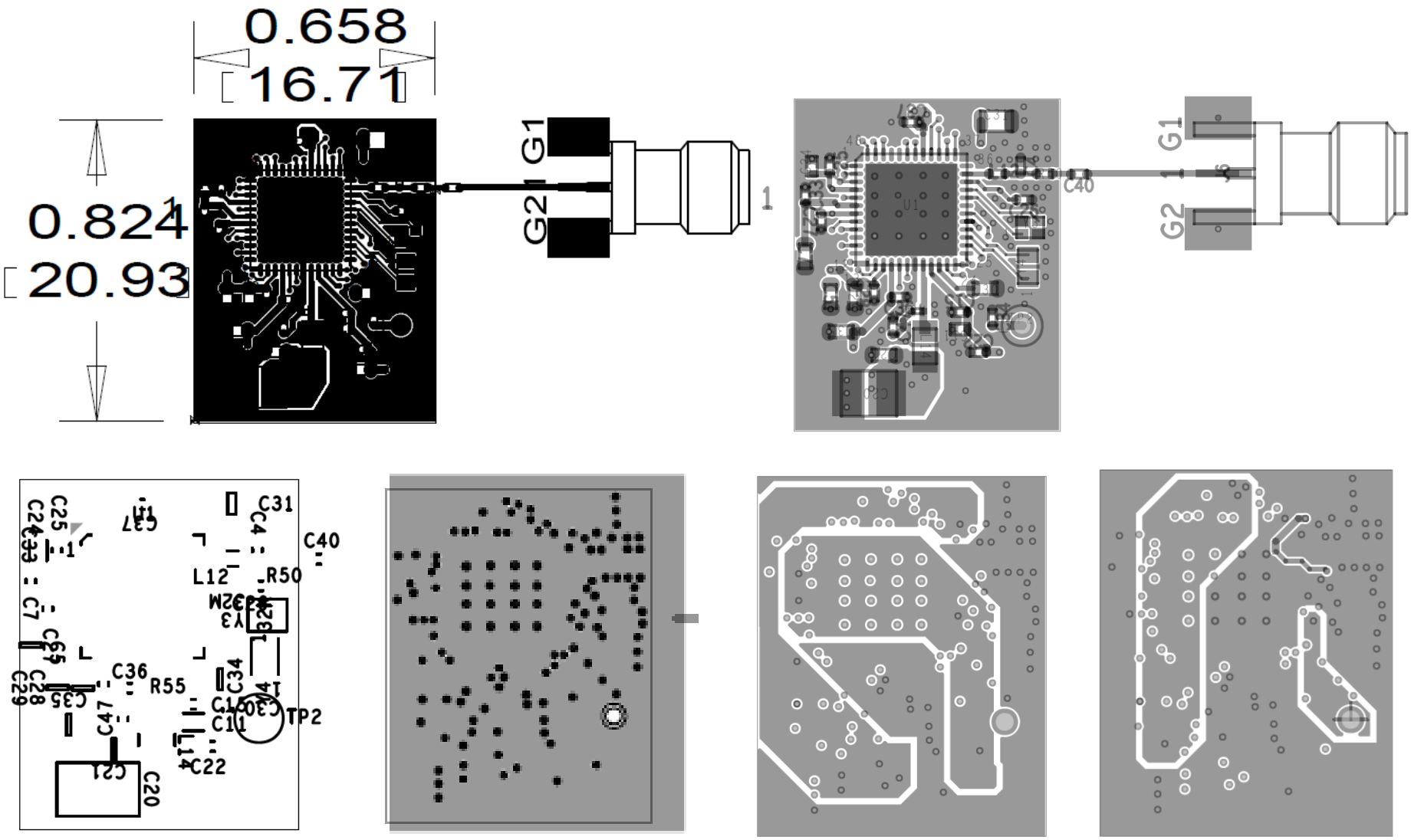
Pin Number	Pin Name	Bypass connection
4	VDD_IO_ABC	1.71-3.6V
5	SWITCH_WAKEUP_B	0-0.7V (connected to ground to be active)
6	VDD_SWITCH	1.71-3.6V
7	VOUT_SWITCH	1.71-3.6V
15	VDD_LDO_CORE	1.15-3.6V
16	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
20	DCDC_LX	1.71-3.6V
21	VDD_DCDC	1.8-3.6V
22	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
29	VDD_ANA	1.71-3.6V
30	VREF_OUT	Floating (except the decoupling capacitor)
34	VDD_RF	1.175-2.5V
36	VPA_2P4GHZ	0.9-2.4V
41	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
49	VSS	GND
19	VSS_DCDC	GND

Warning: During fuse programing, the Vout sys must be set to 2.5V.

➔ Do not connect the pin VDD_SYS (internal connection)

Note: To reach RF output power higher than +7dBm, VPA_2P4GHZ must be supplied to 2.425V minimum.

Layout example on buck mode HVQFN48WF – 7x7



CONFIDENTIAL AND PROPRIETARY

KW45 ONLY
HVQFN40 – 6X6

BYPASS

KW45 - EVK – Power config diagram – DCDC Bypass

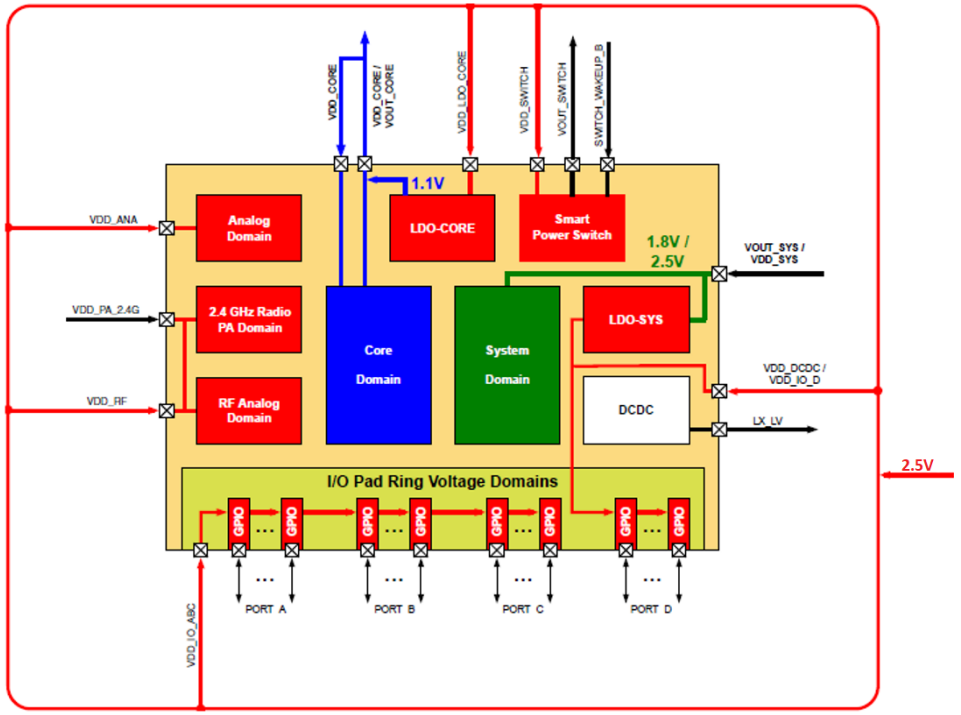
Configuration

- Bypass DCDC
- External 3.3 V for LDO-CORE, LDO-SYS, VDD_IO
- Generate VPA_2PGHZ internally from VDD_RF

Regulator	Output	Input voltage range
DCDC	**1.8V to 2.5 V**	**1.8V to 2.5 V**
LDO-SYS	1.8 / 2.5 V	1.8~3.6 V
LDO-CORE	1.05 / 1.1 / 1.15 V	1.71~3.6 V (Enable); 0.84~1.21 V (Bypass)

VPA_2P4GHZ	Tx Output Power	VPA source	VDD_RF
0.9 V	+1.8 dBm	External or internal	1.175 ~3.6 V
1.525 V	+7 dBm		1.8 ~ 3.6 V
2.2 V	+10 dBm		2.475~3.6 V

Note: VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally.

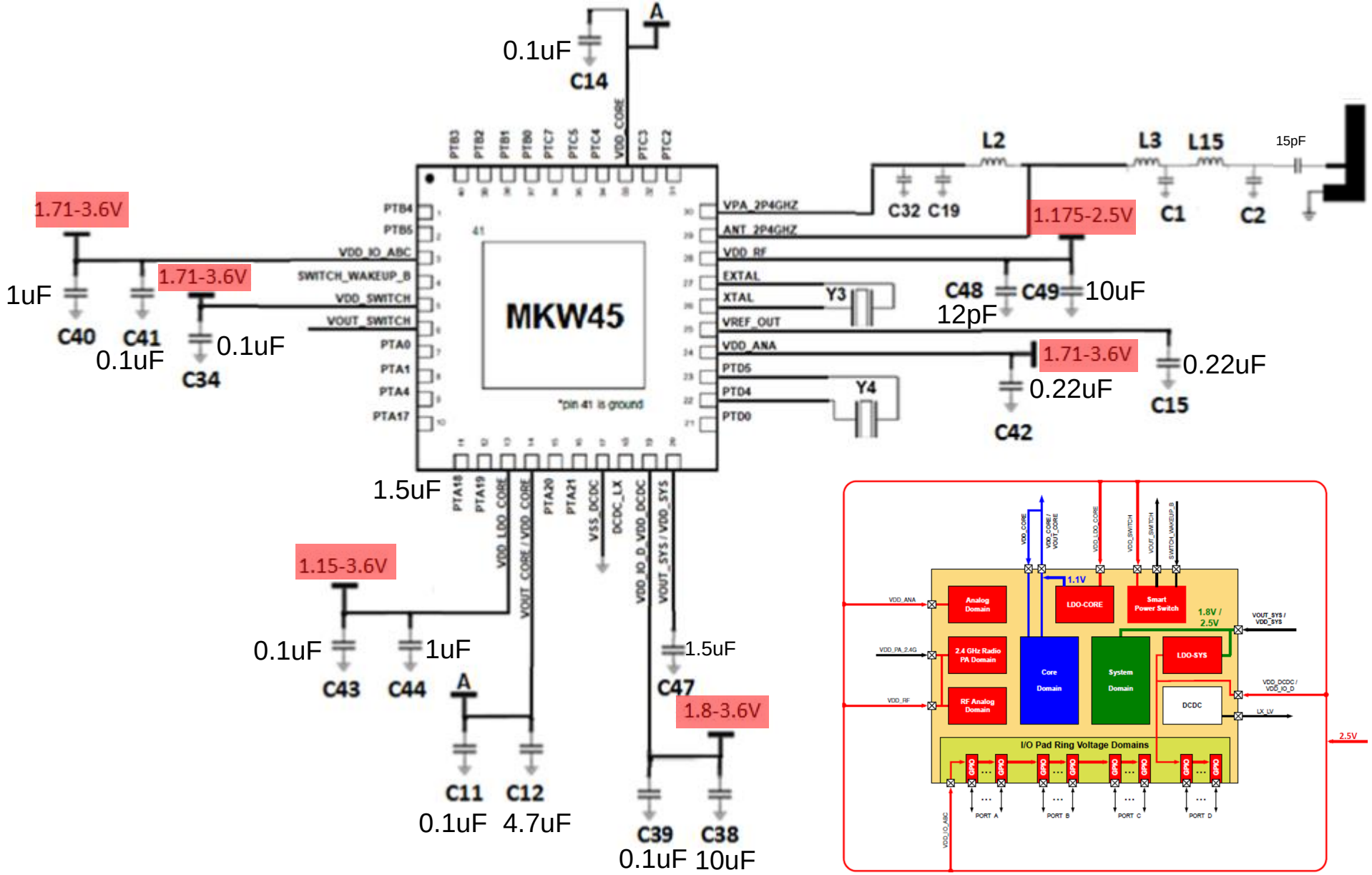


VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally.
For internal generation, VDD_RF voltage must be equal to or exceed VPA + 275 mV.

Warning: During fuse programing, the Vout sys must be set to 2.5V.
➔ Do not connect the pin VDD_SYS (internal connection)

KW45 - DCDC Bypass Schematic HVQFN40 – 6x6

DCDC bypass mode with the possibility of Bluetooth LE Low Power mode active.



KW45 - DCDC Bypass BOM HVQFN40 – 6x6

Bluetooth LE Low Power mode option available (32kHz populated)

Reference	Value
C40,C44	1uF
C11,C14,C34,C39,C41,C43	0.1uF
C12	4.7uF
C15,C42	0.22uF
C48	12pF
C12,C44	4.7uF
C47	1.5uF (or 1uF)
C38,C49	10uF
Printed IFA antenna	2.4GHZ
U1	KW45B41Z Or K32W148
Y3	32MHz
Y4	32.768 kHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(LQG15HZ15NJ02D)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

DCDC Buck Pin configuration HVQFN48 – 7x7

Pin Number	Pin Name	Bypass connection
4	VDD_IO_ABC	1.71-3.6V
6	VDD_SWITCH	1.71-3.6V
7	VOUT_SWITCH	Floating (when not used)
15	VDD_LDO_CORE	1.15-3.6V
16	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
20	DCDC_LX	1.71-3.6V
21	VDD_DCDC	1.8-3.6V
22	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
29	VDD_ANA	1.71-3.6V
30	VREF_OUT	Floating (except the decoupling capacitor)
34	VDD_RF	1.175-2.5V
36	VPA_2P4GHZ	0.9-2.4V
41	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
49	VSS	GND
19	VSS_DCDC	GND

Warning: ➔ Do not connect the pin VDD_SYS (internal connection)

Bluetooth LE Low Power mode option available (32kHz populated)

KW45 - DCDC Bypass Pin configuration

HVQFN40 – 6x6

Pin Number	Pin Name	Bypass connection
3	VDD_IO_ABC	1.71-3.6V
5	VDD_SWITCH	1.71-3.6V
6	VOUT_SWITCH	Floating (when not used)
13	VDD_LDO_CORE	1.15-3.6V
14	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
18	DCDC_LX	floating
19	VDD_DCDC	1.8-3.6V
20	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
24	VDD_ANA	1.71-3.6V
25	VREF_OUT	Floating (except the decoupling capacitor)
28	VDD_RF	1.175-2.5V
30	VPA_2P4GHZ	0.9-2.4V
33	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
41	VSS	GND
17	VSS_DCDC	GND

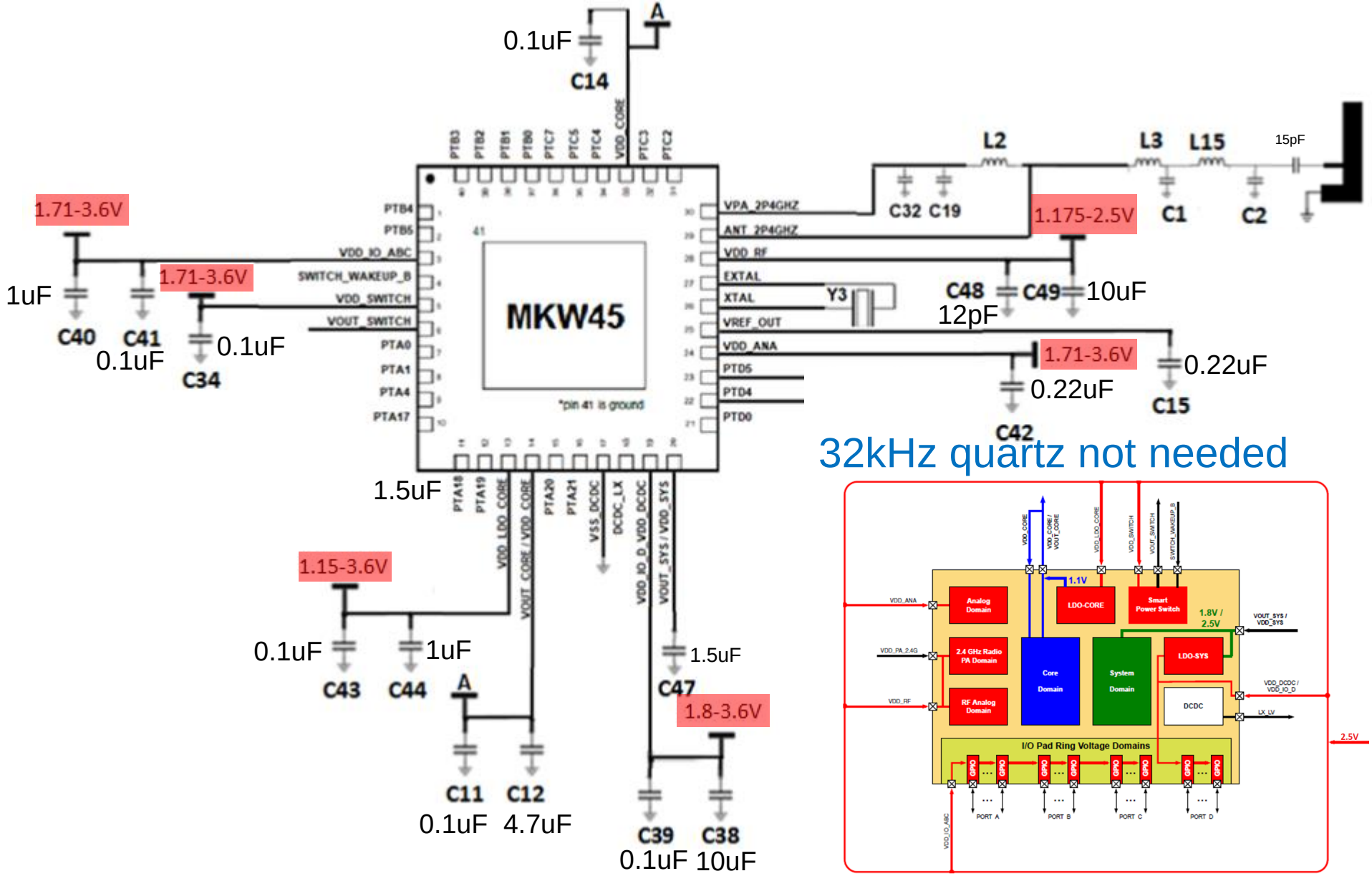
Warning: Do not connect the pin VDD_SYS (internal connection)

BYPASS MODE
NO BLUETOOTH LE
LOW POWER MODE

KW45 - DCDC Bypass Schematic

HVQFN40 – 6x6

No Bluetooth LE Low Power mode



32kHz quartz not needed

KW45 - DCDC Bypass BOM HVQFN40 – 6x6

No Bluetooth LE Low Power mode

Reference	Value
C40	1uF
C38	10uF
C11,C14,C34,C39,C41,C43, C44	0.1uF
C15,C42	0.22uF
C48	12pF
C12	4.7uF
C47	1.5uF (or 1uF)
C49	22uF
Printed IFA antenna	2.4GHZ
U1	KW45B41Z
Y3	32MHz

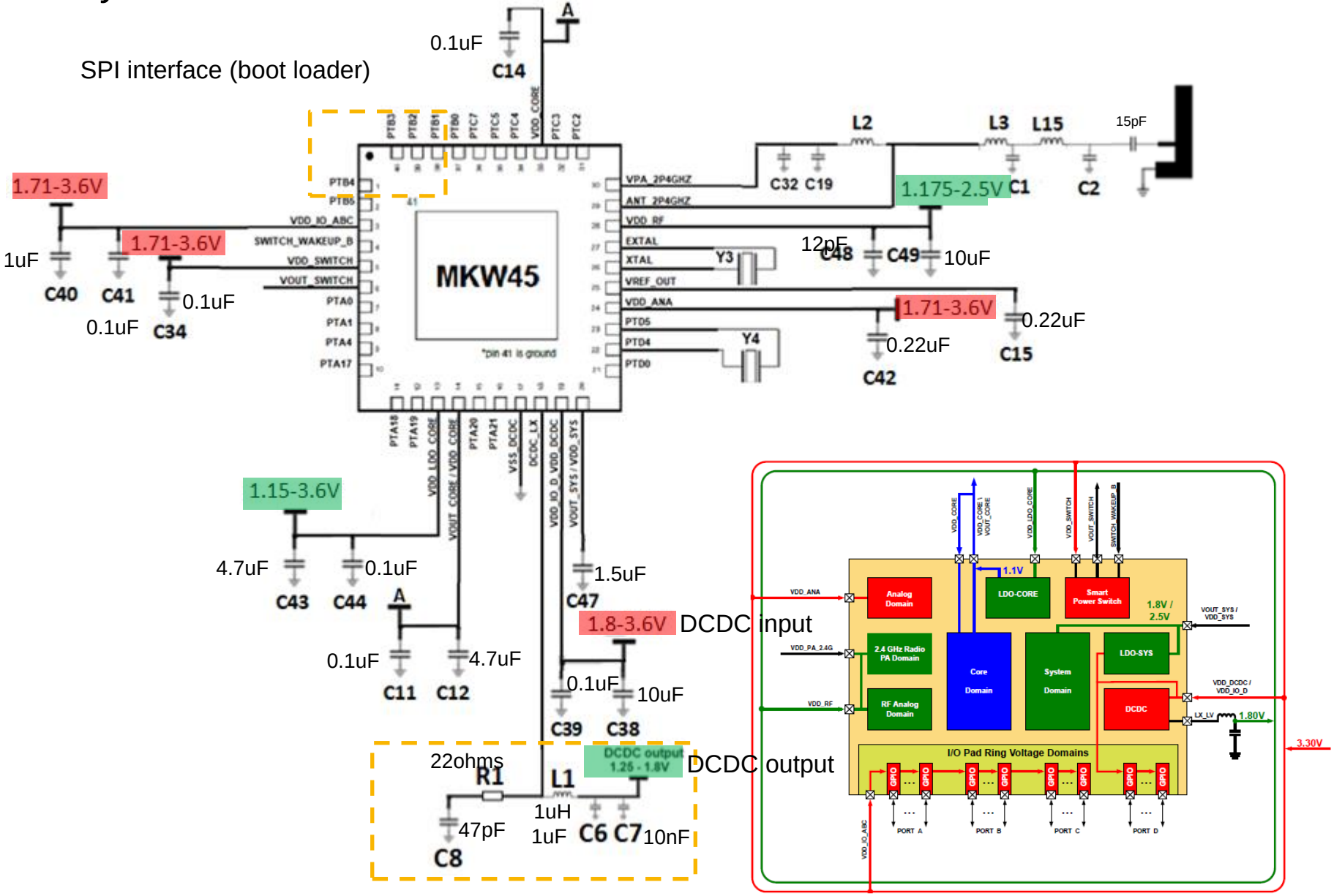
RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(*LQG15HZ15NJ02D*)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

BUCK

KW45 - DCDC Buck Schematic HVQFN40 – 6x6

Possibility of Bluetooth LE Low Power mode active.



KW45 - DCDC Buck Schematic HVQFN40 – 6x6

Possibility of Bluetooth LE Low Power mode active.

FLEXIBLE POWER ARCHITECTURE – DCDC CONFIGURATION

RECOMMENDED SOLUTION FOR TRADEOFF BETWEEN COST AND POWER EFFICIENCY

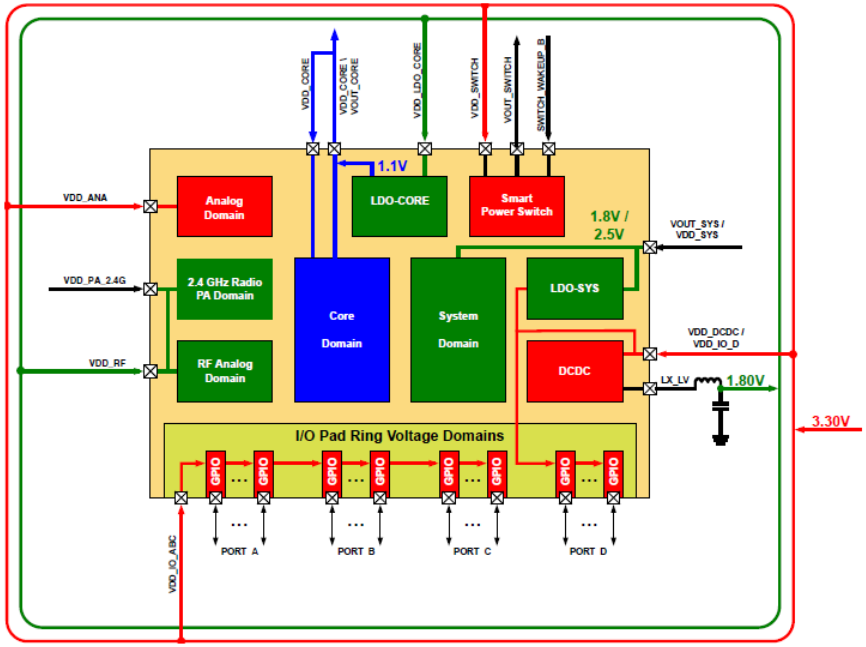
Configuration

- External 3.3V for DCDC , VDD_IO, LDO-SYS
- LDO-CORE, VDD_RF come from DCDC output
- Generate VPA_2PGHZ internally from VDD_RF

Regulator	Output	Input voltage range
DCDC	1.25 / 1.35 / 1.8 / 2.5 V	1.71~3.6 V; >= output + 500 mV
LDO-SYS	1.8 / 2.5 V	1.8~3.6 V
LDO-CORE	1.05 / 1.1 / 1.15 V	1.71~3.6 V (Enable); 0.84~1.21 V (Bypass)

VPA_2P4GHZ	Tx Output Power	VPA source	VDD_RF
0.9 V	+1.8 dBm	External or internal	1.175 ~3.6 V
1.525 V	+7 dBm		1.8 ~ 3.6 V
2.2 V	+10 dBm		2.475~3.6 V

VPA_2P4GHZ voltage depends on Tx power level. It can be powered externally or internally.
For internal generation, VDD_RF voltage must be equal to or exceed VPA + 275 mV.



CONFIDENTIAL AND PROPRIETARY

KW45 - DCDC Buck BOM HVQFN40 – 6x6

Bluetooth LE Low Power mode possible.

Reference	Value
C38,C49	10uF
C6,C40,C44	1uF
C11,C14,C34,C39,C41,C43	0.1uF
C12	4.7uF
C15,C42	0.22uF
C7	10nF
C8	47pF
C48	12pF
C47	1.5uF (or 1uF)
Printed IFA antenna	2.4GHZ
R1	22 ohms
L1 (MLZ2012A1R0WTD25)	1uH
U1	KW45B41Z
Y3	32MHz
Y4	32.768 kHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(*LQG15HZ15NJ02D*)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

KW45 - DCDC Buck Pin configuration

HVQFN40 – 6x6

Pin Number	Pin Name	Bypass connection
3	VDD_IO_ABC	1.71-3.6V
5	VDD_SWITCH	1.71-3.6V
6	VOUT_SWITCH	Floating (when not used)
13	VDD_LDO_CORE	1.15-3.6V
14	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
18	DCDC_LX	1.71-3.6V
19	VDD_DCDC	1.8-3.6V
20	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
24	VDD_ANA	1.71-3.6V
25	VREF_OUT	Floating (except the decoupling capacitor)
28	VDD_RF	1.175-2.5V
30	VPA_2P4GHZ	0.9-2.4V
33	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
41	VSS	GND
17	VSS_DCDC	GND

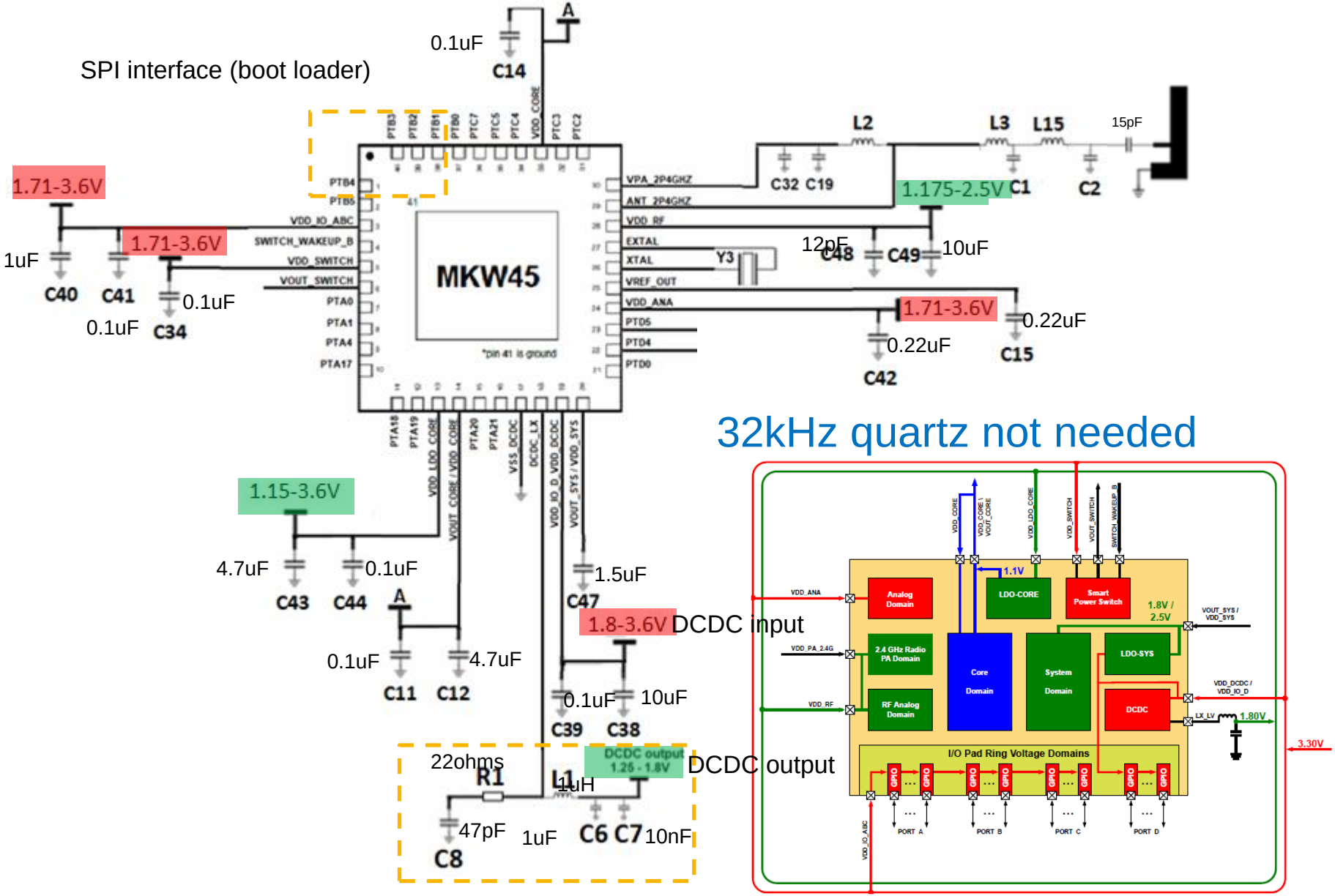
Warning: Do not connect the pin VDD_SYS (internal connection)

BUCK MODE
NO BLUETOOTH LE
LOW POWER MODE

KW45 - DCDC Buck Schematic

HVQFN40 – 6x6

No Bluetooth LE Low Power mode



KW45 - DCDC Buck BOM HVQFN40 – 6x6

No Bluetooth LE Low Power mode.

Reference	Value
C38,C49	10uF
C6,C40,C44	1uF
C11,C14,C34,C39,C41,C43	0.1uF
C12	4.7uF
C15	0.22uF
C7	10nF
C8	47pF
C48	12pF
C47	1.5uF (or 1uF)
Printed IFA antenna	2.4GHZ
R1	22 ohms
L1 (MLZ2012A1R0WTD25)	1uH
U1	KW45B41Z Or K32W148
Y3	32MHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(LQG15HZ15NJ02D)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

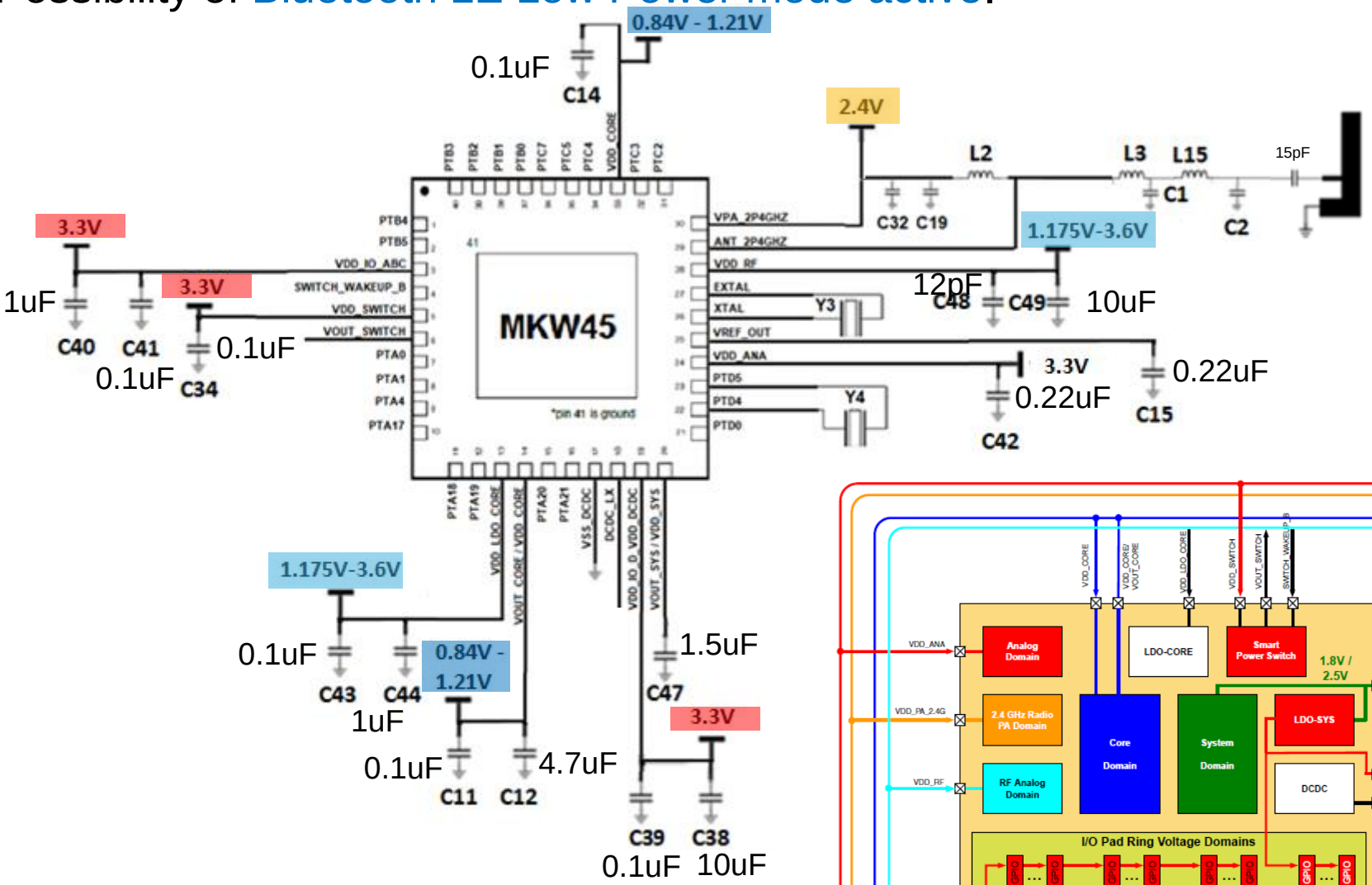
Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

PMIC SUPPLY

KW45 – PMIC supply

HVQFN40 – 6x6

Possibility of Bluetooth LE Low Power mode active.



POWER SWITCH

KW45 EVK – Power config diagram – Power Switch

SMART POWER SWITCH LOW POWER USE CASE

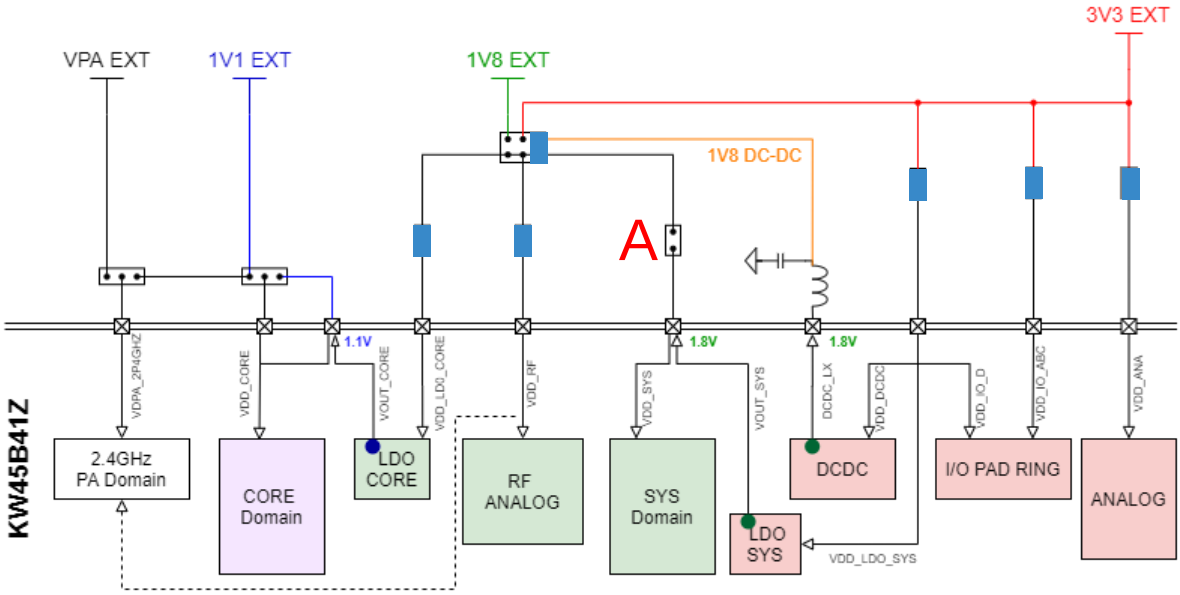
<100 NA TOTAL LEAKAGE CURRENT

Configuration

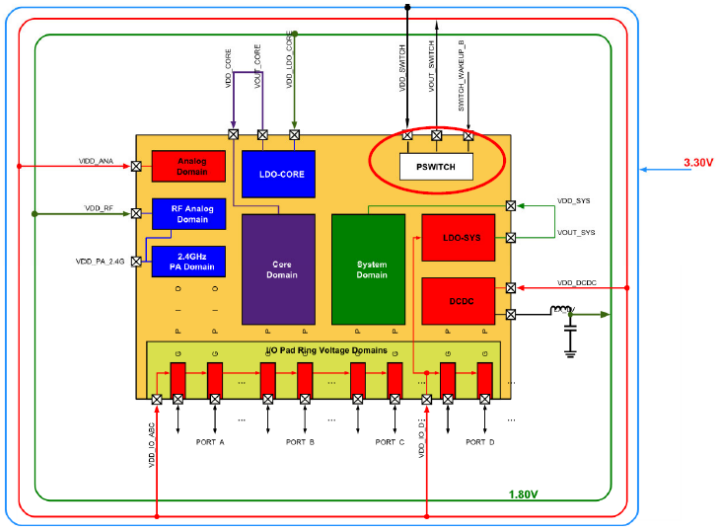
- External 3.3 V supply to Smart Power Switch
- Power switch output connected to
  - DCDC, LDO-SYS, VDD_ANA and VDD_IO
- DCDC output connected to
  - LDO-CORE, VDD_RF

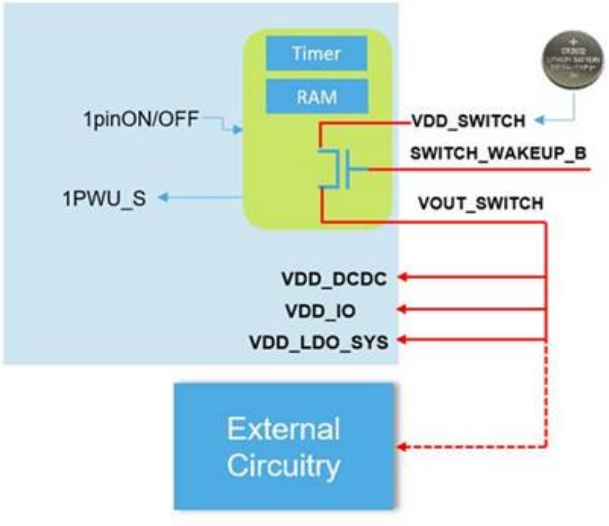
Usage

- Software can disable smart power switch in Deep Power Down modes
- Reenable Switch from:
  - External wakeup pin
  - Internal timer with FRO16K
- Standby RAM regulator support 8KB RAM retention
- Can configure to disable during manufacturing process that disconnects battery from device in order to maximize battery life



Warning: During fuse programing, the Vout sys must be set to 2.5V.
➔ Do not connect the pin VDD_SYS (pin) jumper on A





SMART POWER SWITCH
ULTRA LOW POWER & FLEXIBLE

Performance
- <100 nA (typ) leakage current when OFF (no RAM retention, timer disabled)
- <700 nA (typ) leakage current when OFF (8KB RAM retention + timer)
- 40 mA active output current capability

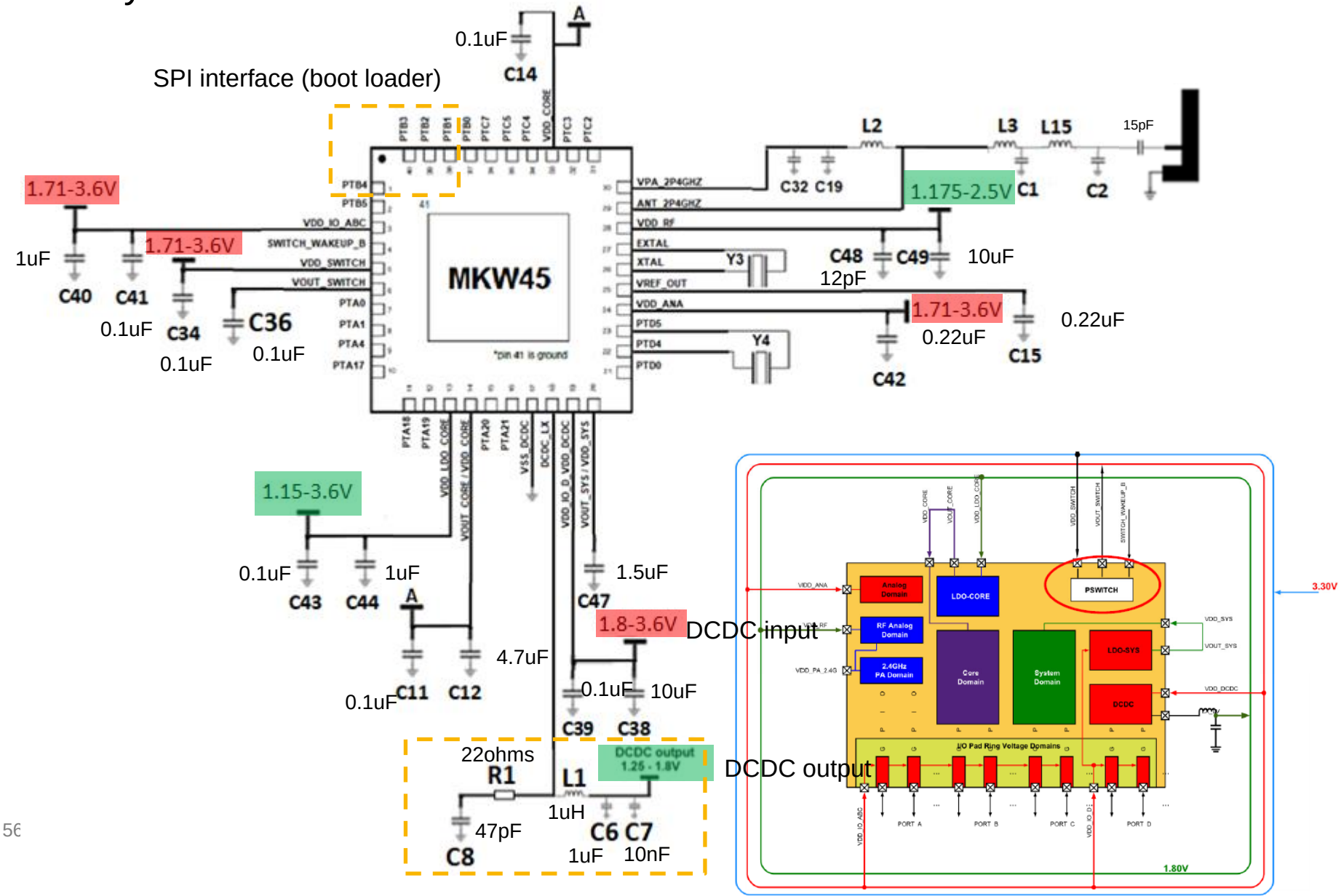
Flexible
- Can be used to power partial or entire chip supply
- Can be used to power external circuits saving BOM costs

Configurable power control
- One external wakeup pin (SWITCH_WAKEUP_B) to enable power switch
- Internal Timer timeout (from 7.8125ms to 1s) to enable power switch
- Dedicated register bits to control power switch in Low Power mode / Active mode

Data storage
- Support up to 8KB RAM retention

KW45 - Power switch Schematic HVQFN40 – 6x6

Possibility of Bluetooth LE Low Power mode active.



KW45 - DCDC Buck BOM

HVQFN40 – 6x6

Reference	Value
C38,C49	10uF
C6,C40,C44	1uF
C11,C14,C34,C36,C39,C41,C43	0.1uF
C12	4.7uF
C15,C42	0.22uF
C7	10nF
C8	47pF
C48	12pF
C47	1.5uF (or 1uF)
Printed IFA antenna	2.4GHZ
R1	22 ohms
L1 (MLZ2012A1R0WTD25)	1uH
U1	KW45B41Z
Y3	32MHz
Y4	32.768 kHz

RF matching *(whatever the RF output power)*	
C9	1 uF
C10	12 pF
L2 *(LQG15HZ15NJ02D)*	15 nH
L3 (resistor shunt)	0 ohm
C1 *(GCM1555C1H1R1BA16)*	1.1 pF
L15 (*LQG15WH1N5B02*)	1.5nH
C2 *(GCM1555C1H2R5BA16)*	2.5 pF

Note: C38,C40, C42, and C46 have different values from the schematic. This is due to the LPC current probe which need bigger decoupling capacitors.

KW45 – Power Switch Pin configuration

HVQFN40 – 6x6

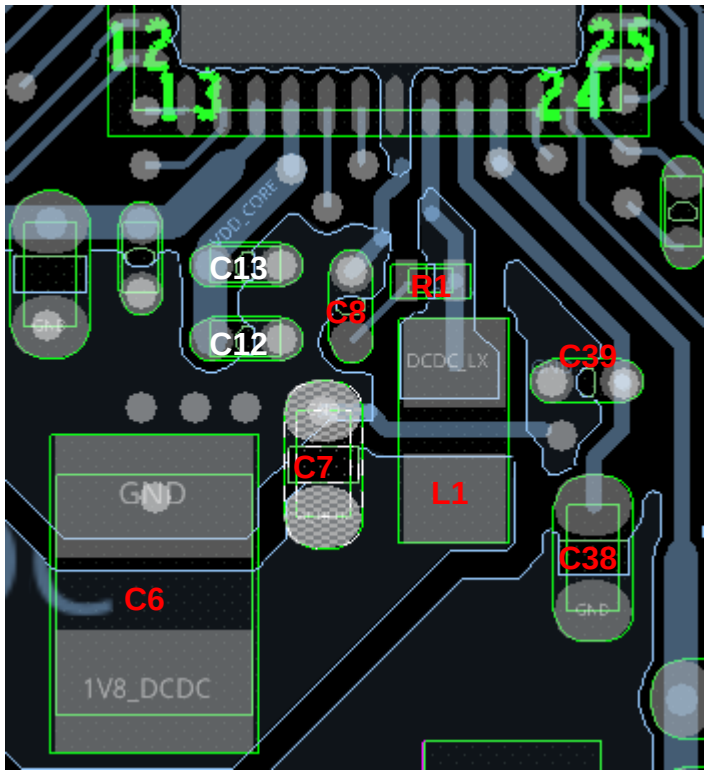
Pin Number	Pin Name	Bypass connection
3	VDD_IO_ABC	1.71-3.6V
5	VDD_SWITCH	1.71-3.6V, Connected to decoupling capacitor 0.1uF
6	VOUT_SWITCH	1.71-3.6V, Connected to decoupling capacitor 0.1uF
13	VDD_LDO_CORE	1.15-3.6V
14	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
18	DCDC_LX	1.71-3.6V
19	VDD_DCDC	1.8-3.6V
20	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
24	VDD_ANA	1.71-3.6V
25	VREF_OUT	Floating (except the decoupling capacitor)
28	VDD_RF	1.175-2.5V
30	VPA_2P4GHZ	0.9-2.4V
33	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
41	VSS	GND
17	VSS_DCDC	GND

Warning: Do not connect the pin VDD_SYS (internal connection)

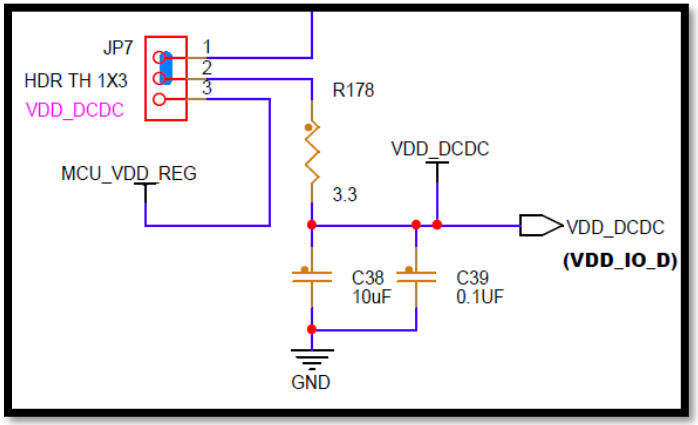
LAYOUT RECOMMENDATION

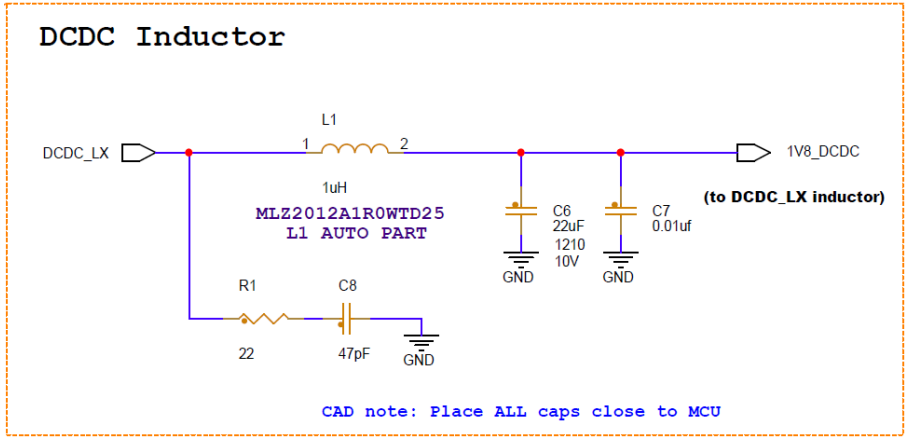
Evaluation board – HW Recommendation - DCDC

1. **C38 & C39** must be as close as possible to the DCDC Vdd but not so much for the DCDC vss. Recommend is to place them with the LX connection to the inductor passing between their terminals. It is really critical to reduce the loop formed by the DCDC VDD/VSS pins and those capacitors. Please add more vias to the ground plane.
2. In a similar fashion place **C7** in a way that it's connection to the inductor **L1** is where it is now and VSS connection gets close to the chip. Adding vias to better connect vss to the ground plane will help.
3. It is interesting to move **C6** closer to the IC and add vias as on this example.
4. **C8** in a similar fashion as **C7** may be helpful for emissions >300MHz.
5. **L1** is 1uH for the KW45/K32W148 (iso 10uH on KW35/36/37/38/39 reference design)



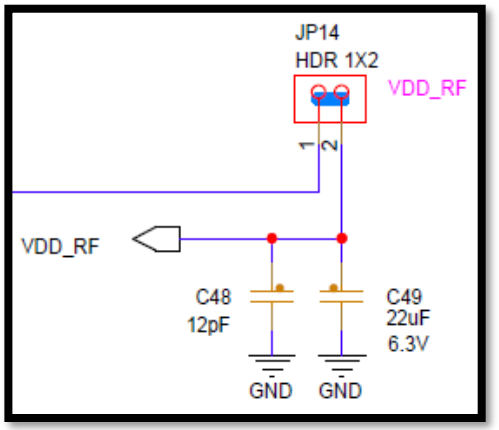
Note:
Having short connection and small area loops is the most important thing to contain any emissions. Bringing those caps closer to the chip will be helpful. And having the ground plane well preserved underneath those components (as it is on the current layout) will greatly help reduce the effect of the inductor not being really close to the chip.



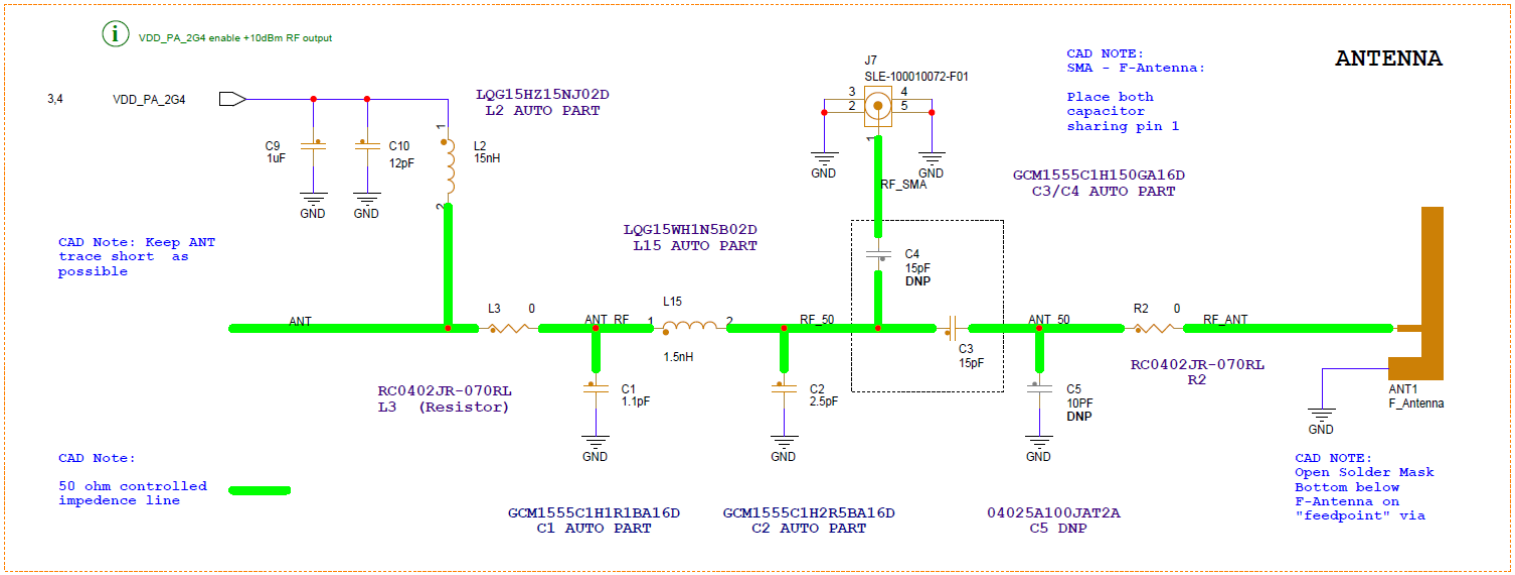


Evaluation board – HW Recommendation - Radio

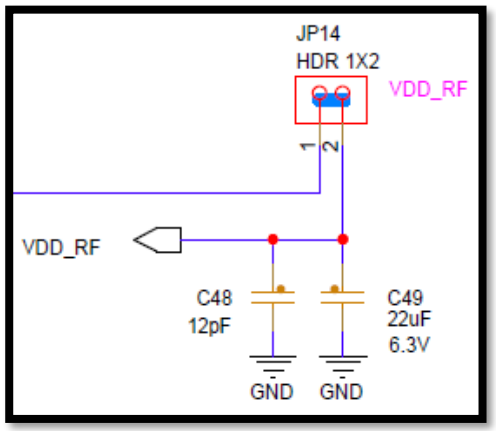
- The value capacitor **C48** used for an RF short are 12pF
- **C10** must be as close to L2 as possible
- **C49**=22uF on VDD_RF could be placed as DNP
- The pull up inductor **L2** placement must follow the layout example
- The **antenna matching** components must be at minimum spacing to the DUT and each other, as on the current layout.
- **C48** needs to be placed in order to have the best isolation with ANT_RF line. VDDRF line needs to be isolated with VDDRF_line. Please copy the current layout
- Need isolation between VDDRF and UART signals.
- VDD_PA_2g4 needs to be isolated vs PTC0

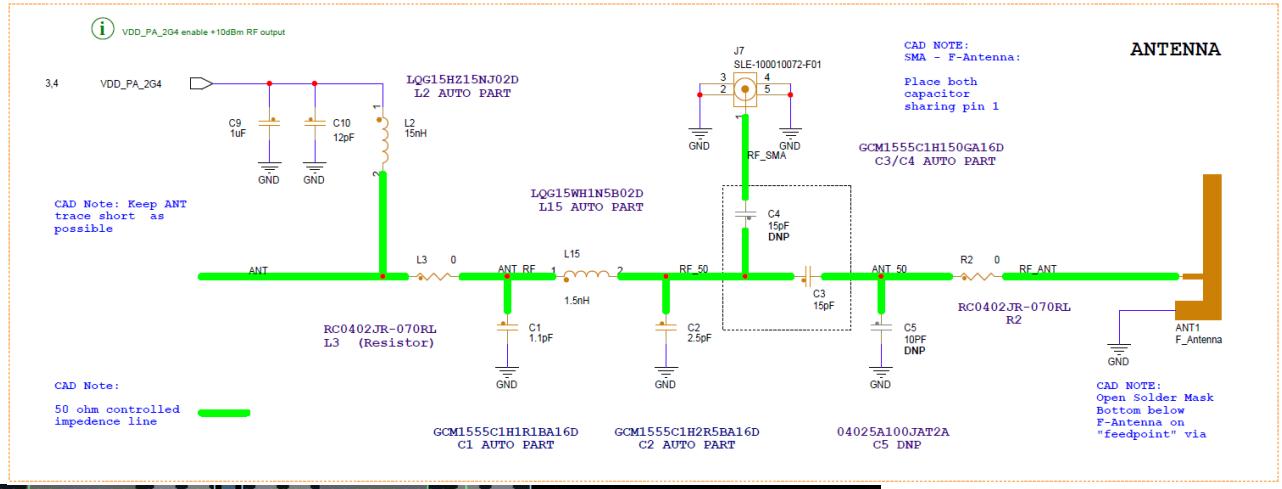


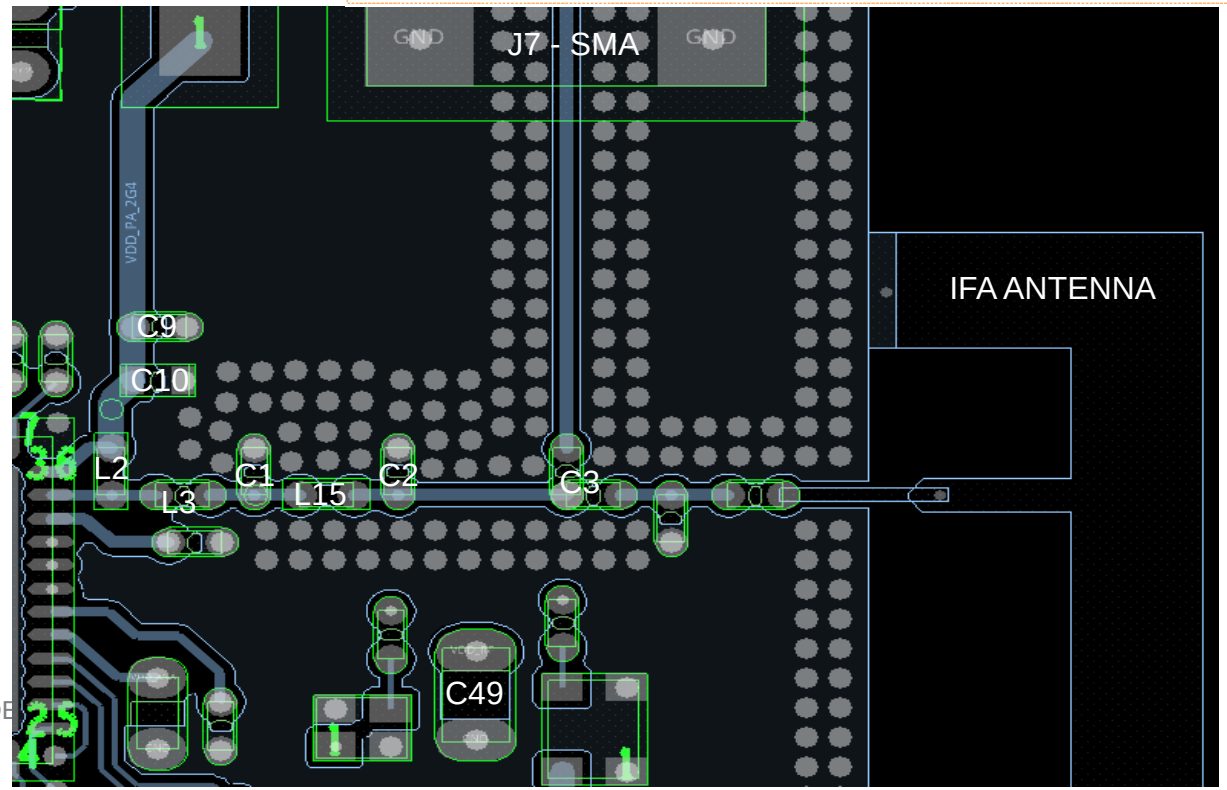
- General comment: The power planes which create huge fat nets are for the VDD_ANA and VDD_SYS. No benefit to reduce the power plane.



Evaluation board – HW Recommendation - Radio

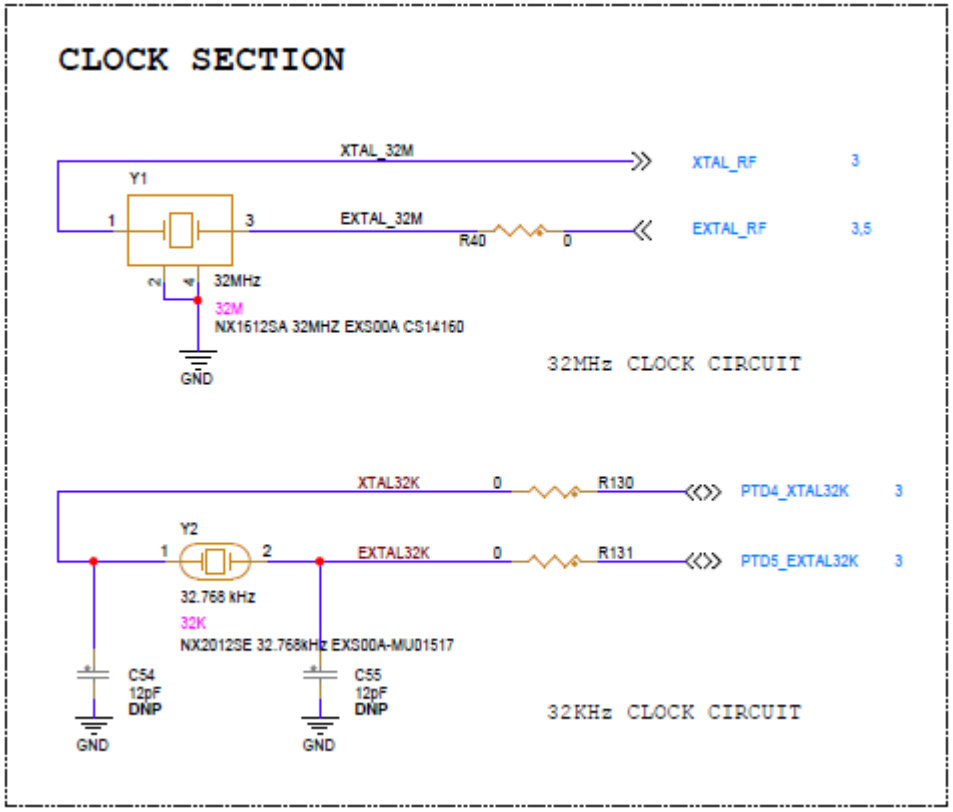


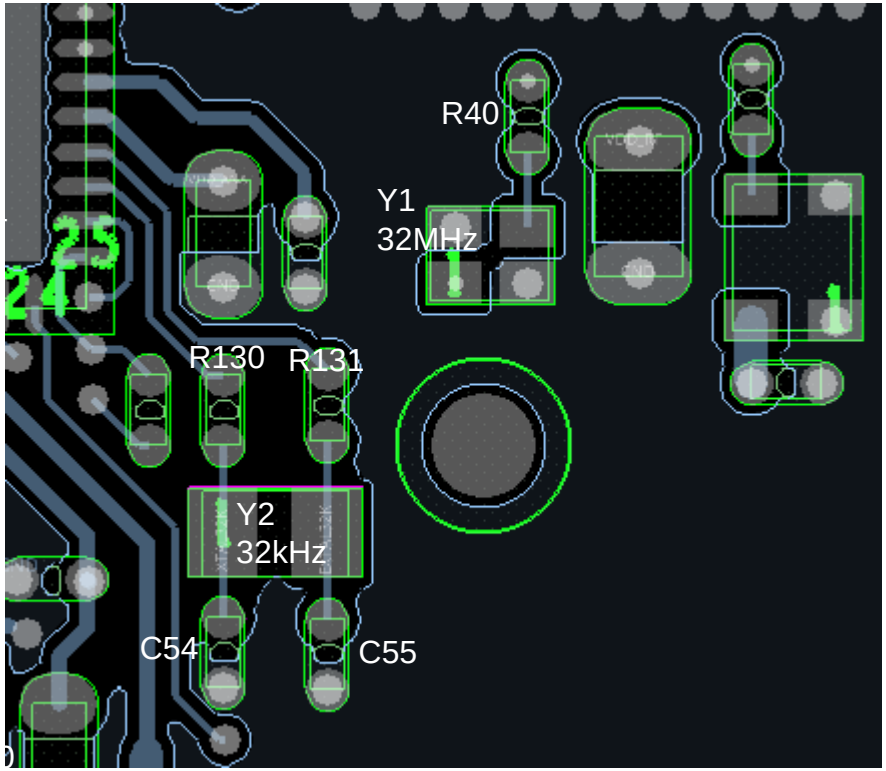




Evaluation board – HW Recommendation - Clocks

- 32MHz & 32kHz wire length must be as symetric as possible
- 32kHz quartz is not necessary to be as closed as possible from the DUT (KW45/K32W148)



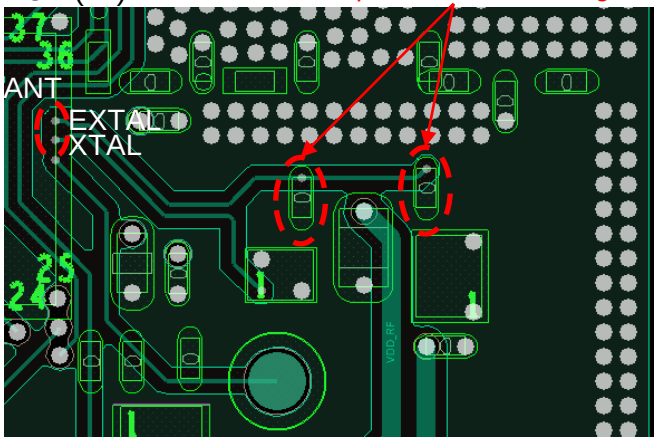


Evaluation board – HW Recommendation - Clocks

- Special focus on 32MHz wires to help on a very good layout.

TOP (L1)

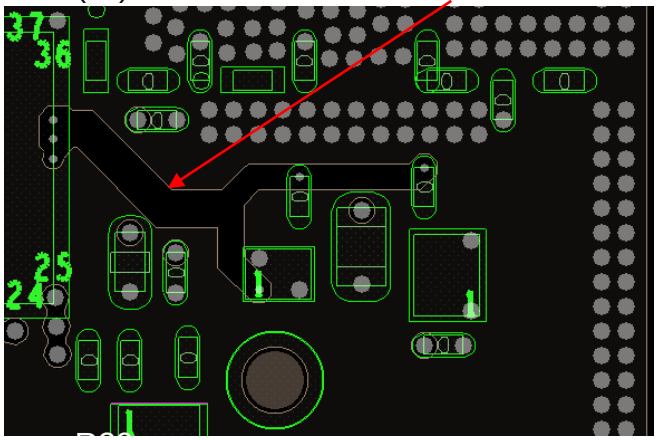
Perpendicular to ANT signal



- Better isolation with perpendicular component to ANT wire
- Via under EXTAL & XTAL to go to L3 are excellent

GND (L2)

Excellent length is as short as possible

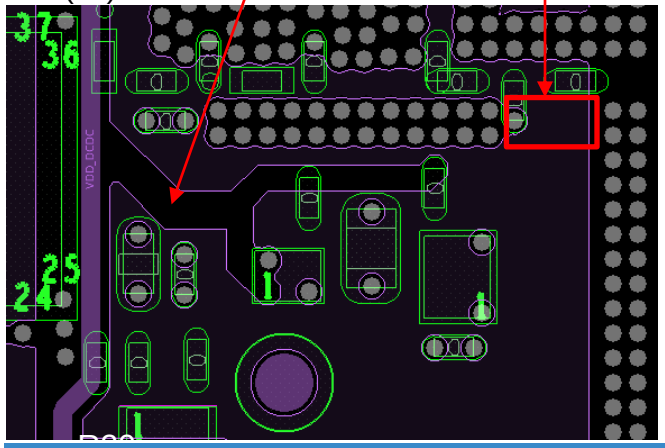


- To reduce capacitance on EXTAL & XTAL GND plane can be opened over XTAL & EXTAL wires
- The shielding is already present on TOP (L1) being GND in these area

Pwr (L4)

Open the Pwr plane Under EXTAL & XTAL

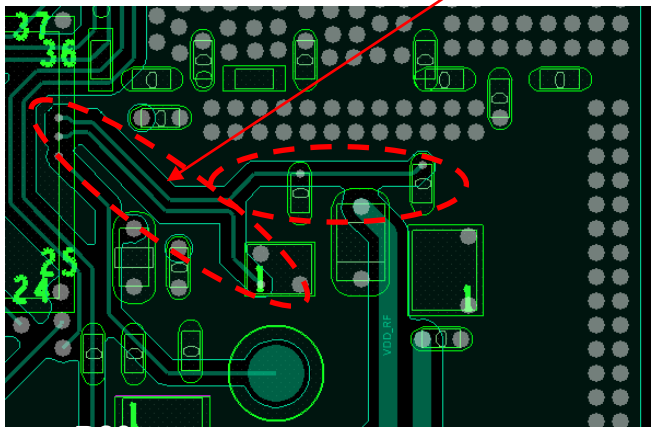
Remove VIAs For a better Pwr



- Under EXTAL & XTAL Pwr net need to be open to reduce coupling capacitance to PWR
- Some GND vias can be removed to have a better connection of PWR signal

In1 (L3)

Shielding area

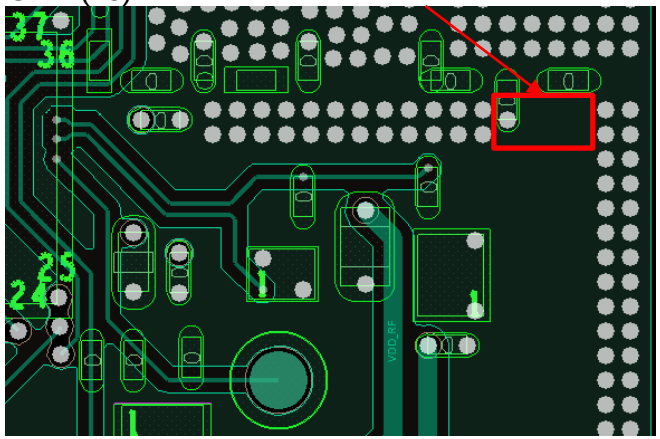


- To avoid coupling XTAL with XTAL_OUT a shield is applied
- To avoid any coupling on XTAL a shield on TOP is applied

Evaluation board – HW Recommendation - Clocks

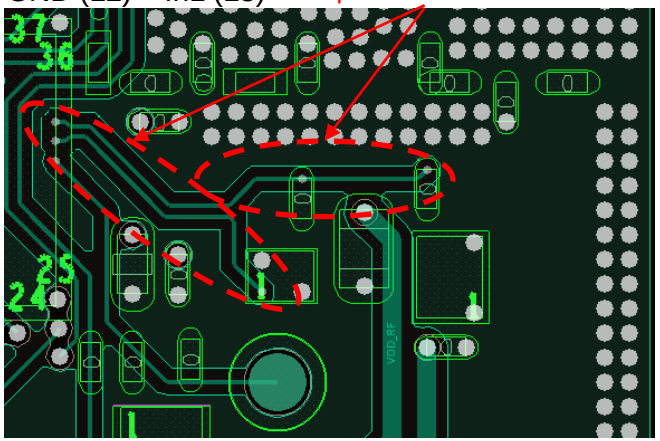
- Special focus on 32MHz wires to help on a very good layout.

GND (L5) Remove some VIAs



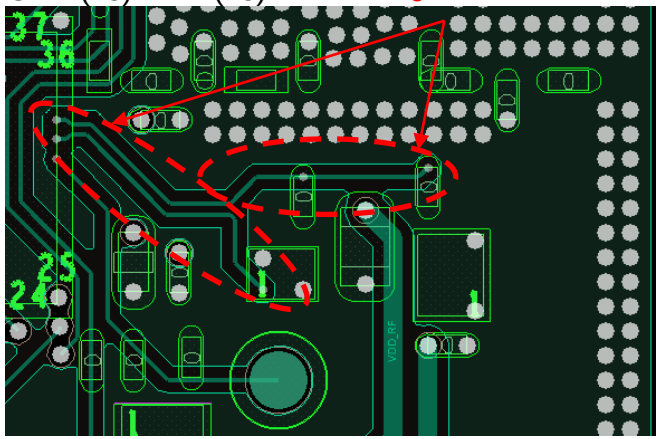
➢ Remove some VIAS for a better Pwr (L4) connection

GND (L2) + In1 (L3) Open L2 over EXTAL & XTAL in L3



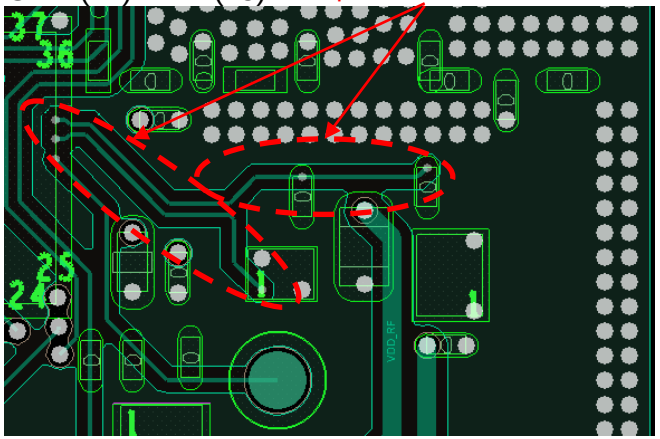
➢ Open L2 over XTAL & EXTAL

GND (L5) + In1 (L3) Shielding the 32MHz wires



➢ Shield to GND near EXTAL & XTAL in In1 (L3)

GND (L2) + In1 (L3) Open L2 over EXTAL & XTAL in L3



➢ Open L2 over XTAL & EXTAL

COMPLEMENTARY INFORMATION

Recommendation

KW45/K32W1 requires signed firmware to be loaded into the NBU. This happens through the Bootloader. **PTC2 and PTC3 are the UART connection to the Bootloader**. We recommend to have an option to connect them to a UART to USB converter (for PC connection).

NXP recommend to have a way to **pull PTA4 to logic high** in order to enter the device in **bootloader mode**.

Make sure that everything connected to PORTD is at the same voltage as VDD_IO_D. Same for PORTA, B and C and VDD_IO_ABC.

Recommendation connection for unused IOs

HVQFN48WF – 7x7

Table 54. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VOUT_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_CORE	Connect to VDD_LDO_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_SYS	Connect to VDD_IO_D	When the LDO is bypassed, the input and output should be connected together and tied to
			an external supply. The regulator should also be disabled in software.
Power	VDD_DCDC	Ground	When the DCDC is not used, the input should be tied to VSS through a 10 kΩ resistor.
Power	DCDC_LX	Float	The input VDD_DCDC should be tied to VSS with 10 Kohm
Power	VDD_IO_D	Must be powered	VDD_IO_D is used to power parts of the system power controller (SPC) and must be powered to use the chip. If LDO_SYS is not being used, then tie VDD_IO_D to VOUT_SYS and supply power from an external source. The regulator should also be disabled in software.
Power	VDD_PA_2.4GHz	Float	VDD_PA_2.4GHz is always driven, either from internal LDO sourced by VDD_RF, or from external supply.

CONFIDENTIAL AND PROPRIETARY

Recommendation connection for unused IOs

HVQFN48WF – 7x7

Power	VDD_SWITCH	Must be powered	Powers FRO16 and a portion of RAM.
Power	VOUT_SWITCH	Float	
Power	VDD_IO_ABC	Must be powered	VDD_IO_ABC powers the mux logic for PORTA, PORTB and PORTC. It must be powered during POR. The recommendation is to keep it powered, but it can be connected to the output of the Smart Power Switch and be left floating in shelf storage mode.
Power	VDD_ANA	Float	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_DCDC	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_RF	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n_x*	Float	
Analog/non-GPIO	VREF_OUT	Float	Analog output - Float
Analog/non-GPIO	TAMPERx	Float	
Analog/non-GPIO	RTC_WAKEUP_B	Float	
Analog/non-GPIO	RTC_RTCCLKOUT	Float	
Analog/non-GPIO	EXTAL32K	Float	
Analog/non-GPIO	XTAL32K	Float	Analog output - Float
Analog/non-GPIO	EXTAL_32M	Float	
Analog/non-GPIO	XTAL_32M	Float	Analog output - Float
GPIO/Analog	PTx/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	PTD1/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)

Additional information – both packages

The DTM pins are available for both 48 pins and 40 pins packages. The options are:

48-pin only:

- PTA16 – RF_UART_SIN
- PTA17 – RF_UART_SOUT
- PTD1 – RF_UART_SIN
- PTD2 – RF_UART_SOUT

Both 40-pin & 48-pin

- PTA18 – RF_UART_SIN
- PTA19 – RF_UART_SOUT
- PTB2 – RF_UART_SIN
- PTB3 – RF_UART_SOUT
- PTC2 – RF_UART_SIN
- PTC3 – RF_UART_SOUT

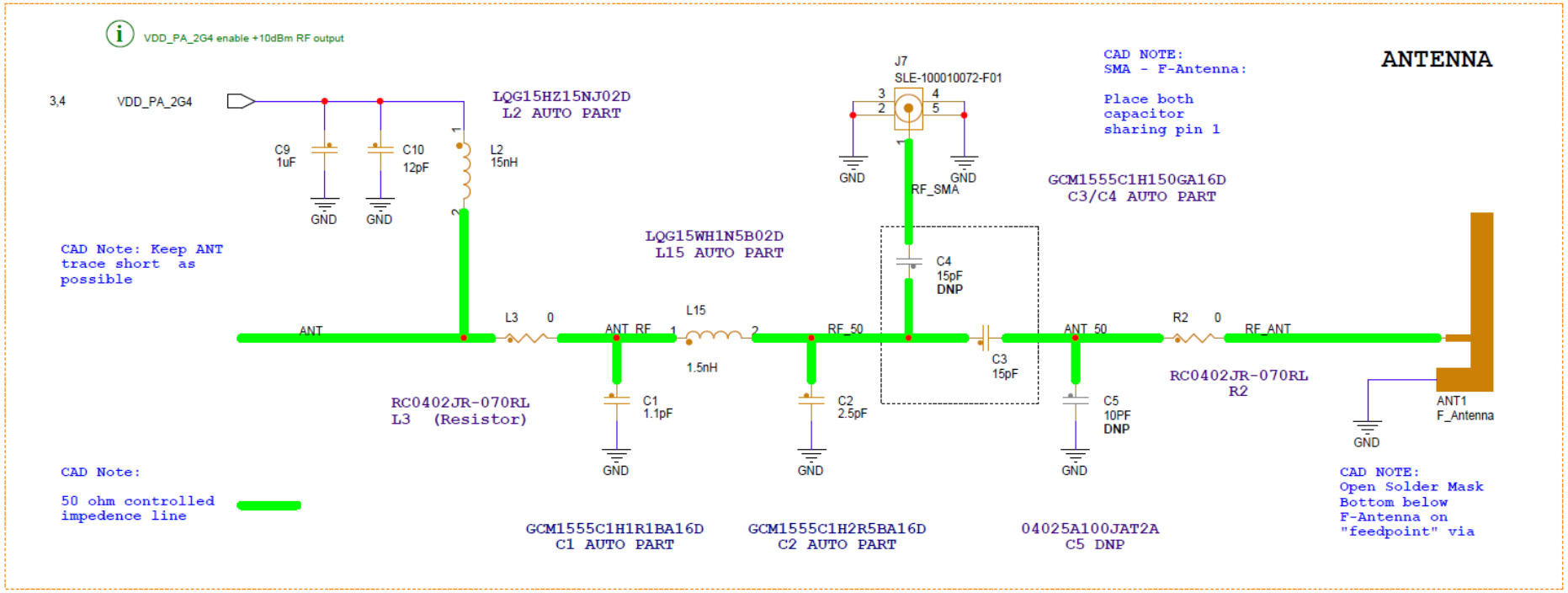
RF Matching – Automotive compliant

RF Matching Goals:

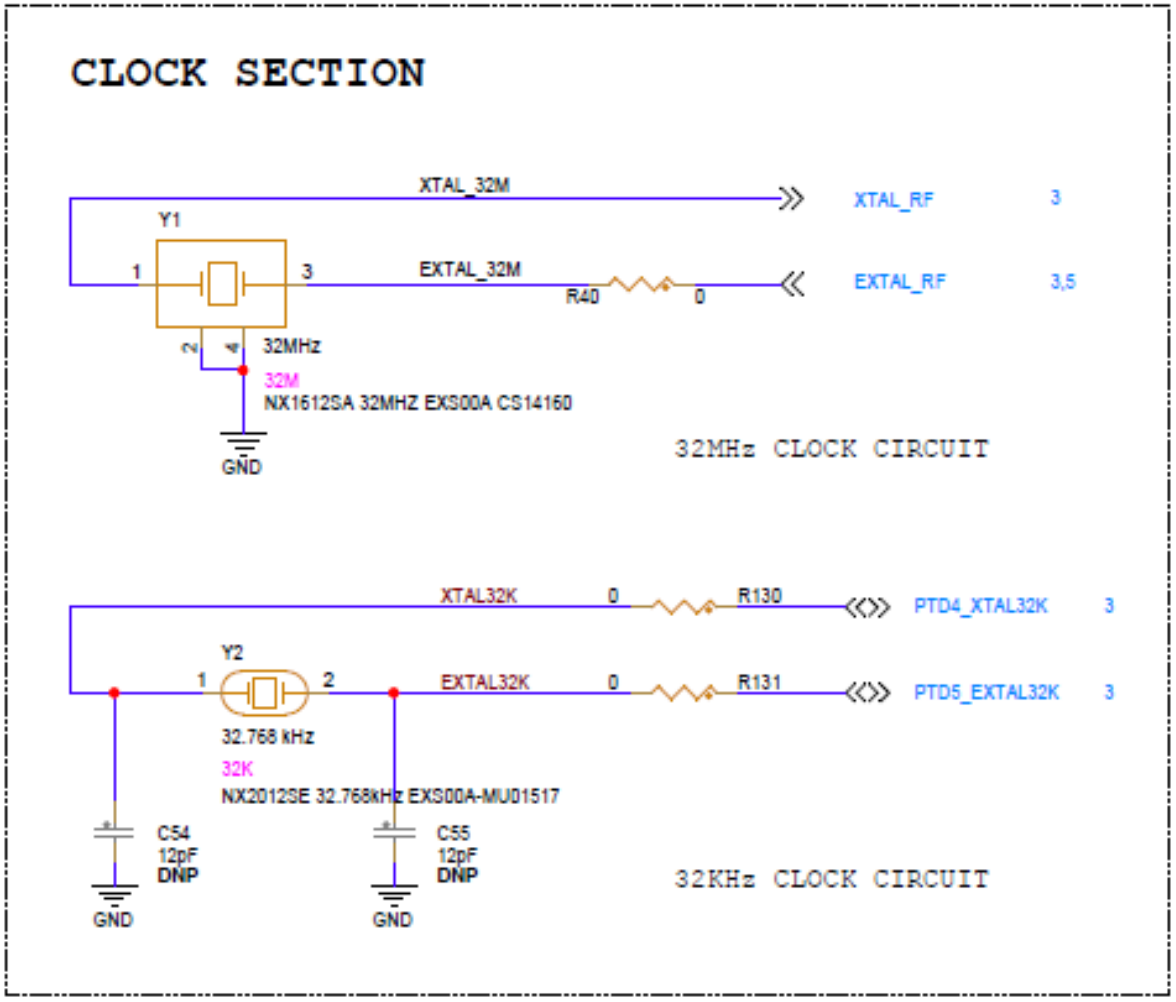
- Only certified automotive component have been used.
- Ensure sensitivity performance was the focus of this RF Matching
- PASS internal specification regarding 2nd and 3rd harmonics with 10dBm output power.
- Same Matching for 0dBm, 4dBm, 7dBm and 10dBm output power.

Based on previous 10dBm RF Matching done with LQW inductance we got a good staring point to found the best compromise with those automotive components.

Evaluation board – Recommendation



Evaluation board – Recommendation – Clocks



Alternate Y1

For Bluetooth LE and GFSK 32MHz and 26MHz quartz references

Manufacturer	Series	Part Number	Frequency
NDK	NX1612SA	EXS00A-CS14160	32MHz
NDK	NX2016SA	EXS00A-CS13636	26MHz

Manufacturer	Series	Part Number	Frequency
NDK	NX2016SA	EXS00A-CS14161	32MHz

Alternate Y2

For Bluetooth LE and GFSK 32kHz quartz reference

Manufacturer	Series	Part Number	Frequency
NDK	NX2016SA	EXS00A-MU01517	32,768kHz
NDK	NX2012SA	EXS00A-MU00801	32,768kHz

IO current drive @12mA

First the list of the specific pins which could handle 12ma current drive instead of 6mA on other IO pins:

- PTA18-19
- PTB4-5
- PTC0-1
- PTC4-5

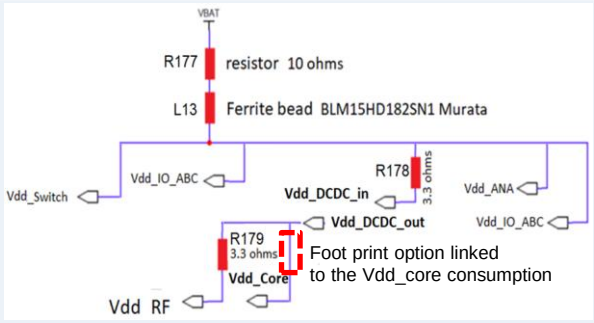
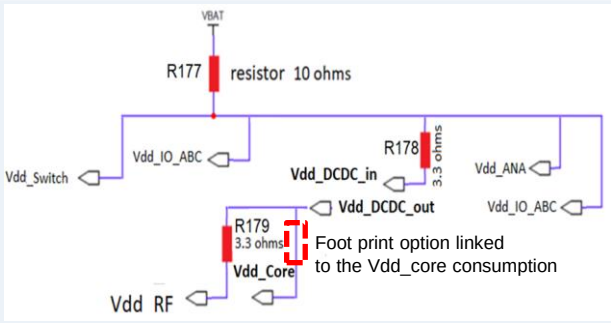
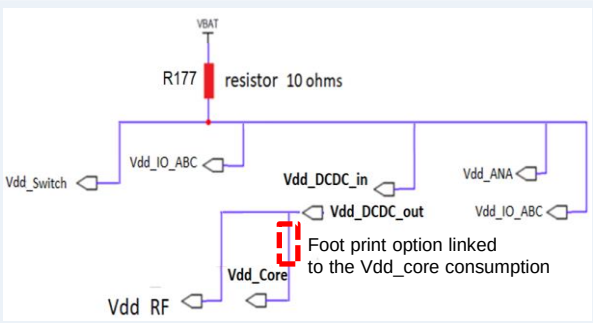
Note that both the DSE0 and DSE1 bits in the control register for that pin must be set in order to get the highest drive strength.

Schematic – Recommandation for coincell only
(peak of current below 10mA)
Reduced current peak

DCDC Buck Mode – Coincell – Summary

Suitable for battery (coincell) applications only

Solution to reduce the DCDC current peaks and current peaks on Tx signals (+10/+7/+0dBm) during Bluetooth LE events (Advertising, Connect & Scan) is to add serial resistor(s) on different supplies.
It will limit the peaks of current below 10mA and avoid voltage drop on the battery.
Voltage drop occurs due to the serial resistor(s) but it never goes down to POR threshold (up to 105°C).

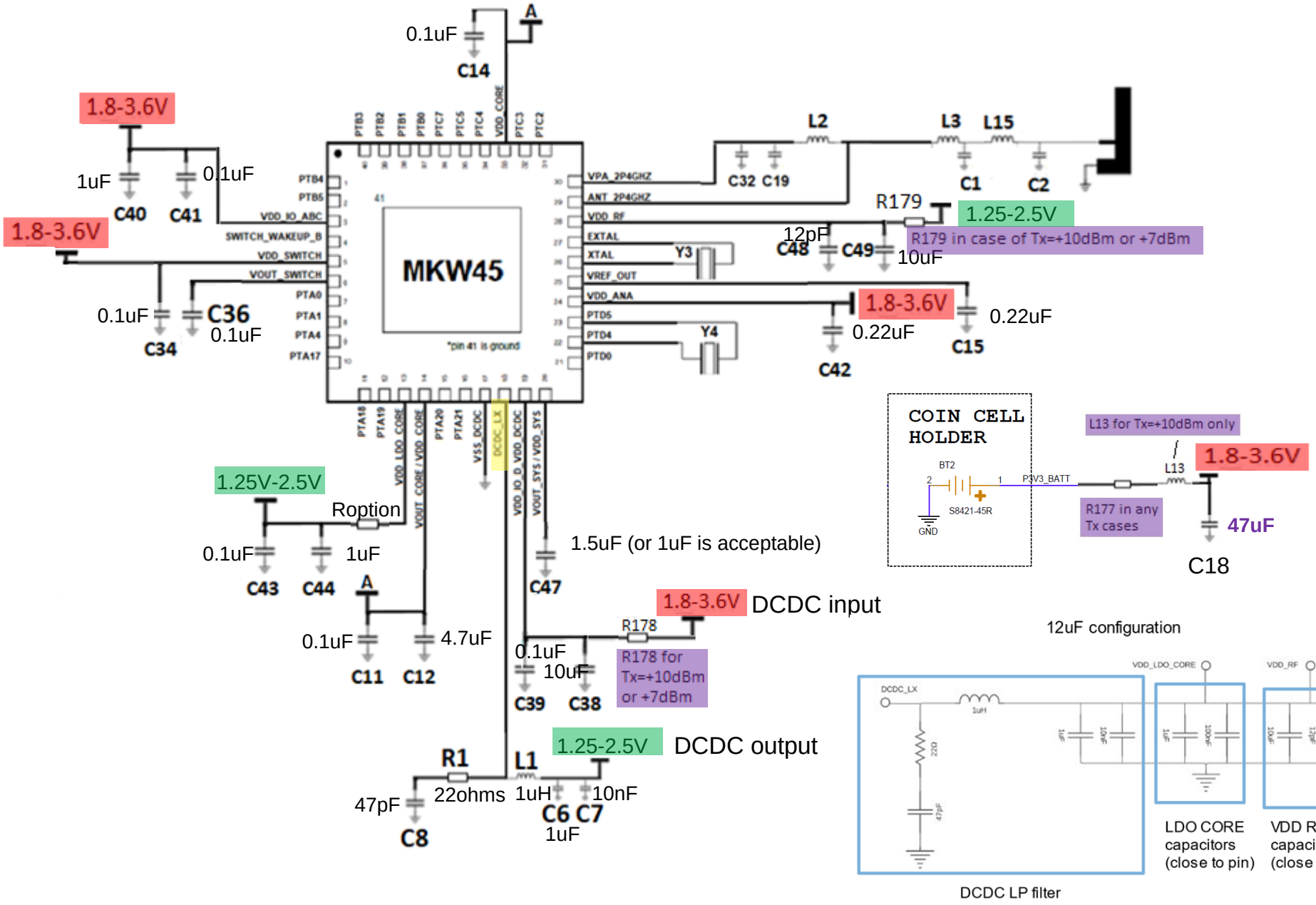
Maximum Tx output @+10dBm	Maximum Tx output @+7dBm	Maximum Tx output @+0dBm
Maximum peak of current: <1mA	Maximum peak of current: 8mA	Maximum peak of current: 4.5mA
		

In addition, change the Vbat decoupling capacitor C18 from 10uF to 47uF.

CONFIDENTIAL AND PROPRIETARY

Buck Mode using coincell

HVQFN48 – 7x7



CISPR25 Automotive Chinese certification

The KW45-EVK and K32W1-EVK could withstand the CISPR25 certification.

To pass this certification for +10dBm Tx output power, the EVK board needs to be modified as follow:

Table 8 (continue)

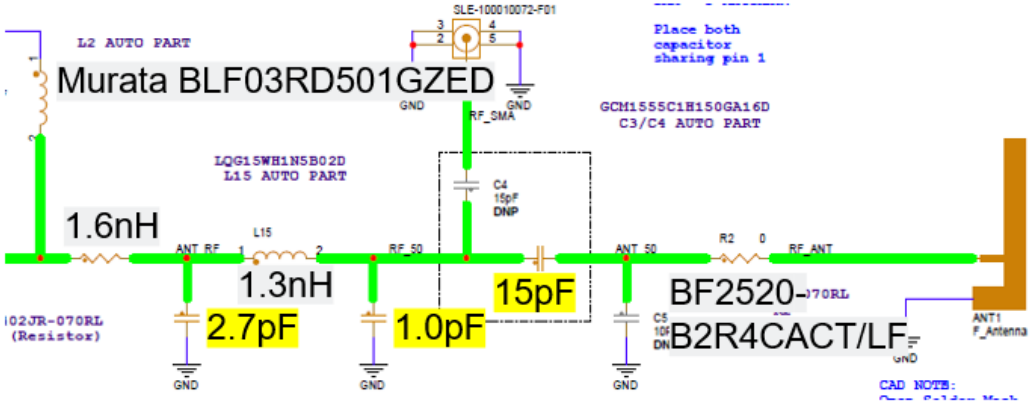
RF Service [User band in MHz]	Frequency [MHz]	RBW (kHz)	Limits [dBuV/m]		
			Peak	Average	Quasi- Peak
Bluetooth	2400 - 2690	120	44	24	N/A
5G	3000 - 5000	≥1000	64	44	N/A
GNSS	5010 – 5030	9/10	N/A	16	N/A
WLAN	5000 - 6000	≥1000	68	48	N/A

1) If test method, RE02, has been performed, these bands may be omitted.

- Replace the RF matching component values

nH	nH	pF	nH	pF	pF
L2	L3	C1	L15	C2	C3
BLF03RD501GZED	1.6	2.7	1.3	1.1	15

- Replace R2 by a Band Pass Filter at R2. Reference BF2520-B2R4CACT/LF



Note: The default EVK board pass the certification with Tx output power at -15dBm.

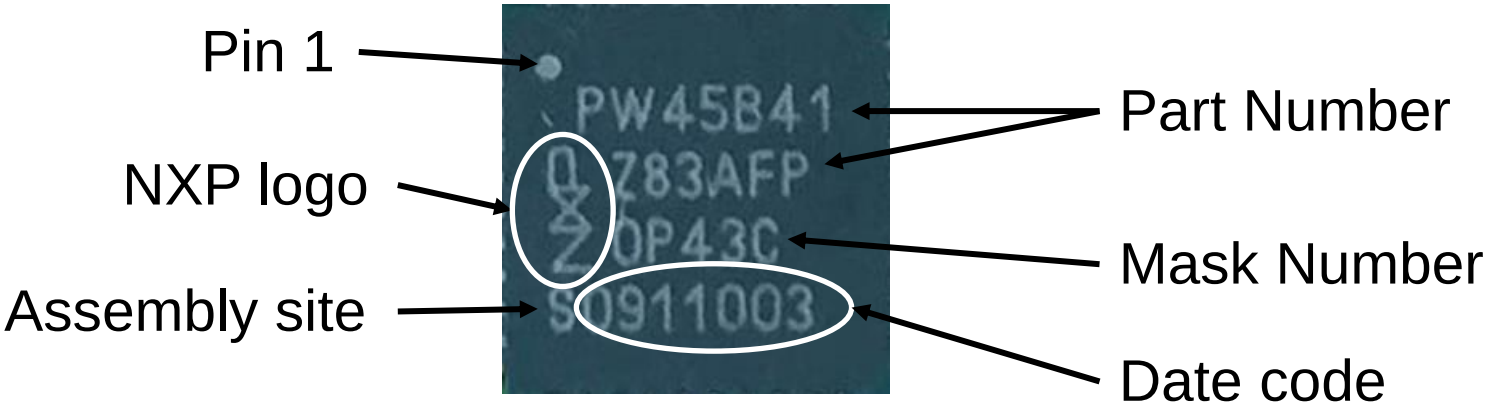
CISPR25 Automotive Chinese certification

The KW45-EVK and K32W1-EVK could withstand the CISPR25 certification.

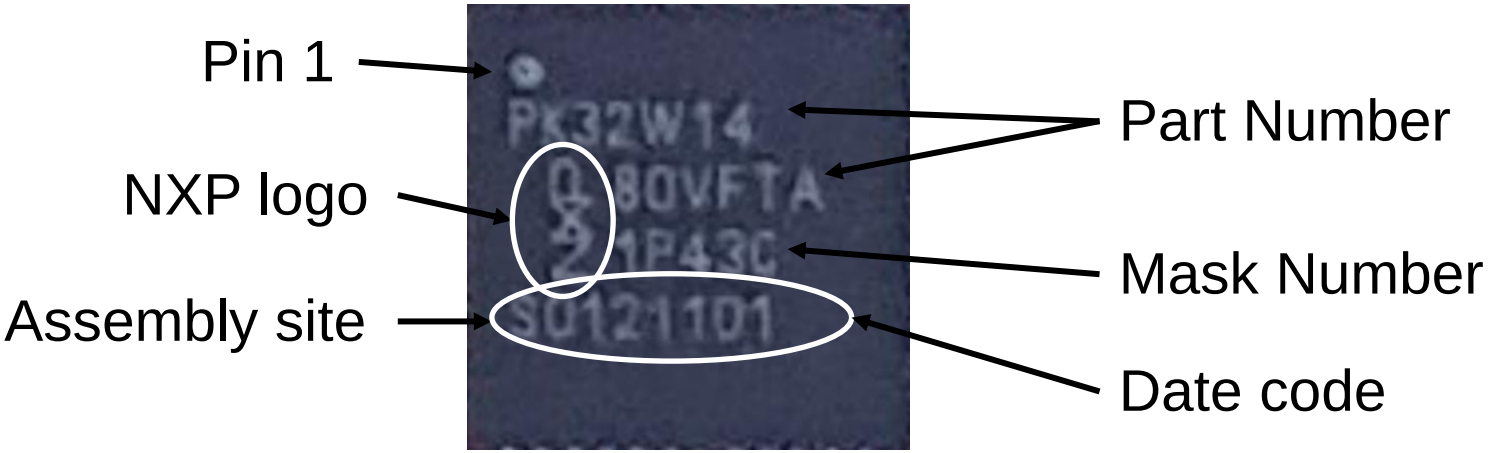
EMC HW modification has an impact on the radio performances:

- **Maximum output power** is impacted by **3dB**: +7dBm maximum.
- The **sensitivity** is also impacted by **2dB** whatever the datarate.

Annex 1: KW45 marking



Annex 2: K32W148 marking



SECURE CONNECTIONS
FOR A SMARTER WORLD