KW45/K32W1 HARDWARE DESIGN RECOMMENDATION

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NOVEMBER 2023

SECURE CONNECTIONS FOR A SMARTER WORLD

PUBLIC

RECOMMENDATION FOR A SUCCESSFUL PLATFORM DESIGN: ENTRY POINT

IC Datasheet & Reference Manual

- Pinout
- Unused pins
- Package (48/40 pins)

5 Pinout

5.1 Pinout Table

48HV QFN	40HV QFN	Pin Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	Wake up
2	1	PTB4		PTB4	LPSPI1_PCS3	LPUART1_CTS_b	LPI2C1_SDA	I3C0_SDA	TRGMUX0_IN0			FLEXIO0_D30			WUU0_P15
3	2	PTB5		PTB5	LPSPI1_PCS2	LPUART1_RTS_b	LPI2C1_SCL	I3C0_SCL	TRGMUX0_OUT0			FLEXIO0_D31			

5.2 Recommended connection for unused analog and digital pins

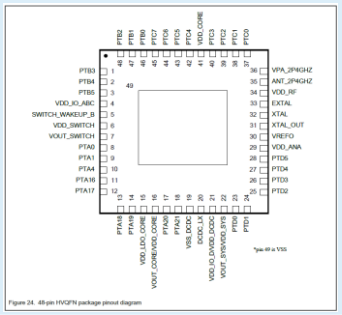
Table 59 shows the recommended connections for pins if those pins are not used in the customer's application

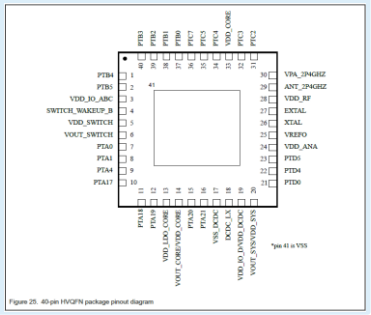
Table 59. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VOUT_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.

5.3 Pinouts diagram

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.





Design In Check List *(schematic & layout part)* Hardware Guideline

Check number	SCHEMATICS DESIGN-IN REVIEW CHECK-LIST	Y/N/NA
10	Programming and Debug	
10.1	Has the debug connector been connected to the correct I/O on the microcontroler?	
10.2	Has a connector been added that allows the microcontroller to be put into programming mode? (RESETn pin)	
10.3	Is RESET_b properly connected (pin PTA2)?	
10.5	Does the design allow for the possibility to perform conducted and radiated tests?	
10.7	If using Kinetis Bootload chosen interface(s)?	
11		
11.1	Has the correct type of to the microcontroller cc	
11.2	Has the flash memory s	
12		
12.1	Is the reset pin being us pushbutton or some oth customer read the Com reset pin as a reset pin?	
12.1	If the NMI pin is being u immediately on power-u	

Check number	LAYOUT DESIGN-IN REVIEW CHECK-LIST	Y/N/NA
1	GENERAL	
1.1	Has the number of layers been clearly discussed?	
1.2	Has the layout been checked versus NXP reference board (KW45-EVK or K32W1-EVK) ?	
1.3	Has the correct PCB material been specified?	
1.4	Has the correct PCB thicknesses been specified?	
2	RF line	
2.1	Is the RF line well sized for 50 ohm? The line width must be calculated according to the transmission line technology (microstrip,coplanar waveguide….), the board thickness and the PCB material.	
2.2	If microstrip is used has the trace been well isolated from the GND plane ? If coplanar waveguide is used have the GND conductors been well connected with vias to the reference GND plane layer ?	
2.3	Is the RF trace as short as possible ?	
2.4	Have vias been avoided in the RF line?	
2.5	Have the matching components been placed close to the KW45/K32W1 RF port ("ANT" pin) and oriented the same way as the reference design?	

NXP Semiconductors
Application Note

Document Number: AN13227
Rev. 3, 08/2022

Hardware Design Considerations for KW45B41Z & K32W148 Bluetooth LE Devices

1. Introduction

This application note describes Printed Circuit Board (PCB) design considerations for the *KW45B41Z83AFTA , KW45B41Z82AFTA and K32W1480VFTAT* 48-pin QFN (HVQFN-7x7 Pitch 0.5mm) wettable flank package and *KW45B41Z83AFPA and KW45B41Z82AFPA* 40-pin QFN (HVQFN-6x6 Pitch 0.5mm) wettable flank package. Included are layouts of the component copper layer, solder mask, and solder paste stencil.
These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

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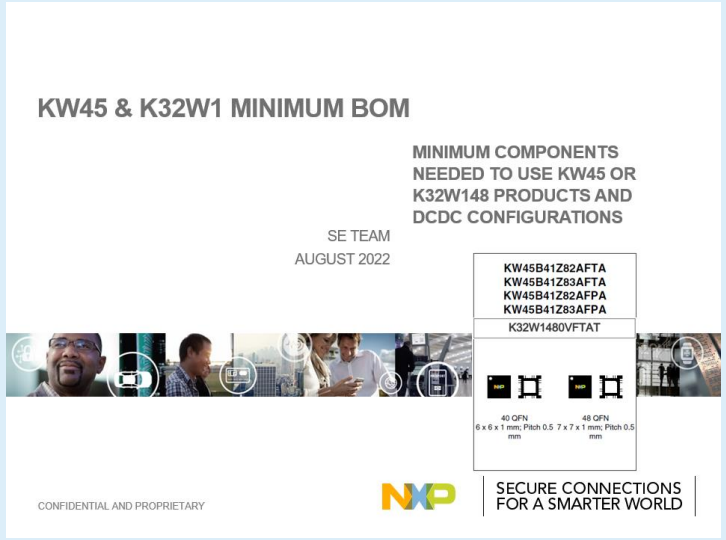
Minimum BoM

- HVQFN48 – 7x7
- HVQFN40 – 6x6
- DCDC modes:
  - Buck
  - Bypass
  - Power Switch
- Low Power or not

NXP boards:

- KW45-EVK (sch-50555)
- K32W1-EVK (sch-50701)



APPLICATION NOTES AND COLLATERALS

All needed documents are available in the NXP Community

The best way to build a PCB using a KW45 or K32W1 first time right - NXP Community

Content: Find the important link to build a PCB using a KW45 and all concerning the radio performances, low power and radio certification (CE/FCC/IC).

Different chapters are available. Focus is done in Hardware part in this document

Hardware:

- KW45/K32W1-EVK schematic, layout and gerber files
- KW45/K32W1-EVK User Manual
- **AN13227** Hardware Guideline
- Minimum BoM
- Design-In check list
- RF matching
- Crystal (Trimming)
- DCDC management guide

HARDWARE DESIGN RECOMMENDATION

- Layout overview
- DCDC modes
- DCDC inductor
- Radio
- Supplies
- Clocks & Crystals
- Bootloader pins
- Wake Up pins
- Level shifter
- IO current drive
- Peripherals
- DTEST pins
- Battery: Coin Cell
- Unused Ios
- Layout general rules
- EMC immunity option
- CISPR25
- Jumper configuration on KW45/K32W1-EVK

Layout overview

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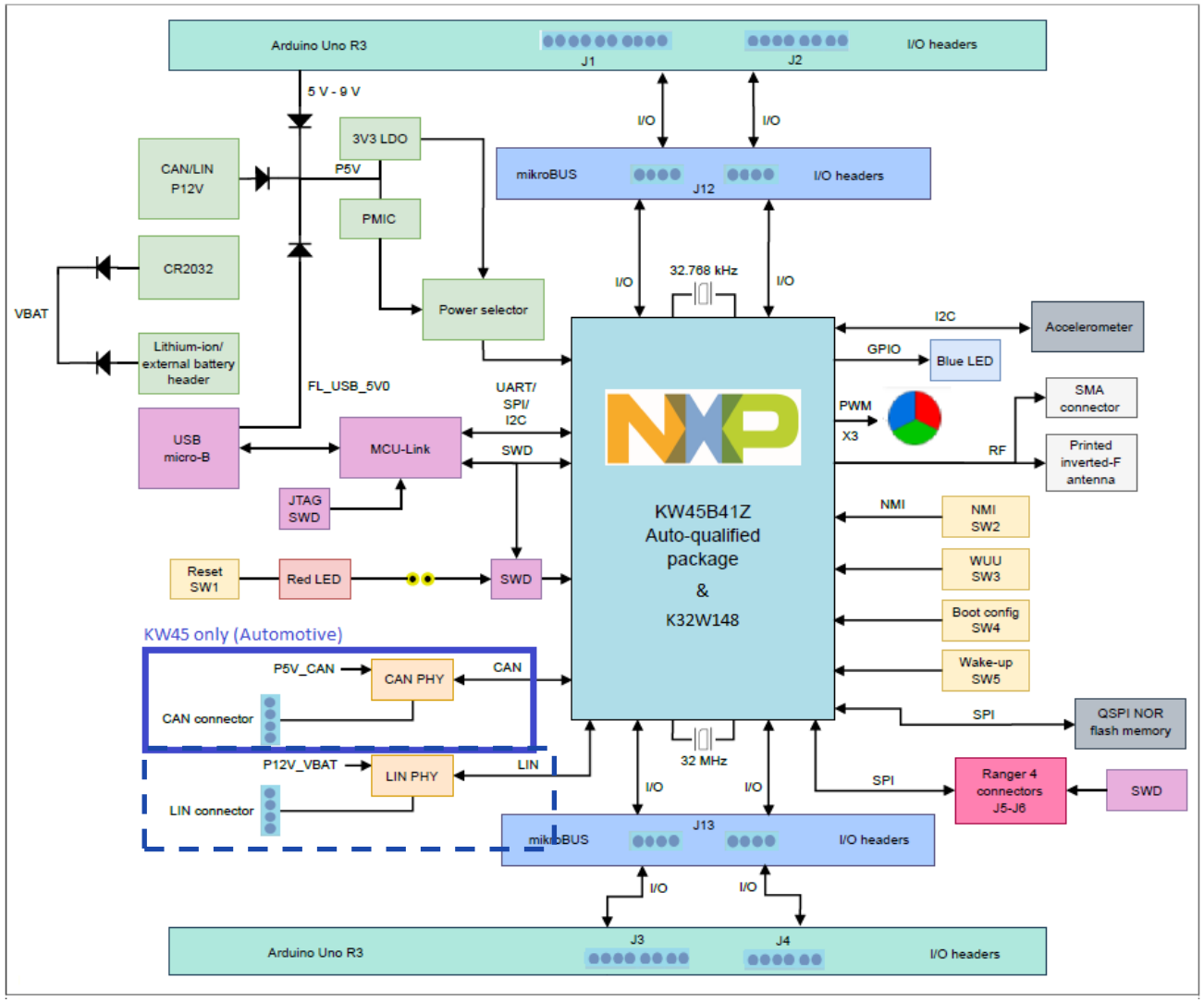
Product Enablement HW

X-KW45B41Z-EVK (SPF-50555) Schematic & Layout

X-K32W148-EVK (SPF-50701)



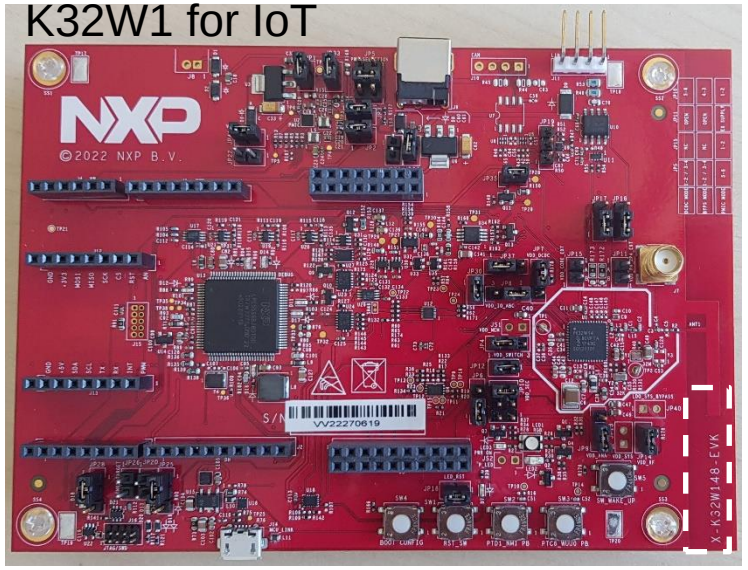
KW45 for Automotive

KW45B41Z82AFTAx
KW45B41Z83AFTAx
KW45B41Z82AFPAx
KW45B41Z83AFPAx

40HVQFN
6 x 6 x 0.85 mm; Pitch
0.5 mm; Wettable Flanks

48HVQFN
7 x 7 x 0.85 mm; Pitch
0.5 mm; Wettable Flanks

K32W1 for IoT

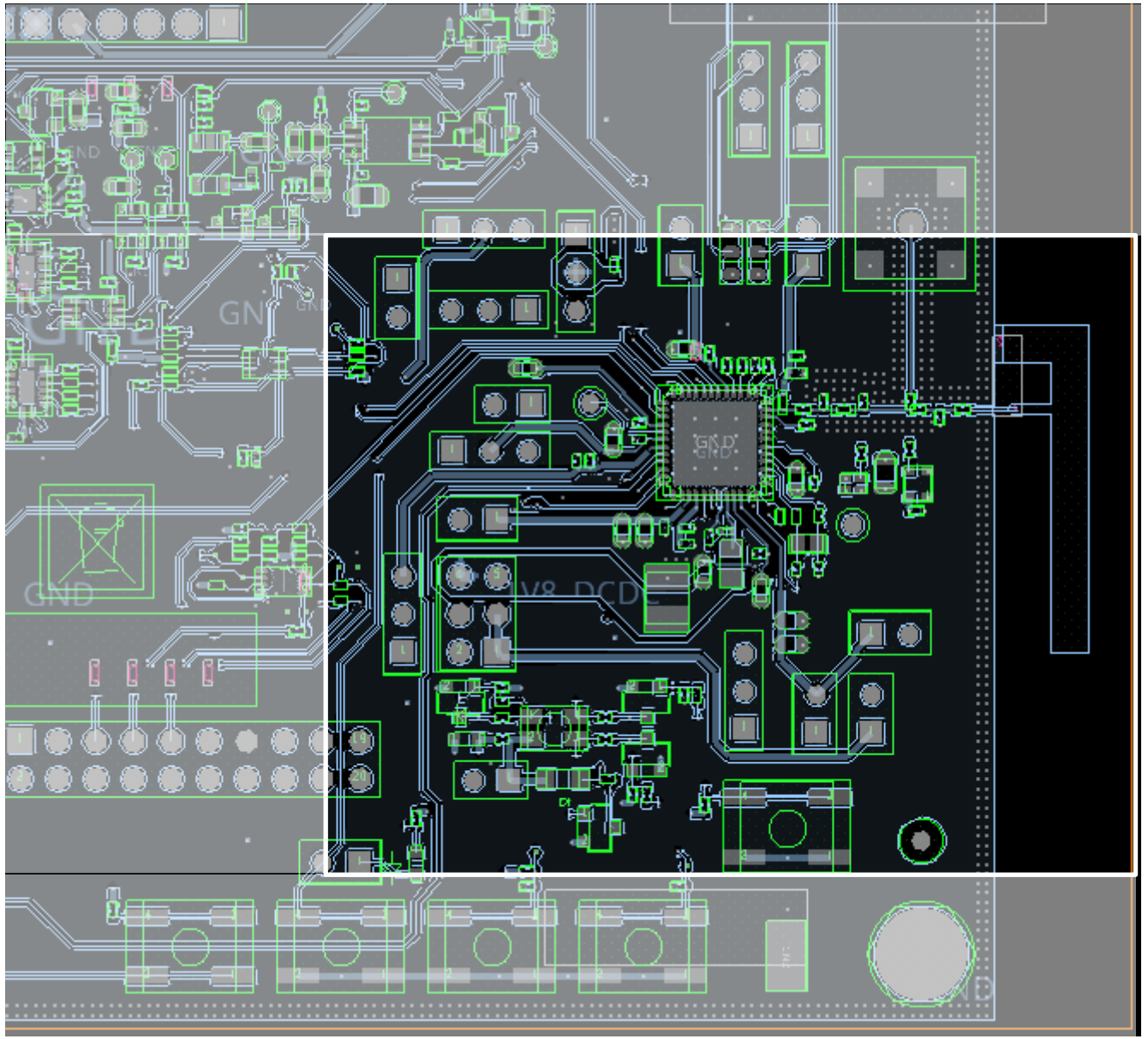


K32W1480VFTAT

48HVQFN
7 x 7 x 0.85 mm; Pitch 0.5 mm

HW RECOMMENDATION – LAYOUT OVERVIEW

Extract from HW guideline:



DCDC modes

SECURE CONNECTIONS
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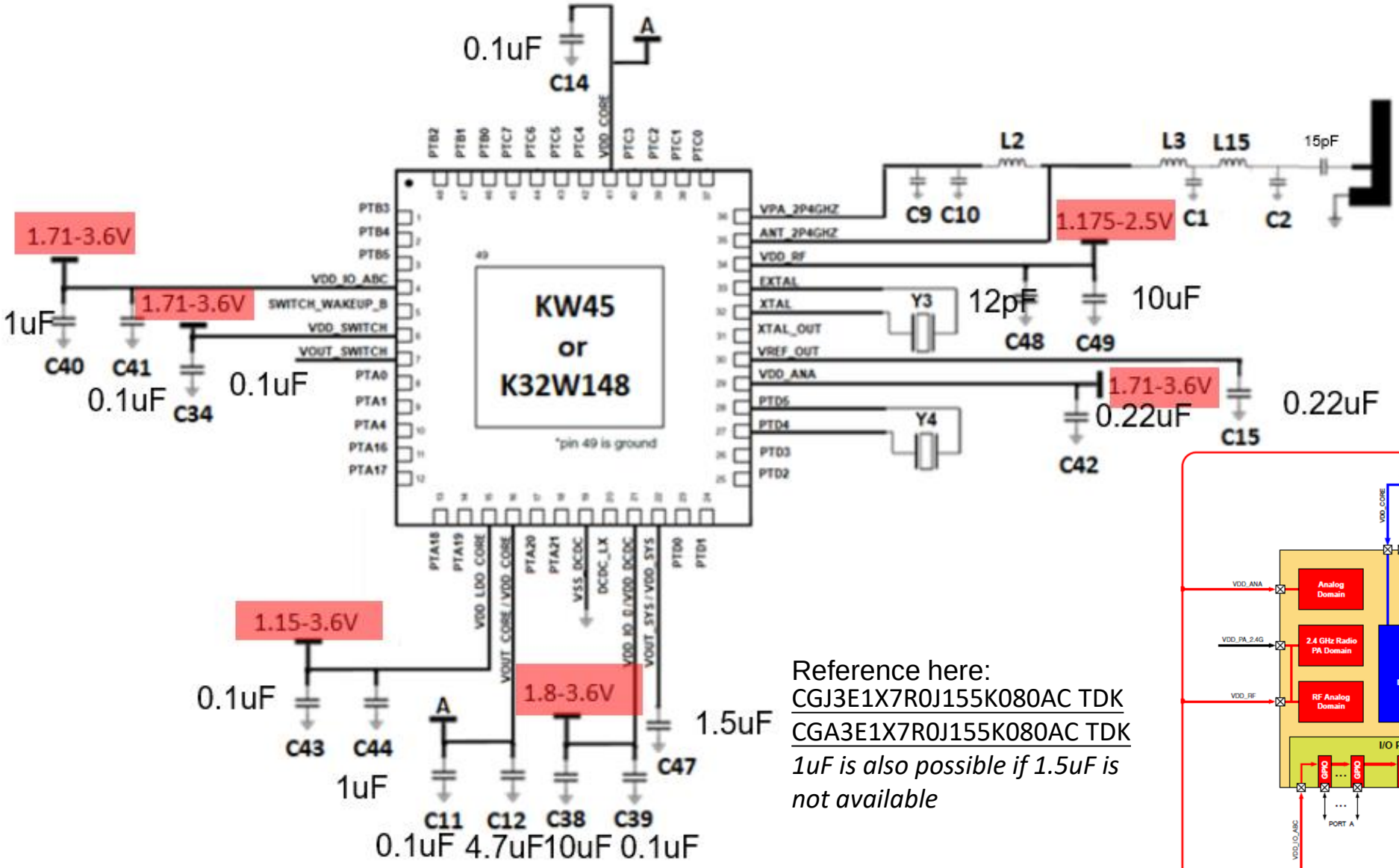
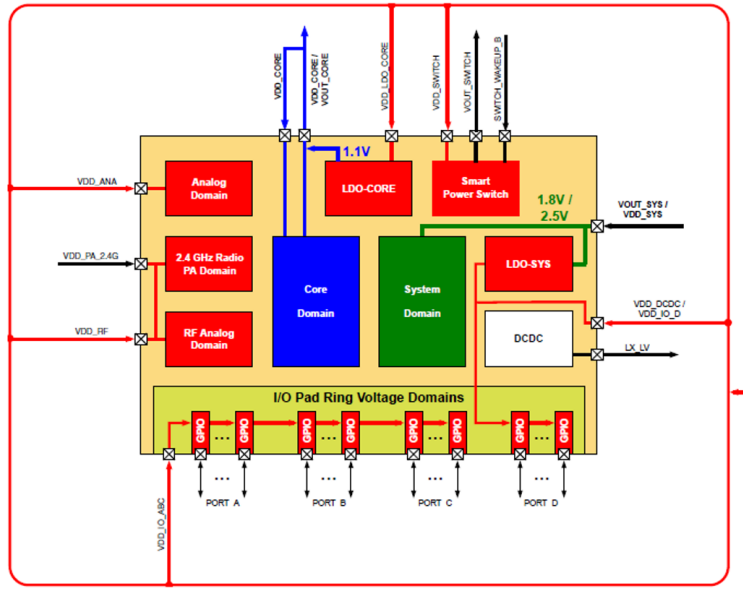
HW RECOMMENDATION – DCDC BYPASS MODE

Possibility of Bluetooth LE Low Power mode active in case 32kHz is populated.



Reference here:
CGJ3E1X7R0J155K080AC TDK
CGA3E1X7R0J155K080AC TDK
1uF is also possible if 1.5uF is not available



DCDC BYPASS PIN CONFIGURATION

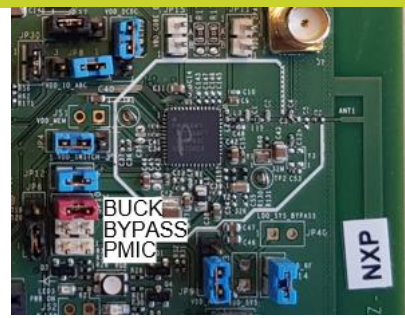
HVQFN48 – 7x7

Pin Number	Pin Name	Bypass connection
4	VDD_IO_ABC	1.71-3.6V
6	VDD_SWITCH	1.71-3.6V
7	VOUT_SWITCH	Floating (when not used)
15	VDD_LDO_CORE	1.15-3.6V
16	VDD_CORE1	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
20	DCDC_LX	Floating (not used)
21	VDD_DCDC	1.8-3.6V
22	VOUT_SYS/VDD_SYS	Floating (except the decoupling capacitor)
29	VDD_ANA	1.71-3.6V
30	VREF_OUT	Floating (except the decoupling capacitor)
34	VDD_RF	1.175-2.5V
36	VPA_2P4GHZ	0.9-2.4V
41	VDD_CORE2	0.95-1.1V (Mid drive) or 1.04-1.21V (Normal drive or safe mode voltage)
49	VSS	GND
19	VSS_DCDC	GND

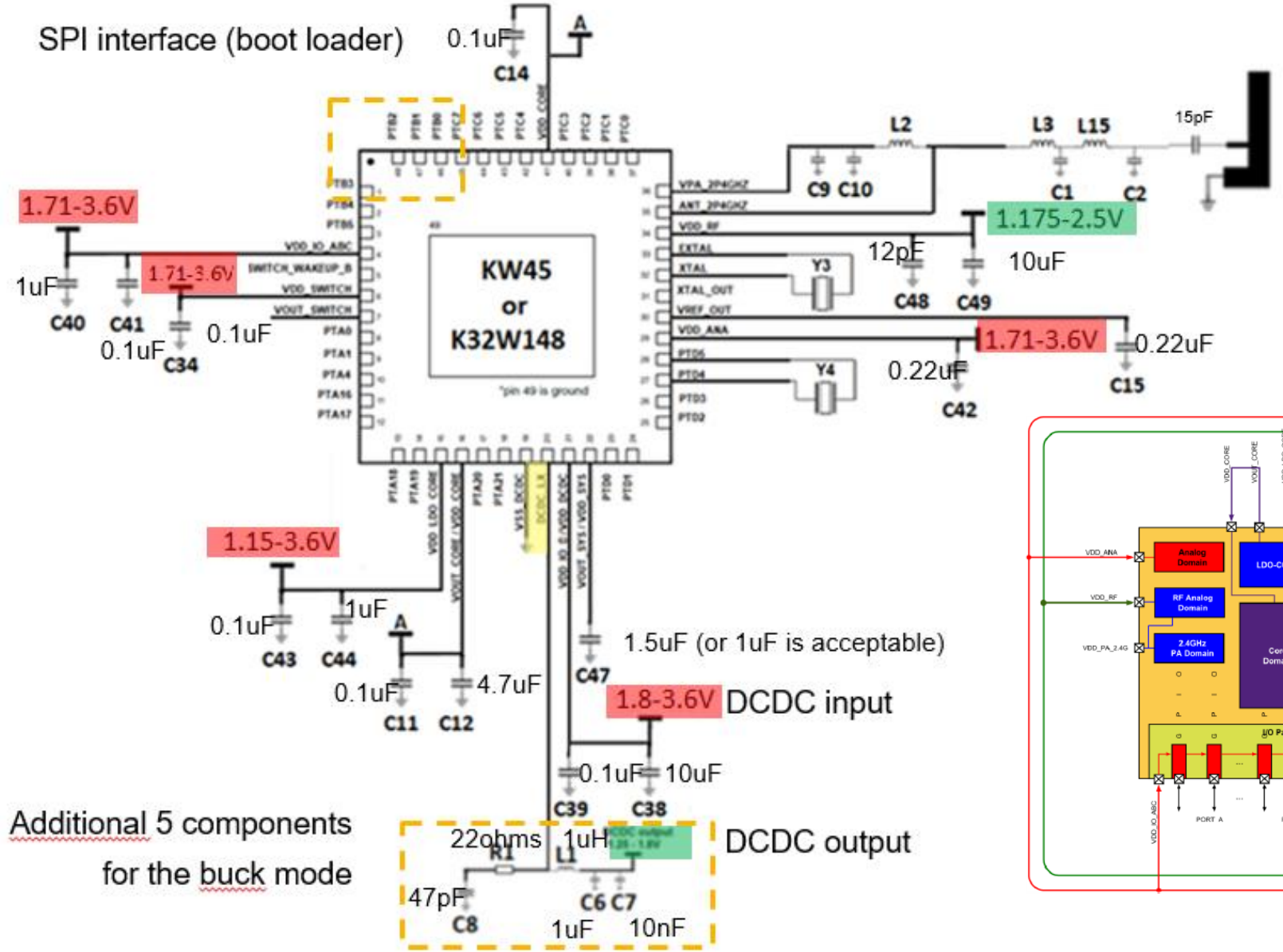
Warning: ➔ Do not connect the pin VDD_SYS (pin)
This pin is set to internal 2.5V for fuse programming.

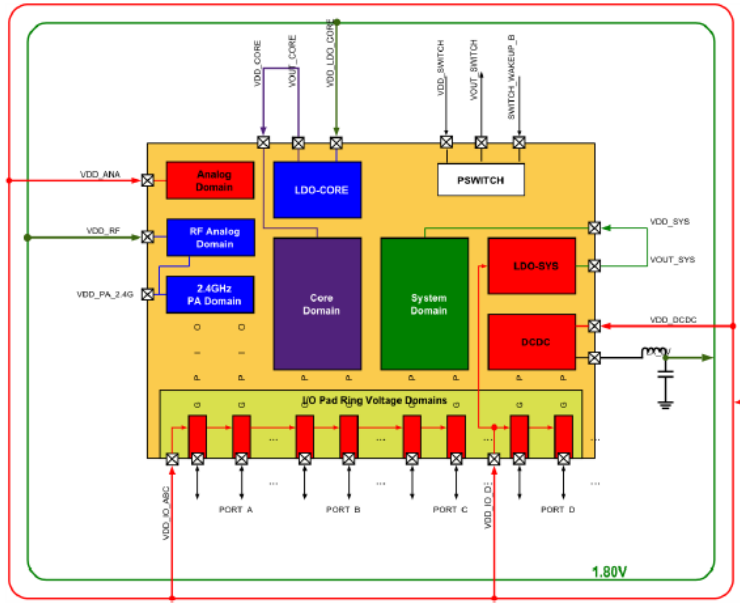
HW RECOMMENDATION – DCDC BUCK MODE

Possibility of Bluetooth LE Low Power mode active in case 32kHz is populated.



DCDC output voltage:
1.25V/1.5V/1.8V/2.5V

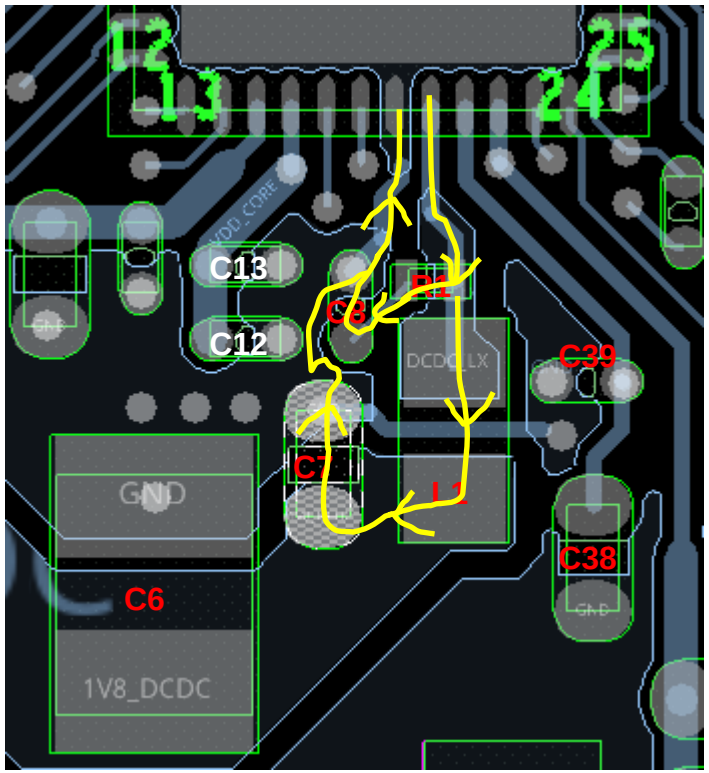


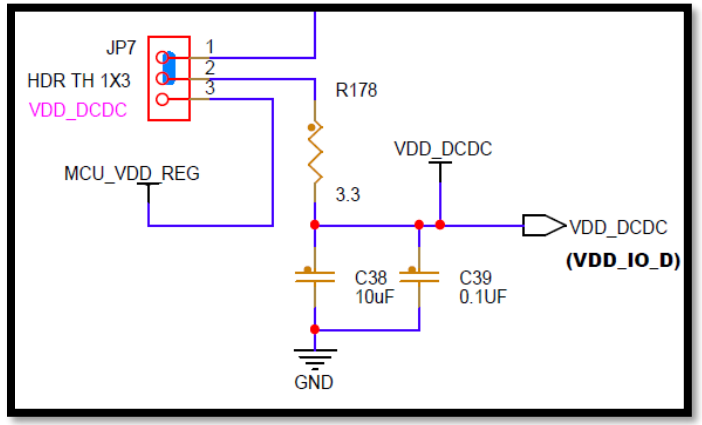


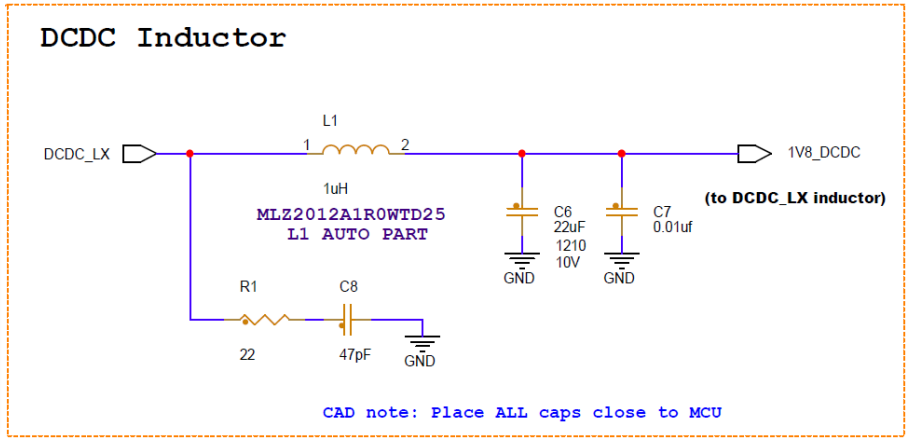
HW RECOMMENDATION – DCDC LAYOUT

1. **C38 & C39** must be as close as possible to the DCDC Vdd but not so much for the DCDC vss. Recommend is to place them with the LX connection to the inductor passing between their terminals. It is really critical to reduce the loop formed by the DCDC VDD/VSS pins and those capacitors. Please add more vias to the ground plane.
2. In a similar fashion place **C7** in a way that it's connection to the inductor **L1** is where it is now and VSS connection gets close to the chip. Adding vias to better connect vss to the ground plane will help.
3. It is interesting to move **C6** closer to the IC and add vias as on this example.
4. **C8** in a similar fashion as **C7** may be helpful for emissions >300MHz.
5. **L1** is 1uH for the KW45/K32W148 (iso 10uH on KW35/36/37/38/39 reference design)

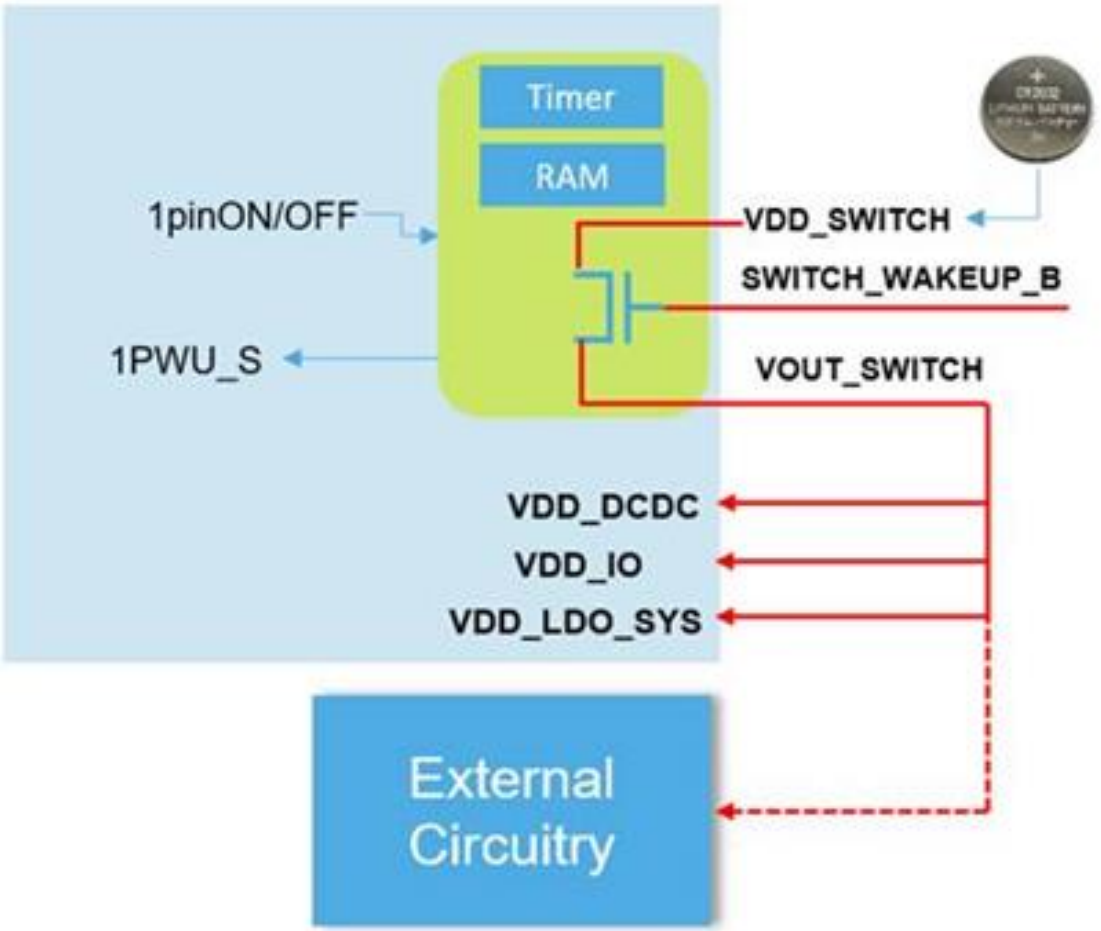
Note:
Having short connection and small area loops is the most important thing to contain any emissions. Bringing those caps closer to the chip will be helpful. And having the ground plane well preserved underneath those components (as it is on the current layout) will greatly help reduce the effect of the inductor not being really close to the chip.

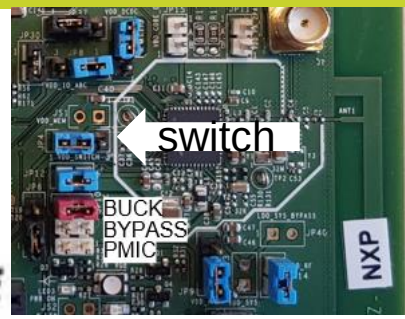






HW RECOMMENDATION – POWER SWITCH & BUCK MODE





SMART POWER SWITCH
ULTRA LOW POWER & FLEXIBLE

Performance

- <100 nA (typ) leakage current when OFF (no RAM retention, timer disabled)
- <700 nA (typ) leakage current when OFF (8KB RAM retention + timer)
- 40 mA active output current capability

Flexible

- Can be used to power partial or entire chip supply
- Can be used to power external circuits saving BOM costs

Configurable power control

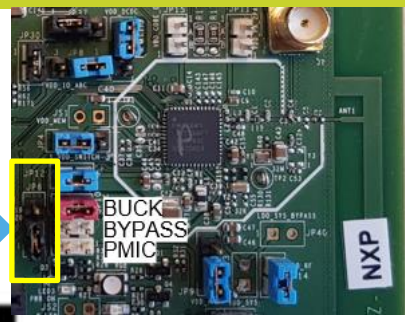
- One external wakeup pin (SWITCH_WAKEUP_B) to enable power switch
- Internal Timer timeout (from 7.8125ms to 1s) to enable power switch
- Dedicated register bits to control power switch in Low Power mode / Active mode

Data storage

- Support up to 8KB RAM retention

HW RECOMMENDATION – POWER SWITCH & BUCK MODE

Possibility of Bluetooth LE Low Power mode active in case 32kHz is populated.



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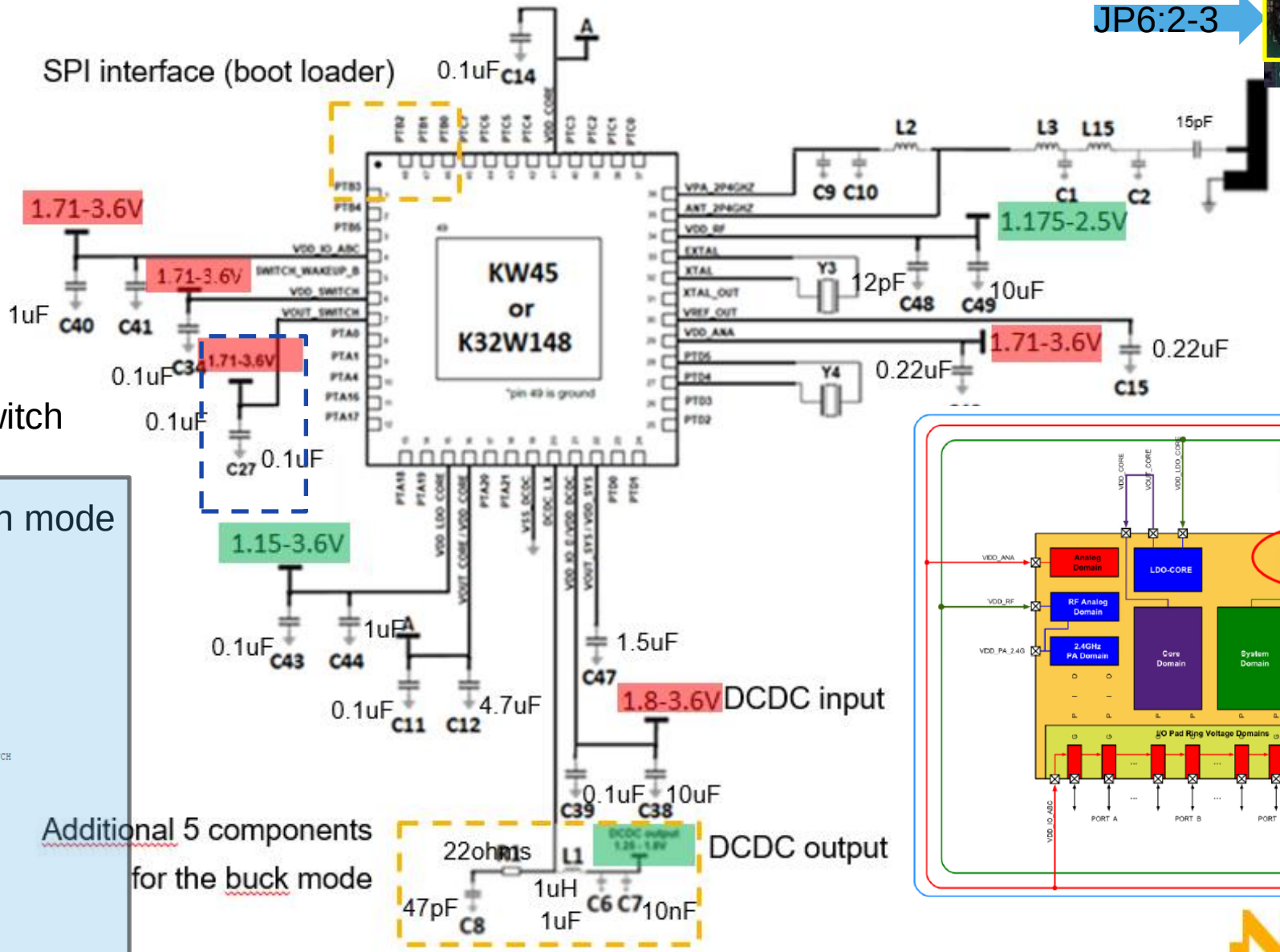
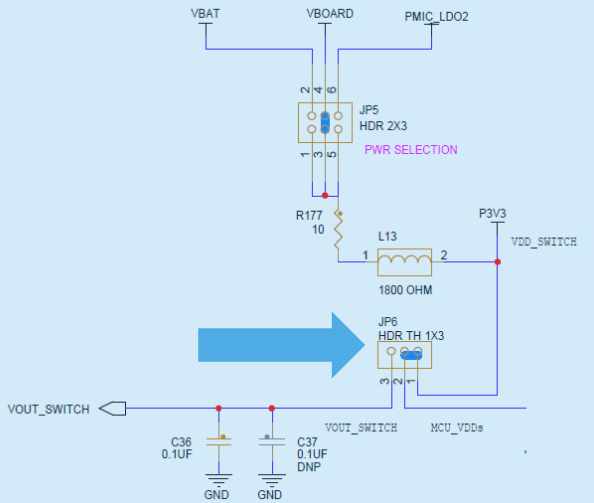
SPI interface (boot loader)



JP6 to switch to power switch mode



DCDC inductor

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DCDC inductor

X-KW45B41Z-EVK – HW UM extract

2.1.2 DC-DC inductor

The KW45B41Z-EVK board uses a 1 µH DC-DC inductor L1 (TDK MLZ2012A1R0WTD25). The inductor is enabled when the board is configured in DC-DC Buck mode. The figure below shows the DC-DC inductor circuit diagram of the KW45B41Z-EVK board.

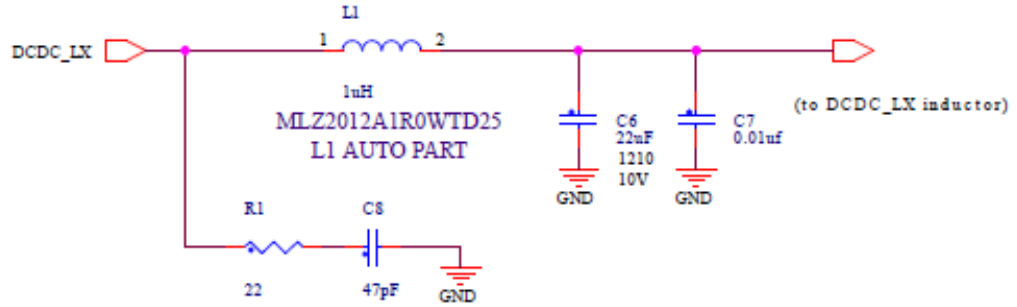


Figure 10. DC-DC inductor circuit diagram

Choosing right DC-DC inductor for your target board is very important. While selecting a DC-DC inductor, look for the following specifications:

- Inductor value: 1 µH or 1.5 µH
- ESR: < 0.3 Ω
- Saturation current (Isat): > 300 mA
- Self-resonant frequency: > 50 MHz

The DC-DC inductor used in the KW45B41Z-EVK board is a good choice for general automotive applications (for example, car access) as it delivers good performance (low ESR, high saturation current). It is also a good choice for keyfob application based on LF technology. It prevents spurious from 100 kHz to 200 kHz that can interact with another reception device (that is, NXP LF device at 125 kHz) on the same board. Other recommended inductors are LQM18PH1R0MFRL from Murata and 78438336010 from Wurth.

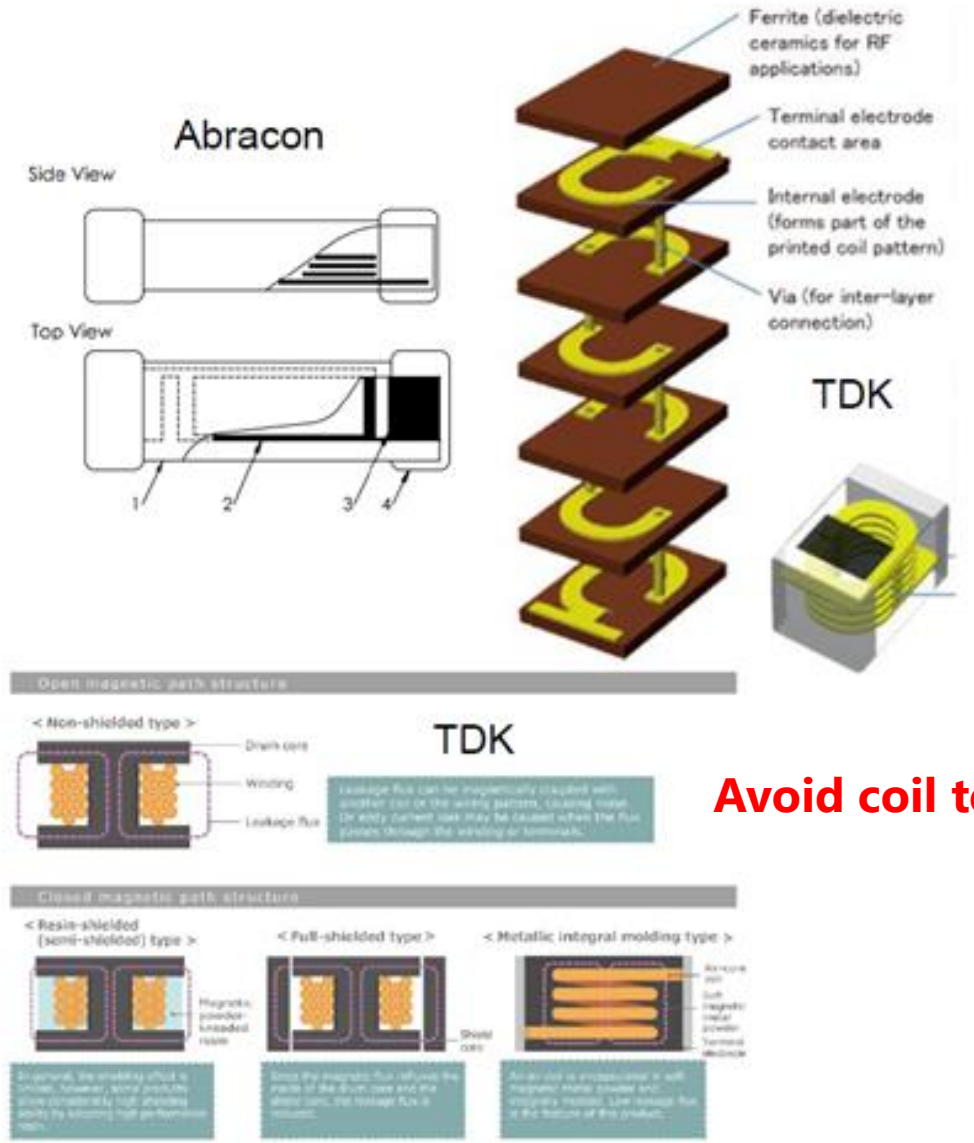
The figure below shows other possible inductor options.

DCDC inductor

Inductor and Shielding

- Normally for chip inductors the coils are in the same plane of the PCB. Any other coil in the same plane, with the same axis, will couple maximally.
  - Rotating inductor does not help unless the plane of the coils are perpendicular to the PCB
  - Coupling is minimal at the axis
- There are different types of shielding applied to inductors with different levels of effectiveness:
  - Electrostatic shielding will probably not help at LF.
  - Magnetic shielding ranges from a simple coating to complete encapsulation. The later is substantially more effective
- **Must make sure inductor is not getting close to saturation! >>300mA.**

1uH inductor: ESR must be closed to 0.2 ohms



Avoid coil technology

PMIC supply

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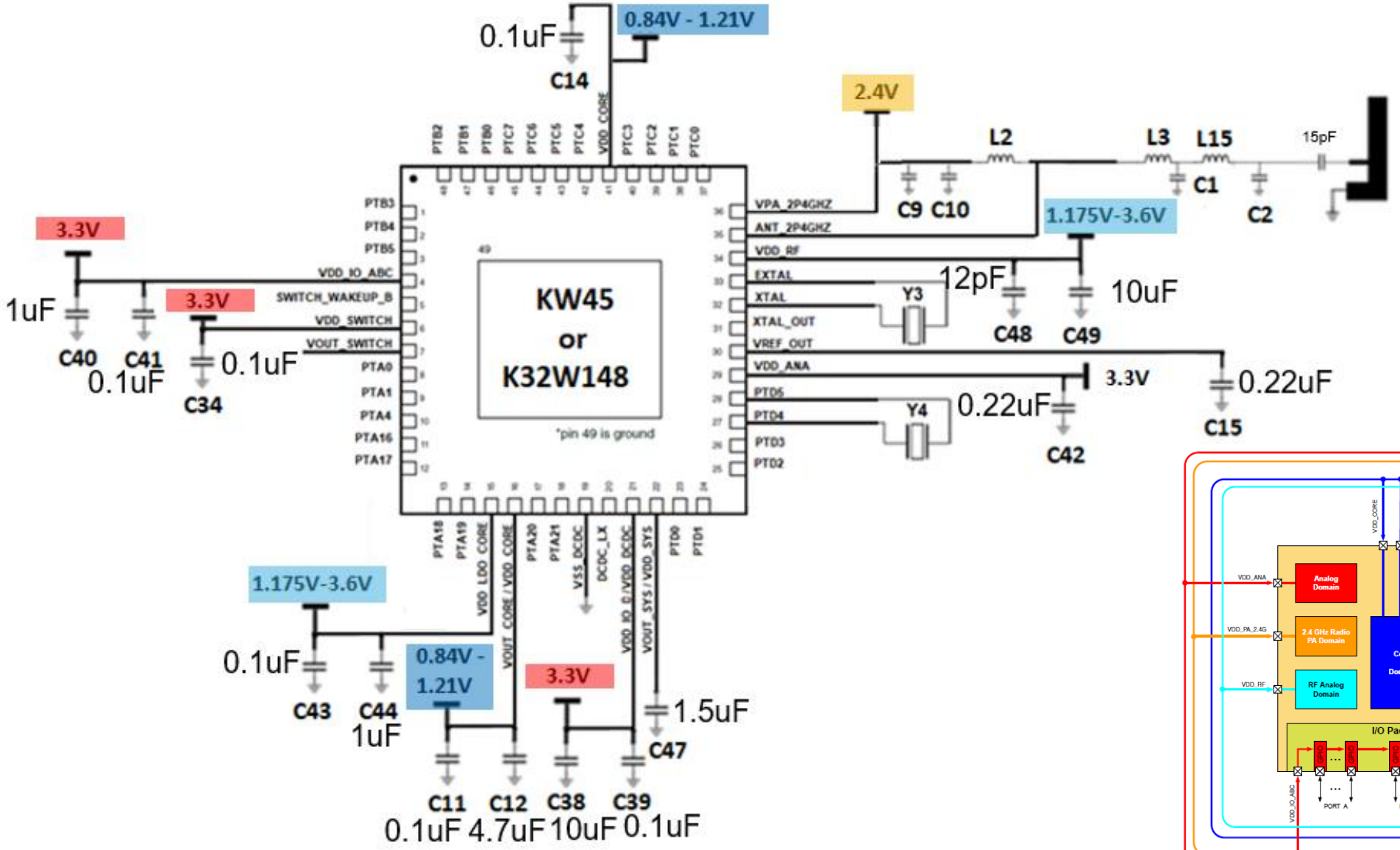
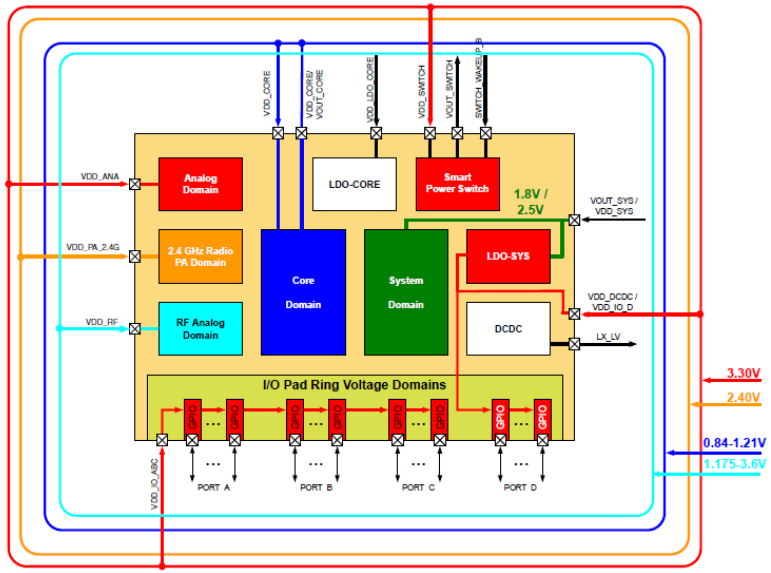
KW45 – PMIC SUPPLY

HVQFN48 – 7x7

Possibility of Bluetooth LE Low Power mode active.





Smart Power Switch

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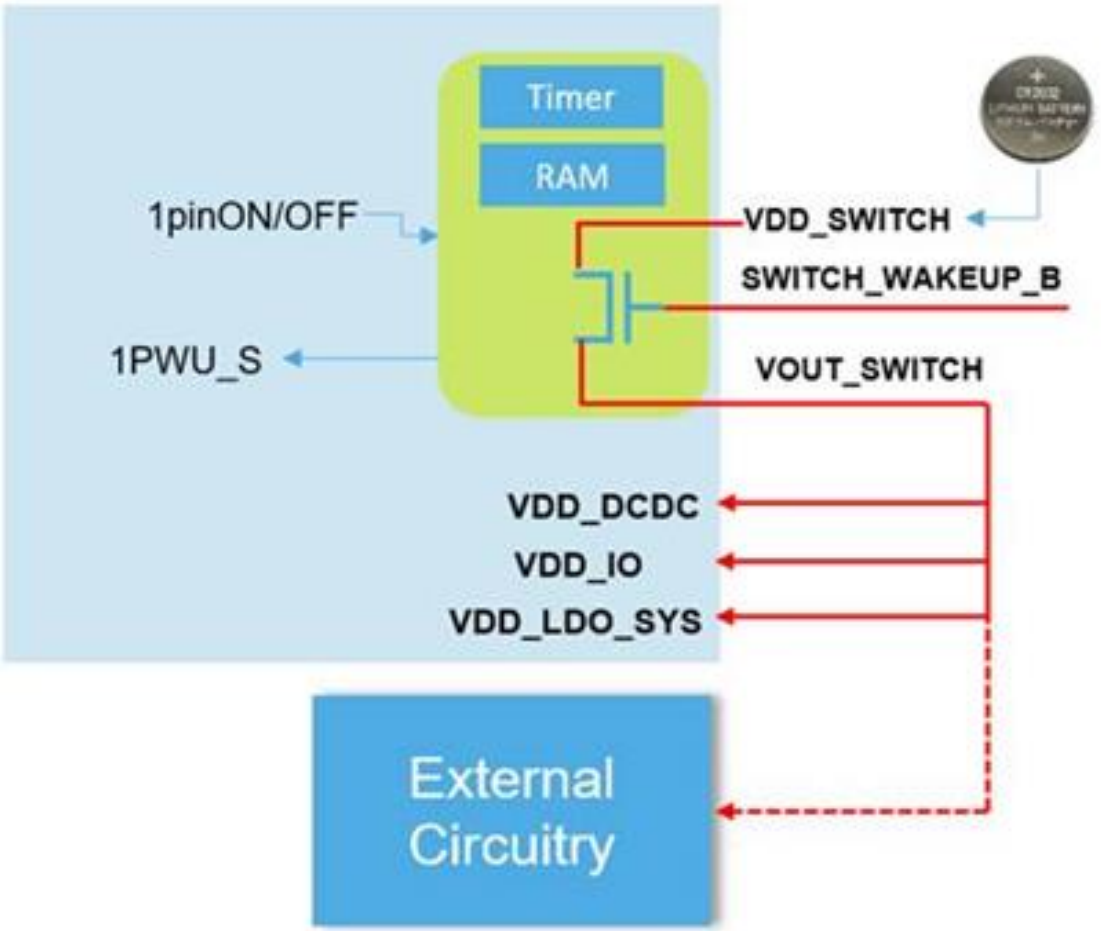
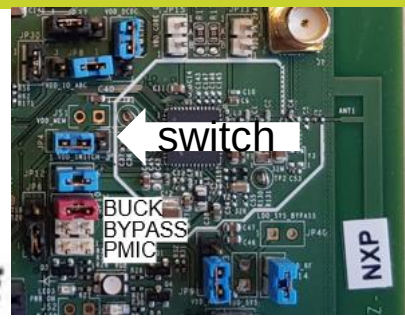
HW RECOMMENDATION – POWER SWITCH & BUCK MODE





SMART POWER SWITCH
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HW RECOMMENDATION – POWER SWITCH & BUCK MODE

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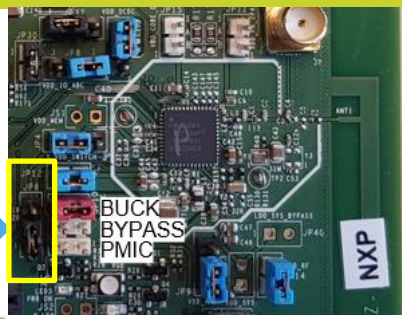

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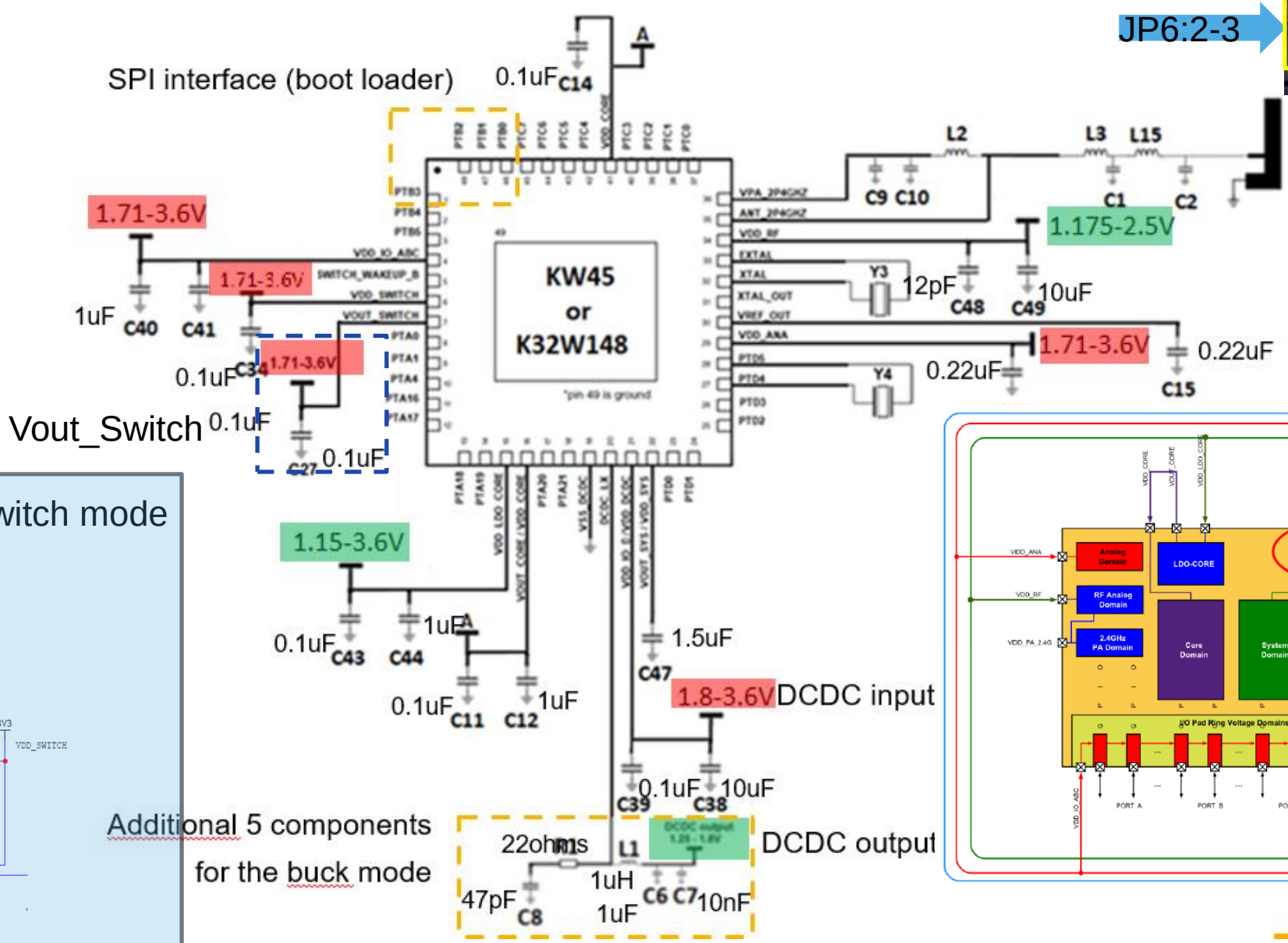
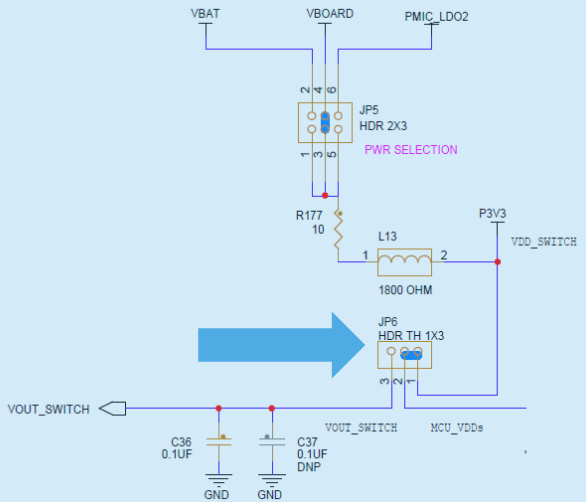


Additional 5 components for the buck mode

JP6 to switch to power switch mode

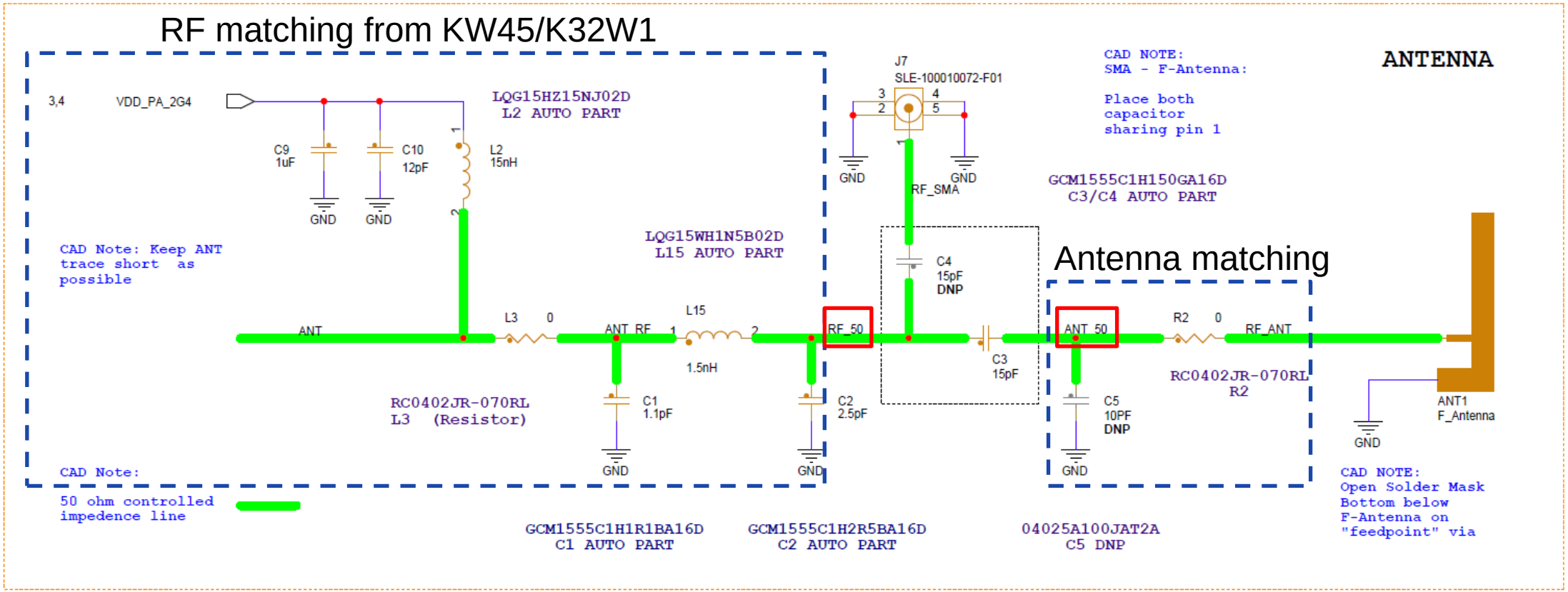


Radio

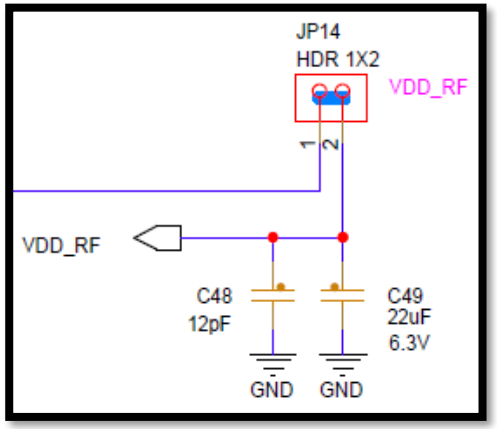
SECURE CONNECTIONS
FOR A SMARTER WORLD

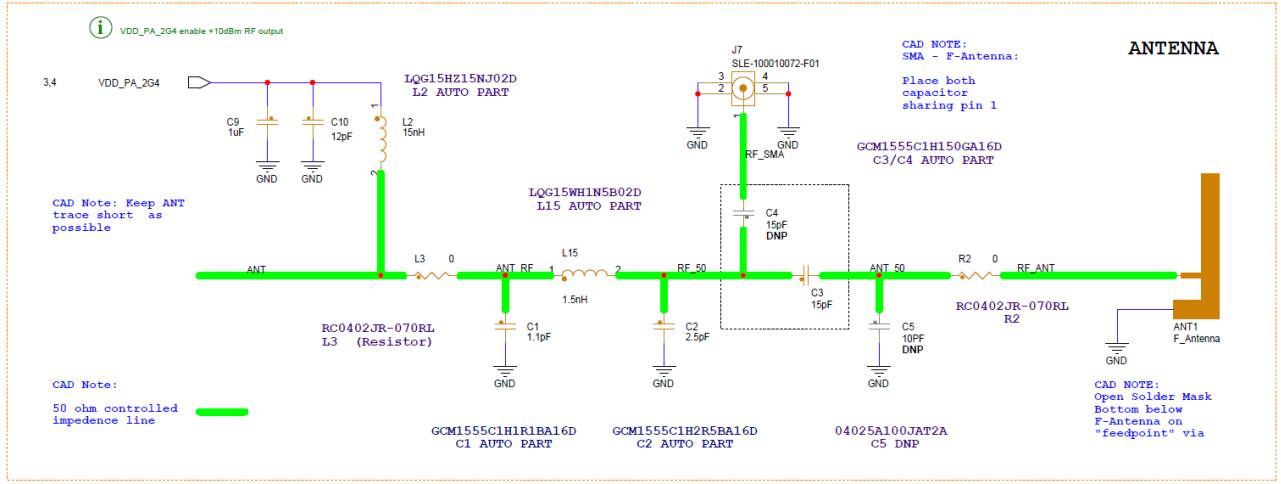
RF Matching Goals:

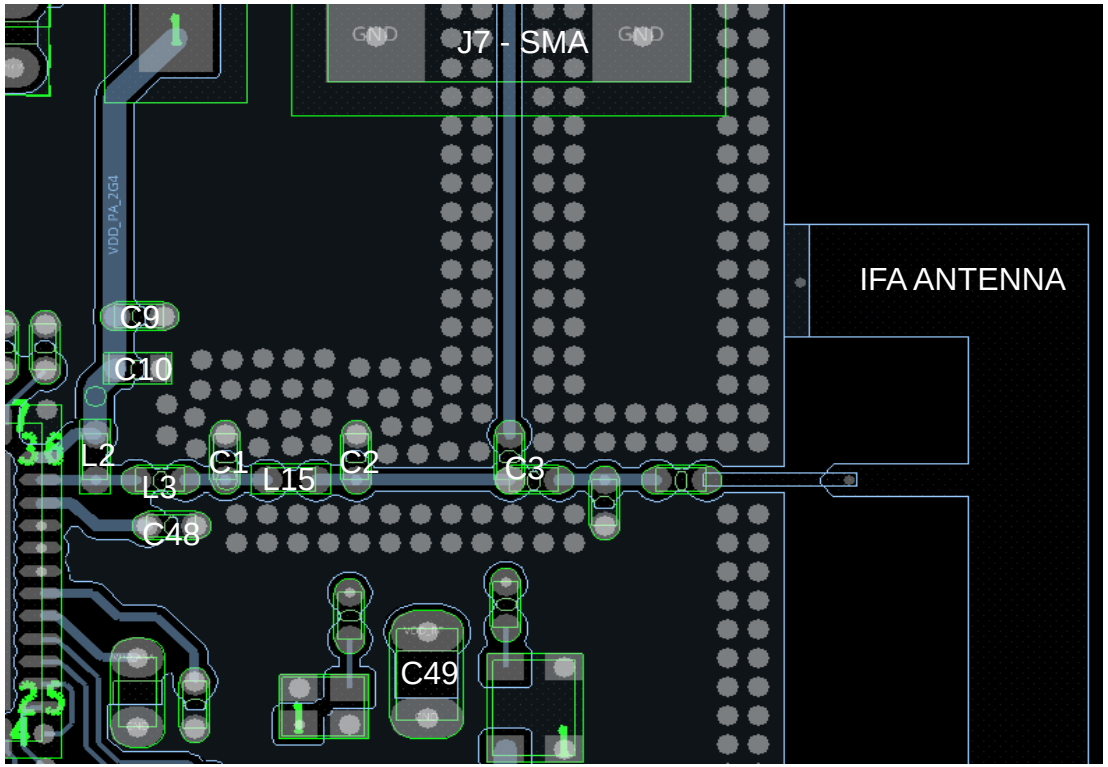
- Only certified automotive component have been used.
- Ensure sensitivity performance was the focus of this RF Matching
- PASS internal specification regarding 2nd and 3rd harmonics with 10dBm output power.
- Same Matching for 0dBm, 4dBm, 7dBm and 10dBm output power.



HW RECOMMENDATION - RADIO





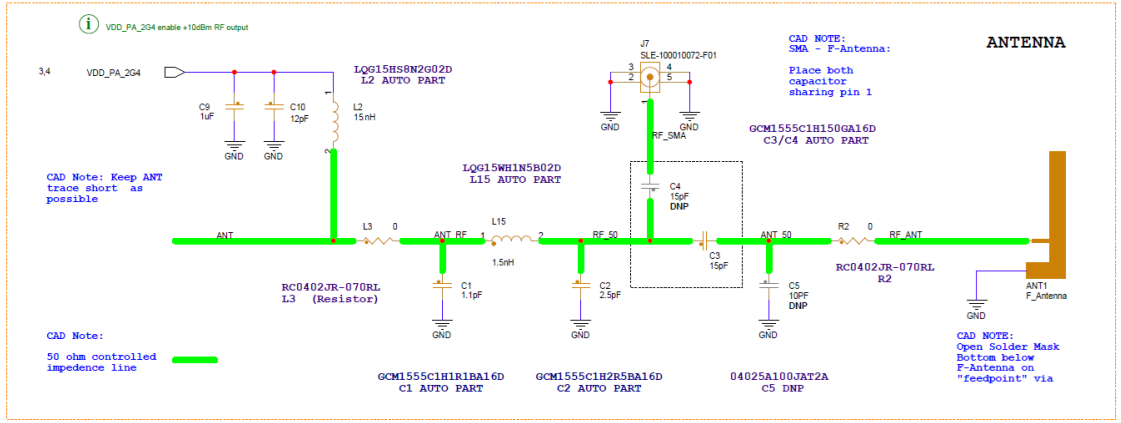


- The value capacitor **C48** used for an RF short are 12pF
- **C10** must be as close to L2 as possible
- **C49**=22uF on VDD_RF could be placed as DNP
- The pull up inductor **L2** placement must follow the layout example
- The **antenna matching** components must be at minimum spacing to the DUT and each other, as on the current layout.
- **C48** needs to be placed in order to have the best isolation with ANT_RF line. VDDRF line needs to be isolated with VDDRF_line. Please copy the current layout
- Need isolation between VDDRF and UART signals.
- VDD_PA_2g4 needs to be isolated vs PTC0

- General comment: The power planes which create huge fat nets are for the VDD_ANA and VDD_SYS. No benefit to reduce the power plane.

Product Enablement HW

X-KW45B41Z-EVK and X-K32W148-EVK Design and board layout considerations (HW guideline extract) – RF matching wave guide 50ohms for RF power output.



Automotive qualified

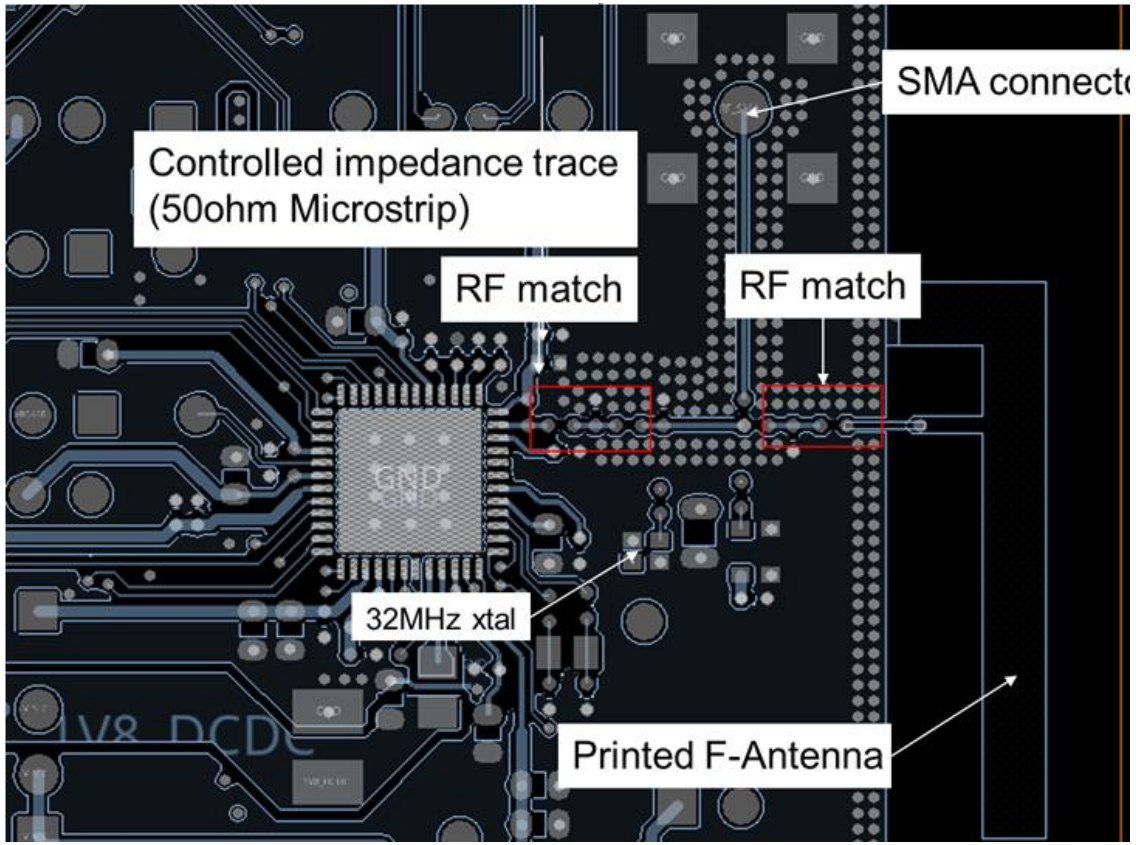
Matching components are:

- Inductors

Reference	Value	Description	Mfr. name	Mfr. part number
L2	15 nH	IND -- 0.015 µH @ 100 MHz 450 mA +/-5% 0402	MURATA	LQG15HZ15NJ02D
L3	0ohm	shunt		
L15	1.5 nH	IND -- 0.0015 µH @ 100 MHz 1000 mA +/-0.1 nH 0402	MURATA	LQG15WH1N5B02

- Capacitors

Reference	Value	Description	Mfr. name	Mfr. part number
C2	2.5 pF	CAP CER 2.5 pF 50 V 0.1 pF C0G 0402	MURATA	GCM1555C1H2R5BA16
C1	1.1 pF	CAP CER 1.1 pF 50 V 0.1 pF C0G 0402	MURATA	GCM1555C1H1R1BA16
C10	12 pF	CAP CER 12pF 50V 5% C0G AEC-Q200 0402	MURATA	GCM1555C1H120JA16D
C1	1 uF	CAP CER 1uF 10V 10% X7S AEC-Q200 0402	MURATA	GCM155C71A105KE38D



Product Enablement HW

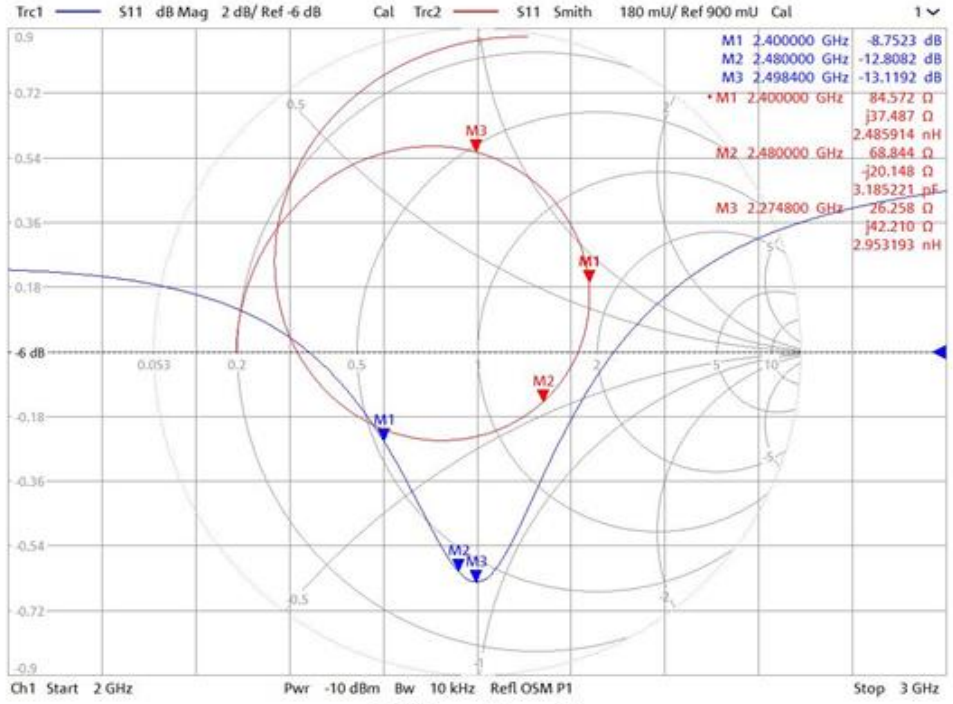
S11 (return loss) results (AN13228 RF report extract) – RF matching 50ohms

[How to measure S11 on FRDM-KW3x & KW45]

4.2 RX

In the Rx mode, the return loss measurement is performed by setting the LNA gain of K32W148 to the maximum.

Hardware: X-K32W148-EVK



S11 diagram (Rx mode)

Results:

- Return loss: -12.8 dB (2.48 GHz) < S11 < -8.7 dB (2.4 GHz)

There is no specification for the return loss.

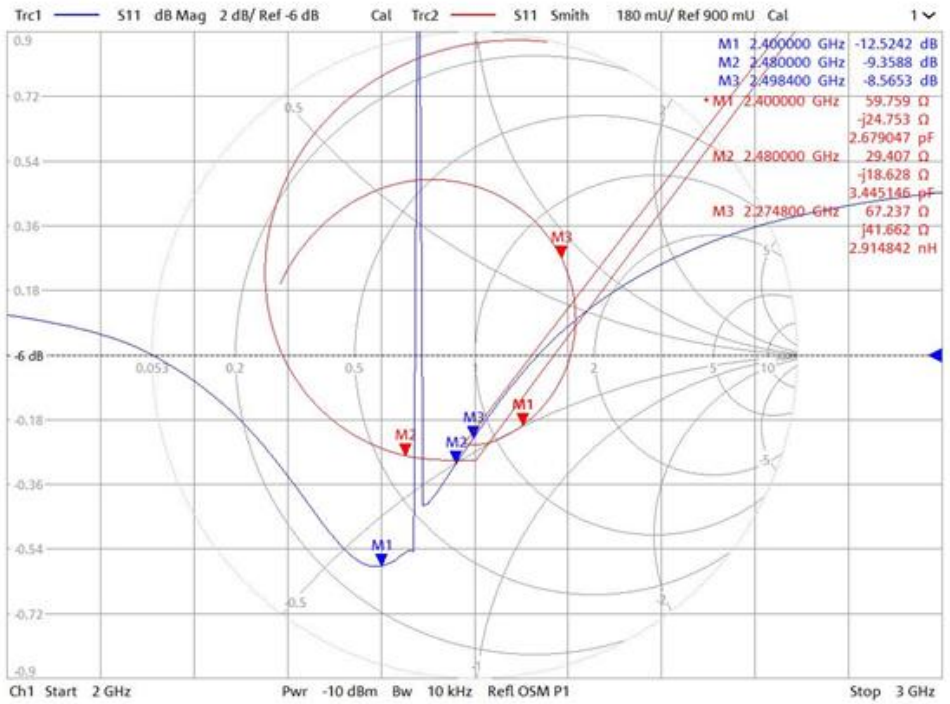
Conclusion:

- The return loss (S11) is lower than -8 dB

4.3 TX

In the Tx mode, the return loss measurement is performed by setting the K32W148 RF output power to the minimum.

Hardware: K32W148 EVK



S11 diagram (Tx mode)

Results:

- Return loss: -12.5 dBm (2.4 GHz) < S11 < -9.3dB (2.48 GHz)

There is no specification for the return loss.

Conclusion:

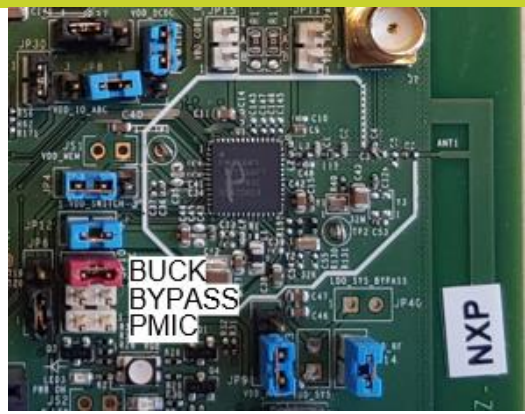
- The return loss (S11) is lower than -9 dB.

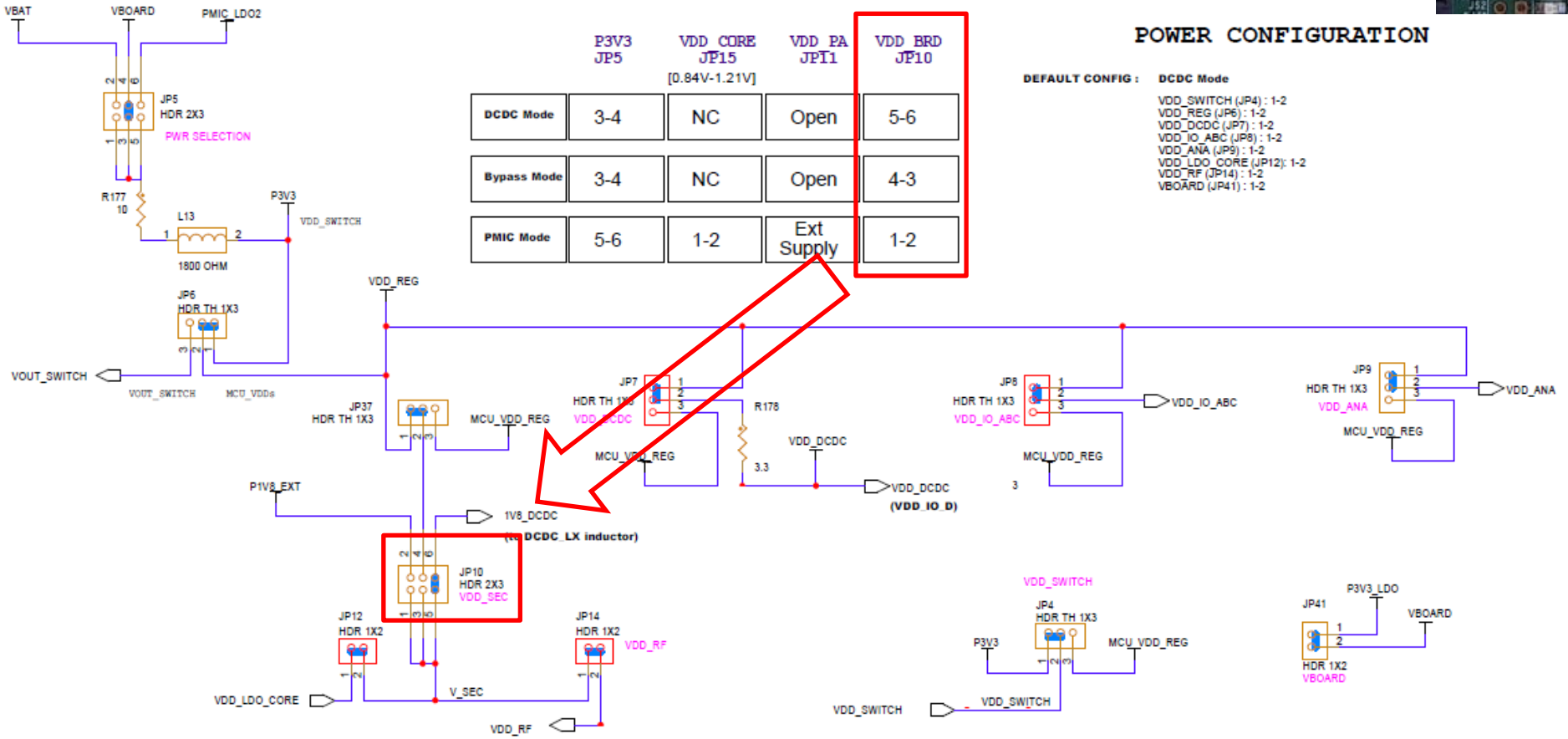
Supplies

SECURE CONNECTIONS
FOR A SMARTER WORLD

HW RECOMMENDATION - SUPPLIES

Power modes: Buck, Bypass or PMIC Switch.





	P3V3 JP5	VDD_CORE JP15 [0.84V-1.21V]	VDD_PA JP11	VDD_BRD JP10
DCDC Mode	3-4	NC	Open	5-6
Bypass Mode	3-4	NC	Open	4-3
PMIC Mode	5-6	1-2	Ext Supply	1-2

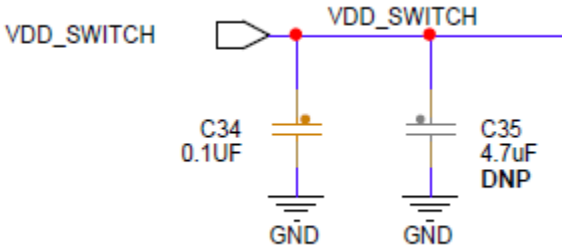
POWER CONFIGURATION

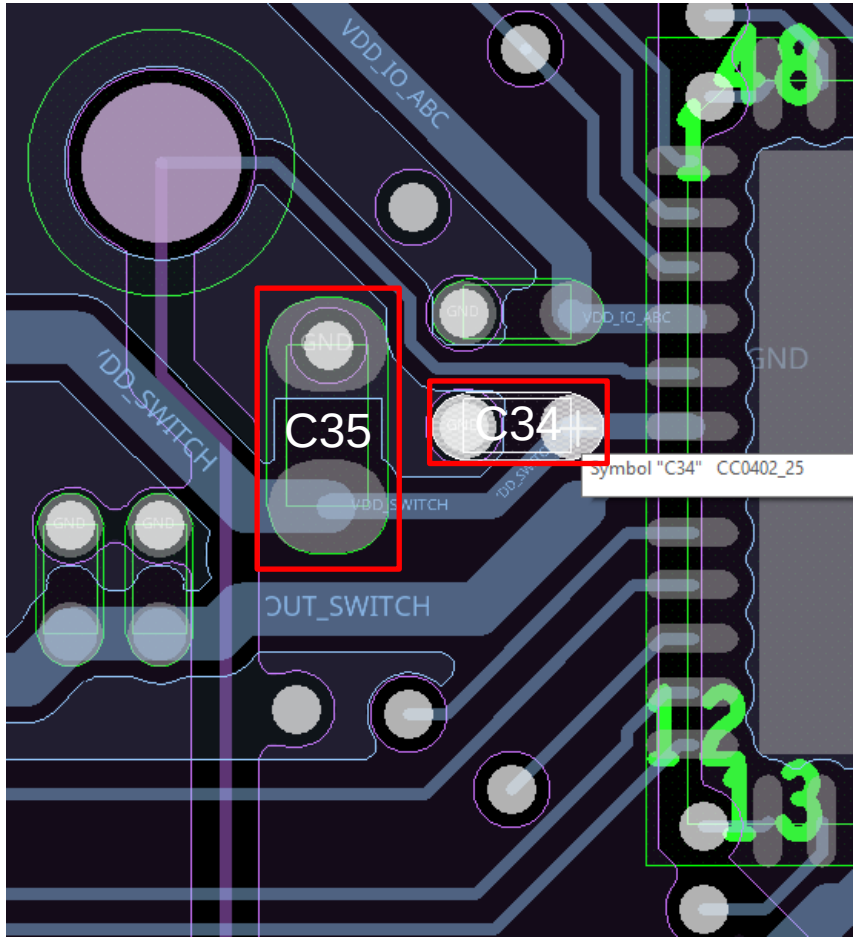
DEFAULT CONFIG : DCDC Mode

VDD_SWITCH (JP4) : 1-2
VDD_REG (JP6) : 1-2
VDD_DCDC (JP7) : 1-2
VDD_IO_ABC (JP8) : 1-2
VDD_ANA (JP9) : 1-2
VDD_LDO_CORE (JP12): 1-2
VDD_RF (JP14) : 1-2
VBOARD (JP41) : 1-2

HW RECOMMENDATION - SUPPLIES

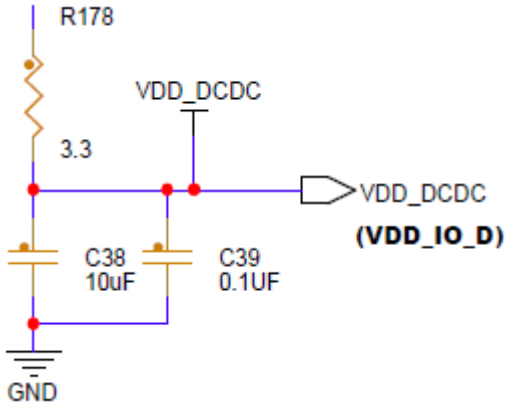
Vdd_Switch (pin6)

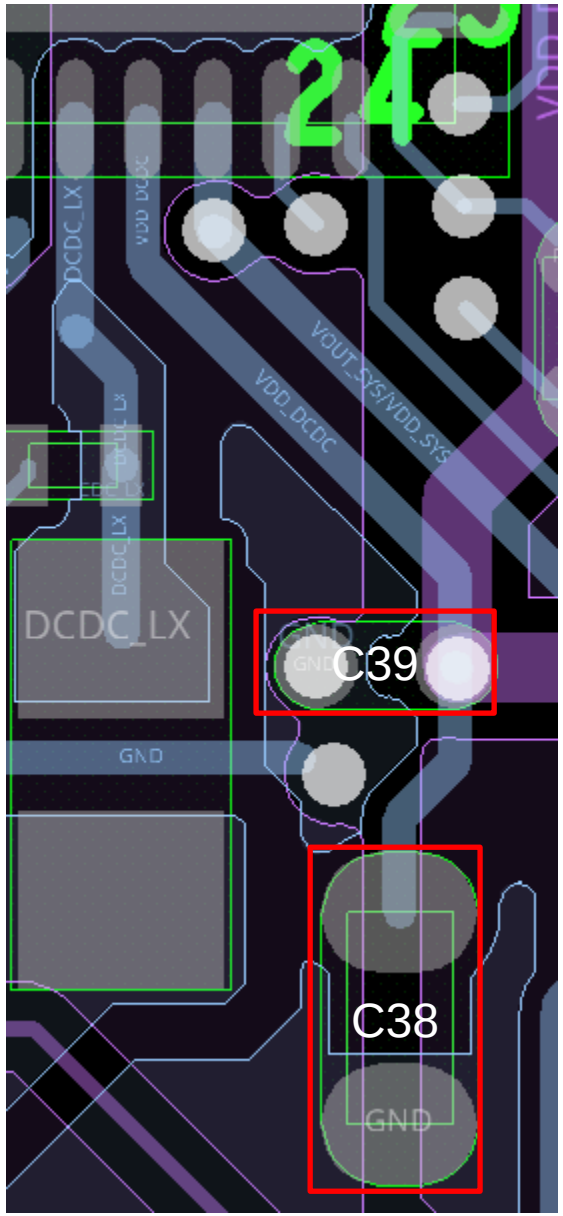




HW RECOMMENDATION - SUPPLIES

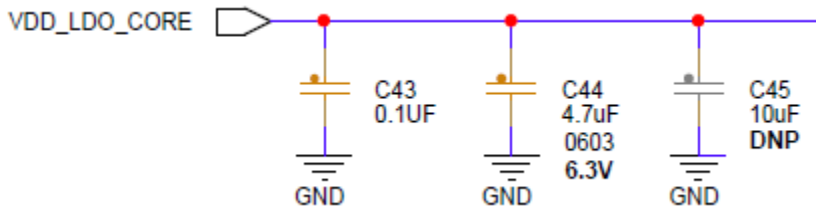
Vdd_DCDC (& VDD_IO_D) (pin21)

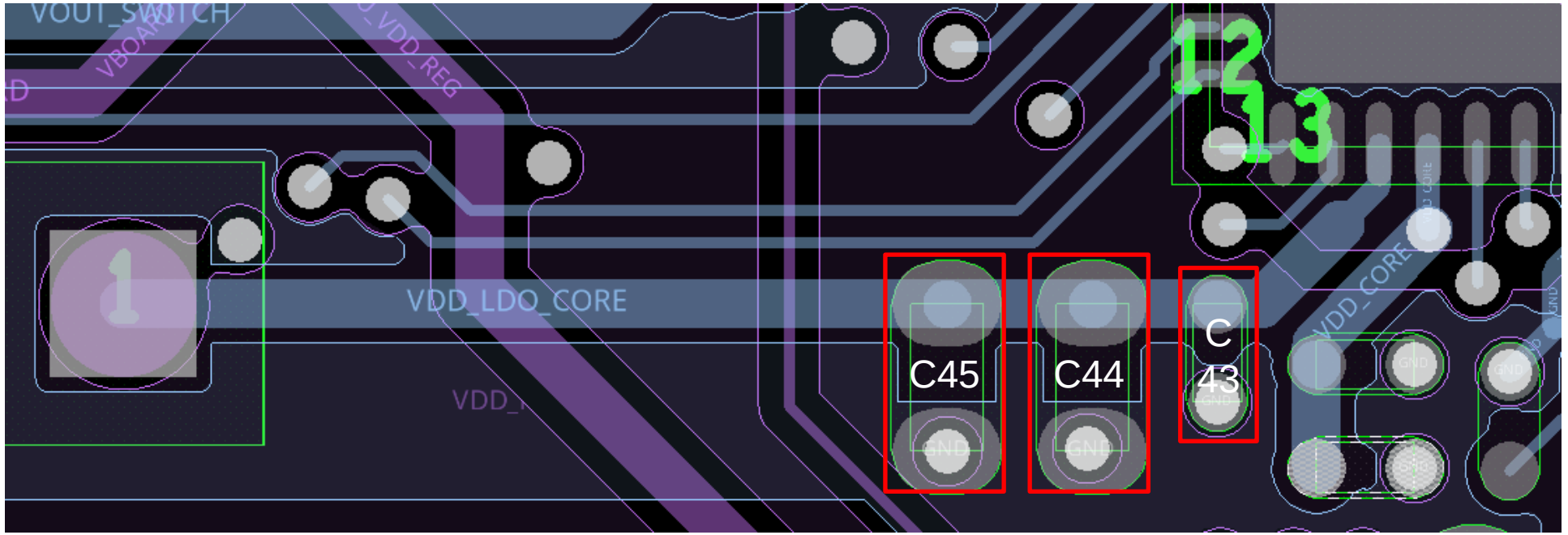




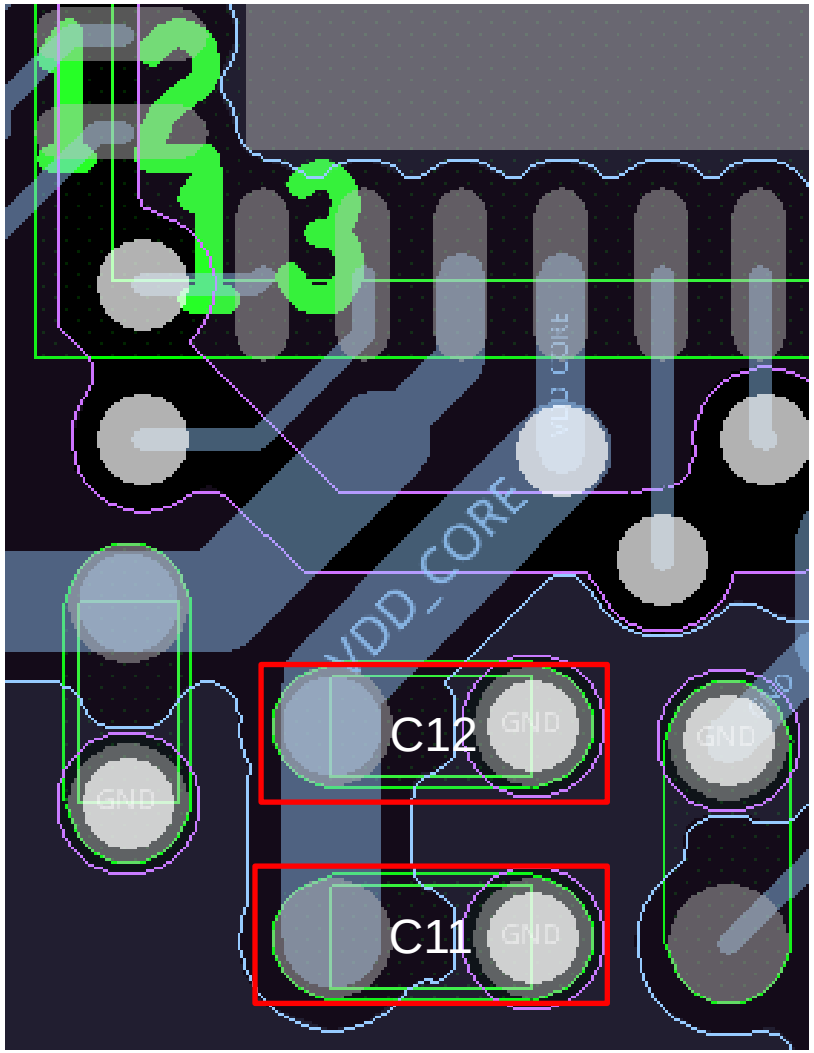
HW RECOMMENDATION - SUPPLIES

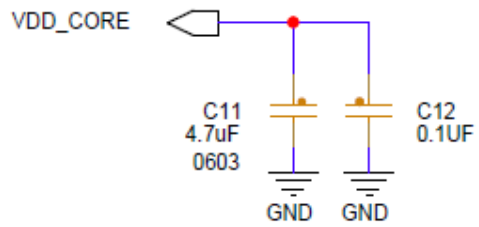
Vdd_LDO_Core (pin15)





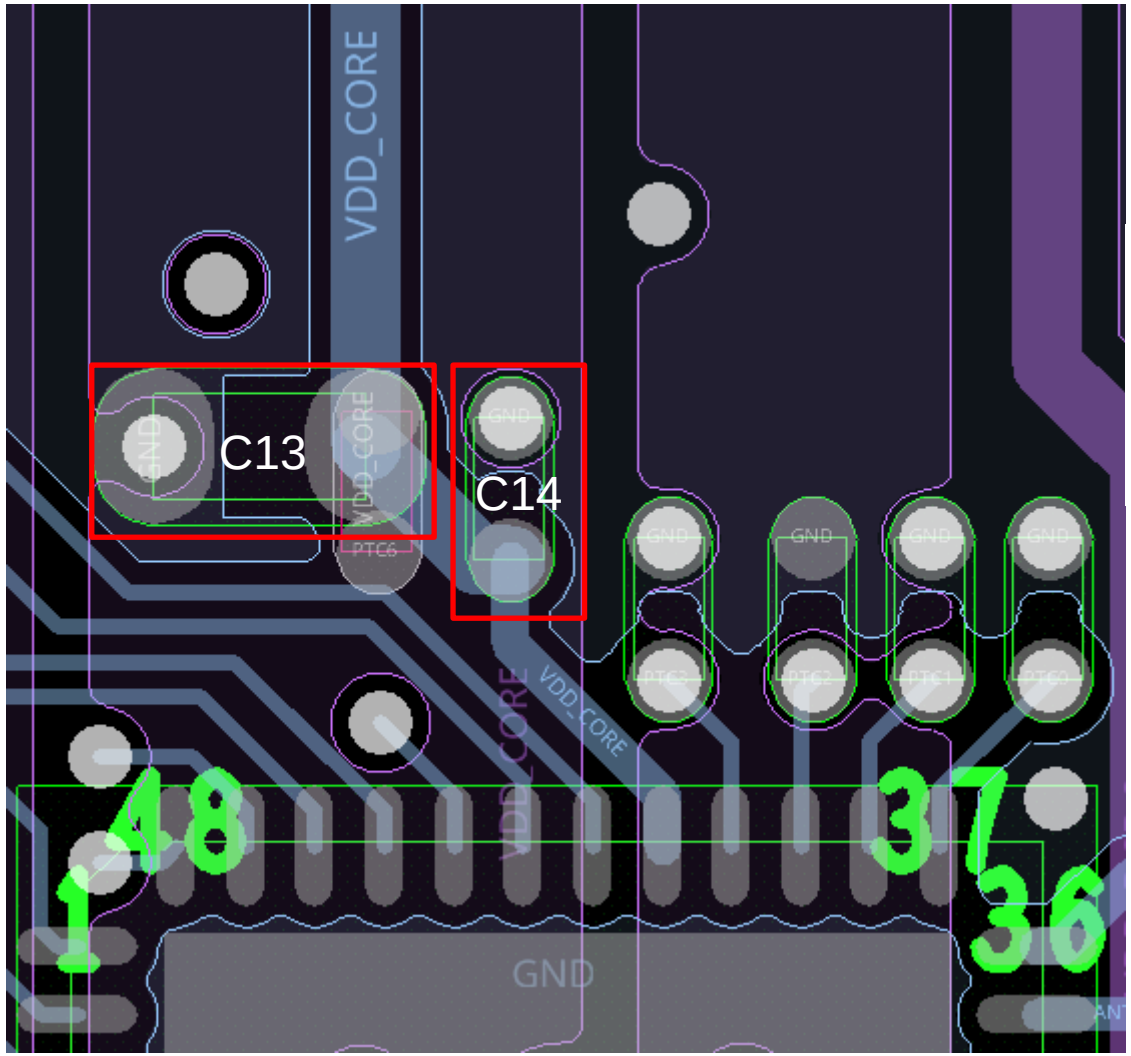
Vdd_Core1 (pin16):

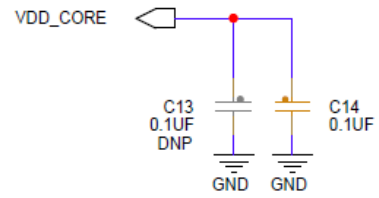




CAD note: Place C11 & C12 caps close to pin16

Vdd_Core2 (pin41):



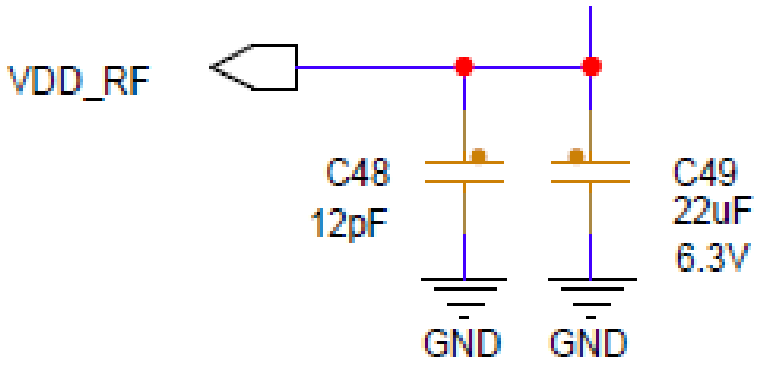


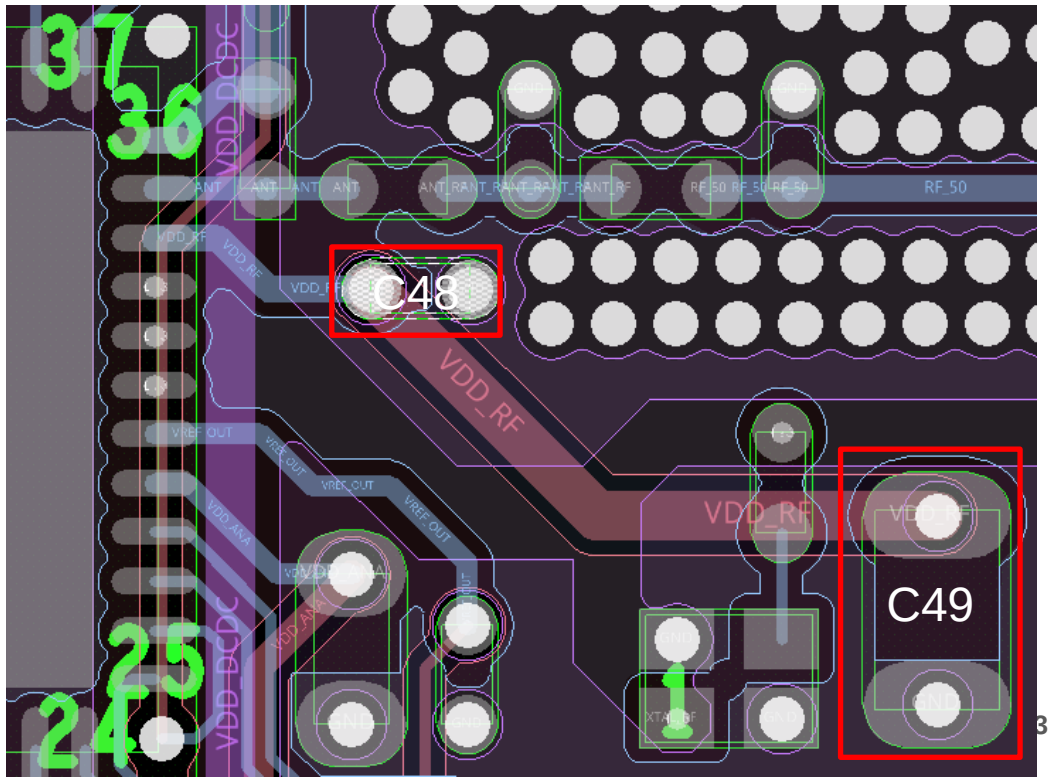
CAD note: Place C13 & C14 caps close to pin41

HW RECOMMENDATION - SUPPLIES

Vdd_RF (pin34):

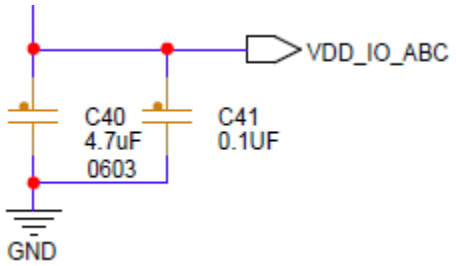
- decoupling near the IC (some mm, not more)
- Decoupling capacitor of 12pF (near the pin 34) between 32MHz crystal RF path
- Decoupling capacitor of 22uF not so closed to the IC due to component size
- Vdd_RF line not superposed to another supply (digital supply is strongly forbidden)
- Vdd_RF line not crossing the expose die pad of the IC

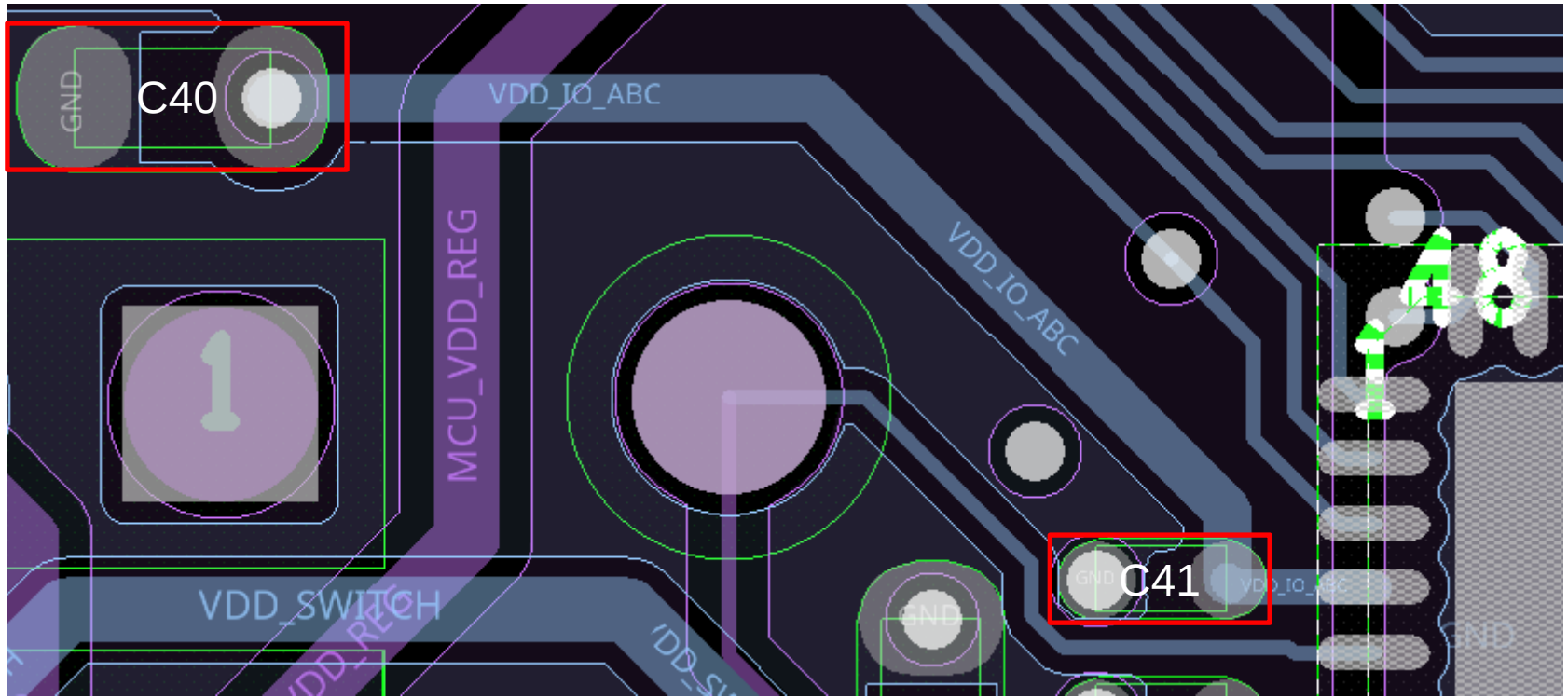




HW RECOMMENDATION - SUPPLIES

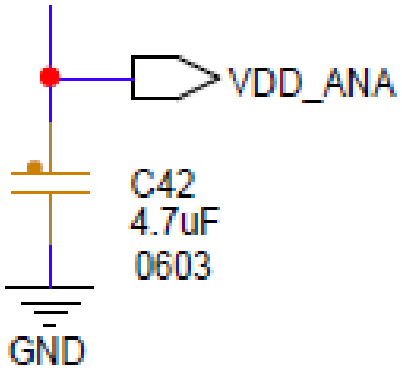
Vdd_IO_ABC (pin4):

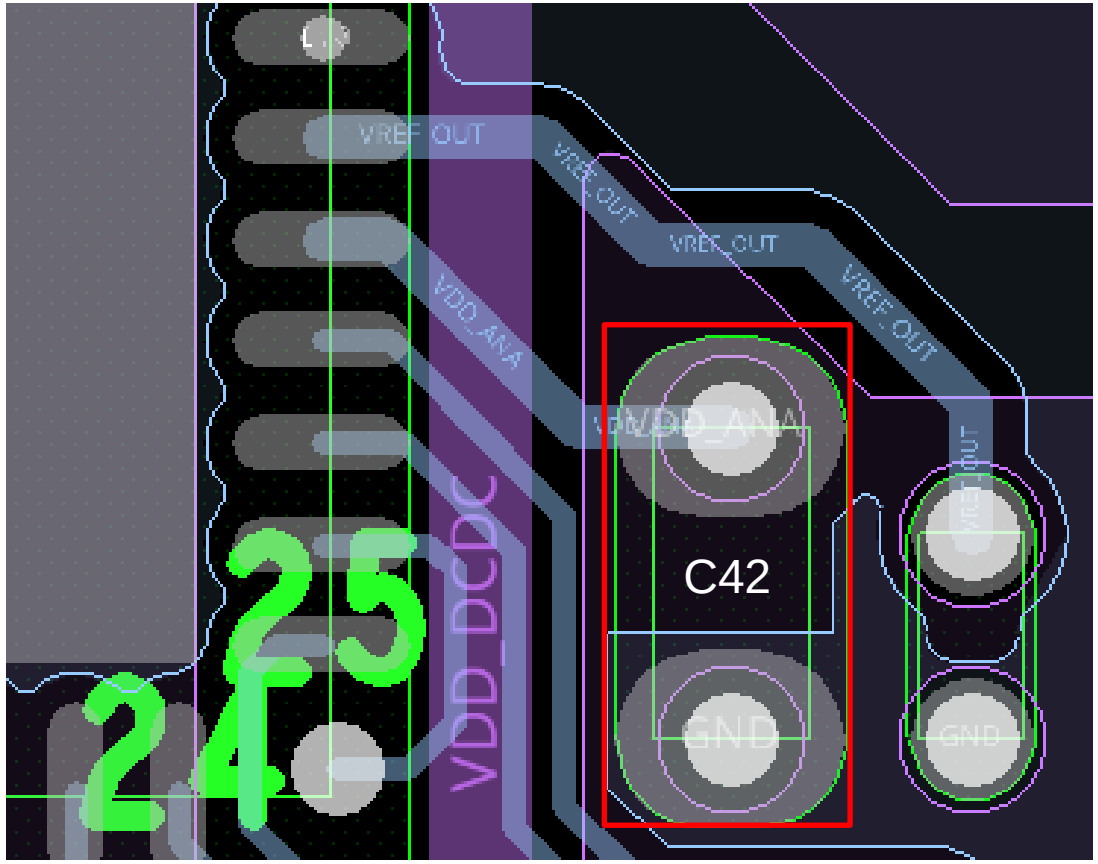




HW RECOMMENDATION - SUPPLIES

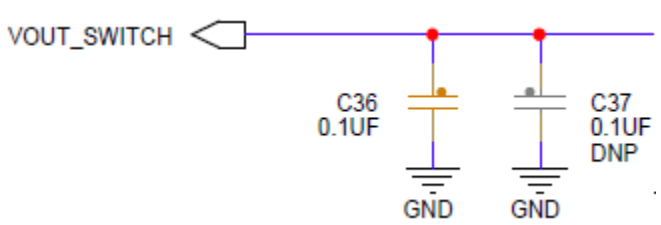
Vdd_Ana (pin29)

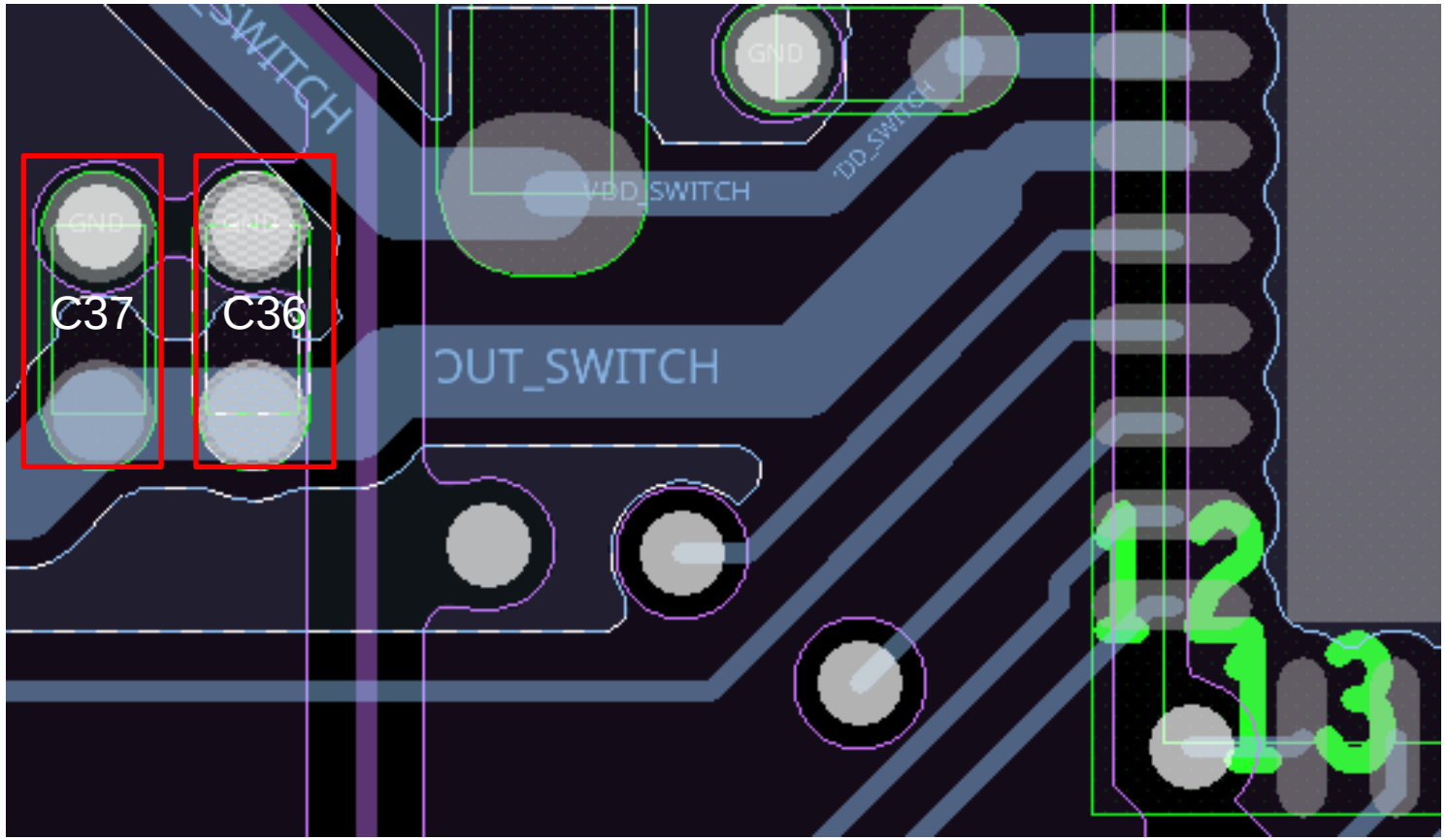




HW RECOMMENDATION - SUPPLIES

Vout_Switch (pin7):

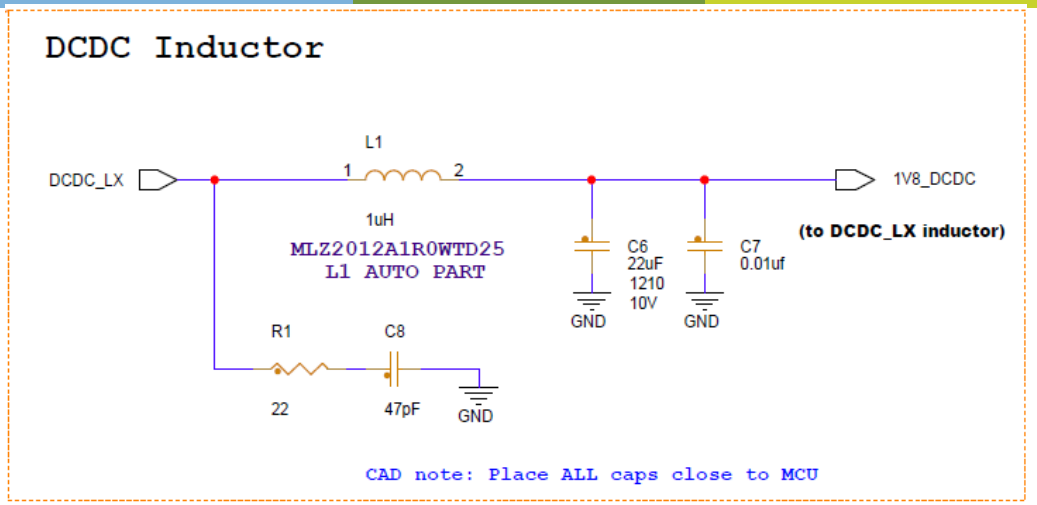


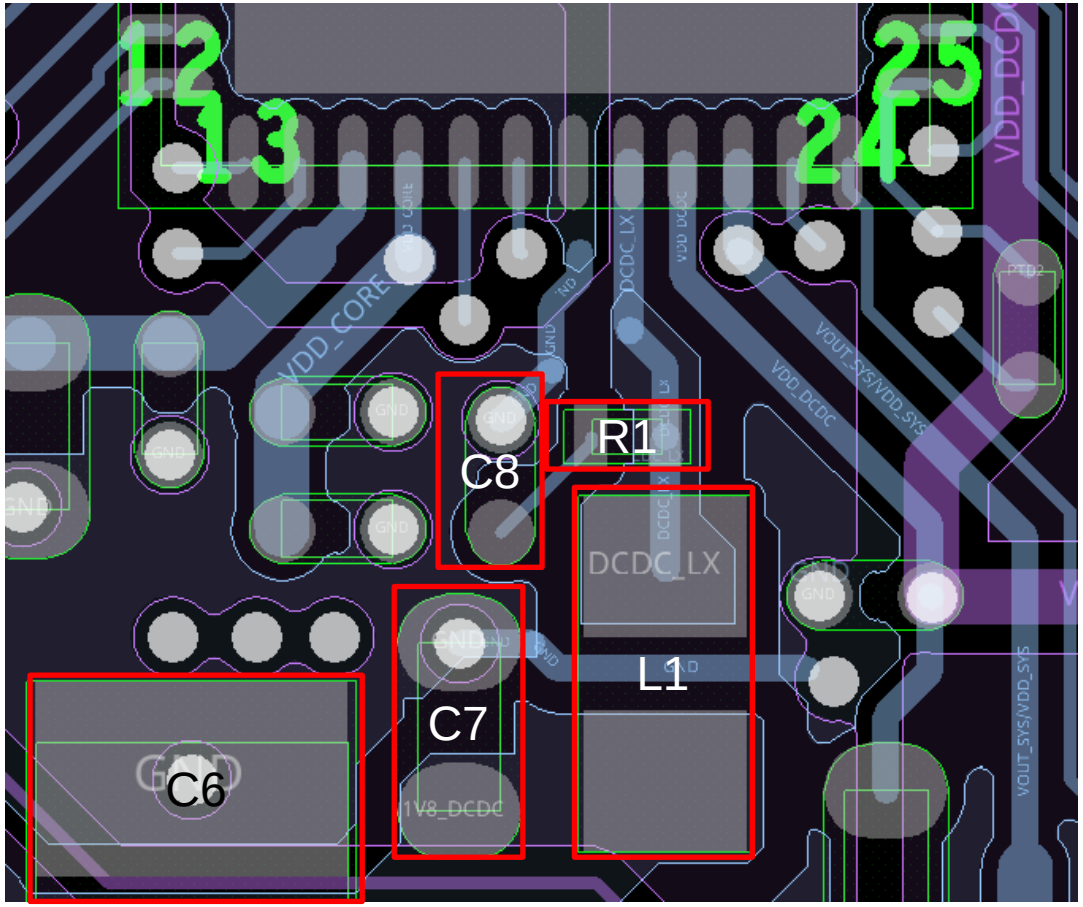


HW RECOMMENDATION - SUPPLIES

Notes

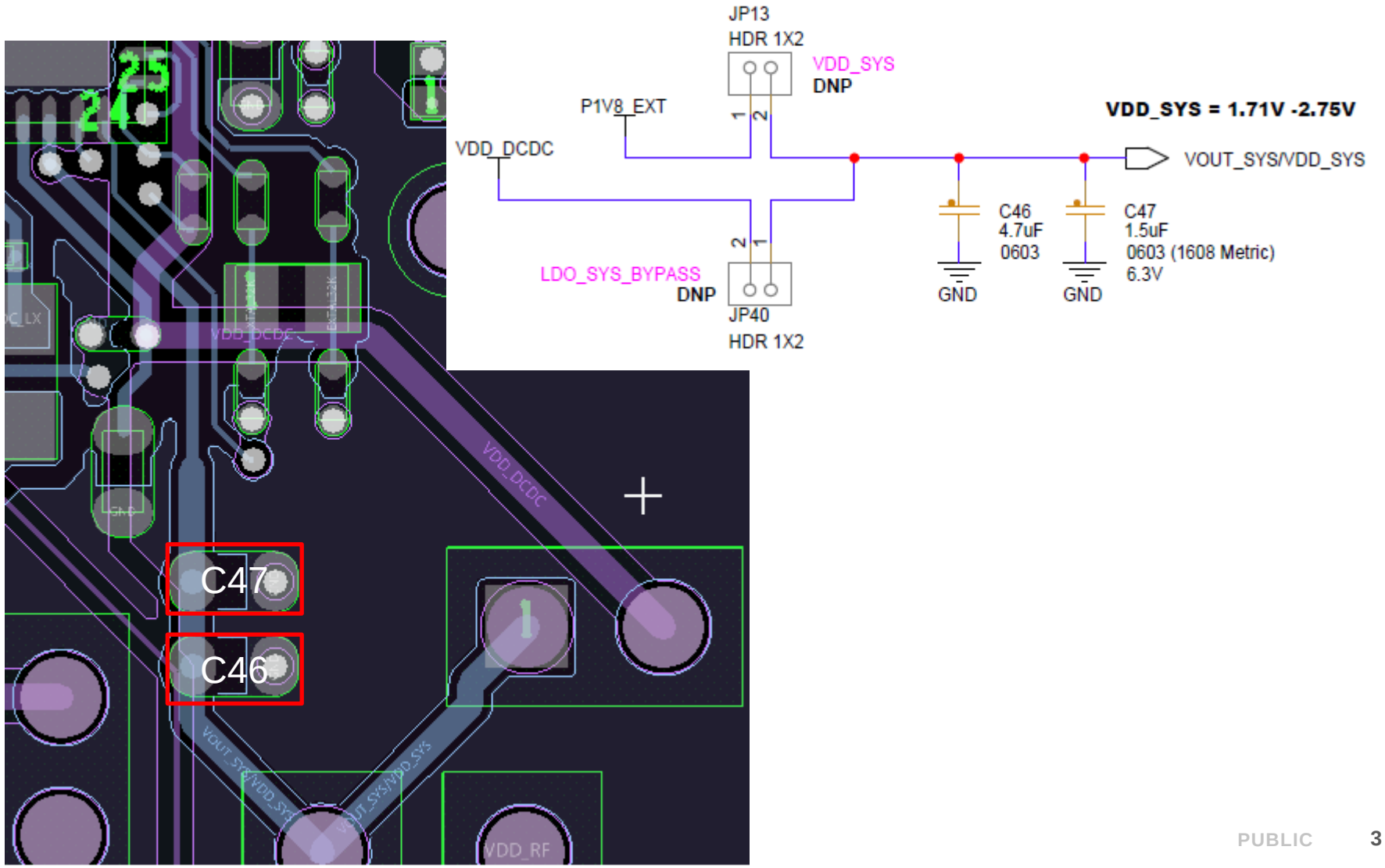
DCDC_LX (pin20):





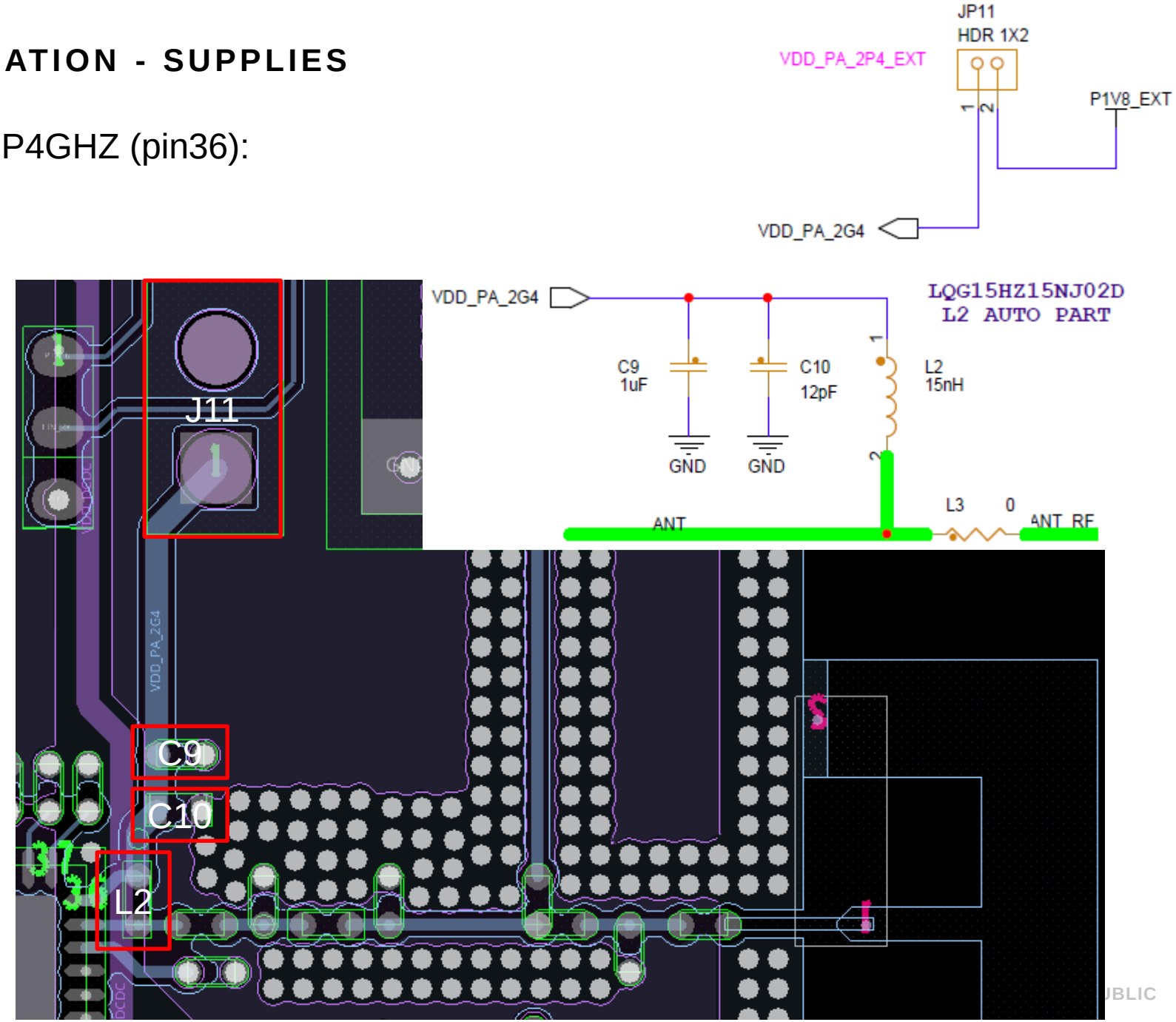
HW RECOMMENDATION - SUPPLIES

VOUT_SYS/VDD_SYS (pin22):



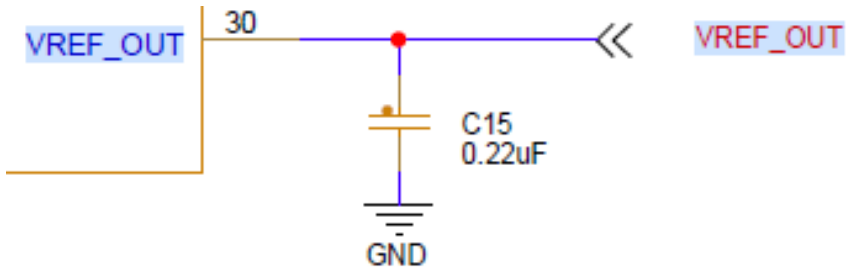
HW RECOMMENDATION - SUPPLIES

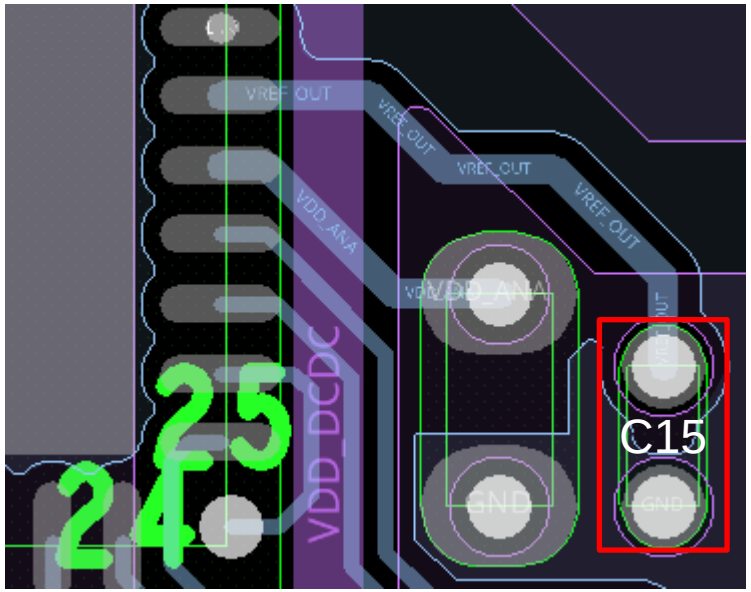
VPA_2P4GHZ (pin36):



VREF_OUT (pin30):

- Reduce the line width (voltage output with low current)
- Decoupling capacitor C15 is not needed to be near the IC (compromize to gain space)
- Vref_out line not superposed to Vdd_RF line



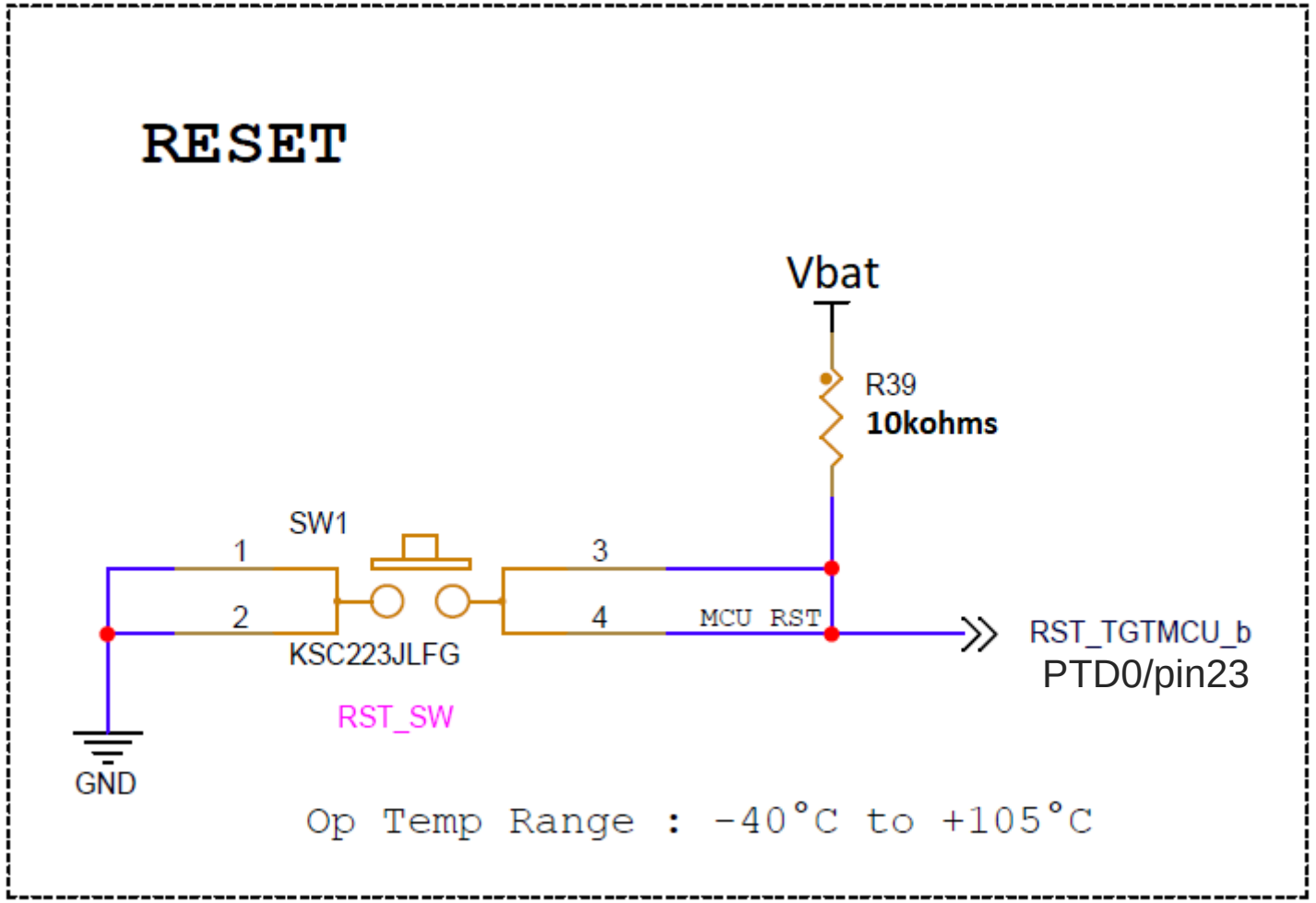


RESET

SECURE CONNECTIONS
FOR A SMARTER WORLD

RESET

Be careful to connect the 10kohms pullup to Vbat, not Vdd_1p8 in buck mode.



Clocks and Crystals

SECURE CONNECTIONS
FOR A SMARTER WORLD

CRYSTAL REFERENCES

For Bluetooth LE, GFSK & 802.15.4 **32MHz** and **26MHz** quartz references

Manufacturer	Series	Part Number	Frequency
NDK	NX1612SA	EXS00A-CS14160	32MHz
NDK	NX2016SA	EXS00A-CS13636	26MHz

Manufacturer	Series	Part Number	Frequency
NDK	NX2016SA	EXS00A-CS14161	32MHz

For Bluetooth LE and GFSK **32kHz** quartz reference

Manufacturer	Series	Part Number	Frequency
NDK	NX2016SA	EXS00A-MU01517	32,768kHz
NDK	NX1612SA	EXS00A-MU00801	32,768kHz

TECHNICAL CRYSTAL PARAMETERS

BLE recommendation: +/-50ppm

- KWxx internal oscillator tolerance is -17/+20pm
- XTal:
  - Initial tolerance is +/-10ppm
  - **Tolerance for external Xtal is -33/+30ppm**
    - Frequency aging (10years) is -6/+1ppm
    - Frequency vs temperature (-40/+105°C) is +/-18ppm
    - Frequency tolerance (reference) is -9/+11ppm

It is OK for BLE with the NDK Xtals (+105°C max Ta temperature) ➔

15.4 recommendation: +/-40ppm

The same unique NDK Xtal reference so far ! ! And it doesn't fit with the +/-40ppm

For 15.4, KWxx internal oscillator tolerance is the same : -17/+20pm
Then Xtal tolerance over Temperature and aging has to be -23/+20ppm!
Is there any existing Xtal with such performance with :
Same Cload at 8pF
for a temperature range of -40+125°
In 1612 package
ESR 50 typical >> 60 max (120 may be acceptable)
Level of drive 200µW max

1. Customer Specifications Number :
2. NDK Specification Number : EXS00A-CS14160
3. Type : NX1612SA

4. Electrical Specifications

	Parameters	SYM.	Electrical Spec. min	typ	max	Units	Notes
1	Nominal frequency	f_{nom}		32.000		MHz	
2	Overtone order	-		Fundamental		-	
3	Frequency tolerance(Overall)	-	-33	-	+30	$\times10^{-6}$	at -40~+105°C Include 4,5 and 6
			-33	-	+62	$\times10^{-6}$	at +105~+120°C Include 4,5 and 6
			-33	-	+72	$\times10^{-6}$	at +120~+125°C Include 4,5 and 6
4	Frequency tolerance(Reference)	-	-9	-	+11	$\times10^{-6}$	at +25°C
5	Frequency versus temperature characteristics(Reference)	-	-18	-	+18	$\times10^{-6}$	at -40~+105°C The reference temperature shall be +25°C
			-18	-	+50	$\times10^{-6}$	at +105~+120°C The reference temperature shall be +25°C
			-18	-	+60	$\times10^{-6}$	at +120~+125°C The reference temperature shall be +25°C
6	Frequency Aging(at +25°C) (Reference)	-	-2	-	+1	$\times10^{-6}$	1year
			-4	-	+1	$\times10^{-6}$	5years
			-6	-	+1	$\times10^{-6}$	10years
7	Equivalent resistance	-	-	40	60	Ω	IEC PI-network/Series
8	Shunt capacitance	C_0	-30%	0.54	+30%	pF	Not grounded

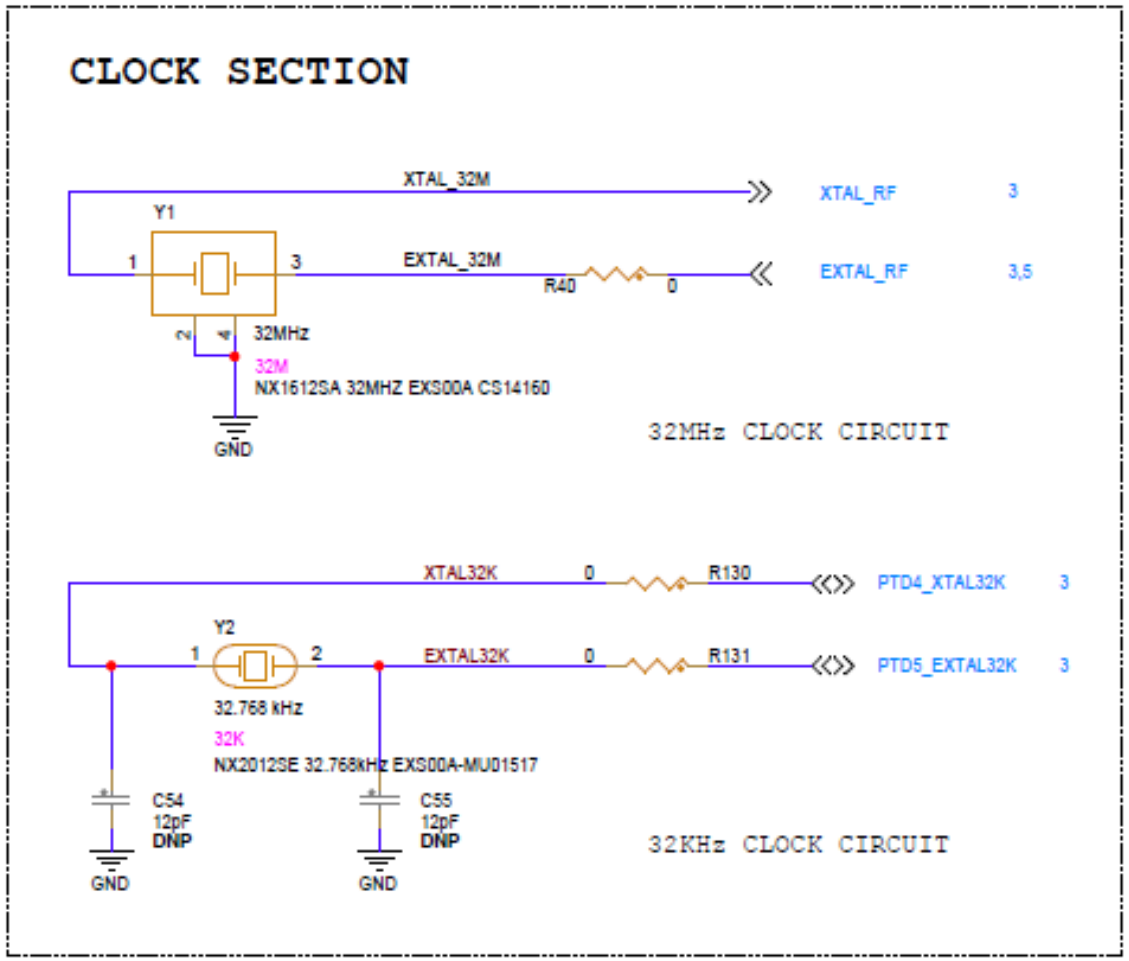
KW45 DS 32MHz:

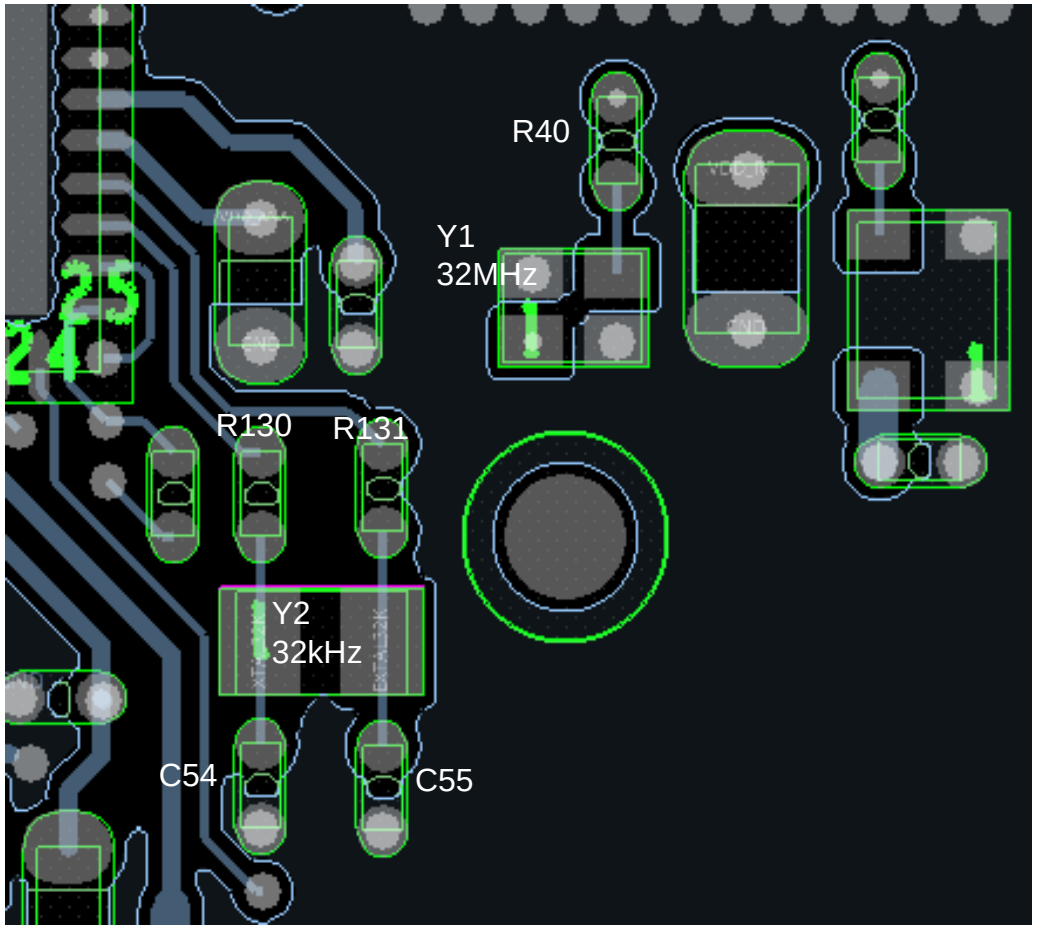
- Target: +/-50ppm (BLE)
  Ta: max at 105°C

Symbol	Description	F0 = 32.0 MHz Min	Typ	Max	F0 = 26.0 MHz Min	Typ	Max	Unit	Notes
T_A	Operating Temperature	–40	—	120	–40	—	120	°C	1
	Crystal initial frequency tolerance	–10	—	10	–10	—	10	ppm	2,3
	Crystal frequency stability and aging	–25	—	25	–25	—	24	ppm	2,4
	Oscillator variation	–12	—	15	–12	—	16	ppm	5
	Total reference oscillator tolerance for Bluetooth LE applications	–50	—	50	–50	—	50	ppm	6

HW RECOMMENDATION - CLOCKS

- 32MHz & 32kHz wire length must be as symetric as possible
- 32kHz quartz is not necessary to be as closed as possible from the DUT (KW45/K32W148)



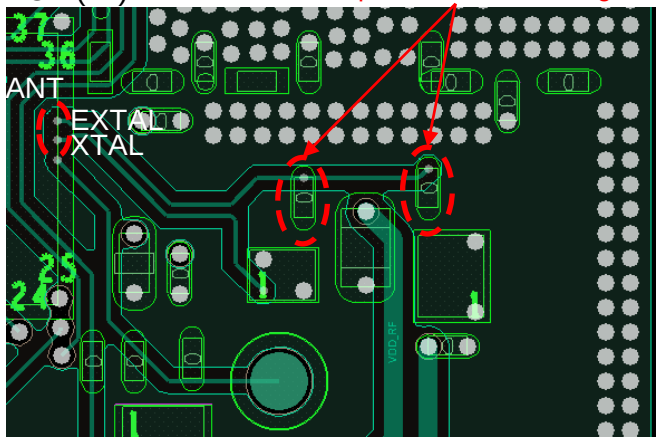


HW RECOMMENDATION - CLOCKS

- Special focus on 32MHz wires to help on a very good layout.

TOP (L1)

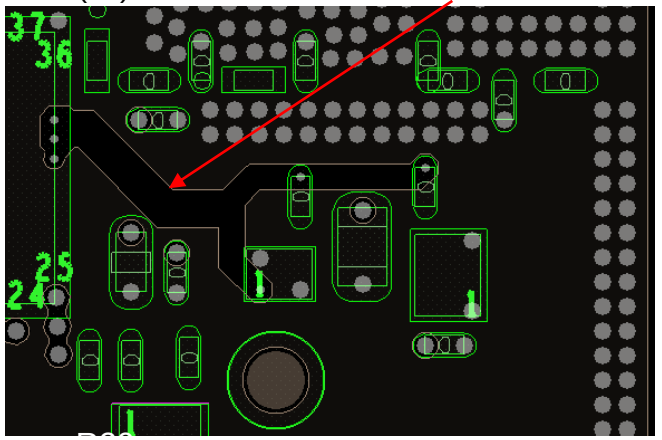
Perpendicular to ANT signal



- Better isolation with perpendicular component to ANT wire
- Via under EXTAL & XTAL to go to L3 are excellent

GND (L2)

Excellent length is as short as possible

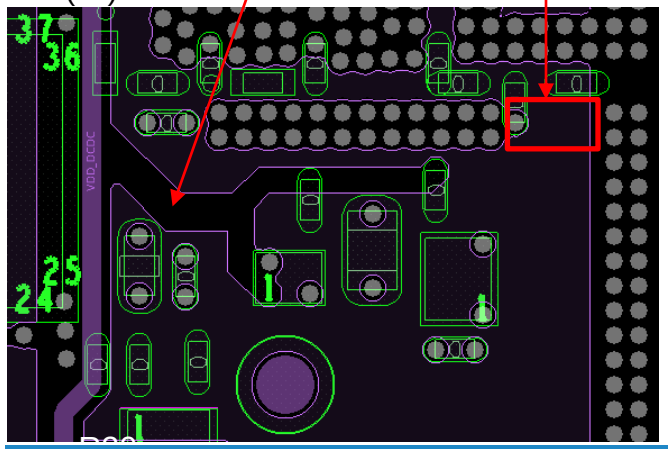


- To reduce capacitance on EXTAL & XTAL GND plane can be opened over XTAL & EXTAL wires
- The shielding is already present on TOP (L1) being GND in these area

Pwr (L4)

Open the Pwr plane
Under EXTAL & XTAL

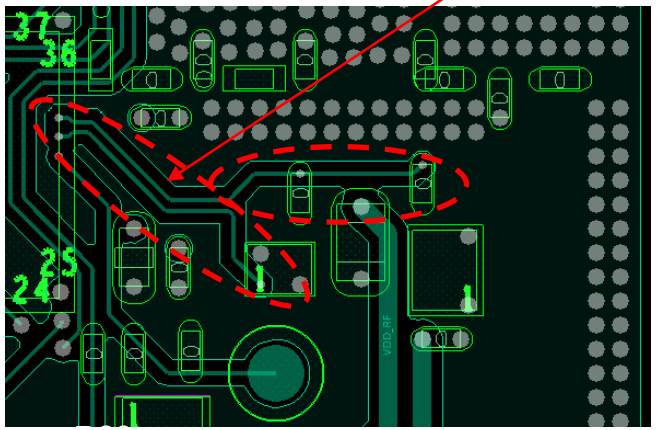
Remove VIAs
For a better Pwr



- Under EXTAL & XTAL Pwr net need to be open to reduce coupling capacitance to PWR
- Some GND vias can be removed to have a better connection of PWR signal

In1 (L3)

Shielding area

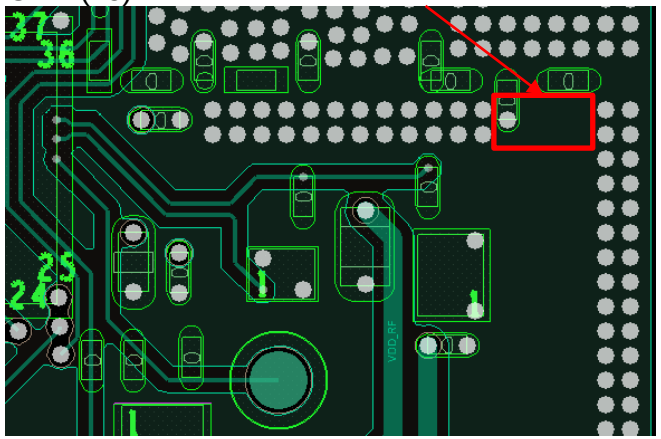


- To avoid coupling XTAL with XTAL_OUT a shield is applied
- To avoid any coupling on XTAL a shield on TOP is applied

HW RECOMMENDATION - CLOCKS

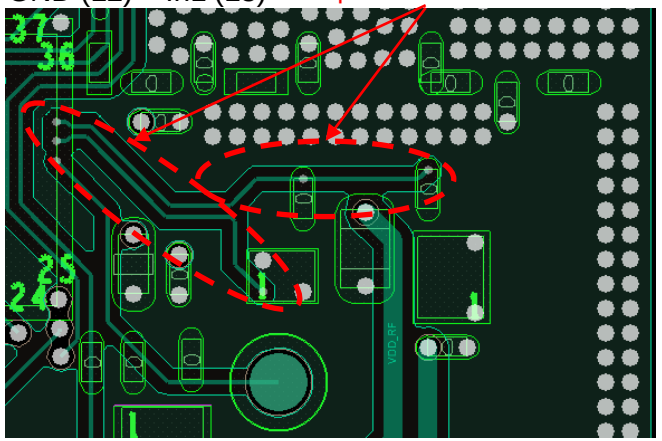
- Special focus on 32MHz wires to help on a very good layout.

GND (L5) Remove some VIAs



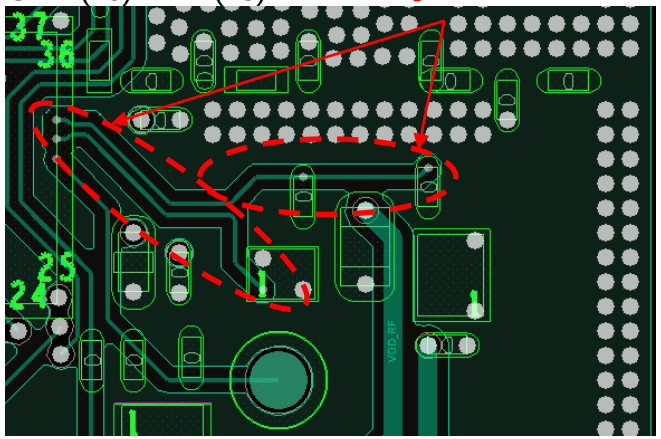
➢ Remove some VIAS for a better Pwr (L4) connection

GND (L2) + In1 (L3) Open L2 over EXTAL & XTAL in L3



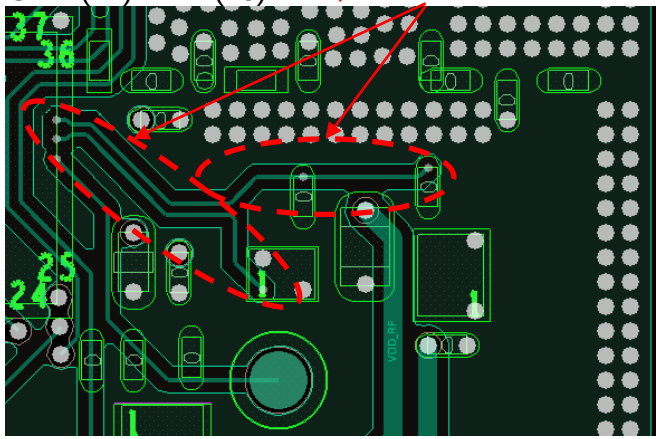
➢ Open L2 over XTAL & EXTAL

GND (L5) + In1 (L3) Shielding the 32MHz wires



➢ Shield to GND near EXTAL & XTAL in In1 (L3)

GND (L2) + In1 (L3) Open L2 over EXTAL & XTAL in L3



➢ Open L2 over XTAL & EXTAL

Bootloader pins

SECURE CONNECTIONS
FOR A SMARTER WORLD

RECOMMENDATION - BOOTLOADER

KW45/K32W1 requires signed firmware to be loaded into the NBU. This happens through the Bootloader. **PTC2 and PTC3 are the UART connection to the Bootloader** (refer to the table below for other peripherals to enter in ISP mode).
NXP recommend to have an option to connect them to a UART to USB converter (for PC connection).
NXP recommend to have a way to **pull PTA4 to logic high** in order to enter the device in **bootloader mode**.

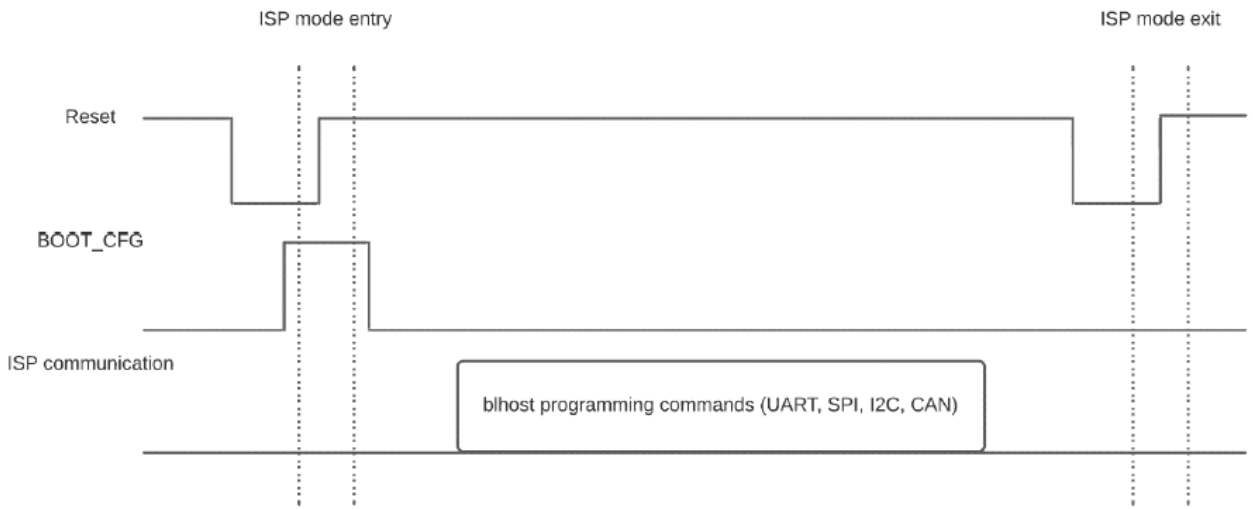


Table 83. Peripheral instances and pin assignments used by ISP

Peripheral instances	Pin name	Pin assignment	Alt
LPUART1	LPUART1_TX	PTC3	3
	LPUART1_RX	PTC2	3
LPSPI1	LPSPI1_PCS0	PTB0	2
	LPSPI1_SIN	PTB1	2
	LPSPI1_SCK	PTB2	2
	LPSPI1_SOUT	PTB3	2
CAN0	CAN0_TX	PTC4	3
	CAN0_RX	PTC5	3
LPI2C1	LPI2C1_SCL	PTB5	4
	LPI2C1_SDA	PTB4	4

Make sure that everything connected to PORTD is at the same voltage as VDD_IO_D.
Same for PORTA, B and C and VDD_IO_ABC.

Wake up pins

SECURE CONNECTIONS
FOR A SMARTER WORLD

RECOMMENDATION – WAKE UP PINS

Some pins could wake up the KW45/K32W1:

48 pins package: PTB4, PTA0, PTA4, PTA17, PTA19, PTA21, PTC0, PTC1, PTC2, PTC4, PTC6, PTC7, PTB0, PTB3

40 pins package: PTB4 , PTA0, PTA4, PTA17, PTA19, PTA21, PTC4, PTC7, PTB0, TPB3

Level shifters

SECURE CONNECTIONS
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RECOMMENDATION – LEVEL SHIFTER

Make sure that everything connected to PORTD is at the same voltage as VDD_IO_D.

Same for PORTA, B and C and VDD_IO_ABC.

Other peripheral ICs connected to the KW45/K32W1 MUST be at the same voltage level. KW45/K32W1 device is capable to set the IO_ABC voltage independently to the other Vdd voltages.

IO current drive

SECURE CONNECTIONS
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RECOMMENDATION – IO CURRENT DRIVE

It’s important to know some pins could handle higher current than others.

This specific pin list could handle 12mA current drive instead of 6mA on other IO pins:

- PTA18-19; PTB4-5; PTC0-1; PTC4-5

Note that both the DSE0 and DSE1 bits in the control register for that pin must be set in order to get the highest drive strength.

20.2 Module Configuration (INTERNAL REVIEW ONLY)

Resolved for module instance: PORTA

Chapter merged also from module instances: PORTB, PORTC, PORTD

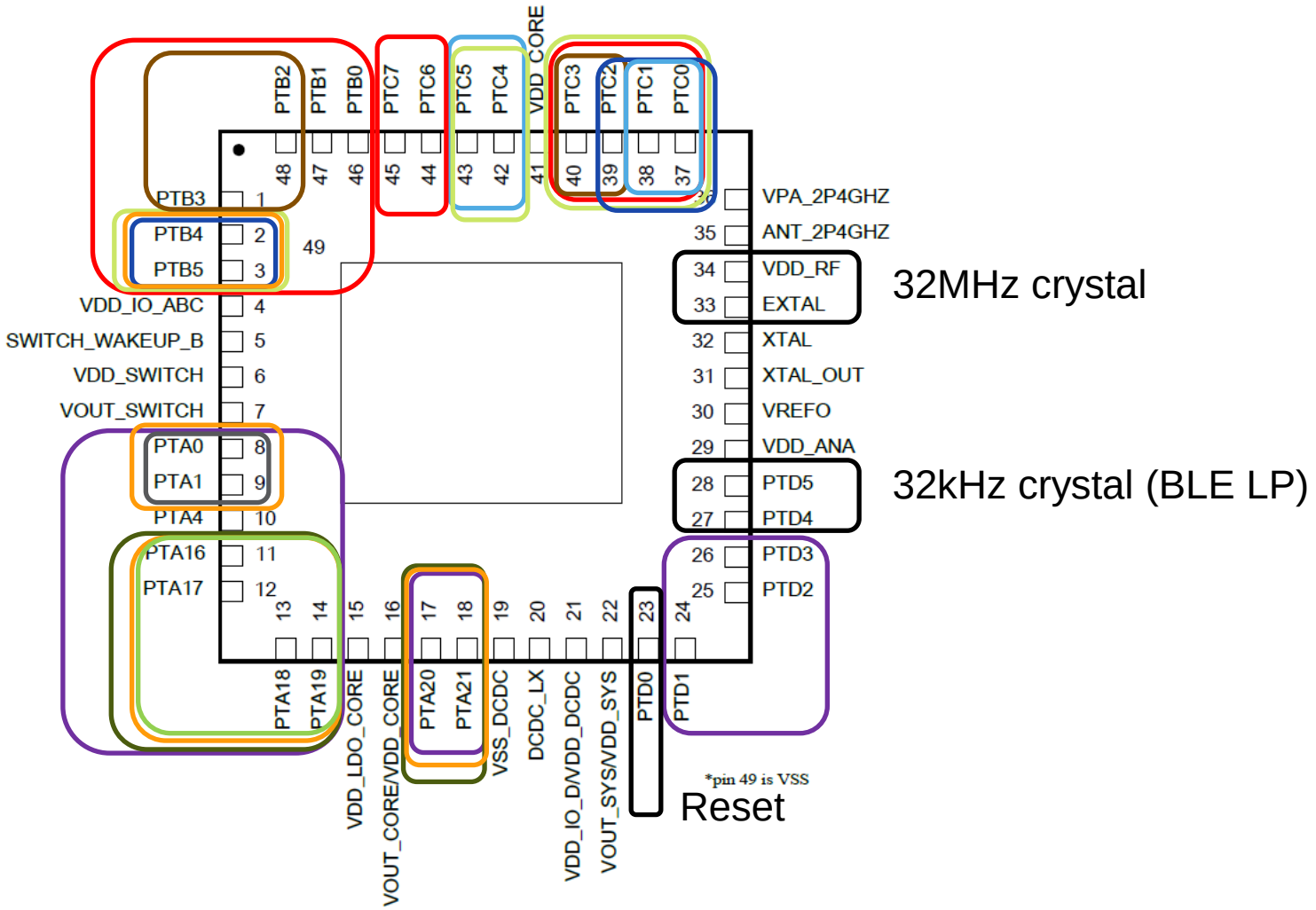
Parameter	Instantiated Value (PORTA)	Differences	Range	Origin	Description
PINDSE0_DIS	0x00 (0)	PORTD: 4294967295	[0-unbounded]	RTL	Disable DSE0 Config Bits
PINDSE0_RST	0x04 (4)	PORTB: 0, PORTC: 0, PORTD: 0	[0-unbounded]	RTL	Pin DSE0 Reset value

Peripherals

SECURE CONNECTIONS
FOR A SMARTER WORLD

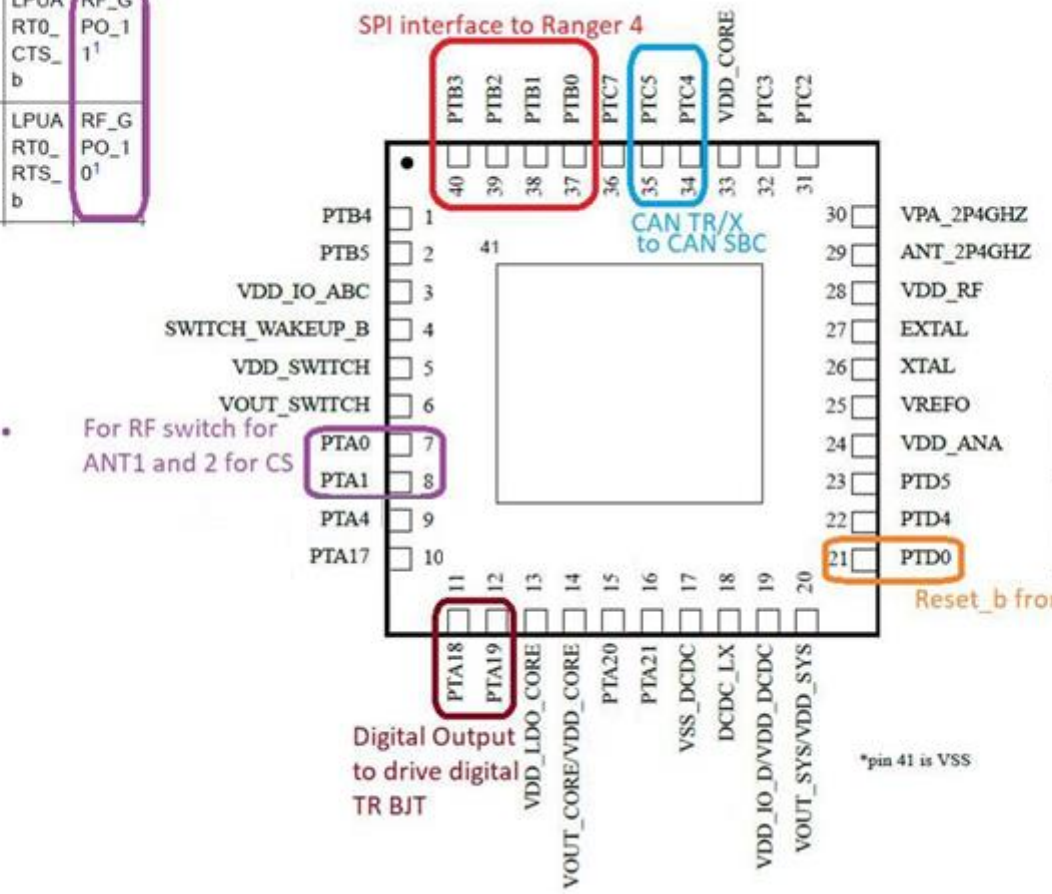
INFORMATION – PERIPHERAL PINS ON 48PINS DEVICE

- SWD
- UART0
- UART1
- SPI0
- SPI1
- RF switch for ANT1&2
- I2C0
- I2C1
- I3C0
- CAN0



INFORMATION – PERIPHERAL PINS ON 40PINS DEVICE

7	PTA0		PTA0	CMP 0_OUT	LPUART0_CTS_b	RF_GPO_11[1]
8	PTA1		PTA1	CMP 1_OUT	LPUART0_RTS_b	RF_GPO_10[1]



37	PTB0	ADC0_B10	PTB0	LPSPI1_PCS0	
38	PTB1	ADC0_B11	PTB1	LPSPI1_SIN	
39	PTB2	ADC0_B12	PTB2	LPSPI1_SCK	
40	PTB3	ADC0_B13	PTB3	LPSPI1_SOUT	

34	PTC4		PTC4	LPSPI1_SIN	CAN0_TX[7]
35	PTC5		PTC5	LPSPI1_PCS0	CAN0_RX[7]

DTEST pins

SECURE CONNECTIONS
FOR A SMARTER WORLD

INFORMATION – DTEST PINS

The DTM (Direct Test Mode) pins are available for both 48 pins and 40 pins packages.

The options are:

PTD1 ALT8 – RF_UART_SIN	(48-pin only)
PTD2 ALT8 – RF_UART_SOUT	(48-pin only)
PTC2 ALT6 – RF_UART_SIN	(48-pin & 40-pin)
PTC3 ALT6 – RF_UART_SOUT	(48-pin & 40-pin)

Battery: CoinCells

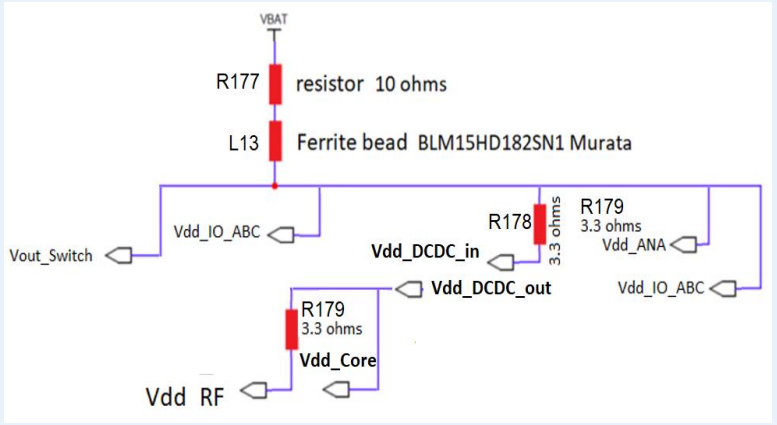
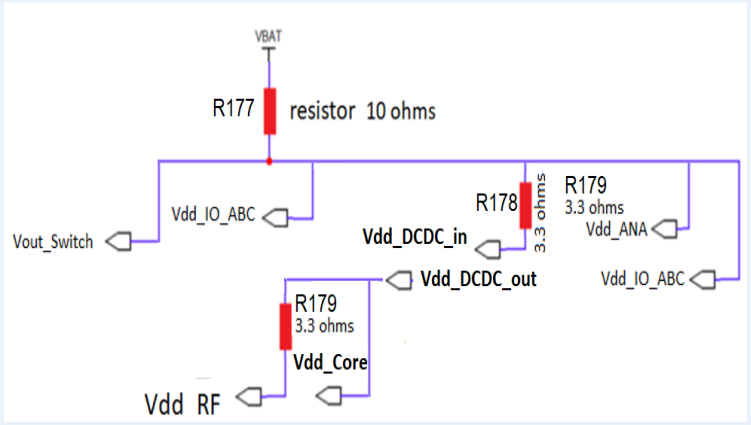
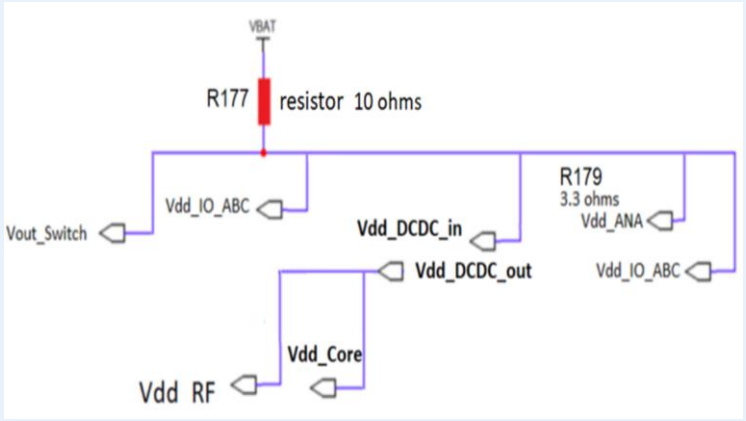
SECURE CONNECTIONS
FOR A SMARTER WORLD

DCDC BUCK MODE – COINCELL – SUMMARY

Schematic – Recommandation for coincell only
(peak of current below 10mA)
Reduced current peak

Suitable for battery (coincell) applications only

Solution to reduce the DCDC current peaks and current peaks on Tx signals (+10/+7/+0dBm) during Bluetooth LE events (Advertising, Connect & Scan) is to add serial resistor(s) on different supplies.
It will limit the peaks of current below 10mA.
Voltage drop occurs due to the serial resistor(s) but it never goes down to POR threshold (up to 105°C).

Maximum Tx output @+10dBm	Maximum Tx output @+7dBm	Maximum Tx output @+0dBm
Maximum peak of current: <1mA	Maximum peak of current: 2mA	Maximum peak of current: 4.5mA
		

Unused IOs

SECURE CONNECTIONS
FOR A SMARTER WORLD

RECOMMENDATION CONNECTION FOR UNUSED IOS

Datasheet extract

HVQFN48WF – 7x7

Table 54. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VOUT_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_CORE	Connect to VDD_LDO_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_SYS	Connect to VDD_IO_D	When the LDO is bypassed, the input and output should be connected together and tied to
			an external supply. The regulator should also be disabled in software.
Power	VDD_DCDC	Ground	When the DCDC is not used, the input should be tied to VSS through a 10 kΩ resistor.
Power	DCDC_LX	Float	The input VDD_DCDC should be tied to VSS with 10 Kohm
Power	VDD_IO_D	Must be powered	VDD_IO_D is used to power parts of the system power controller (SPC) and must be powered to use the chip. If LDO_SYS is not being used, then tie VDD_IO_D to VOUT_SYS and supply power from an external source. The regulator should also be disabled in software.
Power	VDD_PA_2.4GHz	Float	VDD_PA_2.4GHz is always driven, either from internal LDO sourced by VDD_RF, or from external supply.

RECOMMENDATION CONNECTION FOR UNUSED IOS

Datasheet extract

HVQFN48WF – 7x7

Power	VDD_SWITCH	Must be powered	Powers FRO16 and a portion of RAM.
Power	VOUT_SWITCH	Float	
Power	VDD_IO_ABC	Must be powered	VDD_IO_ABC powers the mux logic for PORTA, PORTB and PORTC. It must be powered during POR. The recommendation is to keep it powered, but it can be connected to the output of the Smart Power Switch and be left floating in shelf storage mode.
Power	VDD_ANA	Float	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_DCDC	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_RF	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n*_*x*	Float	
Analog/non-GPIO	VREF_OUT	Float	Analog output - Float
Analog/non-GPIO	TAMPERx	Float	
Analog/non-GPIO	RTC_WAKEUP_B	Float	
Analog/non-GPIO	RTC_RTCCLKOUT	Float	
Analog/non-GPIO	EXTAL32K	Float	
Analog/non-GPIO	XTAL32K	Float	Analog output - Float
Analog/non-GPIO	EXTAL_32M	Float	
Analog/non-GPIO	XTAL_32M	Float	Analog output - Float
GPIO/Analog	PTx/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	PTD1/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)

Layout general rules

SECURE CONNECTIONS
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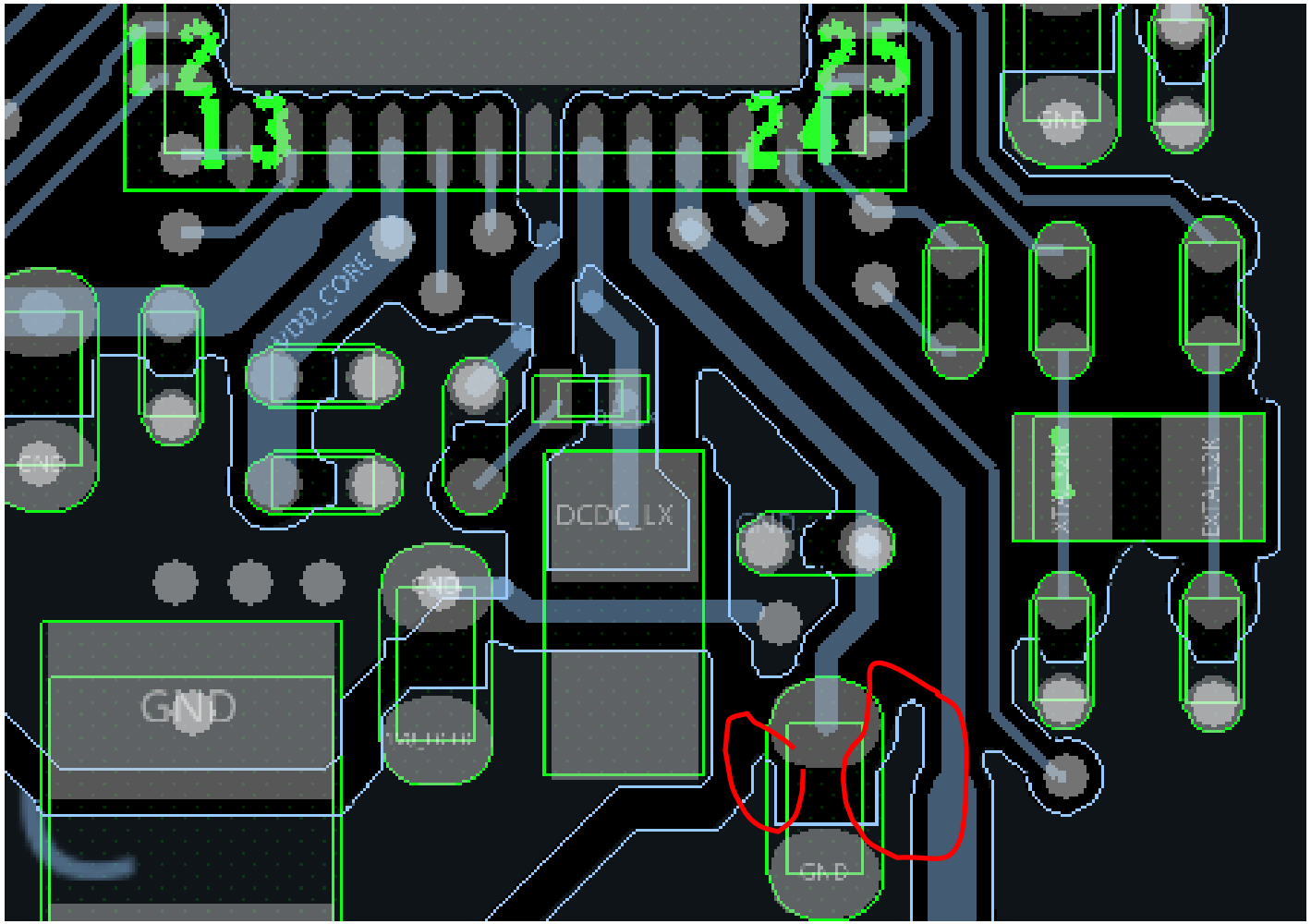
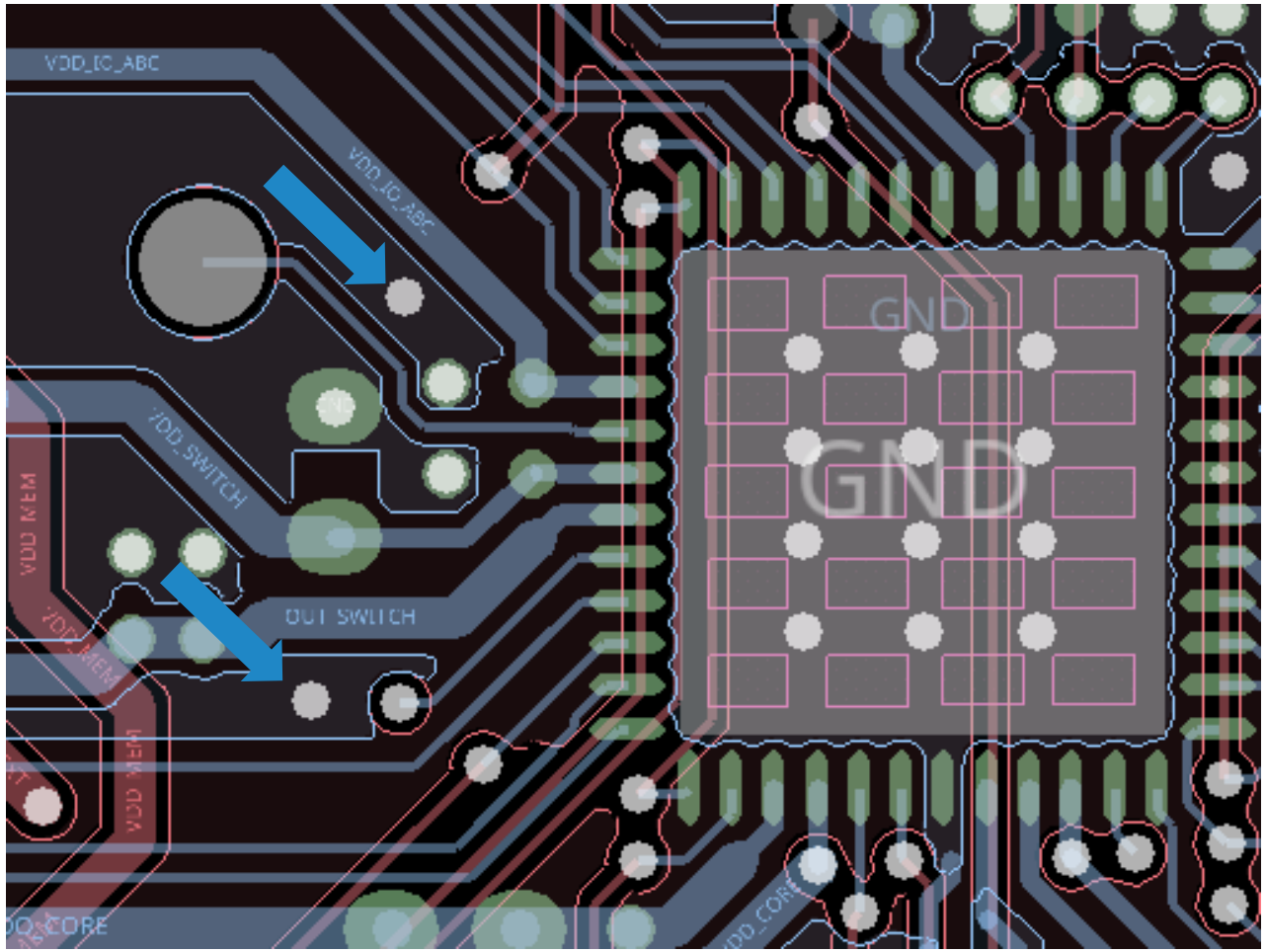
HW RECOMMENDATION – LAYOUT GENERAL RULES: FINGERPRINT

Avoid fingerprint like below example:



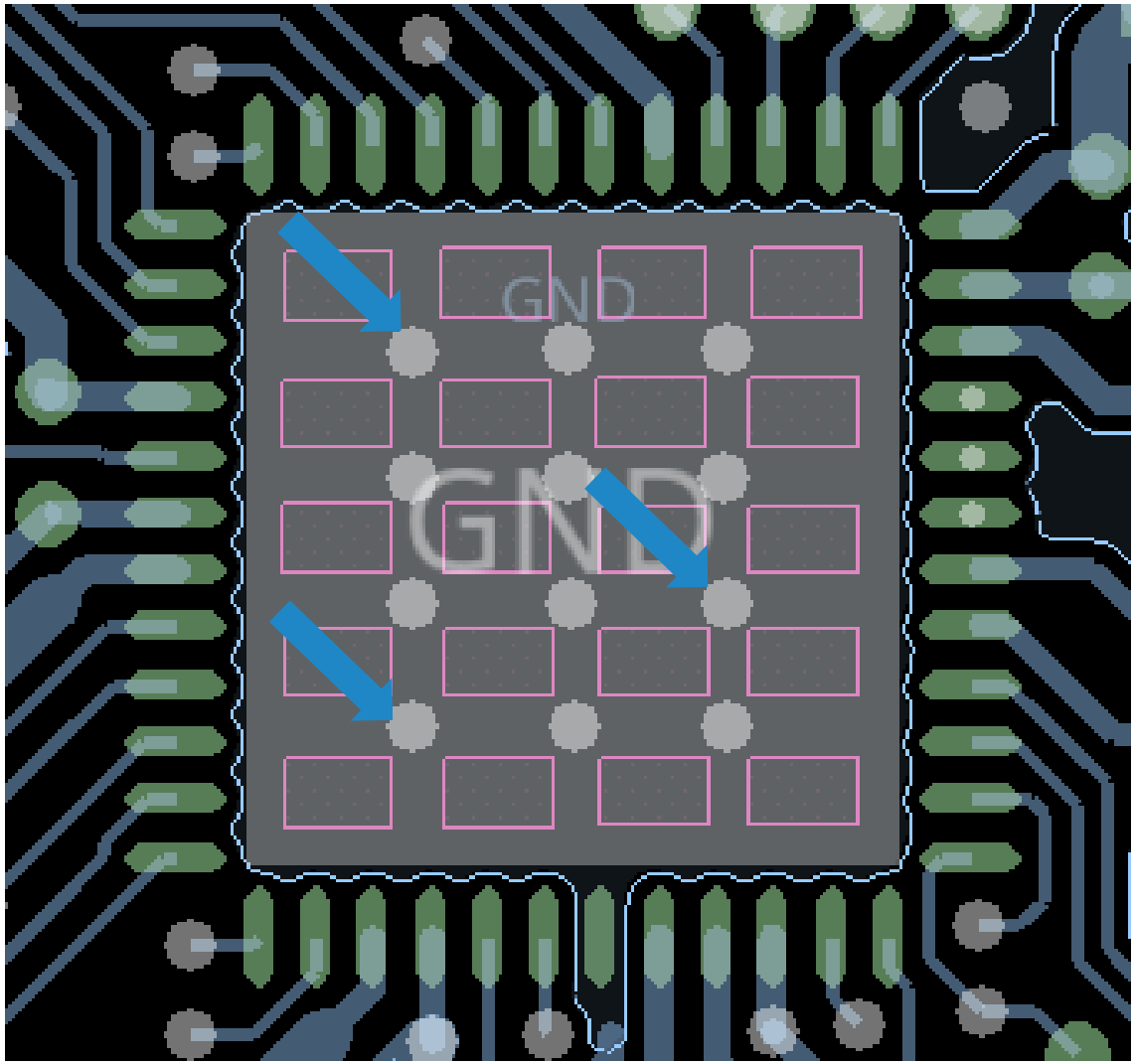
HW RECOMMENDATION – LAYOUT GENERAL RULES: VIAS

Add vias at the end of the ground area: 2 examples below:



HW RECOMMENDATION – LAYOUT GENERAL RULES: DIEPAD

Diepad & Vias connected to GND: Matrix of 4x5



EMC immunity option

SECURE CONNECTIONS
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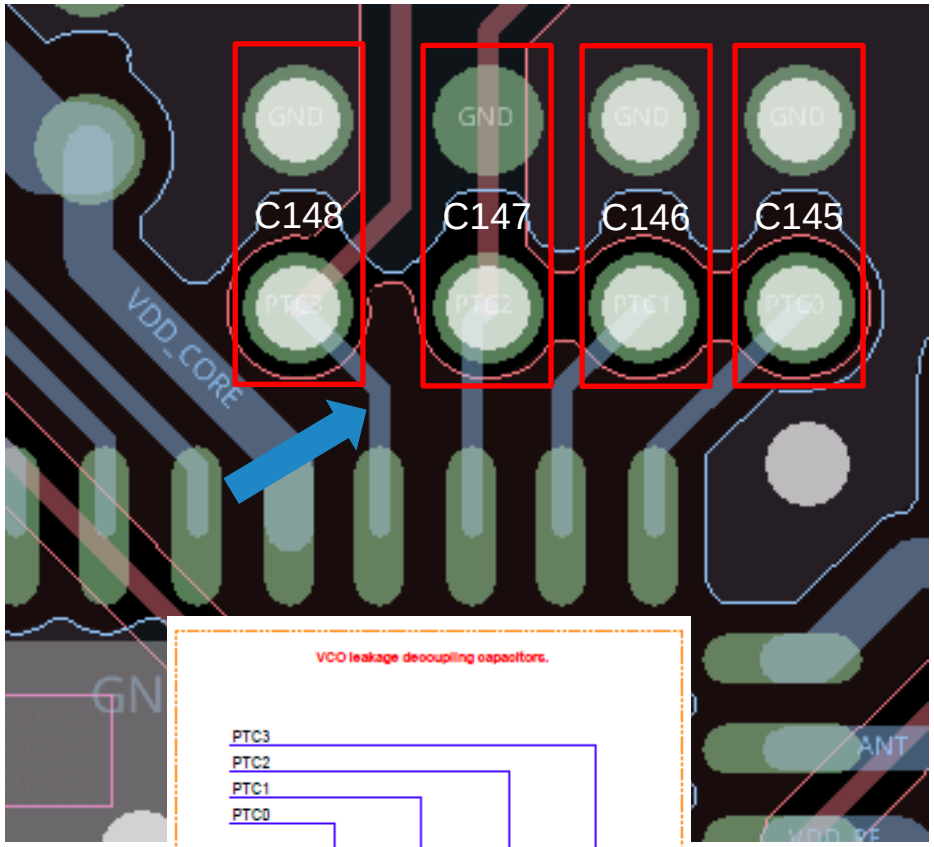
ONE WAY TO REDUCE VCO IMPACT (4.8GHZ) ON EMC

Possible way to avoid VCO noise on the PCB is to place a 3pF decoupling capacitor with resonance @4.8GHz on pins PTC0, PTC1, PTC2 & PTC3.

- Decoupling capacitor must be very closer to the pin.
- Wire must be as short as possible.
- No vias allowed



Recommendation:
Add footprint in case of in your design

CISPR25

SECURE CONNECTIONS
FOR A SMARTER WORLD

CISPR25 AUTOMOTIVE CHINESE CERTIFICATION

The KW45-EVK and K32W1-EVK could withstand the CISPR25 certification.

To pass this certification for +10dBm Tx output power, the EVK board needs to be modified as follow:

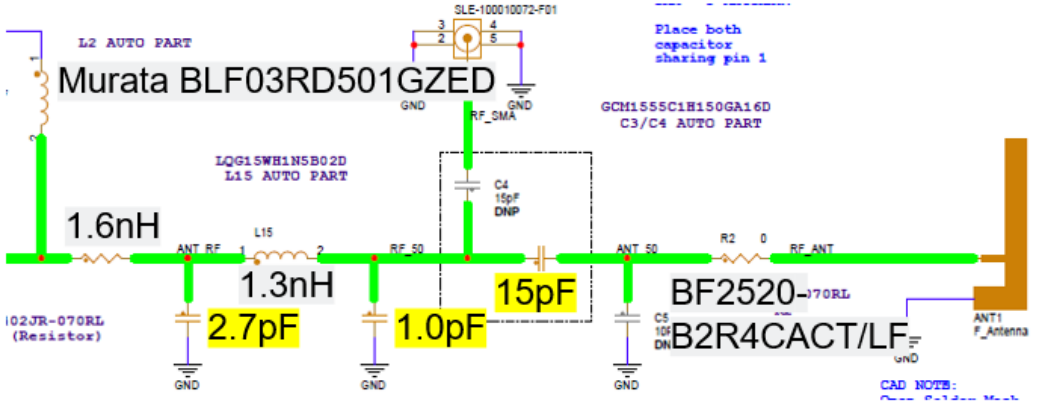
Table 8 (continue)

RF Service [User band in MHz]	Frequency [MHz]	RBW (kHz)	Limits [dBuV/m]		
			Peak	Average	Quasi- Peak
Bluetooth	2400 - 2690	120	44	24	N/A
5G	3000 - 5000	≥1000	64	44	N/A
GNSS	5010 – 5030	9/10	N/A	16	N/A
WLAN	5000 - 6000	≥1000	68	48	N/A
[1)] If test method, RE02, has been performed, these bands may be omitted.					

- Replace the RF matching component values

nH	nH	pF	nH	pF	pF
L2	L3	C1	L15	C2	C3
BLF03RD501GZED	1.6	2.7	1.3	1.1	15

- Replace R2 by a Band Pass Filter at R2. Reference BF2520-B2R4CACT/LF



Note: The default EVK board pass the certification with Tx output power at -15dBm.

Jumper configuration on KW45/K32W1-EVK

SECURE CONNECTIONS
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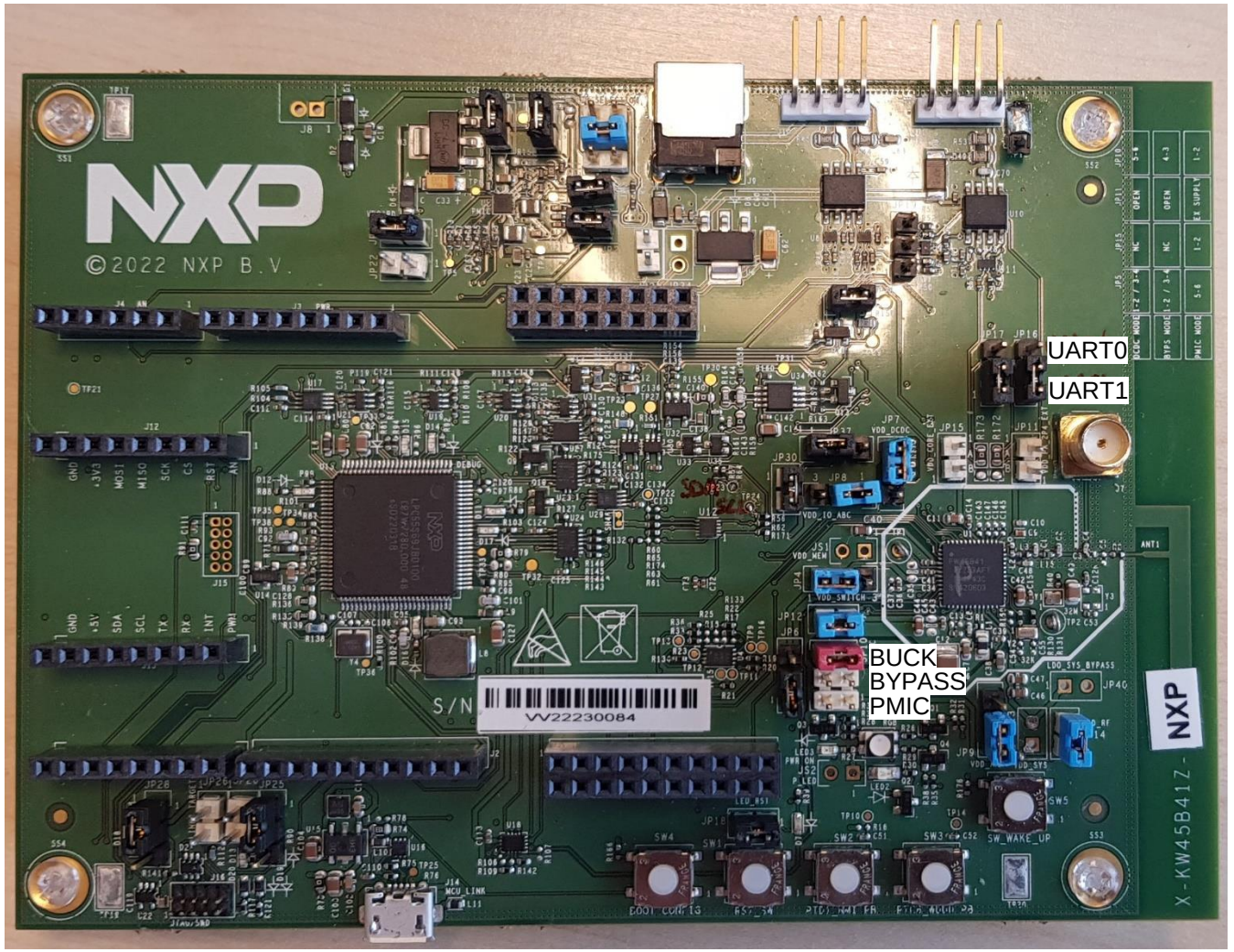
GENERAL INFORMATION - JUMPER CONFIGURATION

- DCDC modes (red jumper)
- Current consumption header (blue jumpers)



SECURE CONNECTIONS
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