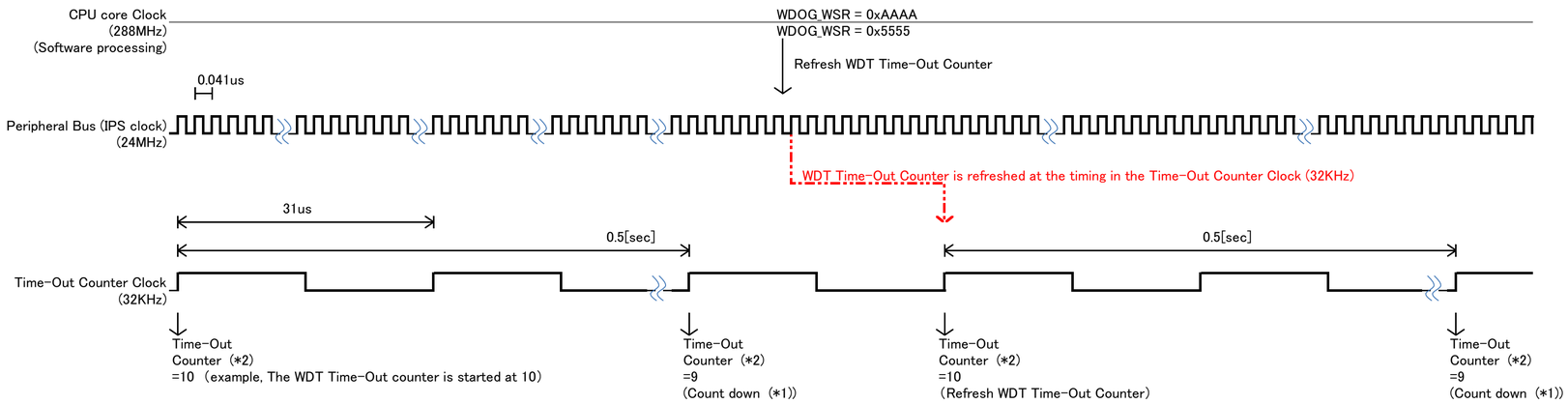
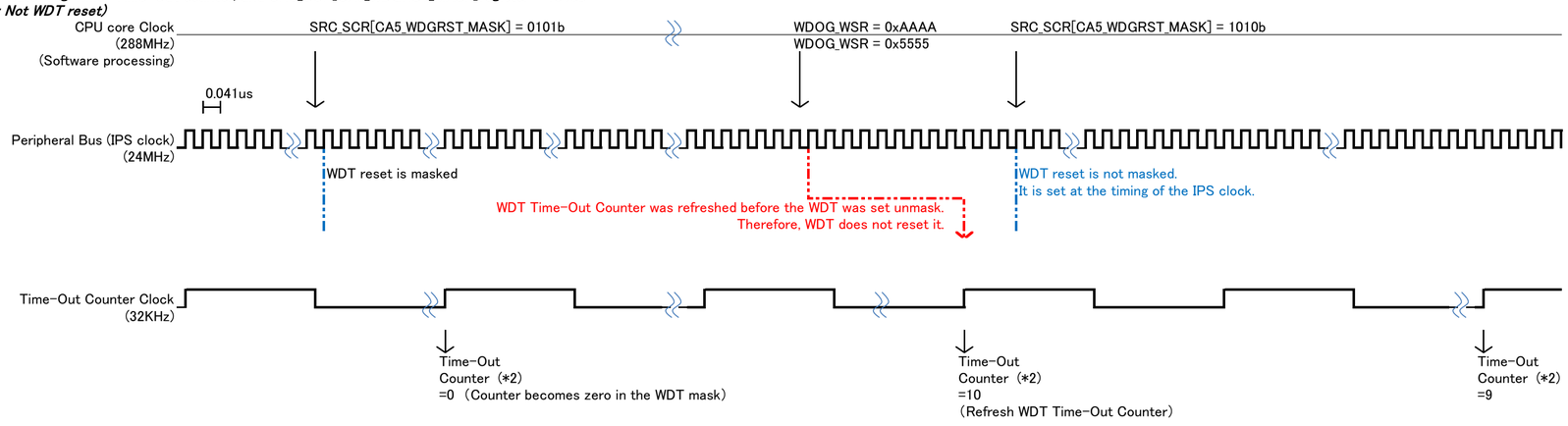
Watchdog Timer Time-Out Couter

Note in Figure
***1 The WDT Time-Out Counter assumes it countdown in a figure.**
***2 When the clock is an edge(Low -> High), the WDT Time-Out Counter is set**

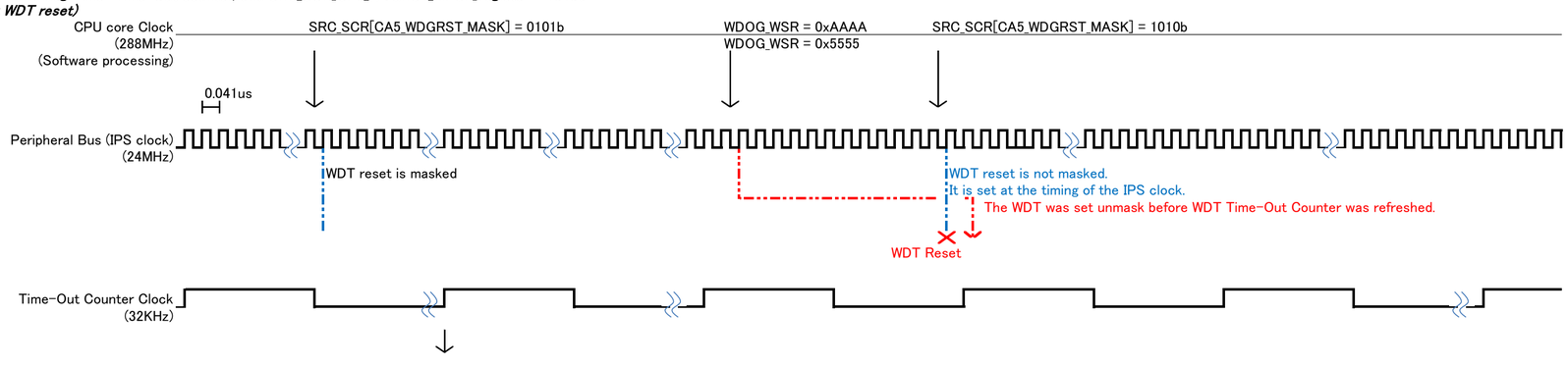
1. Refresh Watchdog Timer Time-Out counter in a CPU active state



2. Refresh Watchdog Timer Time-Out counter, and SRC_SCR[CA5_WDGRST_MASK]register = 1010b
(case1: Not WDT reset)



2. Refresh Watchdog Timer Time-Out counter, and SRC_SCR[CA5_WDGRST_MASK]register = 1010b
(case2: WDT reset)



Time-Out
Counter （*2）
=0 （Counter becomes zero in the WDT mask）