Errata Description:

Due to an issue in the boundary scan logic, the outputs remain in High Impedance state when driven by an EXTEST instruction during JATG operation. The problem is that the drive strength is set to 0 when in JTAG mode and this overrides the output-enable that is driven by the JTAG data.

Errata Workaround:

There are two workarounds.
1. Use the CLAMP instruction after the EXTEST instruction to enable the outputs after the scan registers are loaded by EXTEST. This method has the disadvantage that the outputs return to high-impedance state when the next EXTEST instruction is executed and therefore this cannot be used to program external memories or perform tests that rely on the state of the previous EXTEST.
The sequence for this work around is as flows:
− JTAG reset (TLR state).
− Verify IDCODE and flush test for boundary scan register.
− Enter EXTEST mode through programming of IR register.
− Program BSR chain for configuring the pads as outputs, and driving “1”s or “0”s from the device to the external world. This is done in “ShiftDR” state.
− Update-DR. Now the pads are set in output state and drive required value.
− Move to “CLAMP” by reprogramming the IR register.
Outputs are now driven but will revert to high-impedance state when the next EXTEST instruction is executed
− Return to “EXTEST” state for further testing. NOTE: This disables the outputs again

2. The second method is to set the drive strength prior to the JTAG operation and prevent this setting from being cleared until all tests are completed. This includes the following requirements:
− The device must not use the security features. Please refer to the security documentation for details if your device has security features enabled.
− A short header for pre-programming the PADs is to be included before EXTEST operation.
− RESETB pin has to be kept asserted {low} throughout the sequence.
− If JTAG TLR is issued anytime during memory interface programming, the header must be executed again.
− The system has to be power-cycled at the end of the boundary scan tests to restore the registers to their default state.
Work-around sequence:
• Assert RESETB=0.
• JTAG reset (TLR state).
• Verify IDCODE and flush test for boundary scan register.
• Include header for pre-programming. (see below)
• Enter EXTEST mode through programming of IR register.

• Program BSR chain for configuring the pads as outputs, and driving “1”s or “0”s from the device to the external world. This is done in “ShiftDR” state.
• Update-DR. Now the pads are set in output state and drive required value.
• → Outputs are now driven and will remain driven even when the next EXTEST is executed.
• Return to “EXTEST” state for further testing.
• Power-cycle the system to clear the registers that were pre-programmed by the header.

Header for pre-programming
JTAG-IR: "1001"
JTAG-IR: "10111“
JTAG-DR: "00000010010001101000101011001110"
JTAG-IR: "10111”
JTAG-DR: "00010011010101111001101111011111"
JTAG-IR: "11000“
JTAG-DR:
"10000000000000000000000000000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000001000000000000000000000001110001001000
010000000000000000000000000000000000000000000000000000000000000000000000000000
000000000000000000"
JTAG-IR: "10010"
JTAG-DR:
"11000000000000000000000000000000000000000000000000000000000000000000000000000
000000000000000000000000000000000000000110000000000000000000000000000001000000
000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000“
JTAG-IR: "11001“, traverse through “pause-dr” state for this step.
JTAG-DR:
"10000000000000000000000000000000000000000000000000000000000000000000000000000
00000000000000000000000000000000000000000000000000000000000000