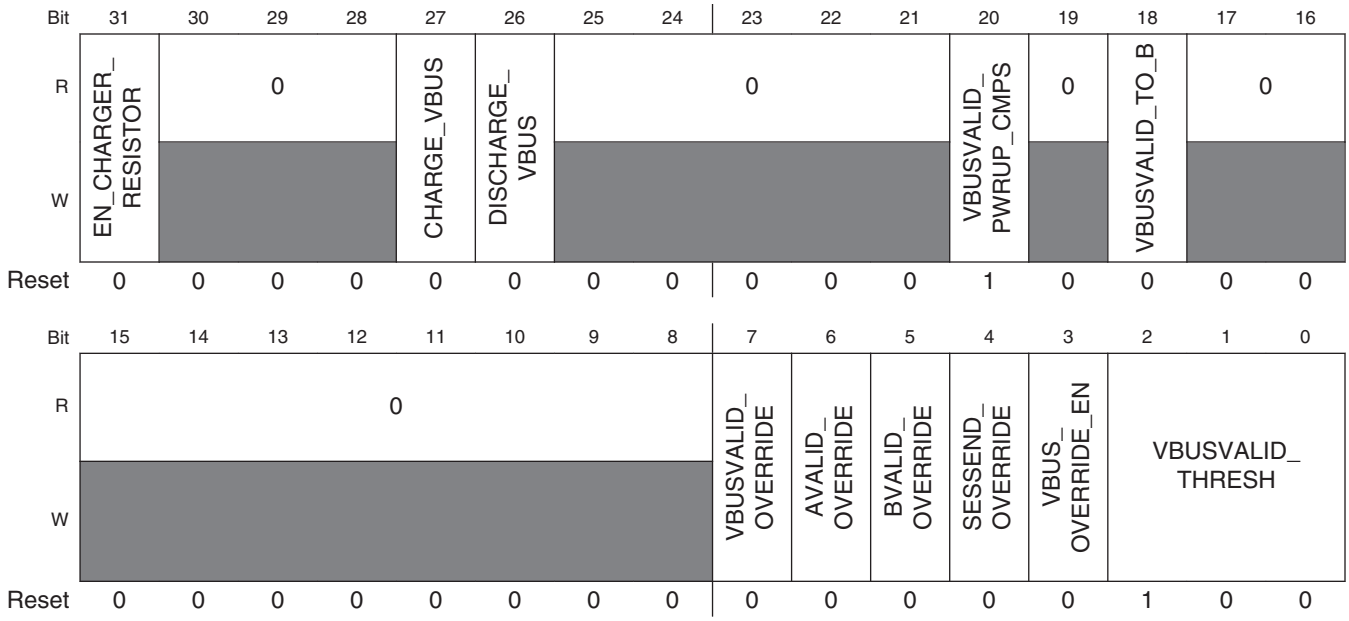
45.3.1 USB0 V_{BUS} Detect control register (USB_ANALOG_USB0_VBUS_DETECT)

This register defines the control bits for V_{BUS} detector of USB0.

Address: 4005_0000h base + 1A0h offset = 4005_01A0h



USB_ANALOG_USB0_VBUS_DETECT field descriptions

Field	Description
31 EN_CHARGER_RESISTOR	Enable 125k pullup on USB_DP and 375k on USB_DM to provide USB_CHARGER functionality for USB. This functionality is a legacy feature held over from USB Battery Charging Specification Revision 1.0 and is incompatible with either the plugged-in detector or Battery Charging Specification Revision 1.2. 0 125k pullup on USB_DP and 375k on USB_DM to provide USB_CHARGER functionality for USB is not enabled 1 Enable 125k pullup on USB_DP and 375k on USB_DM to provide USB_CHARGER functionality for USB
30–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 CHARGE_VBUS	USB OTG charge V_{BUS}. 0 Charging of the V_{BUS} is not enabled 1 Enable charging of the V_{BUS}
26 DISCHARGE_VBUS	USB OTG discharge V_{BUS}. 0 Discharging of the V_{BUS} is not enabled 1 Enable discharging of the V_{BUS}

Table continues on the next page...

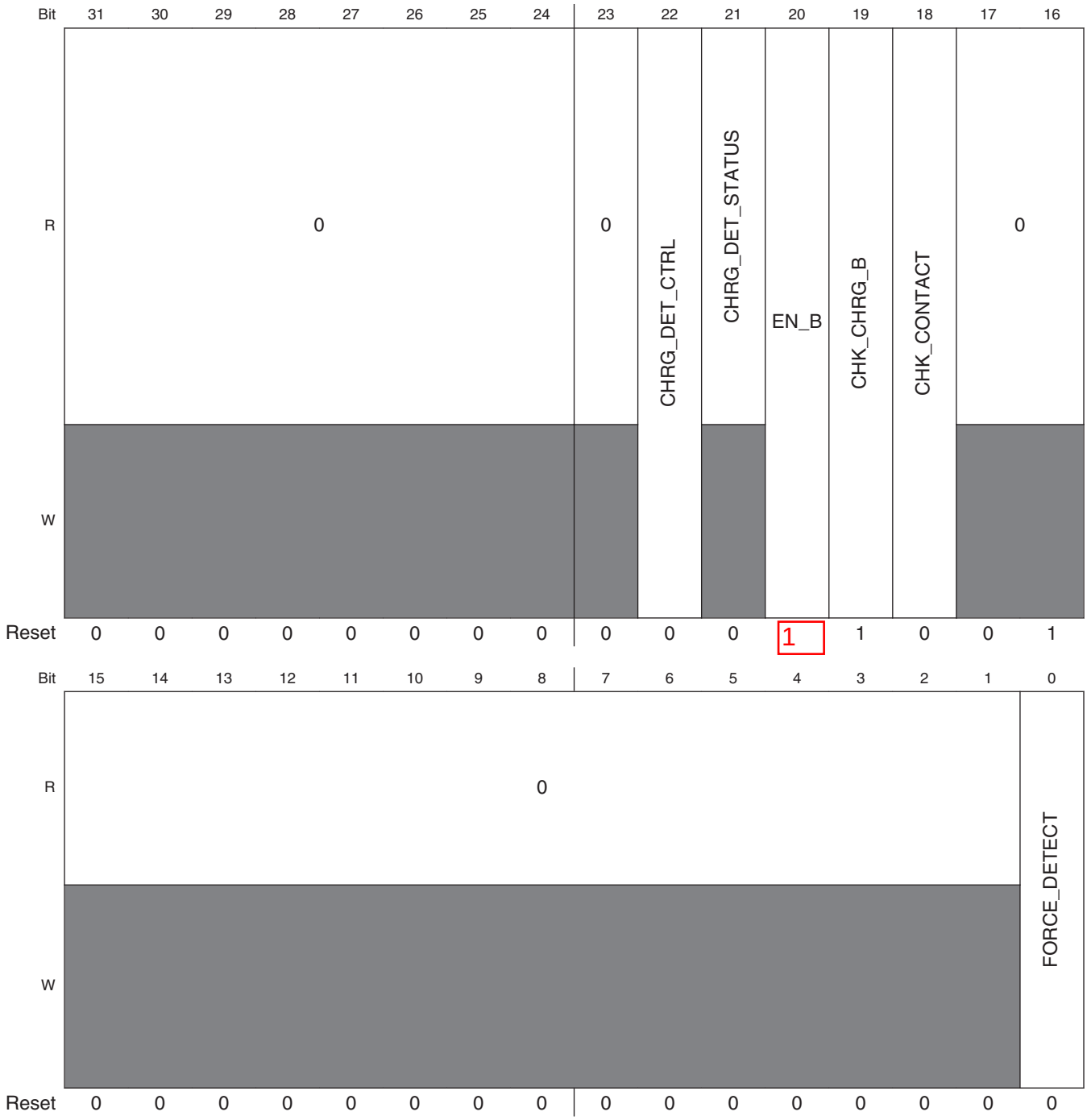
USB_ANALOG_USB0_VBUS_DETECT field descriptions (continued)

Field	Description
25–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 VBUSVALID_ PWRUP_CMPS	Powers up comparators for V_{BUS}_valid detector. 0 Powering up comparators for V_{BUS}_valid detector is not enabled 1 Enable powering up comparators for V_{BUS}_valid detector.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 VBUSVALID_ TO_B	This bit muxes the Bvalid comparator to the VBUSVALID comparator and is used for test purposes only. 0 Multiplexing of the Bvalid comparator to the VBUSVALID comparator is not enabled 1 Enable multiplexing of the Bvalid comparator to the VBUSVALID comparator
17–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 VBUSVALID_ OVERRIDE	Override value for the VBUSVALID hardware signal. 0 Value for the VBUSVALID hardware signal is not overrided 1 Override value for the VBUSVALID hardware signal.
6 AVALID_ OVERRIDE	Override value for the AVALID hardware signal. 0 AVALID hardware signal is not overrided 1 Override value for the AVALID hardware signal
5 BVALID_ OVERRIDE	Override value for the BVALID hardware signal. 0 BVALID hardware signal is not overrided 1 Override value for the BVALID hardware signal
4 SESSEND_ OVERRIDE	Override value for the SESSEND hardware signal. 0 SESSEND hardware signal is not overrided 1 Override value for the SESSEND hardware signal
3 VBUS_ OVERRIDE_EN	Enable the override of the VBUSVALID, AVALID, BVALID, and SESSEND signals from the USB OTG PHY with override register bit values. 0 Use hardware generated values 1 Use the software controlled values.
2–0 VBUSVALID_ THRESH	Set the threshold for the VBUSVALID comparator. This comparator is the most accurate method to determine the presence of 5v, and includes hystersis to minimize the need for software debounce of the detection. This comparator has ~50mV of hystersis to prevent chattering at the comparator trip point. 000 4.0 V 001 4.1 V 010 4.2 V 011 4.3 V 100 4.4 V (default) 101 4.5 V 110 4.6 V 111 4.7 V

45.3.2 USB0 Charger Detect control register (USB_ANALOG_USB0_CHRG_DETECT)

This register defines the control bits for the USB charger detector of USB0.

Address: 4005_0000h base + 1B0h offset = 4005_01B0h



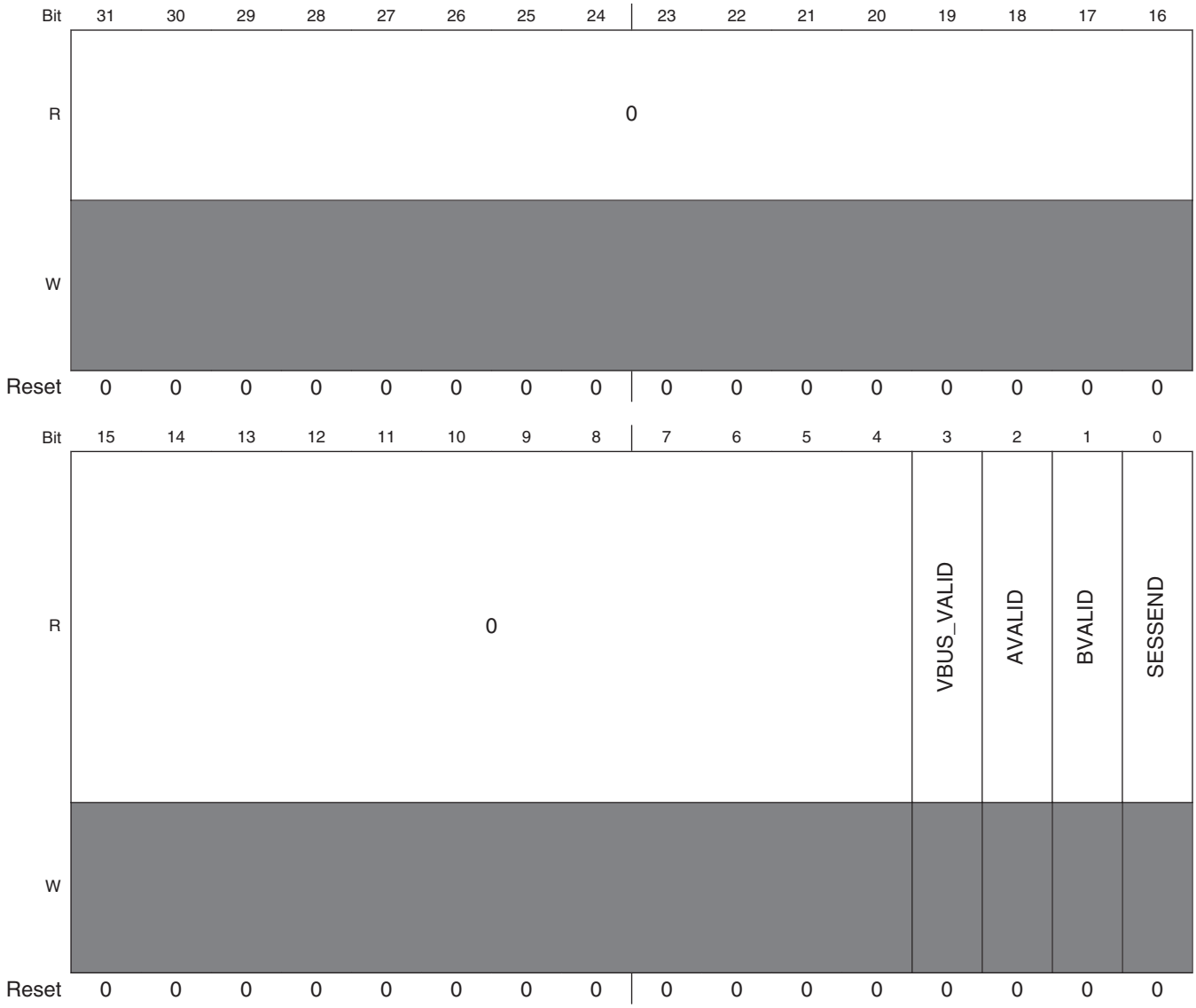
USB_ANALOG_USB0_CHRG_DETECT field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 CHRG_DET_ CTRL	Forces internal USB charging circuitery to enable basic USB battery charging v1.1 device charger detection functionality. 0 USB battery charging v1.1 device charger detection functionality is not enabled 1 Enable basic USB battery charging v1.1 device charger detection functionality
21 CHRG_DET_ STATUS	Status of internal charge detection. 0 Charger not detected. 1 Charger detected.
20 EN_B	This bit enables the charger detector. 0 Enable the charger detector. 1 Disable the charger detector.
19 CHK_CHRG_B	This bit checks whether a charger (either a dedicated charger or a host charger) is connected to USB port. 0 Check whether a charger (either a dedicated charger or a host charger) is connected to USB port. 1 Do not check whether a charger is connected to the USB port.
18 CHK_CONTACT	This bit checks whether the USB plug has been in contact with each other. 0 Do not check the contact of USB plug. 1 Check whether the USB plug has been in contact with each other.
17–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 FORCE_ DETECT	Set this bit to 1 to force the charger detector circuit to signal the presence of a charger. 0 The charger detector circuit is not forced to signal the presence of a charger. 1 Force the charger detector circuit to signal the presence of a charger.

45.3.3 USB0 V_{BUS} Detect Status definition register (USB_ANALOG_USB0_VBUS_DETECT_STATUS)

This register defines the status bits of the V_{BUS} detectors of USB1.

Address: 4005_0000h base + 1C0h offset = 4005_01C0h



USB_ANALOG_USB0_VBUS_DETECT_STATUS field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

USB_ANALOG_USB0_VBUS_DETECT_STATUS field descriptions (continued)

Field	Description
3 VBUS_VALID	V_{BUS} valid for USB OTG. This bit is a read only version of the state of the analog signal. It cannot be overwritten by software. 0 V_{BUS} not valid for USB OTG 1 V_{BUS} valid for USB OTG
2 AVALID	Indicates V_{BUS} is valid for a A-peripheral. This bit is a read only version of the state of the analog signal. It cannot be overritten by software. 0 V_{BUS} is not valid for a A-peripheral 1 V_{BUS} is valid for a A-peripheral
1 BVALID	V_{BUS} valid for USB B-session. This bit is a read only version of the state of the analog signal. It cannot be overwritten by software. 0 V_{BUS} is not valid for USB B-session 1 V_{BUS} valid for USB B-session
0 SESSEND	Session end for USB OTG. This bit is a read only version of the state of the analog signal. It cannot be overwritten by software like the SESSEND bit below. Note: This bit's default value depends on whether VDD5V is present. 0 VDD5V is present. 1 VDD5V is not present.

45.3.4 USB0 Charger Detect Status definition register (USB_ANALOG_USB0_CHRG_DETECT_STATUS)

This register defines the status bits for the USB charger detector of USB1.

Address: 4005_0000h base + 1D0h offset = 4005_01D0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												DP_STATE	DM_STATE	CHRG_DETECTED	PLUG_CONTACT
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

USB_ANALOG_USB0_CHRG_DETECT_STATUS field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 DP_STATE	DP line state output of the charger detector.
2 DM_STATE	DM line state output of the charger detector.
1 CHRG_ DETECTED	This bit is a read only version of the state of the analog signal. 0 The USB port is not connected to a charger. 1 A charger (either a dedicated charger or a host charger) is connected to the USB port.
0 PLUG_ CONTACT	This bit shows the contact status of the USB plug. 0 The USB plug has not been contacted. 1 The USB plug has made good contact.

45.3.5 USB0 Loopback register (USB_ANALOG_USB0_LOOPBACK)

This register defines the status bits for the USB charger detector.

Address: 4005_0000h base + 1E0h offset = 4005_01E0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							UTMO_DIG_TST1	UTMO_DIG_TST0	TSTI_TX_HIZ	TSTI_TX_EN	TSTI_TX_LS_MODE	TSTI_TX_HS_MODE	UTMI_DIG_TST1	UTMI_DIG_TST0	UTMI_TESTSTART
W																
Reset	0	0	0	0	0	0	0	x*	x*	0	0	0	0	0	0	0

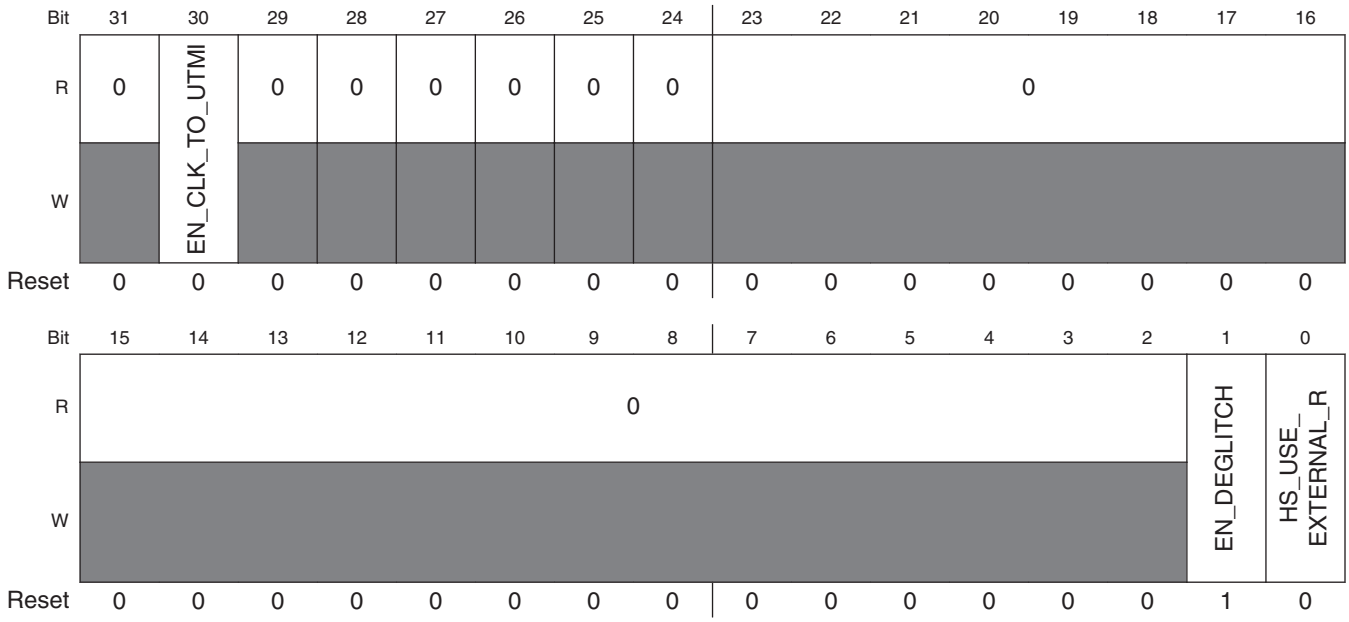
* Notes:
- x = Undefined at reset.

USB_ANALOG_USB0_LOOPBACK field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 UTMO_DIG_ TST1	This read-only bit is a status bit for USB0 Loopback. 0 Pass 1 Not pass
7 UTMO_DIG_ TST0	This read-only bit is a status bit for USB0 Loopback. 0 Not pass 1 Pass
6 TSTI_TX_HIZ	Makes TX HIZ for USB0. 0 TX is not HIZ for USB0. 1 Make TX HIZ for USB0.
5 TSTI_TX_EN	Enables TX for USB0. 0 TX for USB0 is not enabled. 1 Enable TX for USB0.
4 TSTI_TX_LS_ MODE	Chooses LS mode for USB0. 0 Choose HS or FS mode which is defined by TSTI1_TX_HS. 1 Choose LS for USB0.
3 TSTI_TX_HS_ MODE	Chooses HS or FS mode for USB0. 0 USB0 FS mode. 1 USB0 HS mode.
2 UTMI_DIG_TST1	Test 1 loopback mode for USB0. 0 USB0 loopback test 1 is not enabled. 1 Enable USB0 loopback test 1.
1 UTMI_DIG_TST0	Test 0 loopback mode for USB0. 0 USB0 loopback test 0 is not enabled. 1 Enable USB0 loopback test 0.
0 UTMI_ TESTSTART	Enables the USB0 loopback test. 0 USB0 loopback test is not enabled. 1 Enable USB0 loopback test.

45.3.6 USB0 Miscellaneous definition register (USB_ANALOG_USB0_MISC)

Address: 4005_0000h base + 1F0h offset = 4005_01F0h



USB_ANALOG_USB0_MISC field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 EN_CLK_TO_UTMI	Enables the clk to the UTMI block.
29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 EN_DEGLITCH	Enables the deglitching circuit of the USB PLL output.

Table continues on the next page...

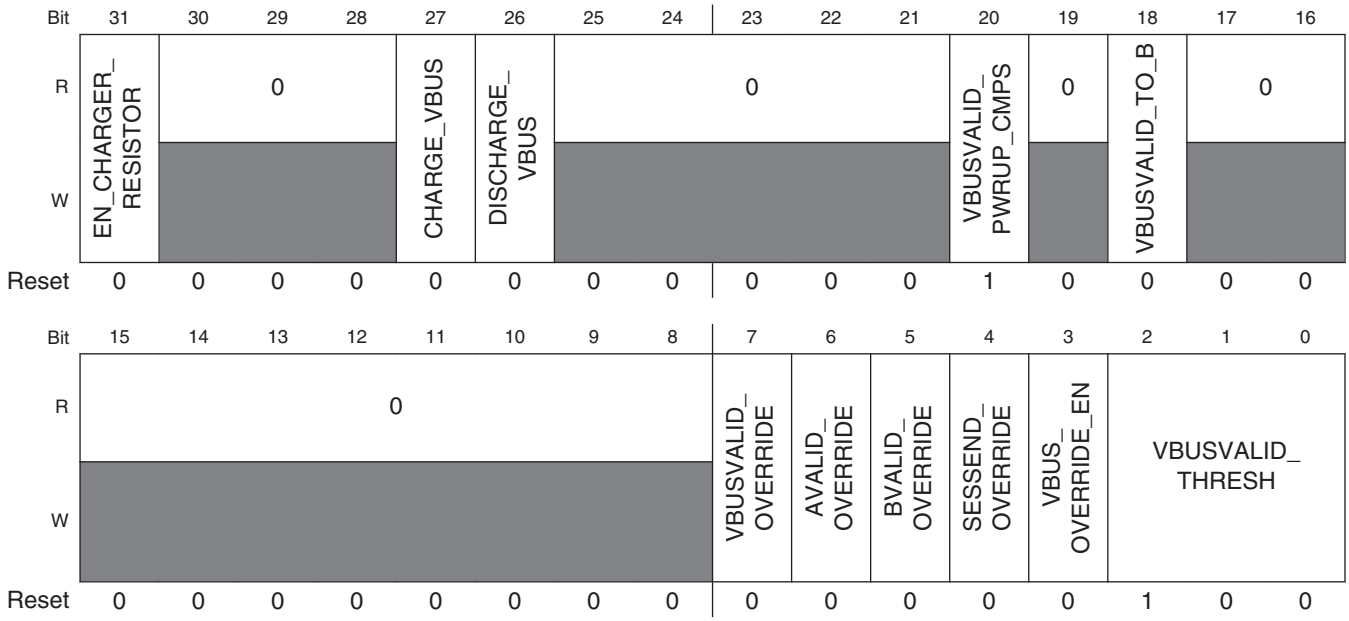
USB_ANALOG_USB0_MISC field descriptions (continued)

Field	Description
0 HS_USE_ EXTERNAL_R	Use external resistor to generate the current bias for the high speed transmitter. This bit should not be changed unless recommended by Freescale.

45.3.7 USB1 V_{BUS} Detect control register (USB_ANALOG_USB1_VBUS_DETECT)

This register defines the control bits for V_{BUS} detector of USB1.

Address: 4005_0000h base + 200h offset = 4005_0200h



USB_ANALOG_USB1_VBUS_DETECT field descriptions

Field	Description
31 EN_CHARGER_ RESISTOR	Enable 125k pullup on USB_DP and 375k on USB_DM to provide USB_CHARGER functionality for USB. This functionality is a legacy feature held over from USB Battery Charging Specification Revision 1.0 and is incompatible with either the plugged-in detector or Battery Charging Specification Revision 1.2. 0 125k pullup on USB_DP and 375k on USB_DM to provide USB_CHARGER functionality for USB is not enabled 1 Enable 125k pullup on USB_DP and 375k on USB_DM to provide USB_CHARGER functionality for USB
30–28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

USB_ANALOG_USB1_VBUS_DETECT field descriptions (continued)

Field	Description
27 CHARGE_VBUS	USB OTG charge V_{BUS}. 0 Charging of the V_{BUS} is not enabled 1 Enable charging of the V_{BUS}
26 DISCHARGE_ VBUS	USB OTG discharge V_{BUS}. 0 Discharging of the V_{BUS} is not enabled 1 Enable discharging of the V_{BUS}
25–21 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
20 VBUSVALID_ PWRUP_CMPS	Powers up comparators for V_{BUS}_valid detector. 0 Powering up comparators for V_{BUS}_valid detector is not enabled 1 Enable powering up comparators for V_{BUS}_valid detector.
19 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
18 VBUSVALID_ TO_B	This bit muxes the Bvalid comparator to the VBUSVALID comparator and is used for test purposes only. 0 Multiplexing of the Bvalid comparator to the VBUSVALID comparator is not enabled 1 Enable multiplexing of the Bvalid comparator to the VBUSVALID comparator
17–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
7 VBUSVALID_ OVERRIDE	Override value for the VBUSVALID hardware signal. 0 Value for the VBUSVALID hardware signal is not overrided 1 Override value for the VBUSVALID hardware signal.
6 AVALID_ OVERRIDE	Override value for the AVALID hardware signal. 0 AVALID hardware signal is not overrided 1 Override value for the AVALID hardware signal
5 BVALID_ OVERRIDE	Override value for the BVALID hardware signal. 0 BVALID hardware signal is not overrided 1 Override value for the BVALID hardware signal
4 SESSEND_ OVERRIDE	Override value for the SESSEND hardware signal. 0 SESSEND hardware signal is not overrided 1 Override value for the SESSEND hardware signal
3 VBUS_ OVERRIDE_EN	Enable the override of the VBUSVALID, AVALID, BVALID, and SESSEND signals from the USB OTG PHY with override register bit values. 0 Use hardware generated values 1 Use the software controlled values.
2–0 VBUSVALID_ THRESH	Set the threshold for the VBUSVALID comparator. This comparator is the most accurate method to determine the presence of 5v, and includes hystersis to minimize the need for software debounce of the detection. This comparator has ~50mV of hystersis to prevent chattering at the comparator trip point. 000 4.0 V 001 4.1 V

Table continues on the next page...

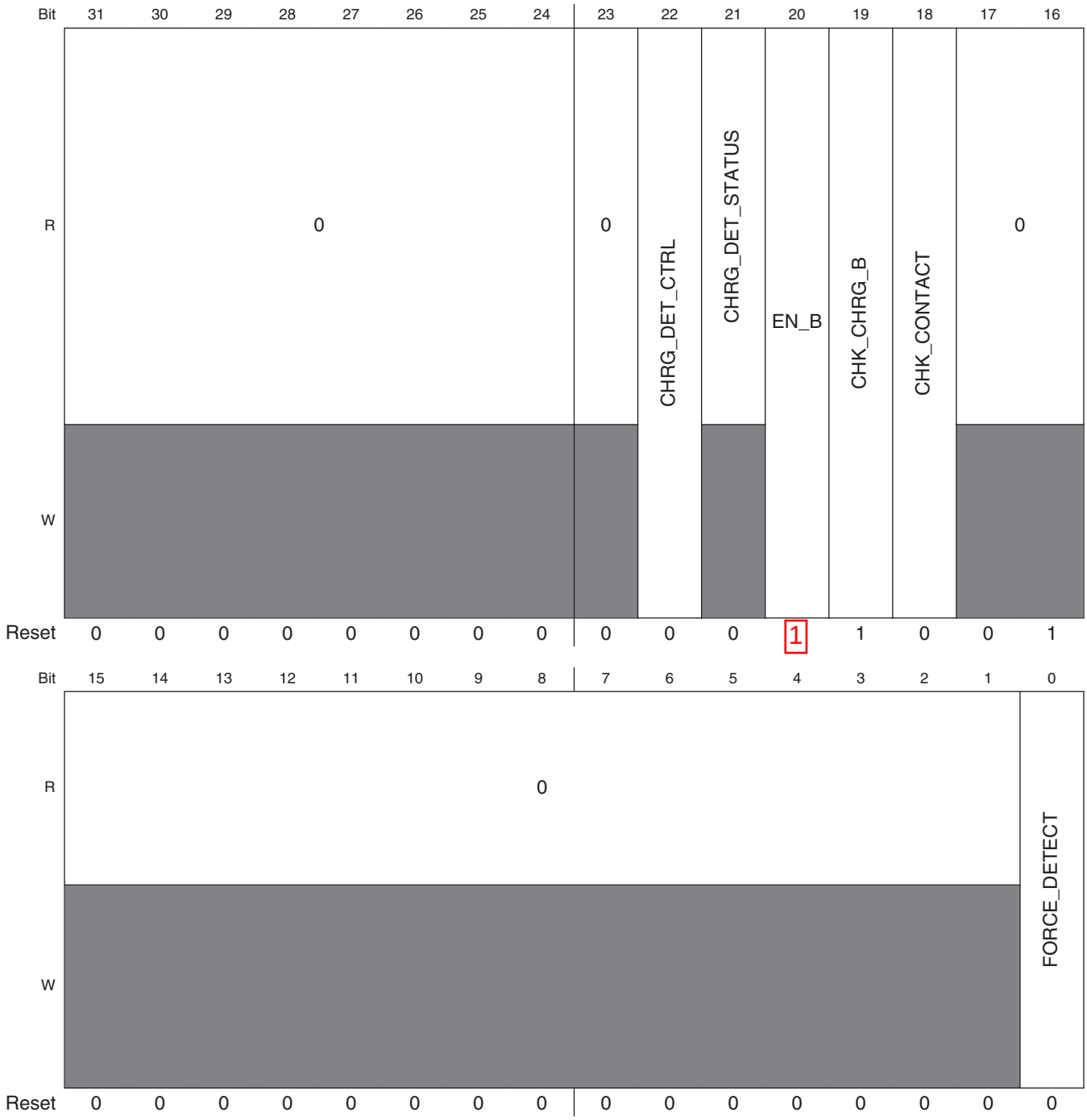
USB_ANALOG_USB1_VBUS_DETECT field descriptions (continued)

Field	Description
	010 4.2 V 011 4.3 V 100 4.4 V (default) 101 4.5 V 110 4.6 V 111 4.7 V

45.3.8 USB1 Charger Detect control register (USB_ANALOG_USB1_CHRG_DETECT)

This register defines the control bits for the USB charger detector of USB1.

Address: 4005_0000h base + 210h offset = 4005_0210h



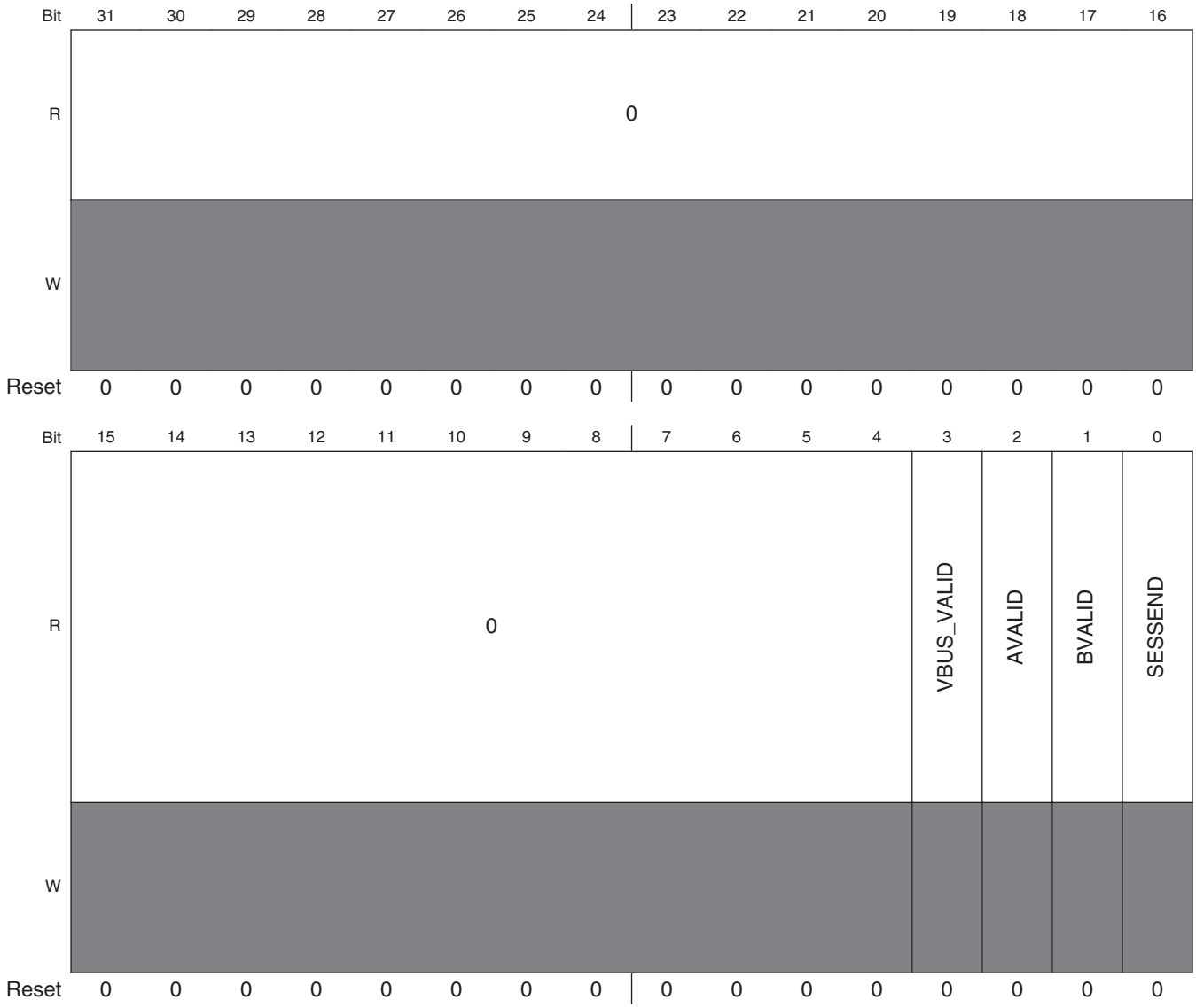
USB_ANALOG_USB1_CHRG_DETECT field descriptions

Field	Description
31–24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
22 CHRG_DET_ CTRL	Forces internal USB charging circuitery to enable basic USB battery charging v1.1 device charger detection functionality. 0 USB battery charging v1.1 device charger detection functionality is not enabled 1 Enable basic USB battery charging v1.1 device charger detection functionality
21 CHRG_DET_ STATUS	Status of internal charge detection. 0 Charger not detected. 1 Charger detected.
20 EN_B	This bit enables the charger detector. 0 Enable the charger detector. 1 Disable the charger detector.
19 CHK_CHRG_B	This bit checks whether a charger (either a dedicated charger or a host charger) is connected to USB port. 0 Check whether a charger (either a dedicated charger or a host charger) is connected to USB port. 1 Do not check whether a charger is connected to the USB port.
18 CHK_CONTACT	This bit checks whether the USB plug has been in contact with each other. 0 Do not check the contact of USB plug. 1 Check whether the USB plug has been in contact with each other.
17–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 FORCE_ DETECT	Set this bit to 1 to force the charger detector circuit to signal the presence of a charger. 0 The charger detector circuit is not forced to signal the presence of a charger. 1 Force the charger detector circuit to signal the presence of a charger.

45.3.9 USB1 V_{BUS} Detect STS definition register (USB_ANALOG_USB1_VBUS_DETECT_STATUS)

This register defines the status bits of the V_{BUS} detectors of USB1.

Address: 4005_0000h base + 220h offset = 4005_0220h



USB_ANALOG_USB1_VBUS_DETECT_STATUS field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

USB_ANALOG_USB1_VBUS_DETECT_STATUS field descriptions (continued)

Field	Description
3 VBUS_VALID	V_{BUS} valid for USB OTG. This bit is a read only version of the state of the analog signal. It cannot be overwritten by software. 0 V_{BUS} not valid for USB OTG 1 V_{BUS} valid for USB OTG
2 AVALID	Indicates V_{BUS} is valid for a A-peripheral. This bit is a read only version of the state of the analog signal. It cannot be overritten by software. 0 V_{BUS} is not valid for a A-peripheral 1 V_{BUS} is valid for a A-peripheral
1 BVALID	V_{BUS} valid for B-session. This bit is a read only version of the state of the analog signal. It cannot be overwritten by software. 0 V_{BUS} is not valid for USB B-session 1 V_{BUS} valid for USB B-session
0 SESSEND	Session end for USB OTG. This bit is a read only version of the state of the analog signal. It cannot be overwritten by software like the SESSEND bit below. Note: This bit's default value depends on whether VDD5V is present. 0 VDD5V is present. 1 VDD5V is not present.

45.3.10 USB1 Charger Detect Status definition register (USB_ANALOG_USB1_CHRG_DETECT_STATUS)

This register defines the status bits for the USB charger detector of USB1.

Address: 4005_0000h base + 230h offset = 4005_0230h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												DP_STATE	DM_STATE	CHRG_DETECTED	PLUG_CONTACT
W																
Reset	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

USB_ANALOG_USB1_CHRG_DETECT_STATUS field descriptions

Field	Description
31–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 DP_STATE	DP line state output of the charger detector.
2 DM_STATE	DM line state output of the charger detector.
1 CHRG_ DETECTED	This bit is a read only version of the state of the analog signal. 0 The USB port is not connected to a charger. 1 A charger (either a dedicated charger or a host charger) is connected to the USB port.
0 PLUG_ CONTACT	This bit shows the contact status of the USB plug. 0 The USB plug has not been contacted. 1 The USB plug has made good contact.

45.3.11 USB1 Loopback register (USB_ANALOG_USB1_LOOPBACK)

This register defines the status bits for the USB1 charger detector.

Address: 4005_0000h base + 240h offset = 4005_0240h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							UTM1_DIG_TST1	UTM1_DIG_TST0	TSTI_TX_HIZ	TSTI_TX_EN	TSTI_TX_LS_MODE	TSTI_TX_HS_MODE	UTMI_DIG_TST1	UTMI_DIG_TST0	UTMI_TESTSTART
W																
Reset	0	0	0	0	0	0	0	x*	x*	0	0	0	0	0	0	0

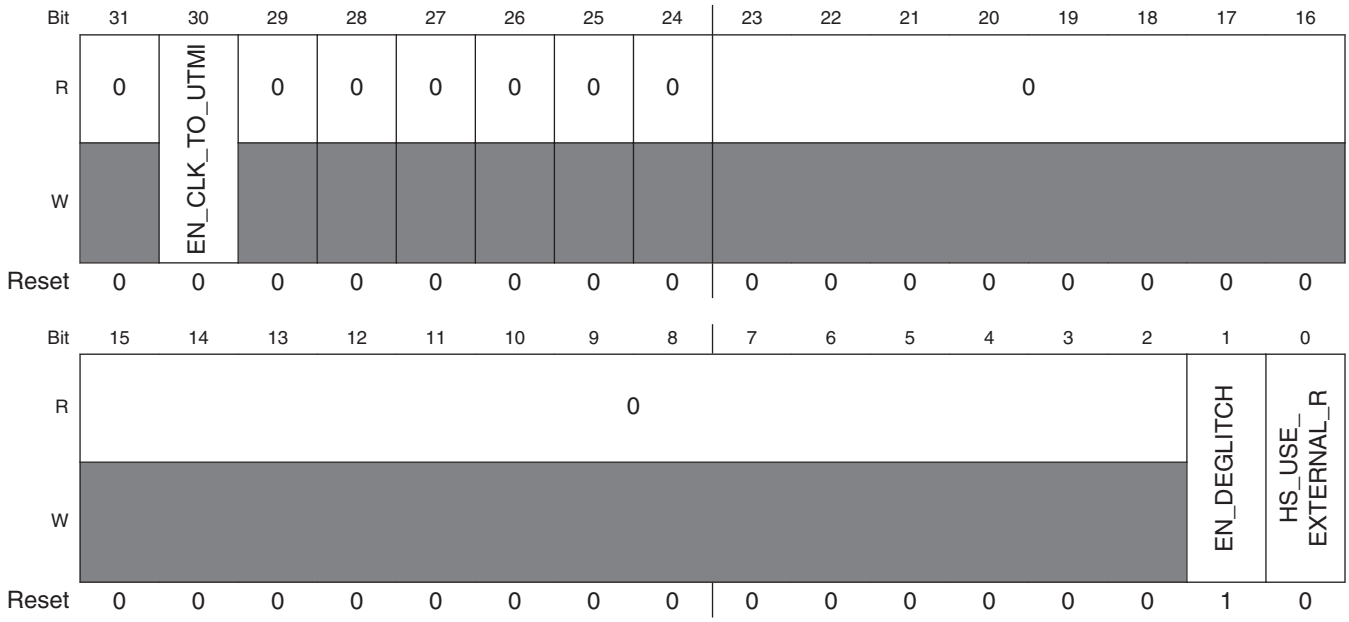
* Notes:
- x = Undefined at reset.

USB_ANALOG_USB1_LOOPBACK field descriptions

Field	Description
31–9 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
8 UTM1_DIG_ TST1	This read-only bit is a status bit for USB0 Loopback. 0 Pass 1 Not pass
7 UTM1_DIG_ TST0	This read-only bit is a status bit for USB1 Loopback. 0 Not pass 1 Pass
6 TSTI_TX_HIZ	Makes TX HIZ for USB1. 0 TX is not HIZ for USB1. 1 Make TX HIZ for USB1.
5 TSTI_TX_EN	Enables TX for USB1. 0 TX for USB1 is not enabled. 1 Enable TX for USB1.
4 TSTI_TX_LS_ MODE	Chooses LS mode for USB1. 0 Choose HS or FS mode which is defined by TSTI1_TX_HS. 1 Choose LS for USB1.
3 TSTI_TX_HS_ MODE	Chooses HS or FS mode for USB1. 0 USB1 FS mode. 1 USB1 HS mode.
2 UTMI_DIG_TST1	Test 1 loopback mode for USB1. 0 USB1 loopback test 1 is not enabled. 1 Enable USB1 loopback test 1.
1 UTMI_DIG_TST0	Test 0 loopback mode for USB1. 0 USB1 loopback test 0 is not enabled. 1 Enable USB1 loopback test 0.
0 UTMI_ TESTSTART	Enables the USB1 loopback test. 0 USB1 loopback test is not enabled. 1 Enable USB1 loopback test.

45.3.12 USB1 Miscellaneous definition register (USB_ANALOG_USB1_MISC)

Address: 4005_0000h base + 250h offset = 4005_0250h



USB_ANALOG_USB1_MISC field descriptions

Field	Description
31 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
30 EN_CLK_TO_UTMI	Enables the clk to the UTMI block.
29 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
28 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
27 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
26 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
25 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
24 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
23–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 EN_DEGLITCH	Enables the deglitching circuit of the USB PLL output.

Table continues on the next page...

USB_ANALOG_USB1_MISC field descriptions (continued)

Field	Description
0 HS_USE_ EXTERNAL_R	Use external resistor to generate the current bias for the high speed transmitter. This bit should not be changed unless recommended by Freescale.

45.4 Operation

The UTM provides a 16-bit interface to the USB controller. This interface is clocked at 30 MHz.

- The digital portions of the USBPHY block include the UTMI, digital transmitter, digital receiver, and the programmable registers.
- The analog transceiver section comprises an analog receiver and an analog transmitter, as shown in Figure 45-116.

45.4.1 UTMI

The UTMI block handles the line_state bits, reset buffering, suspend distribution, transceiver speed selection, and transceiver termination selection.

The PLL supplies a 120 MHz signal to all of the digital logic. The UTMI block does a final divide-by-four to develop the 30 MHz clock used in the interface.

45.4.2 Digital Transmitter

The digital transmitter receives the 16-bit transmit data from the USB controller and handles the tx_valid, tx_validh and tx_ready handshake.

In addition, it contains the transmit serializer that converts the 16-bit parallel words at 30 MHz to a single bitstream at 480 Mbit for high-speed or 12 Mbit for full-speed or 1.5 Mbit for low-speed. It does this while implementing the bit-stuffing algorithm and the NRZI encoder that are used to remove the DC component from the serial bitstream. The output of this encoder is sent to the low-speed (LS), full-speed (FS) or high-speed (HS) drivers in the analog transceiver section's transmitter block.