



DDR initialization tuning on Vybrid



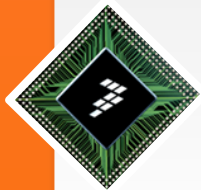
Confidential and Proprietary

Freescale, the Freescale logo, AllVec, C-5, CodeTEST, CodeWarrior, ColdFire, C-Ware, the Energy Efficient Solutions logo, mobileGT, PowerQUICC, QorIQ, StarCore and Symphony are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast, BeeKit, BeeStack, ColdFire+, CoreNet, Flexis, Kinetis, MagniV, MXC, Platform in a Package, Processor Expert, QorIQ Converge, Qorivva, QUICC Engine, Ready Play, SafeAssure, the SafeAssure logo, SMARTMOS, TurboLink, VortiQa and Xtrinsic are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © 2012 Freescale Semiconductor, Inc.



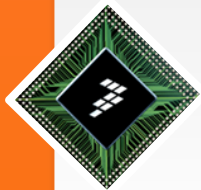
Why is tuning needed?

- Most of the DDR controller registers are configured using fixed values, but some values might need adjustment to actually work with your board.
- There are a number of DDR PHY registers that can be used to make adjustments to the timing of DDR signals to tailor the timing specifically to your board.
- These PHY settings can vary from design to design, so there isn't a way for a tool with no connection to the hardware to identify the correct parameters to use.



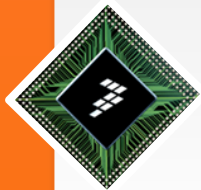
Read timing parameters

- The following registers contain parameters controlling read timing that might need tuning:
 - PHY_GATE_CTRL[RD_DL_SET]
 - PHY_GATE_CTRL[Gate_CFG]
 - PHY_GATE_CTRL[EN_HALF_CAS]
- All of these values are programmed into the DDRMC_PHY02, DDRMC_PHY18, and DDRMC_PHY34.
- If tuning these values doesn't result in a working configuration, then you might need a different setting for CR132[RDLAT_ADJ].



Write tuning parameters

- The following register contains a parameter controlling write timing that might need tuning:
 - PHY_SLAVE_CTRL[DLL_WRITE_DL] (in registers DDRMC_PHY04, DDRMC_PHY20, DDRMC_PHY36)
- If tuning DLL_WRITE_DL doesn't result in a working configuration, you might need to change CR132[WRLAT_ADJ]



Recommended Manual Tuning Procedure

1. Create a short memory test that runs in a loop that reports the number of failures vs. number of successes.
2. If you don't have any passing values using the starting values, then experiment with the write parameters until you get at least a few passes per loop.
3. Then move on to tuning read parameters. One parameter at a time increment and decrement that parameters value. The idea is to find the upper and lower limit for that parameter that give the best possible result (at this point you might still have failures).
4. After you determine the upper and lower limit for a given parameter, set that parameter to the middle value within those limits. Then move on to the next parameter.
5. After all read parameters have been centered, go back to the write parameter and find the center passing value for it (at this point you should reach a point where you don't see failures except at the limits of the write parameter).