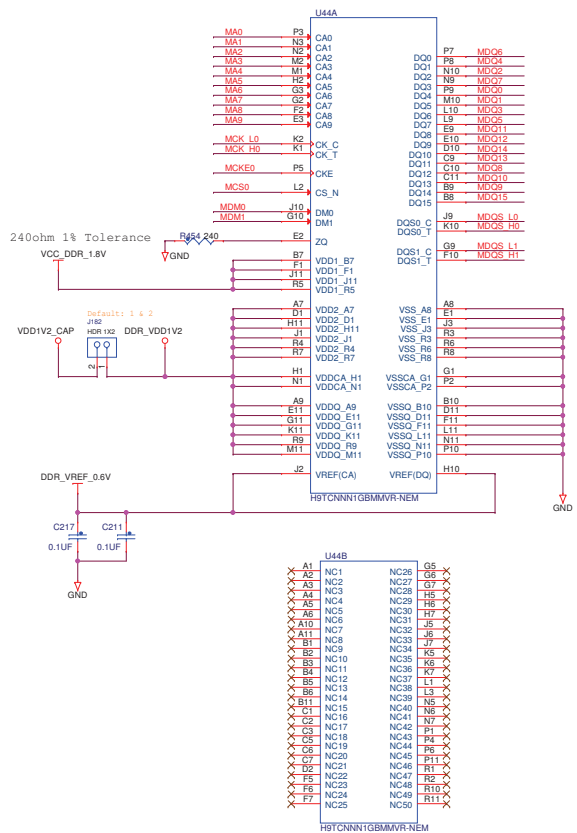
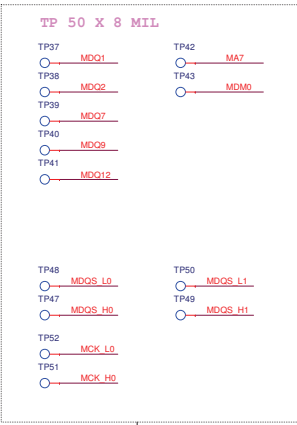


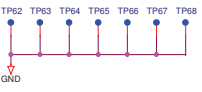
## LPDDR2 Interface



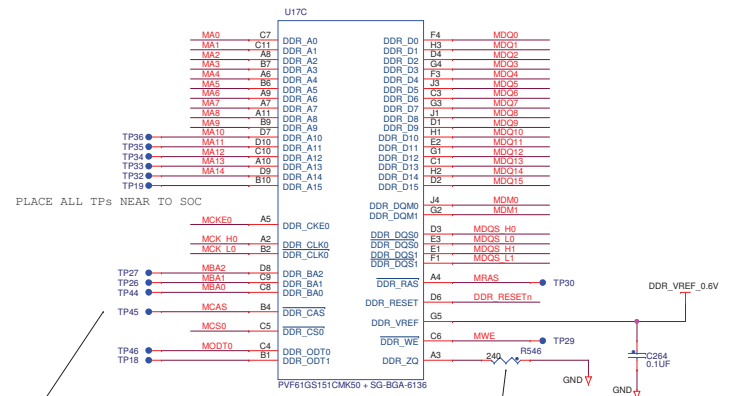
To be placed close to memory



To be placed close to the test points

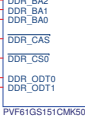
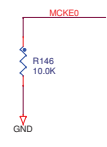


## LPDDR2 Interface ( FARADAY )



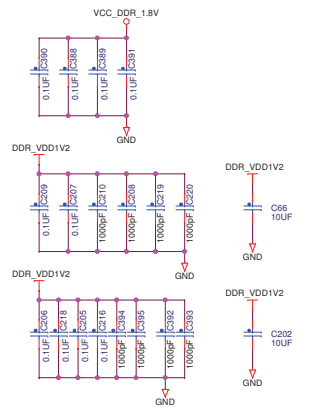
PLACE ALL TPs NEAR TO SOC

To be placed close to the test points

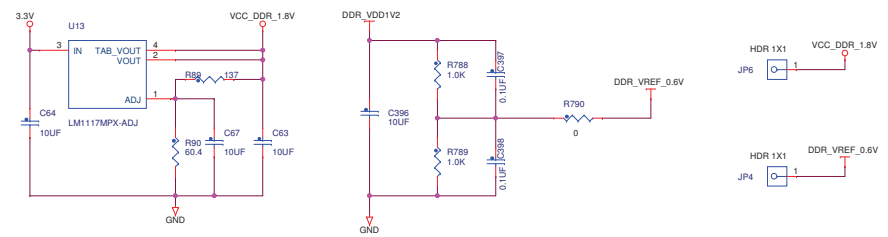


1% Tolerance

## LPDDR2 Memory Decoupling



## LPDDR2 REGULATOR



**freescale**  
semiconductor

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