Freescale AutoEVB-Board (Redboard S/N XC0069)
Using original MQX 4.0.2 BSP for AutoEVB and httpsrv-example

PTA6 (Clock_OUT) ——— 50MHz ———▶ Clock_IN

Clock_Out

Vybrid

PHY
LAN8720

RMII TXD[0:1] ——————▶ RMII TXD[0:1]
RMII RXD[0:1] ◀—————— RMII RXD[0:1]
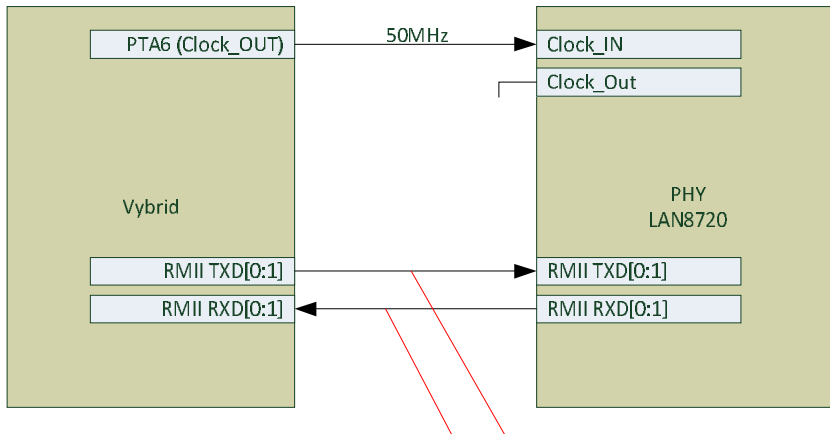
Does not working stable cause vybrid uses the wrong edge of the RMII-Clock to put data on his TX-lines.

Working fine

Measure 1 (see diagramm on next page):
Is done using a freescale AutoEVB-Board and the original MQX 4.0.2 with httpsrv-example.
Ethernet-Test : ping the AutoEVB-Board from a PC
Test-Result : ping works fine

Problem : signal-waveforms are not very good. Especially the RMII-Clock.
Cause : pad settings are not optimal (drive-strength)

Measure 2 (see diagramm on next page) :
Same source-code as used in measure 1 expectiong following pad-settings:
PTA6 (RMII-Clockout : changed drive strength from 125Ohm to 75Ohm an speed from 50MHz to 200MHz)
TXD1 (changed drive strength from 20 Ohm to 50Ohm)

Ethernet-Test : ping the AutoEVB-Board from a PC
Test-Result : ping does not work. Incoming ethernet-communication works fine. No outgoing ethernet-communication.

Conclusion:
In my opinion there is a problem inside the vybrid-cpu. The vybrid-cpu puts data to the RMII-interface on the wrong edge of the RMII-Clock.

The original source-code from MQX only works, cause the pad-settings are wrong. The trigger-point is shifted a little bit to the right by the wrong settings. But it is not a stable solution.
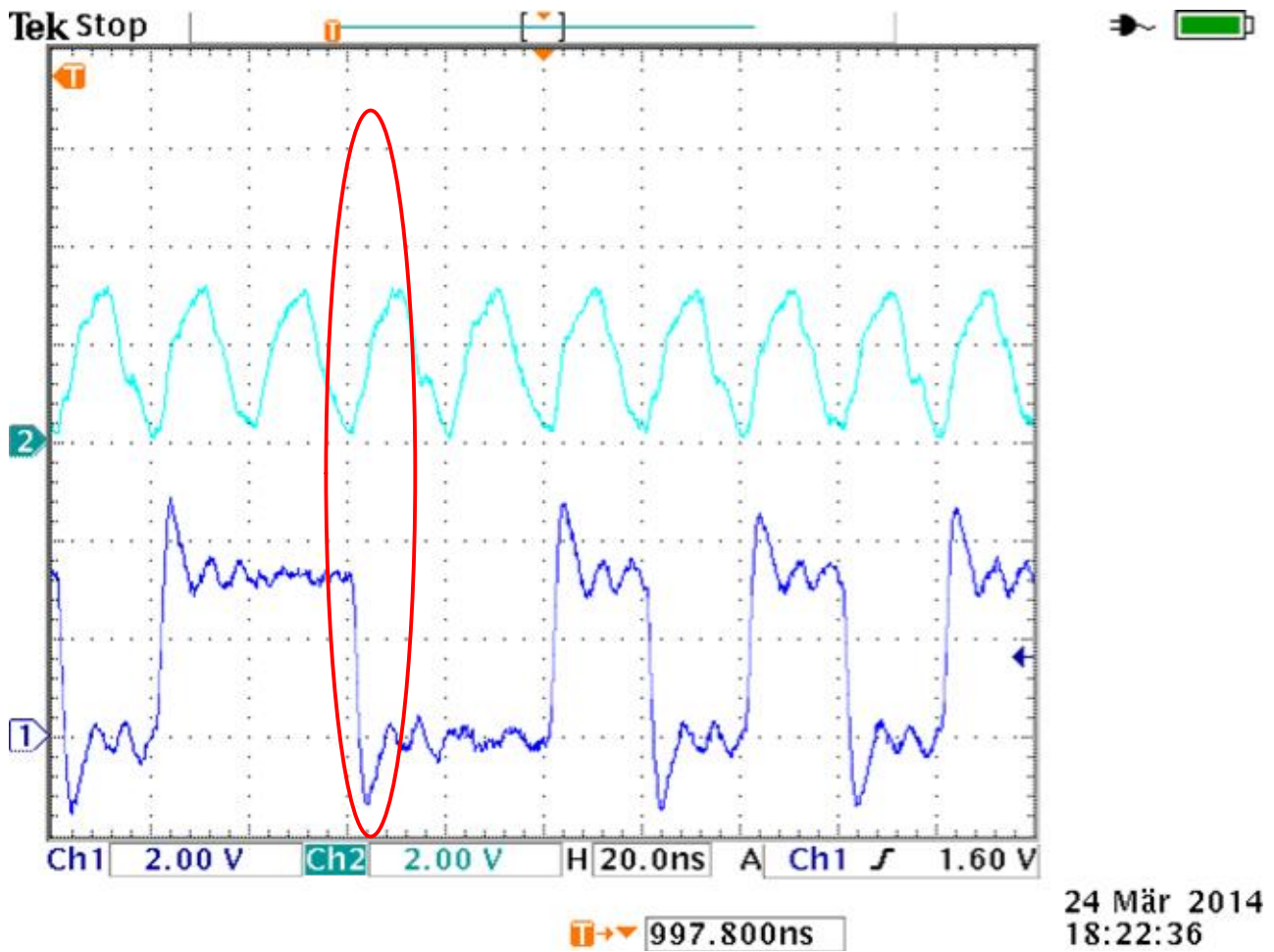
Measure 1 – original settings freescale source-code - channel 2 RMII-Clock – channel 1 TXD1
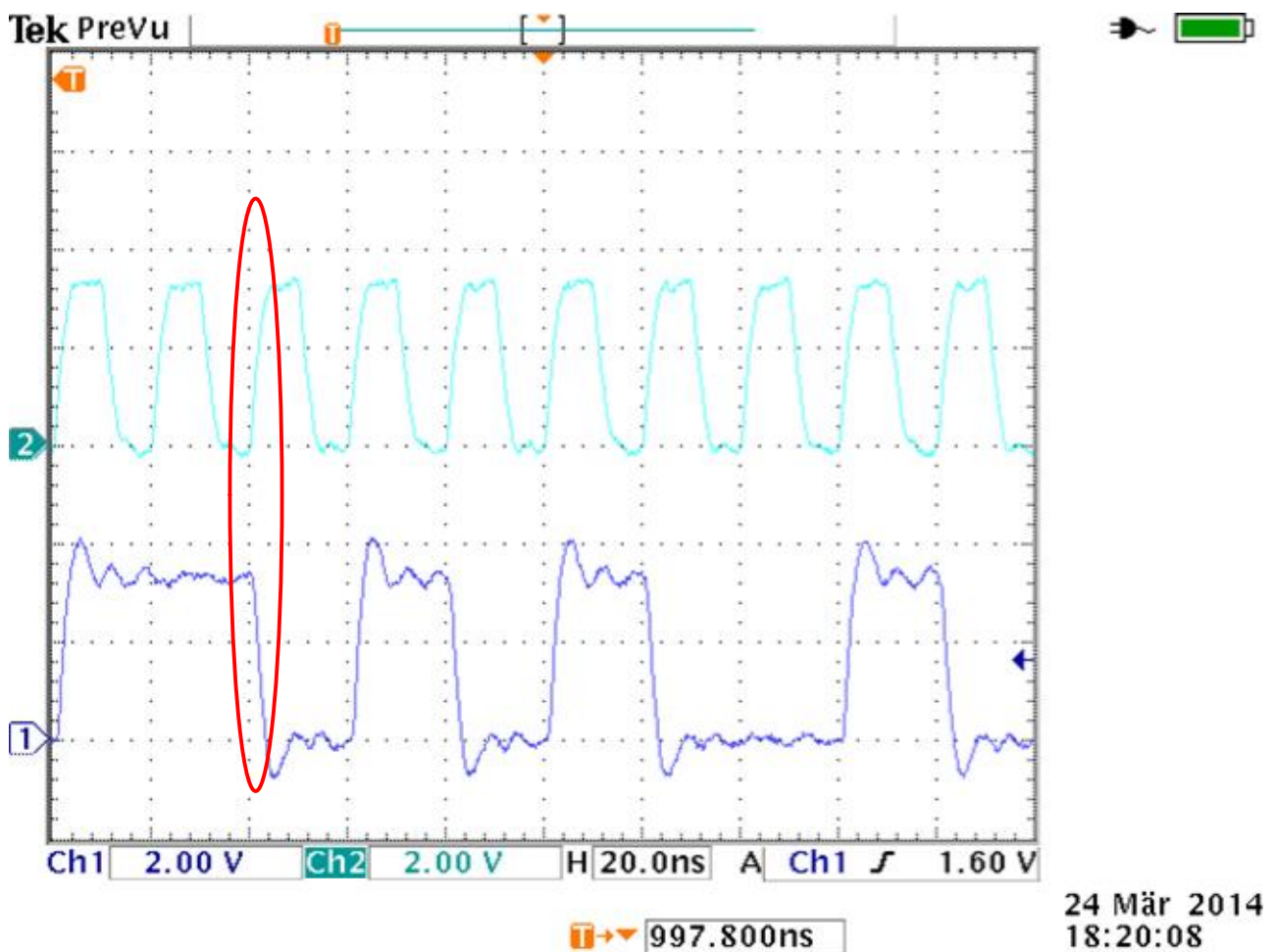
Measure 2 – modified pad-settigs – channel 2 RMII-Clock – channel 1 TXD1

5.5.4.2 RMII Timing (REF_CLK In Mode)

The 50MHz REF_CLK IN timing applies to the case when nINTSEL is floated or pulled-high. In this mode, a 50MHz clock must be input on the CLKIN pin. For more information on REF_CLK In Mode, see Section 3.7.4.1, "REF_CLK In Mode," on page 34.
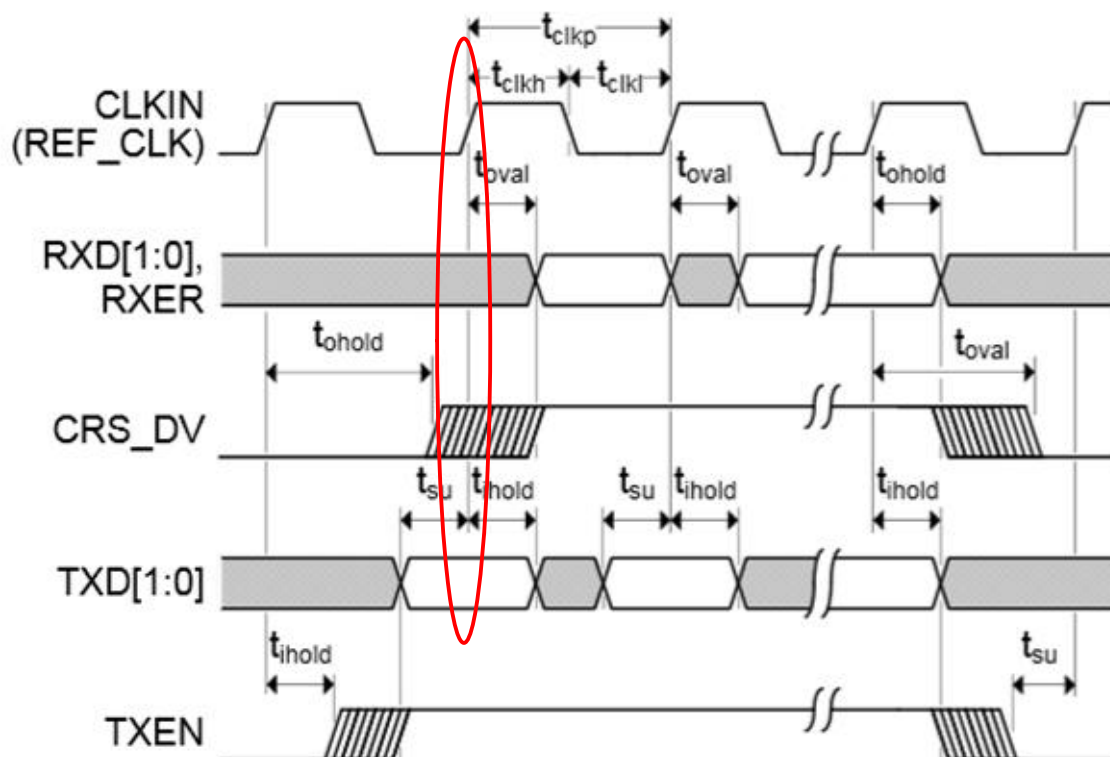

Figure 5.5 RMII Timing (REF_CLK In Mode)

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