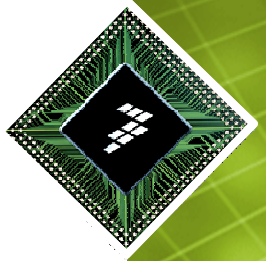
MCG

Multipurpose Clock Generator



Agenda

1. Overview
2. Diagram Connections
3. Modes of Operation
4. MCG Hands-On

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The Multipurpose Clock Generator

- Overview
  - The Multipurpose Clock Generator (MCG) module in the Kinetis KL25 is responsible for generating clocks throughout the microcontroller. It is capable of generating a range of clock speeds from any one of its several input sources.
- Learning Objectives
  - This class will help you learn about the Multipurpose Clock Generator (MCG) in the Kinetis KL25. Understanding how the MCG generates clocks for the MCU is a requirement for using timers and many of the Kinetis communication interfaces.
- Success Criteria
  - At the end of this module, you will be able to configure the MCG to generate your desired clock speed (up to 48MHz) on the Kinetis KL25.

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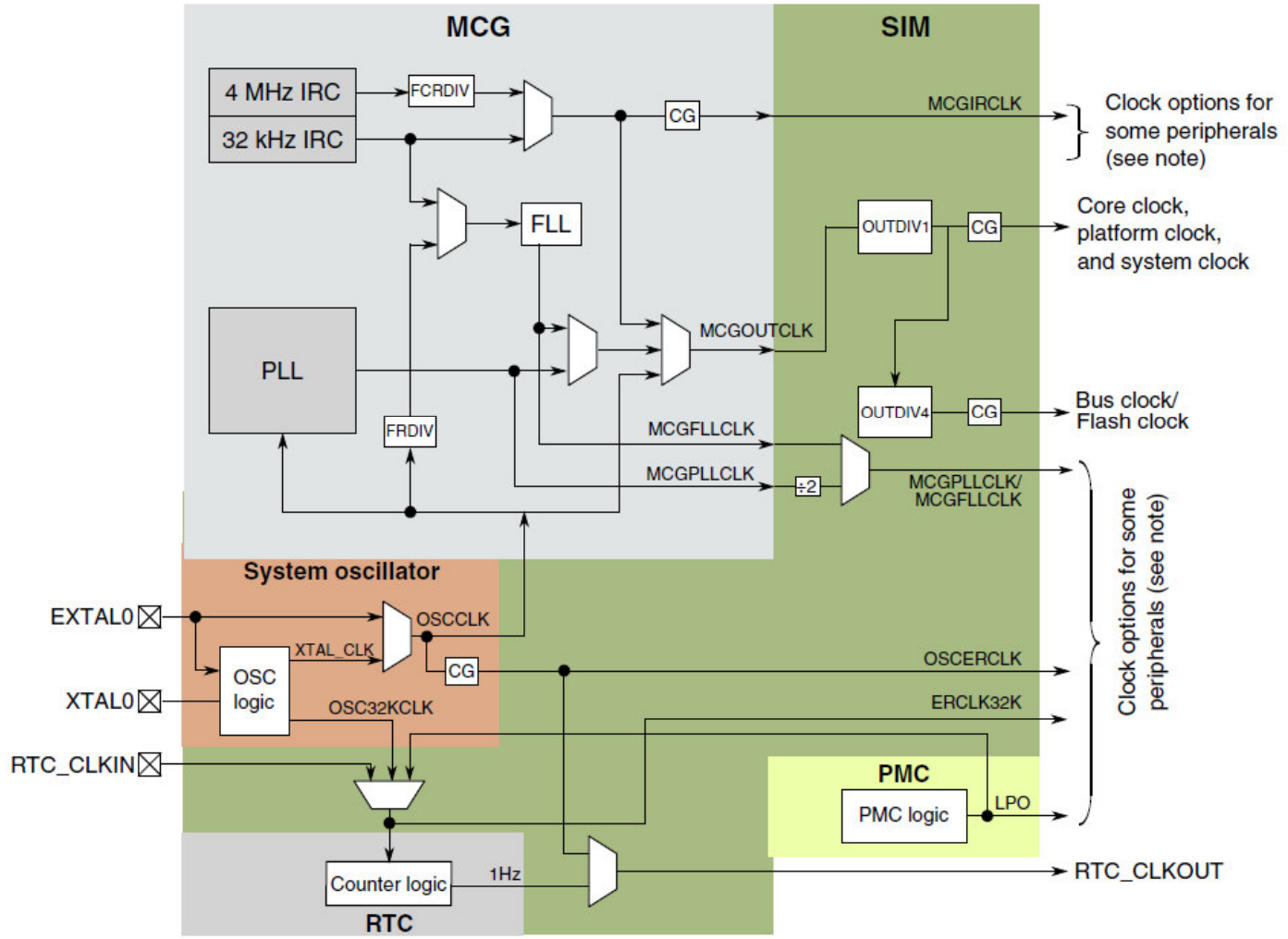
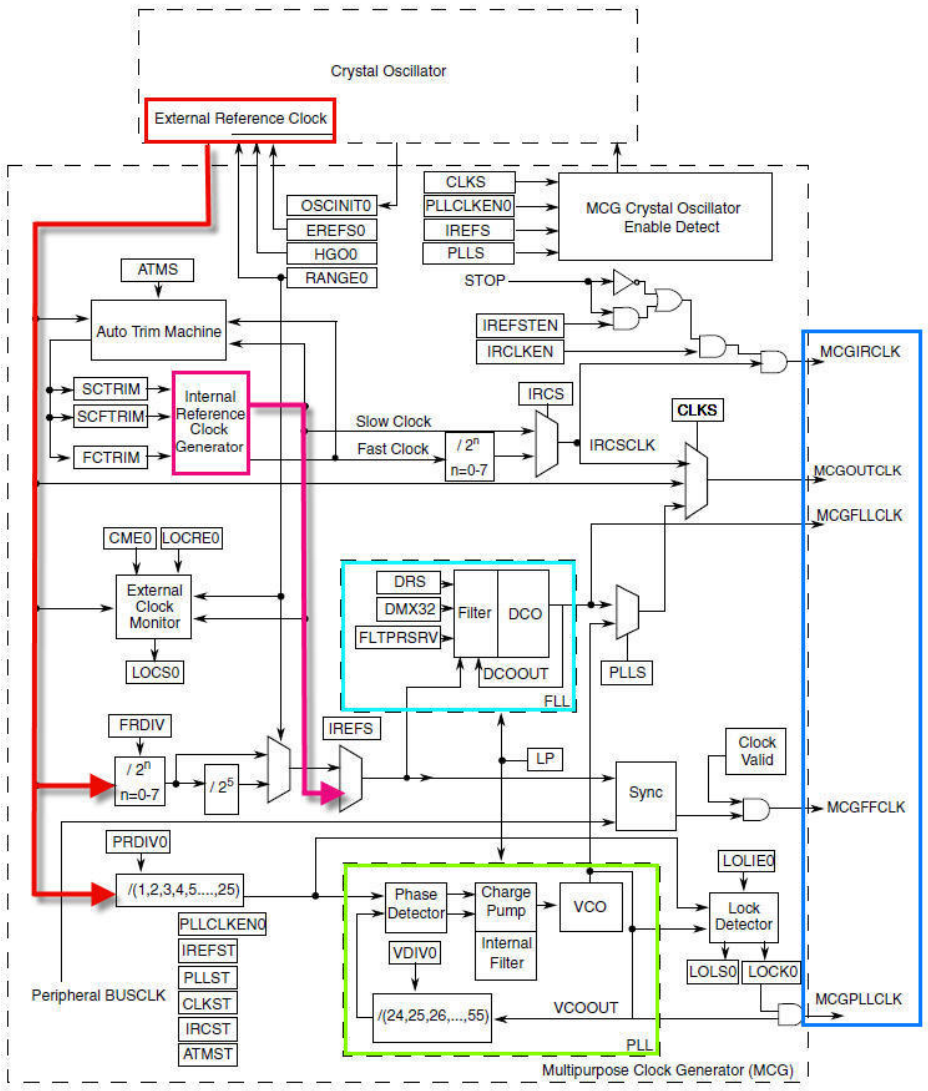
MCG Block Diagram and Key Features



MCG Block Diagram and Key Features



Multipurpose Clock Generator (MCG) block diagram

MCG Block Diagram and Key Features

- Frequency-locked loop (FLL):
  - Digitally-controlled oscillator (DCO)
  - DCO frequency range is programmable for up to four different frequency ranges.
  - Option to program and maximize DCO output frequency for a low frequency external reference clock source.
  - Internal or external reference clock can be used as the FLL source.
  - Can be used as a clock source for other on-chip peripherals.
- Phase-locked loop (PLL):
  - Voltage-controlled oscillator (VCO)
  - External reference clock is used as the PLL source.
  - Modulo VCO frequency divider
  - Phase/Frequency detector
  - Integrated loop filter
  - Can be used as a clock source for other on-chip peripherals.

MCG Block Diagram and Key Features

- Internal reference clock generator:
  - Slow clock with nine trim bits for accuracy
  - Fast clock with four trim bits
  - Can be used as source clock for the FLL. In FEI mode, only the slow Internal Reference Clock (IRC) can be used as the FLL source.
  - Either the slow or the fast clock can be selected as the clock source for the MCU.
  - Can be used as a clock source for other on-chip peripherals.

MCG Block Diagram and Key Features

- External clock from the Crystal Oscillator :
  - Can be used as a source for the FLL and/or the PLL.
  - Can be selected as the clock source for the MCU.
- MCG PLL Clock (*MCGPLLCLK*) is provided as a clock source for other on-chip peripherals
- MCG FLL Clock (*MCGFLLCLK*) is provided as a clock source for other on-chip peripherals
- MCG Fixed Frequency Clock (*MCGFFCLK*) is provided as a clock source for other on-chip peripherals
- MCG Internal Reference Clock (*MCGIRCLK*) is provided as a clock source for other on-chip peripherals

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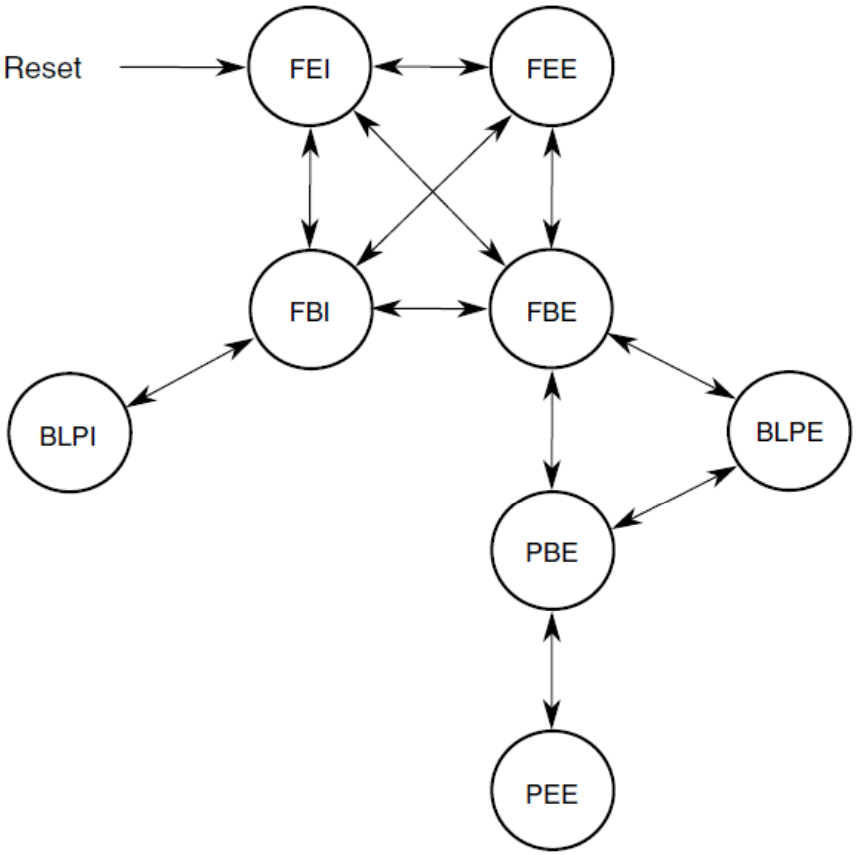
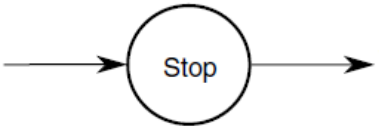
Modes of Operation

- The MCG has the following modes of operation: FEI, FEE, FBI, FBE, PBE, PEE, BLPI,BLPE, and Stop.
  - FLL Engaged Internal (FEI) clock mode
  - FLL Bypassed Internal (FBI) clock mode
  - FLL Bypassed External (FBE) clock mode
  - FLL Engaged External (FEE) clock mode
  - PLL Bypassed External (PBE) clock mode
  - PLL Engaged External (PEE) clock mode
  - Bypassed Low Power External (BLPE) clock mode
  - Bypassed Low Power Internal (BLPI) clock mode
- FEI, FBI, and BLPI modes require no external components
- All modes are software selectable
- User program can switch between modes at any time
- Bus frequency = ½ MCGOUT

MCG mode state diagram



Entered from any state when the MCU enters Stop mode



Returns to the state that was active before the MCU entered Stop mode, unless a reset occurs while in Stop mode.

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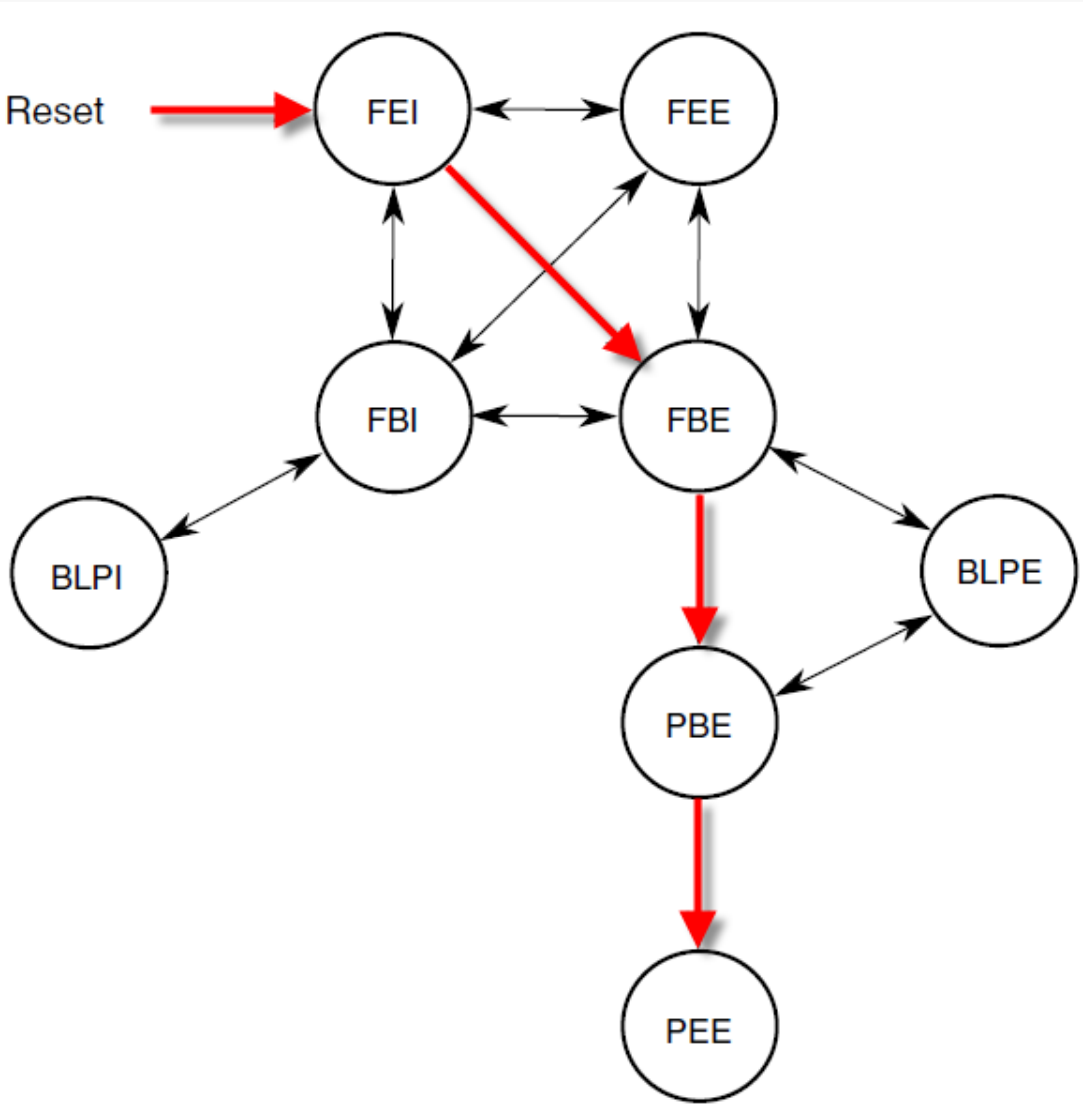
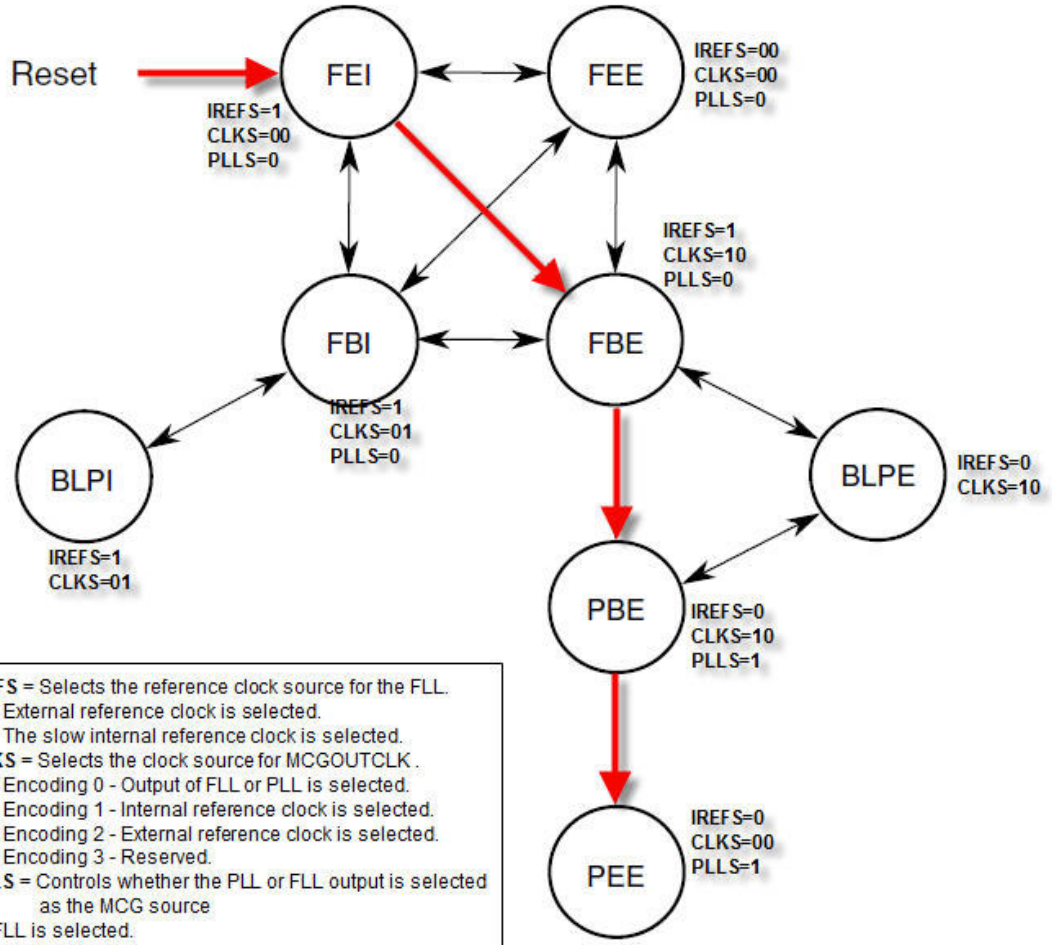
MCG Hands-On



MCG Hands-On

- For PEE mode, you must first configure the MCG for FBE mode, then for PBE mode, and lastly for PEE mode.



IREFS = Selects the reference clock source for the FLL.
0 - External reference clock is selected.
1 - The slow internal reference clock is selected.
CLKS = Selects the clock source for MCGOUTCLK .
00 Encoding 0 - Output of FLL or PLL is selected.
01 Encoding 1 - Internal reference clock is selected.
10 Encoding 2 - External reference clock is selected.
11 Encoding 3 - Reserved.
PLLS = Controls whether the PLL or FLL output is selected as the MCG source
0 FLL is selected.
1 PLL is selected.

MCG Hands-On

- In the diagram, note that the IREFS bit switches between an internal and external reference clock.
- The PLLS bit switches between the FLL and PLL clock, and the CLKS bit selects the output to the system clock.
- In every mode, each time the PLLS, IREFS, or CLKS bits are changed, the corresponding bits in the MCG status and control register -- PLLST, IREFST, or CLKST -- must be checked before moving on. Care must be taken to ensure that the RDIV bits are set properly for the mode being switched to.

MCG Hands-On

- Moving from FEI to PEE mode:
  External Crystal = 8 MHz,
  MCGOUTCLK frequency = 48 MHz

- In this example, the MCG will move through the proper operational modes from FEI to PEE to achieve 48 MHz MCGOUTCLK frequency from 8 MHz external crystal reference. First, the code sequence will be described. Then there is a flowchart that illustrates the sequence.

MCG Hands-On

- 1. First, FEI must transition to FBE mode:

  a. C2 = 0x94
  - C2[LOCRE0] set to 1 to Generate a reset request on a loss of OSC0 external reference clock..
  - C2[RANGE0] set to 01 because the frequency of 8 MHz is within the high frequency range.
  - C2[HGO0] set to 0 to configure the crystal oscillator for low-power operation.
  - C2[EREFS0] set to 1, because a crystal is being used.

  b. C1 = 0x98
  - C1[CLKS] set to 10 to select external reference clock as system clock source
  - C1[FRDIV] set to 111, or divide-by-256 because 8 MHz / 256 = 31.25kHz which is in the 31.25 kHz to 39.0625 kHz range required by the FLL
  - C1[IREFS] cleared to 0, selecting the external reference clock and enabling the external oscillator.

  c. Loop until S[OSCINIT0] is 1, indicating the crystal selected by C2[EREFS0] has been initialized.

  d. Loop until S[IREFST] is 0, indicating the external reference is the current source for the reference clock.

  e. Loop until S[CLKST] is 10, indicating that the external reference clock is selected to feed MCGOUTCLK.

MCG Hands-On

2. Then configure C5[PRDIV0] to generate correct PLL reference frequency.
   a. C5 = 0x03
      - C5[PRDIV0] set to 111, or divide-by-4 resulting in a pll reference frequency of 8 MHz/4 = 2 MHz.

MCG Hands-On

3. Then, FBE must transition either directly to PBE mode or first through BLPE mode and then to PBE mode:
   a. BLPE/PBE: C6 = 0x40
      - C6[PLLS] set to 1, selects the PLL. At this time, with a C1[PRDIV] value of 0b111, the PLL reference divider is 4 (see PLL External Reference Divide Factor table), resulting in a reference frequency of 8 MHz/ 4 = 2 MHz.
      - C6[VDIV0] set to 0b0000, or multiply-by-24 because 2 MHz reference * 24 = 48 MHz.
   b. PBE: Loop until S[PLLST] is set, indicating that the current source for the PLLS clock is the PLL.
   c. PBE: Then loop until S[LOCK0] is set, indicating that the PLL has acquired lock.

MCG Hands-On

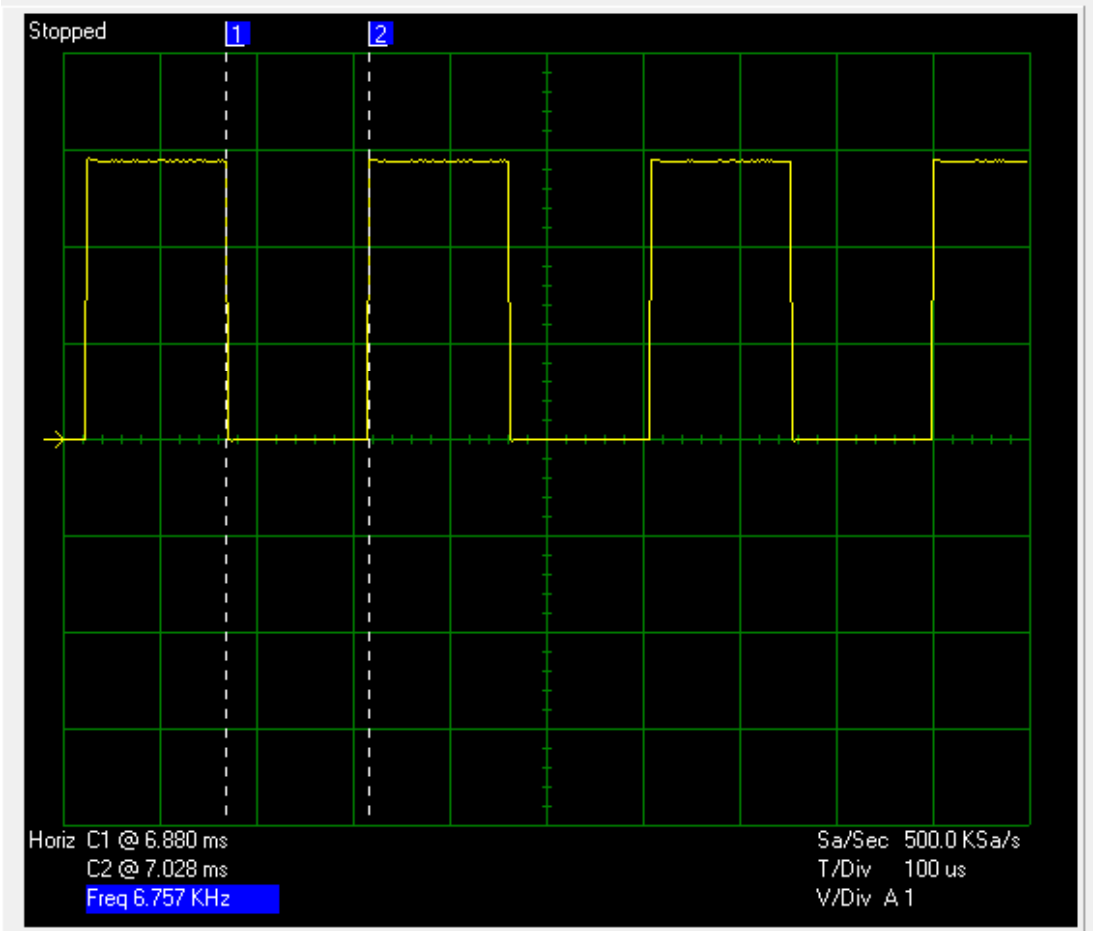
4. Lastly, PBE mode transitions into PEE mode:
   a. C1 = 0x18
      - C1[CLKS] set to 0b00 to select the output of the PLL as the system clock source.
   b. Loop until S[CLKST] are 0b11, indicating that the PLL output is selected to feed MCGOUTCLK in the current clock mode.
      - Now, with PRDIV0 of divide-by-4, and C6[VDIV0] of multiply-by-24, MCGOUTCLK = [(8 MHz / 4) * 24] = 48 MHz.

MCG Hands-On

- Once the core is running at 48Mhz, Write a C program that will blink an LED using a delay and compare with no MCG initialization.

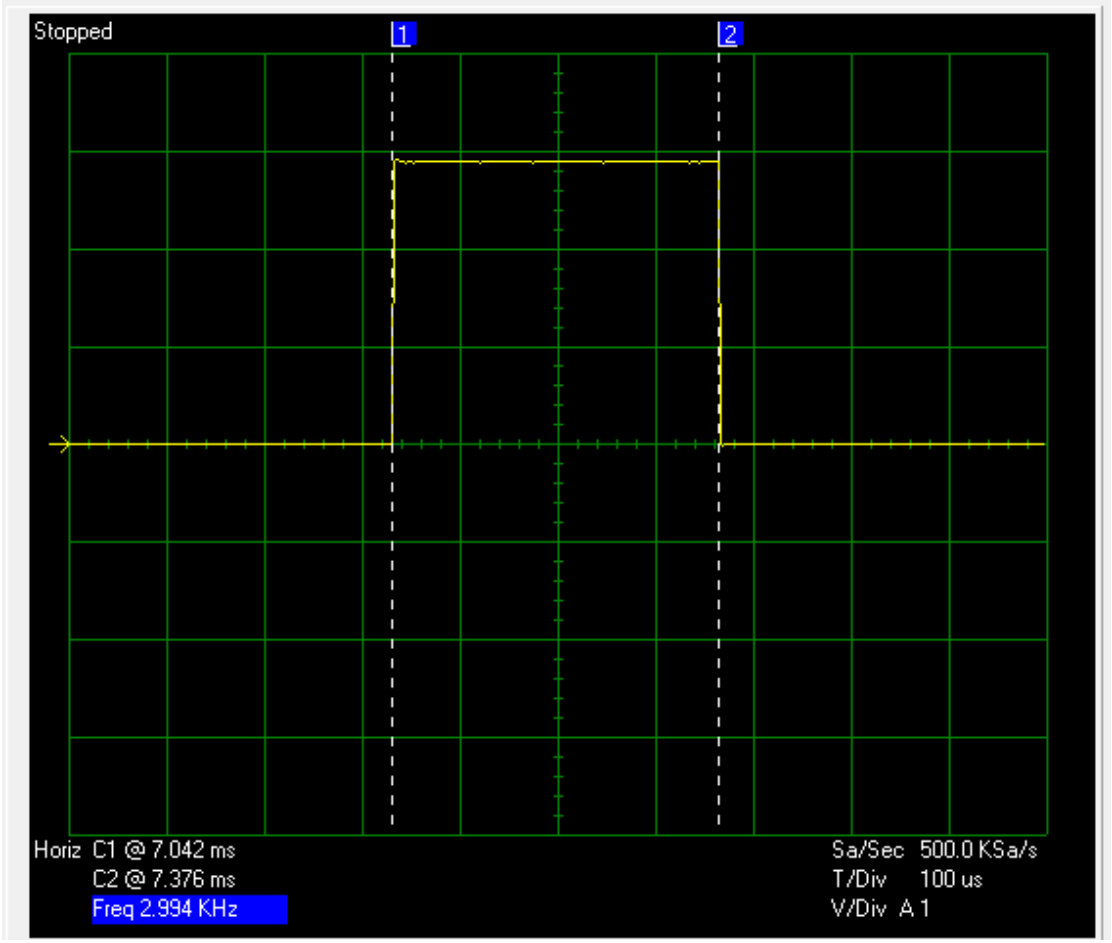
MCG Hands-On

- Running at 48MHz



MCG Hands-On

- Running at 20.9MHz

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