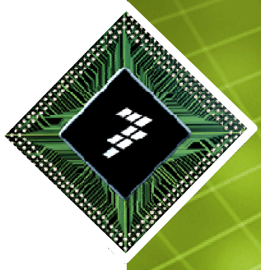
NVIC

Nested Vector Interrupt Controller



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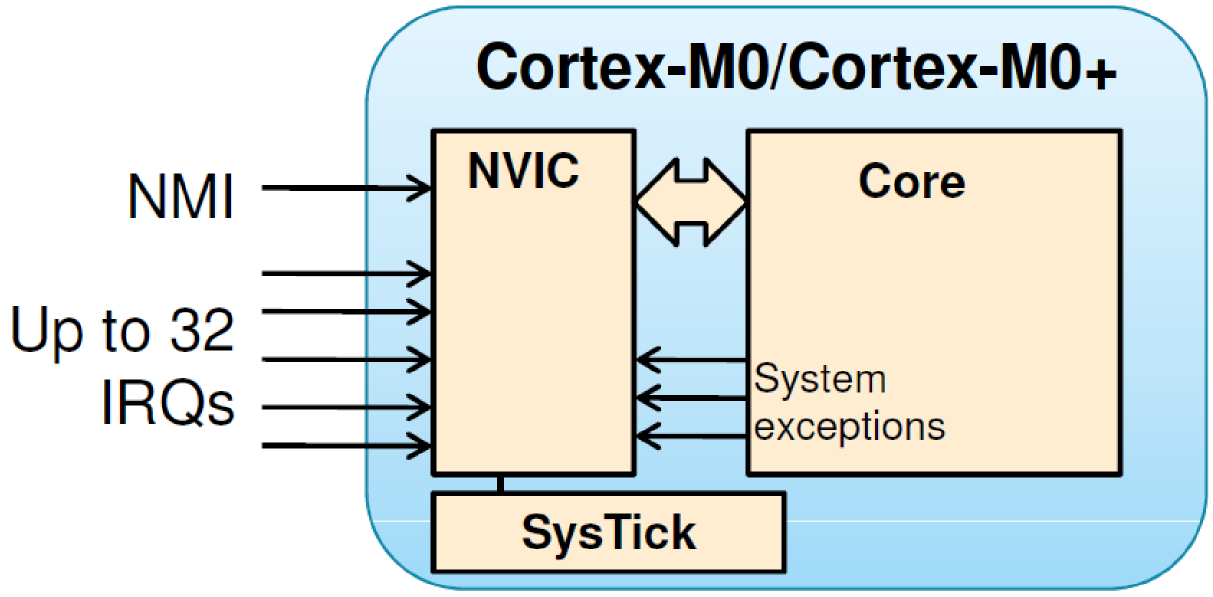
Alí Piña

Technical Support Engineer

NVIC Introduction

- The NVIC is a standard module on the ARM Cortex M series. This module is closely integrated with the core and provides very low latency entering and exiting an interrupt service routine (ISR).



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NVIC Introduction

- Low latency interrupt
  - 15 cycles to PUSH on ISR entry
  - 15 cycles to POP on ISR exit
  - 11 cycles to change (tail-chain) from an ISR to another (lower priority)
- When an exception is triggered the processor will push 8 registers:
  - XPSR
  - PC
  - Link Register
  - R12
  - R3
  - R2
  - R1
  - R0
- XPSR contains the current executing interrupt number
- Link Register holds the address to return to when an ISR finishes.

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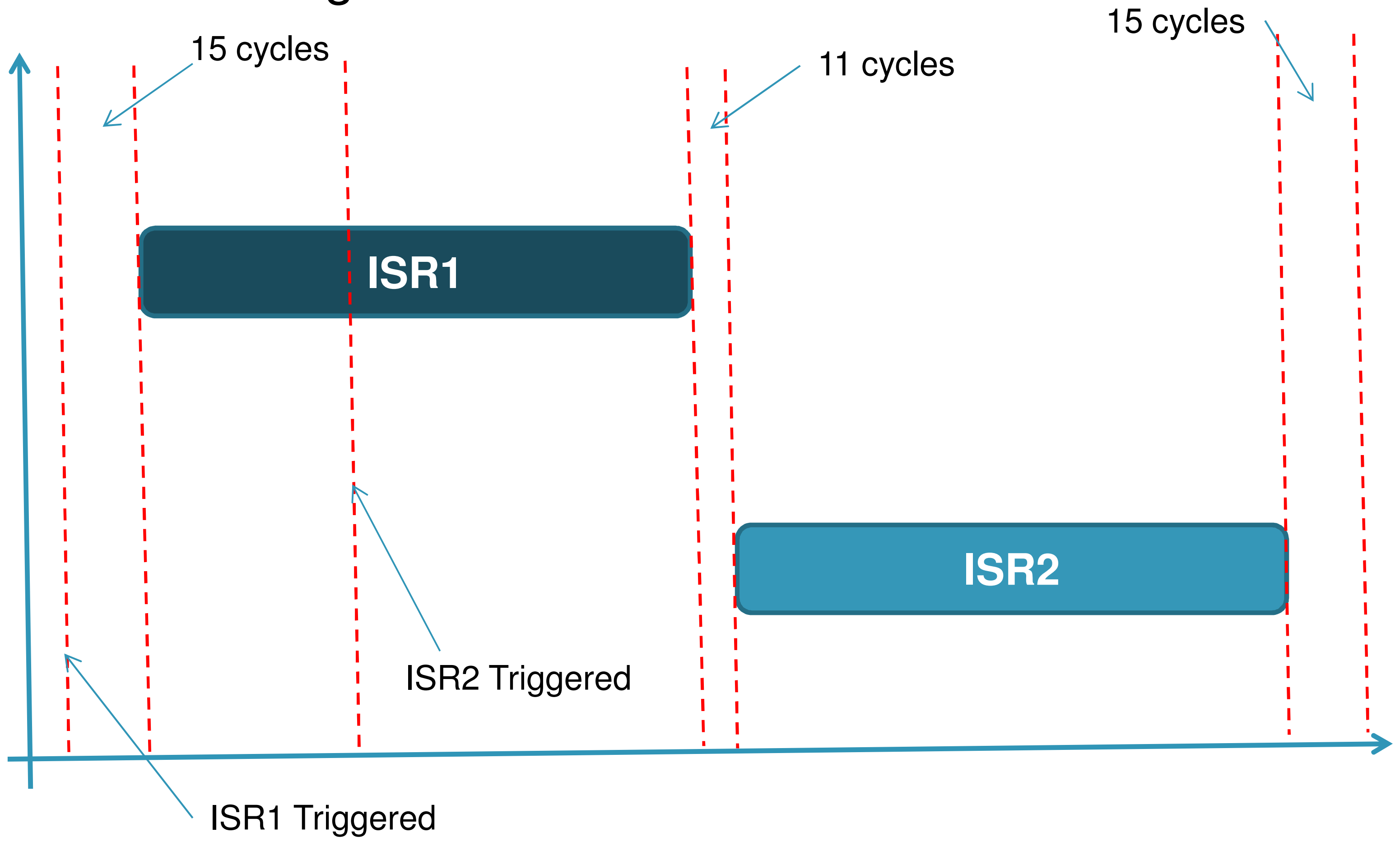
NVIC Introduction

- Tail-Chaining



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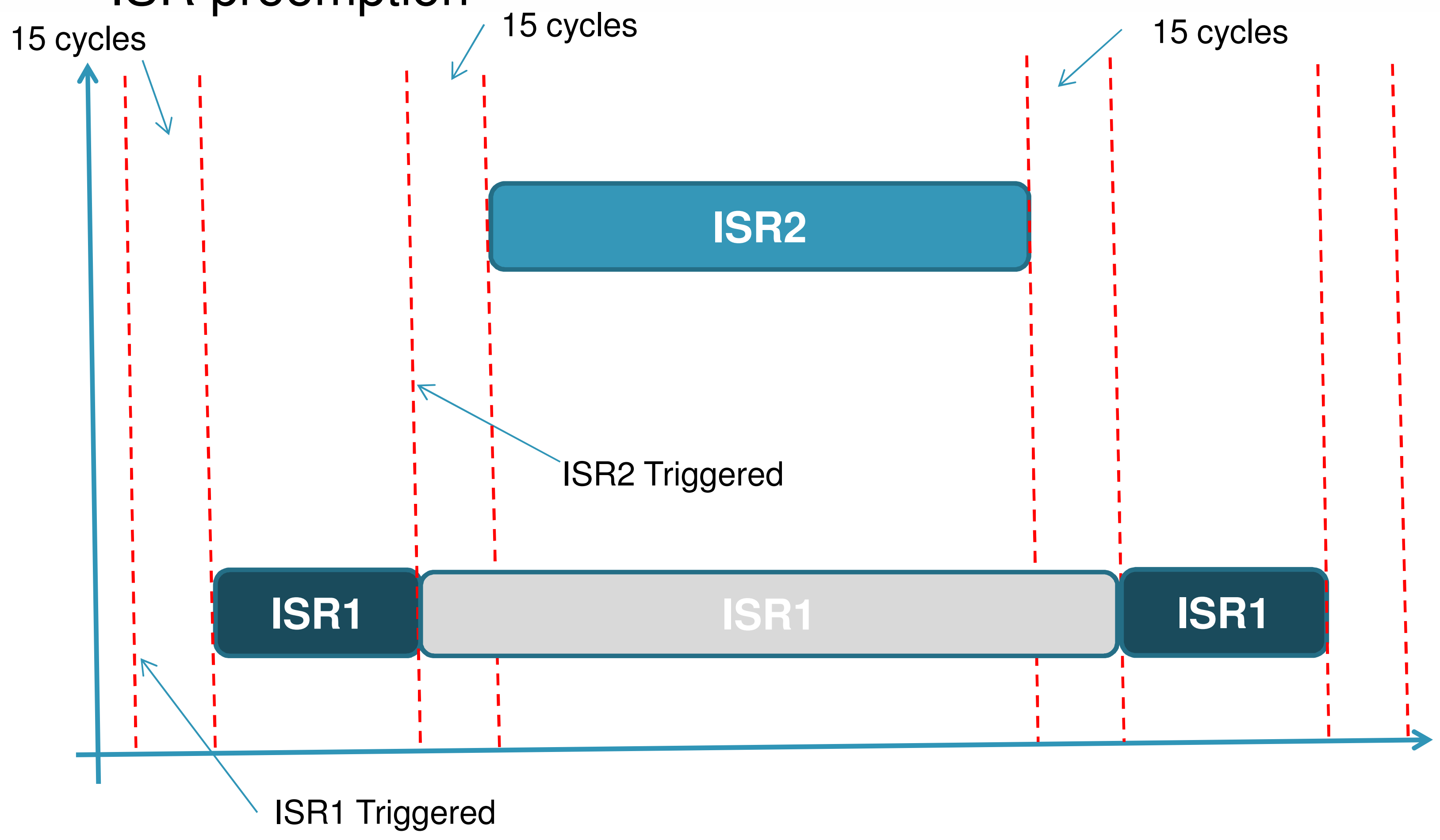
NVIC Introduction

- ISR preemption



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NVIC Features

- The NVIC provides four different interrupt priorities which can be used to control the order in which interrupts must be serviced. Priorities are 0-3, with 0 receiving the highest priority.
- On Kinetis L series MCUs the NVIC provides up to 48 interrupt sources including 16 that are core specific. It also implements up to four priority levels that are fully programmable. The NVIC uses a vector table to manage the interrupts. This vector table can be stored in either flash or RAM, depending on the application.

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NVIC Configuration

- Configuring the NVIC for the specific module involves writing three registers:
  - NVIC Set Enable Register (NVICSERx)
  - NVIC Clear Pending Register (NVICCPRx)
  - NVIC Interrupt Priority (NVICIPxx)

    - Note: NVIC registers are not documented in the KL25Z RM. These register are part of the core (Cortex M0+)

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NVIC Configuration

– NVIC Set Enable Register (NVICSERx)

This register enable interrupts, and show which interrupts are enabled.

Write:

0 = no effect

1 = enable interrupt.

Read:

0 = interrupt disabled

1 = interrupt enabled

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority

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NVIC Configuration

– NVIC Clear Pending Register (NVICCPRx)

- This register remove the pending state from interrupts, and show which interrupts are pending.

– **Write:**

0 = no effect

1 = removes pending state an interrupt.

– **Read:**

0 = interrupt is not pending

1 = interrupt is pending.

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NVIC Configuration

– NVIC Interrupt Priority (NVICIPxx)

- This device supports 4 priority levels for interrupts. Therefore, in the NVIC each source in the IPR registers contains 2 bits. For example, IPR0 is shown below:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IRQ3		0	0	0	0	0	0	IRQ2		0	0	0	0	0	0	IRQ1		0	0	0	0	0	0	IRQ0		0	0	0	0	0	0
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NVIC Configuration

– NVIC Interrupt Priority (NVICIPxx)

- To determine the particular IRQ's bitfield location within these particular registers:

NVICIPRx bitfield starting location = 8 * (IRQ mod 4) + 6

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IRQ3		0	0	0	0	0	0	IRQ2		0	0	0	0	0	0	IRQ1		0	0	0	0	0	0	IRQ0		0	0	0	0	0	0
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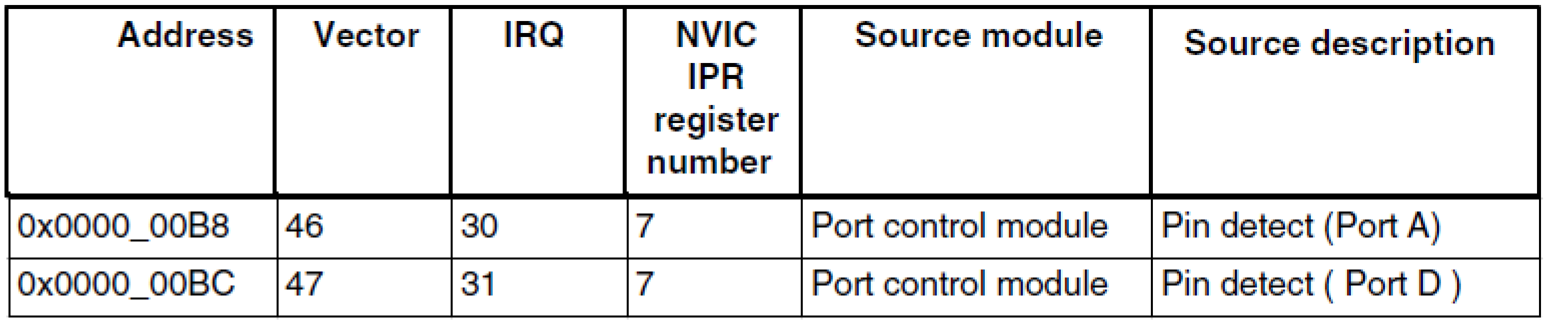
Hands-On

- Configure the NVIC for a IRQ interrupt, using PORTx module.
- The steps to configure the NVIC for this module are:
  1. Identify the vector number and the IRQ number of the module from the vector table in the device-specific reference manual in the section Interrupt Channel Assignments. For the PORTA the vector is 46.

Table 3-7. Interrupt vector assignments (continued)



Address	Vector	IRQ	NVIC IPR register number	Source module	Source description
0x0000_00B8	46	30	7	Port control module	Pin detect (Port A)
0x0000_00BC	47	31	7	Port control module	Pin detect (Port D)

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Hands-On

2. Determine which NVICSERx register contains the IRQ. Each NVICSERx register contains 32 IRQs. Therefore, the NVICSER can enable from IRQ 0 to IRQ 31. In this example, NVICSER is used, and the PORTA IRQ is 30. The NVICCPRx uses the same number, in this case, NVICCPR.
3. To find out which bit to set, perform a modulo operation dividing the IRQ number by 32. This number is used to enable the interrupt on NVICSER and to clear the pending interrupts from NVICCPR.

   PORTA BIT = 30 mod 32

   PORTA BIT = 30
4. At this point, the interrupt for the PORTA can be configured.

   NVICICPR |= (1<<30); //Clear any pending interrupts on PORTA

   NVICISER |= (1<<30); //Enable interrupts from PORTA module
5. Next, set the interrupt priority level. This is application dependent. On Kinetis L series MCUs there are four different priority levels. To set the priority, write to the NVICIPxx register; the "xx" represents the IPR number, which is NVICIPR7 in this example.The PORTA example sets the priority to 1

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Hands-On

6. After the NVIC registers are set up, finish the peripheral configuration that must enable the interrupt.

```
PORTA_PCR1 |= PORT_PCR_MUX(1)|PORT_PCR_IRQC(0xA);
```

7. In the ISR, clear the peripheral interrupt flag and read back the status register to avoid re-entrance. For this example:

```
void PORTA_ISR(void)
{
        PORTA_ISFR=0xFFFFFFFF;
        RED_TOGGLE;
}
```

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Hands-On

- What’s next?

Low-Power Timer

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