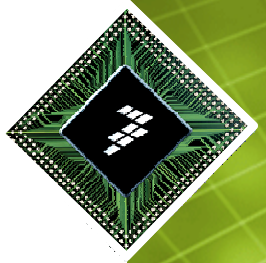
LPTMR

Low-Power Timer

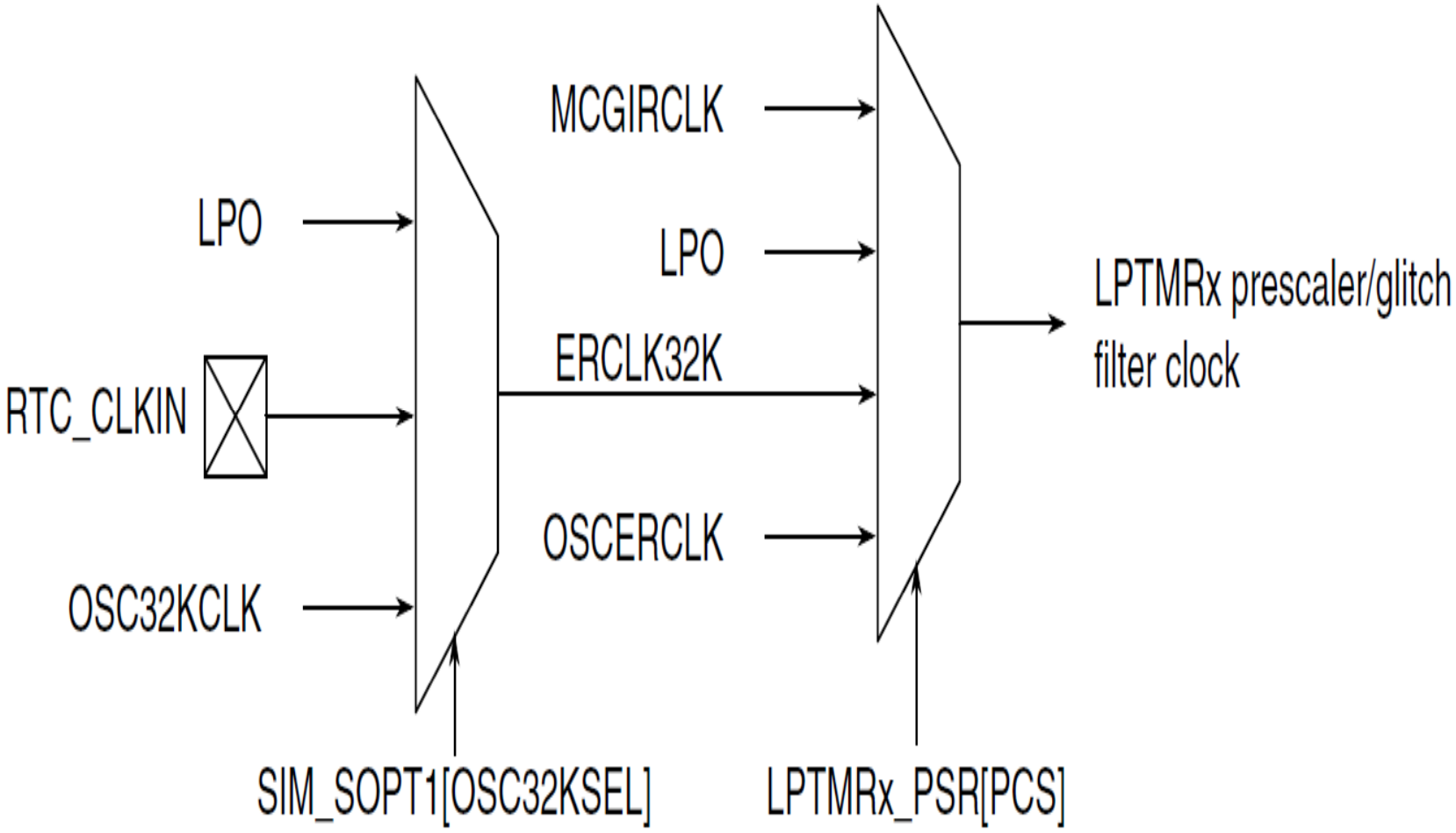


Feature List

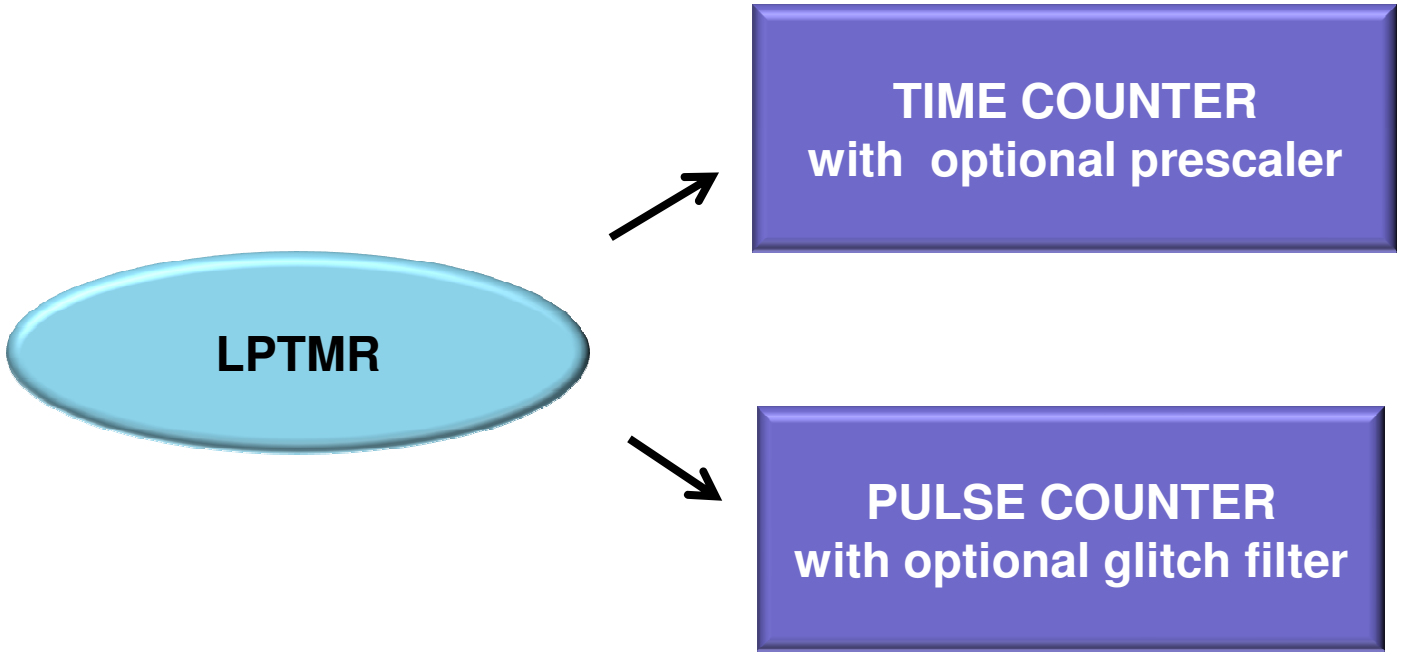
The features of the LPTMR module include:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

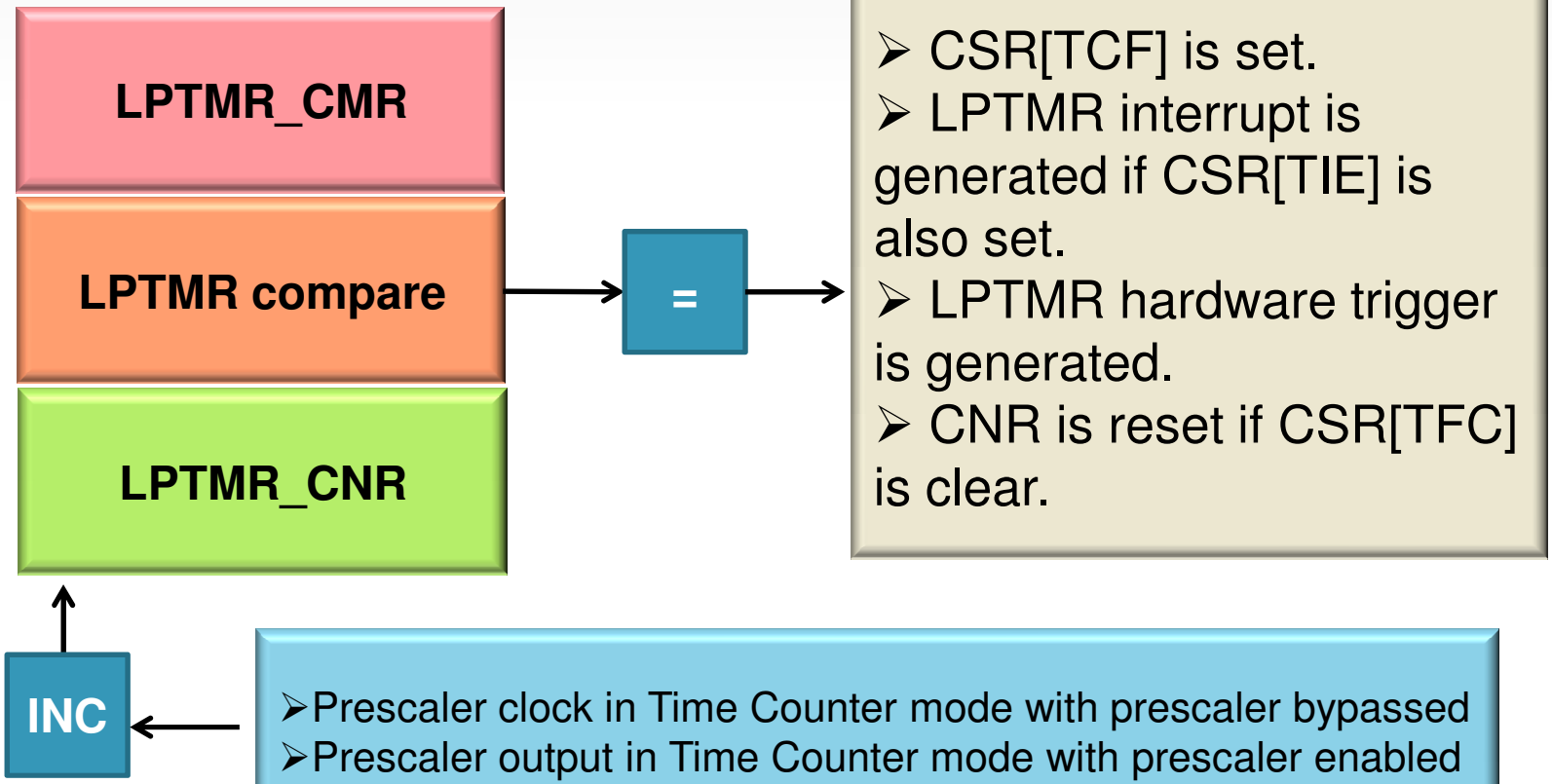
Clocks sources



Functional description



Functional description



LPTMR Register

Register name	Width (in bits)	Access	Reset value
Low Power Timer Control Status Register (LPTMR0_CSR)	32	R/W	0000_0000h
Low Power Timer Prescale Register (LPTMR0_PSR)	32	R/W	0000_0000h
Low Power Timer Compare Register (LPTMR0_CMR)	32	R/W	0000_0000h
Low Power Timer Counter Register (LPTMR0_CNR)	32	R	0000_0000h

LPTMR Register

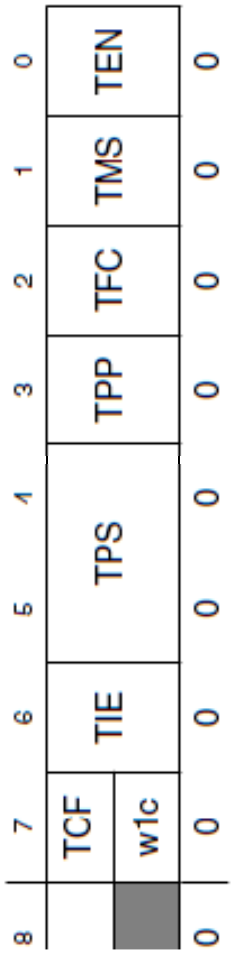
Low Power Timer Control Status Register (LPTMR*x*_*CSR*)

Address: 4004_0000h base + 0h offset = 4004_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								TCF	TIE	TPS		TPP	TFC	TMS	TEN
W									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Low Power Timer Control Status Register (LPTMR*x*_CSR)



Field	Description
7 TCF	Timer Compare Flag 0 The value of CNR is not equal to CMR and increments. 1 The value of CNR is equal to CMR and increments.
6 TIE	Timer Interrupt Enable 0 Timer interrupt disabled. 1 Timer interrupt enabled.
5–4 TPS	Timer Pin Select Configures the input source to be used in Pulse Counter mode. 00 Pulse counter input 0 is selected. 01 Pulse counter input 1 is selected. 10 Pulse counter input 2 is selected. 11 Pulse counter input 3 is selected.
3 TPP	Timer Pin Polarity Configures the polarity of the input source in Pulse Counter mode. 0 Pulse Counter input source is active-high, and the CNR will increment on the rising-edge. 1 Pulse Counter input source is active-low, and the CNR will increment on the falling-edge.
2 TFC	Timer Free-Running Counter 0 CNR is reset whenever TCF is set. 1 CNR is reset on overflow.
1 TMS	Timer Mode Select 0 Time Counter mode. 1 Pulse Counter mode.
0 TEN	Timer Enable 0 LPTMR is disabled and internal logic is reset. 1 LPTMR is enabled.

LPTMR Register

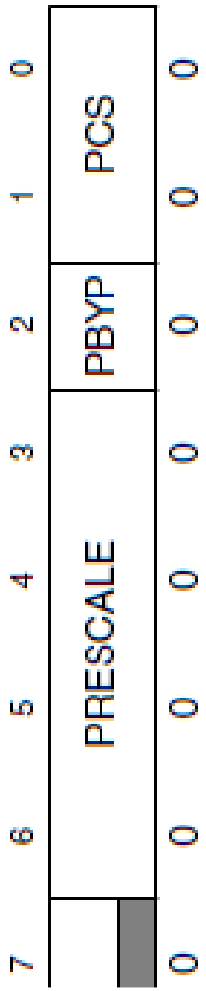
Low Power Timer Prescale Register (LPTMR*x*_*PSR*)

Address: 4004_0000h base + 4h offset = 4004_0004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								PRESCALE					PBYP	PCS	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Low Power Timer Prescale Register (LPTMR*x*_*PSR*)

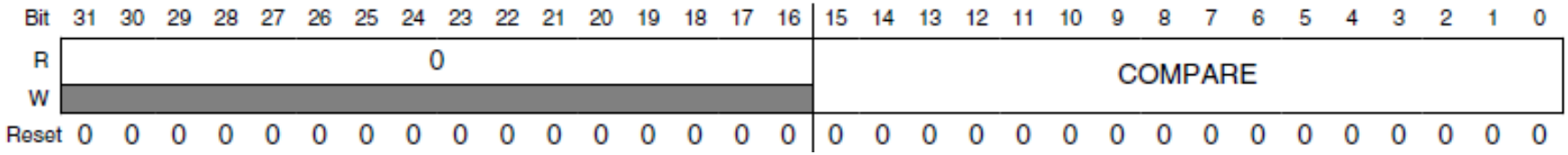


Field	Description
6–3 PRESCALE	Prescale Value Configures the size of the Prescaler in Time Counter mode or width of the glitch filter in Pulse Counter mode.
2 PBYP	Prescaler Bypass 0 Prescaler/glitch filter is enabled. 1 Prescaler/glitch filter is bypassed.
1–0 PCS	Prescaler Clock Select 00 Prescaler/glitch filter clock 0 selected. 01 Prescaler/glitch filter clock 1 selected. 10 Prescaler/glitch filter clock 2 selected. 11 Prescaler/glitch filter clock 3 selected.

LPTMR Register

Low Power Timer Compare Register (LPTMR*x*_*CMR*)

Address: 4004_0000h base + 8h offset = 4004_0008h

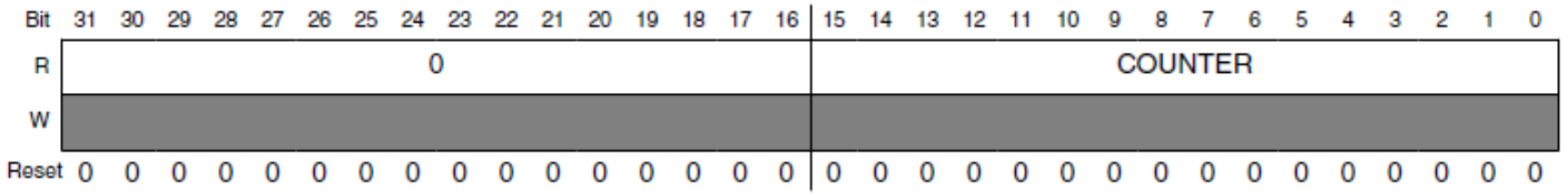


Field	Description
15–0 COMPARE	Compare Value When the LPTMR is enabled and the CNR equals the value in the CMR and increments, TCF is set and the hardware trigger asserts until the next time the CNR increments. If the CMR is 0, the hardware trigger will remain asserted until the LPTMR is disabled. If the LPTMR is enabled, the CMR must be altered only when TCF is set.

LPTMR Register

Low Power Timer Counter Register (LPTMR*x*_*CNR*)

Address: 4004_0000h base + Ch offset = 4004_000Ch



Field	Description
15–0 COUNTER	Counter Value

Hands-On

- Configure the LPTMR toggle a LED every X time using a compare value.
- The steps to configure the LPTMR for this module are:
  1. Set the clock for the LPTMR (SIM_SCGC5)
  2. Reset the module to clear any flag/ value (LPTMR0_CSR)
  3. Set the compare value (LPTMR0_CMR)
  4. Set the clock use it and the prescaler (LPTMR0_PSR)
  5. Enable the LPTMR (LPTMR0_CSR
  6. Wait for counter to reach compare value
  7. Clear the flag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