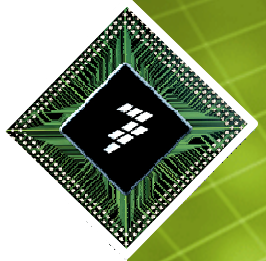
TPM

Timer/PWM Module

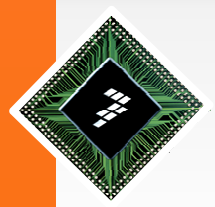


Agenda

1. Overview
2. Diagram Connections
3. TPM Register Definition
4. Modes of Operation
5. TPM Hands-On

Overview

- Learning Objectives
  - The goal of the unit is to describe the Timer/PWM module and a few of its uses.
    - Timer Overflow Interrupt
    - Output Compare
    - Input Capture
    - PWM
- Success Criteria
  - When you have completed this module you will be able to setup and use the Timer/PWM module in the Kinetis L Family of Microcontrollers



Overview

- One thing that microcontrollers are especially good at is counting. The TPM does just that, and is designed to be flexible enough to accommodate a very wide range of uses.
- Running in parallel with the core processor, the TPM can increment its own counters at a selected rate up to and including the system clock-speed. At each increment, the TPM can compare the current count against several registers, and depending on configuration can cause any of several things to happen. At the simplest, it can set a flag to let you know that it's reached the requested value, and in more complex configurations can automatically initiate DMA transfers or activate other peripherals such as the ADC.

TPM Features

- TPM clock mode is selectable.
- TPM includes a 16-bit counter.
- Includes 6 channels that can be configured for input capture, output compare, or edge-aligned PWM mode.
- Support selectable trigger input to optionally reset or cause the counter to start incrementing.
- Support the generation of hardware triggers when the counter overflows and per channel.

Diagram Connections

- TPM clocking

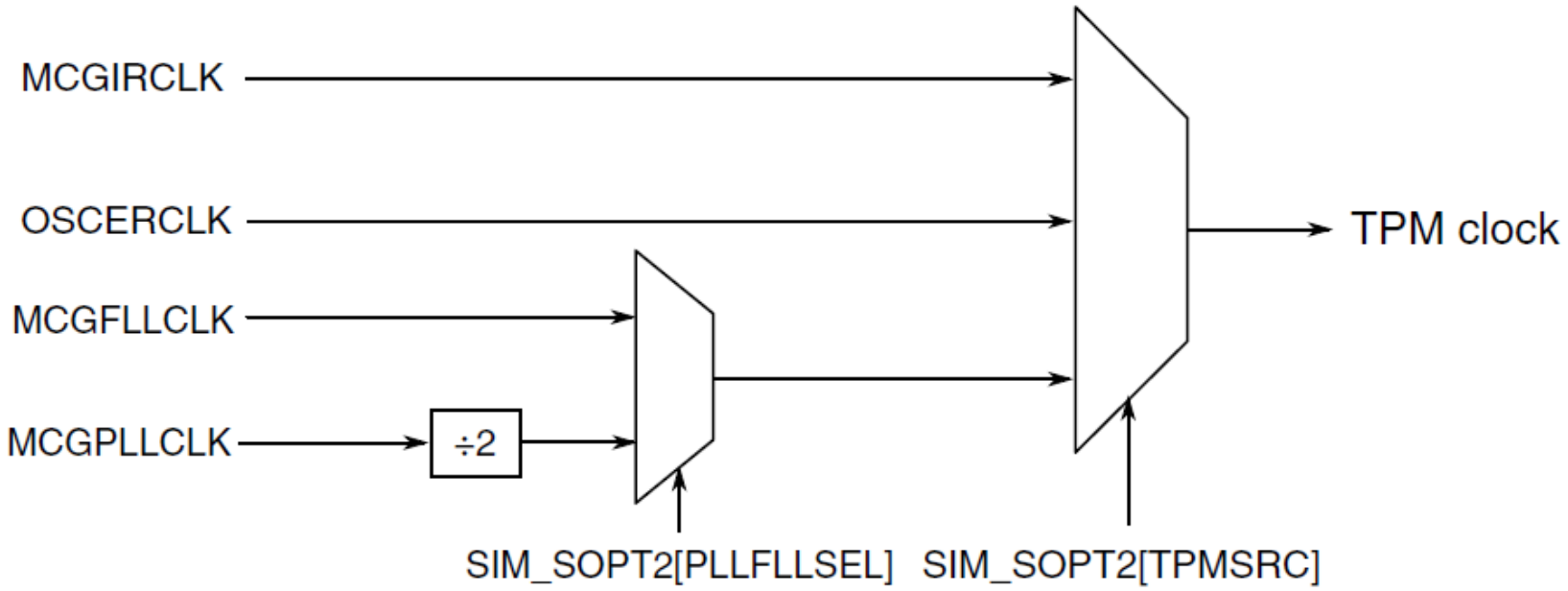


Diagram Connections

- TPM Block Diagram

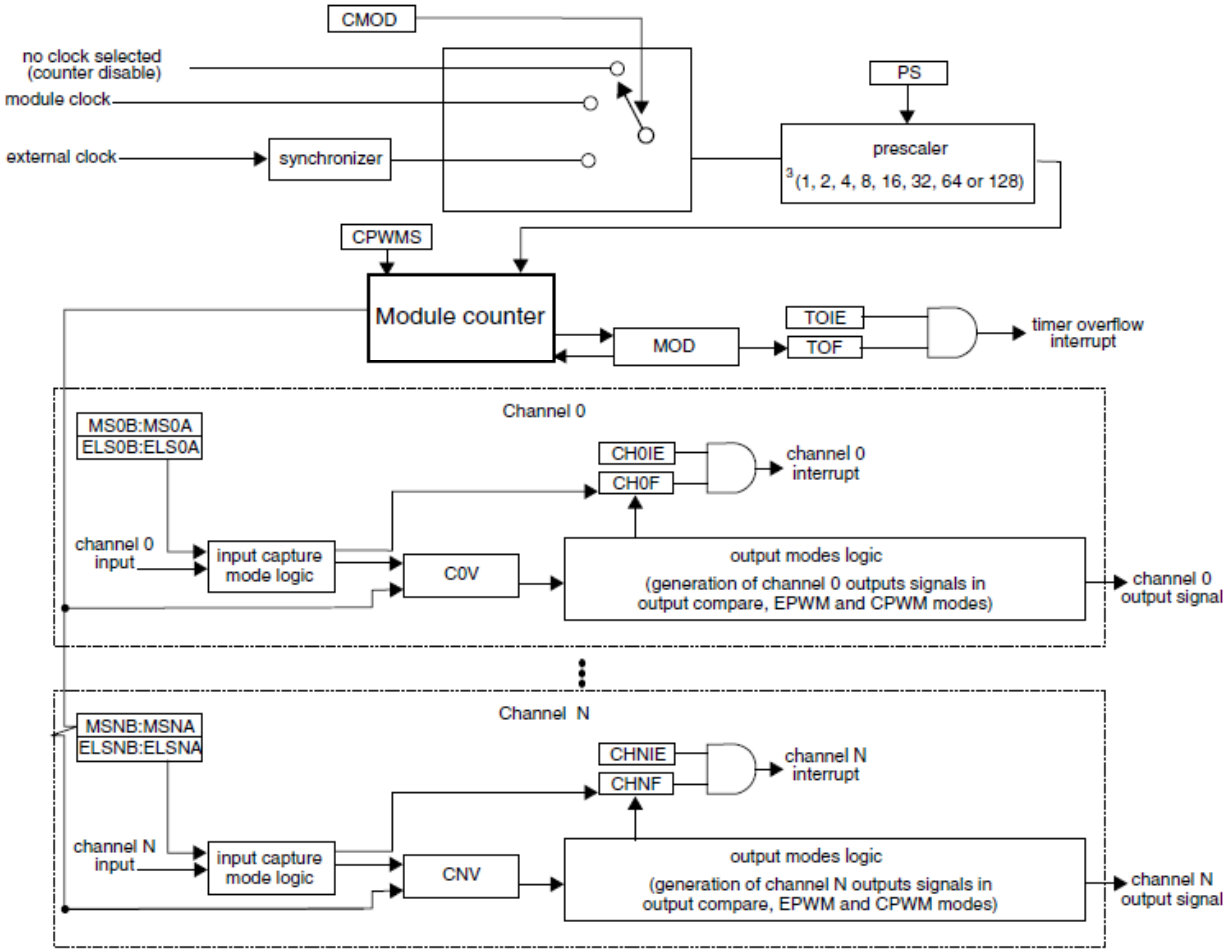


Diagram Configuration

- TPM Signal Description

Signal	Description	I/O
TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM_CHn	TPM channel (n = 5 to 0)	I/O

TPM Register Definition

- TPMx_SC Status and Control:
  - **DMA: DMA enable**: Enables DMA transfers for the overflow flag.
  - **TOF: Timer Overflow (w1c):** Set by hardware when the TPM counter equals the value in the MOD register and increments.
  - **TOIE: Timer Overflow Interrupt Enable**: Enables TPM overflow interrupts.
  - **CMOD: Clock Mode Selection**: Selects the TPM counter clock modes. When disabling the counter, this field remain set until acknowledged in the LPTPM clock domain.
  - **PS: Prescale Factor Selection**: Selects one of 8 division factors for the clock mode selected by CMOD.(1,2,3,4,16...)

TPM Register Definition

- Counter (TPMx_CNT)
  - The **CNT** register contains the LPTPM counter value. Reset clears the CNT register. Writing any value to COUNT also clears the counter.

- Modulo (TPMx_MOD)
  - The Modulo register contains the modulo value for the TPM counter. When the TPM counter reaches the modulo value and increments, the overflow flag (TOF) is set and the next value of TPM counter depends on the selected counting method

TPM Register Definition

- Channel (n) Status and Control (TPMx_CnSC)
  - **CnSC** contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function.
    - **CHF Channel Flag**: Set by hardware when an event occurs on the channel.
    - **CHIE Channel Interrupt Enable**
    - **MSB Channel Mode Select**
    - **MSA Channel Mode Select**
    - **ELSB Edge or Level Select**
    - **ELSA Edge or Level Select**
    - **DMA Enable:** Enables DMA transfers for the channel.

Modes of Operation

- Channel (n) Status and Control (TPMx_CnSC)

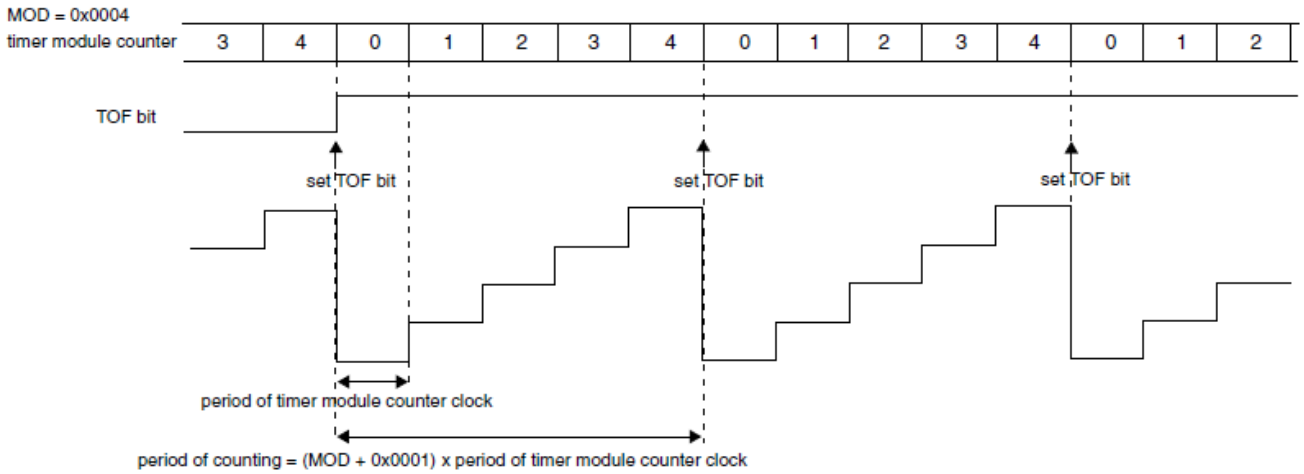
CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	00	00	None	Channel disabled
X	01/10/11	00	Software compare	Pin not used for LPTPM
0	00	01	Input capture	Capture on Rising Edge Only
		10		Capture on Falling Edge Only
		11		Capture on Rising or Falling Edge
	01	01	Output compare	Toggle Output on match
		10		Clear Output on match
		11		Set Output on match
	10	10	Edge-aligned PWM	High-true pulses (clear Output on match, set Output on reload)
		X1		Low-true pulses (set Output on match, clear Output on reload)
	11	10	Output compare	Pulse Output low on match
		X1		Pulse Output high on match
1	10	10	Center-aligned PWM	High-true pulses (clear Output on match-up, set Output on match-down)
		X1		Low-true pulses (set Output on match-up, clear Output on match-down)

Modes of Operation

- **Channel (n) Value (TPMx_CnV)**
  - These registers contain the captured TPM counter value for the input modes or the match value for the output modes.
    - In input capture mode, any write to a CnV register is ignored.
    - In compare modes, writing to a CnV register latches the value into a buffer. A CnV register is updated with the value of its write buffer according to CnV Register Update .
- **Capture and Compare Status (TPMx_STATUS)**
  - The STATUS register contains a copy of the status flag CHnF bit (in CnSC) for each TPM channel, as well as the TOF bit (in SC), for software convenience.
- **Configuration (TPMx_CONF)**
  - This register selects the behavior in debug and wait modes and the use of an external global time base.

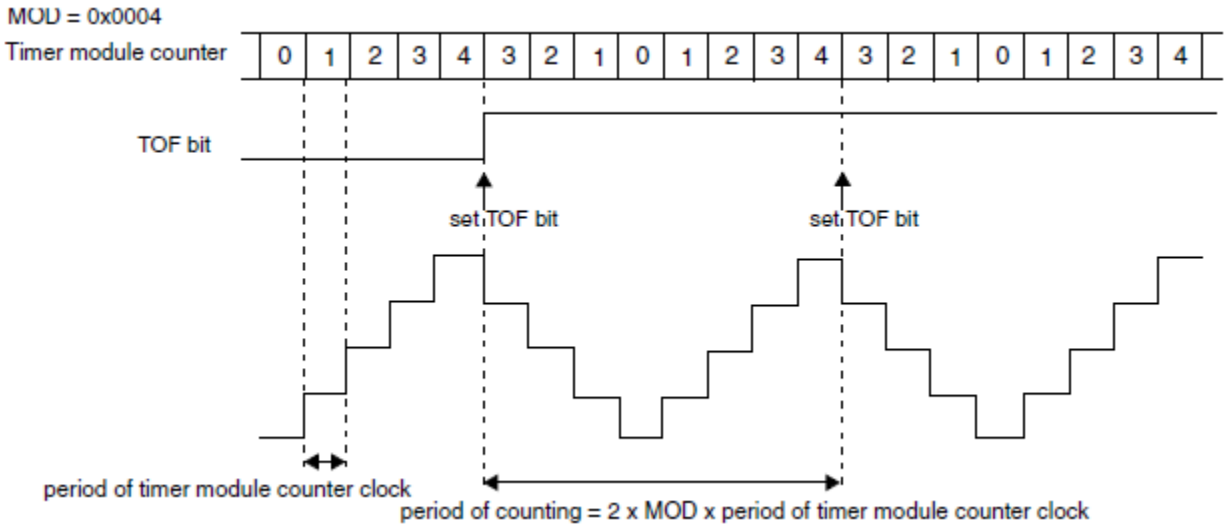
Modes of Operation - Counter

- **Up Counting (CPWMS = 0)**
  - The value of zero is loaded into the TPM counter, and the counter increments until the value of MOD is reached, at which point the counter is reloaded with zero.
  - The TPM period when using up counting is (MOD + 0x0001) × period of the TPM counter clock.
  - The TOF bit is set when the TPM counter changes from MOD to zero.



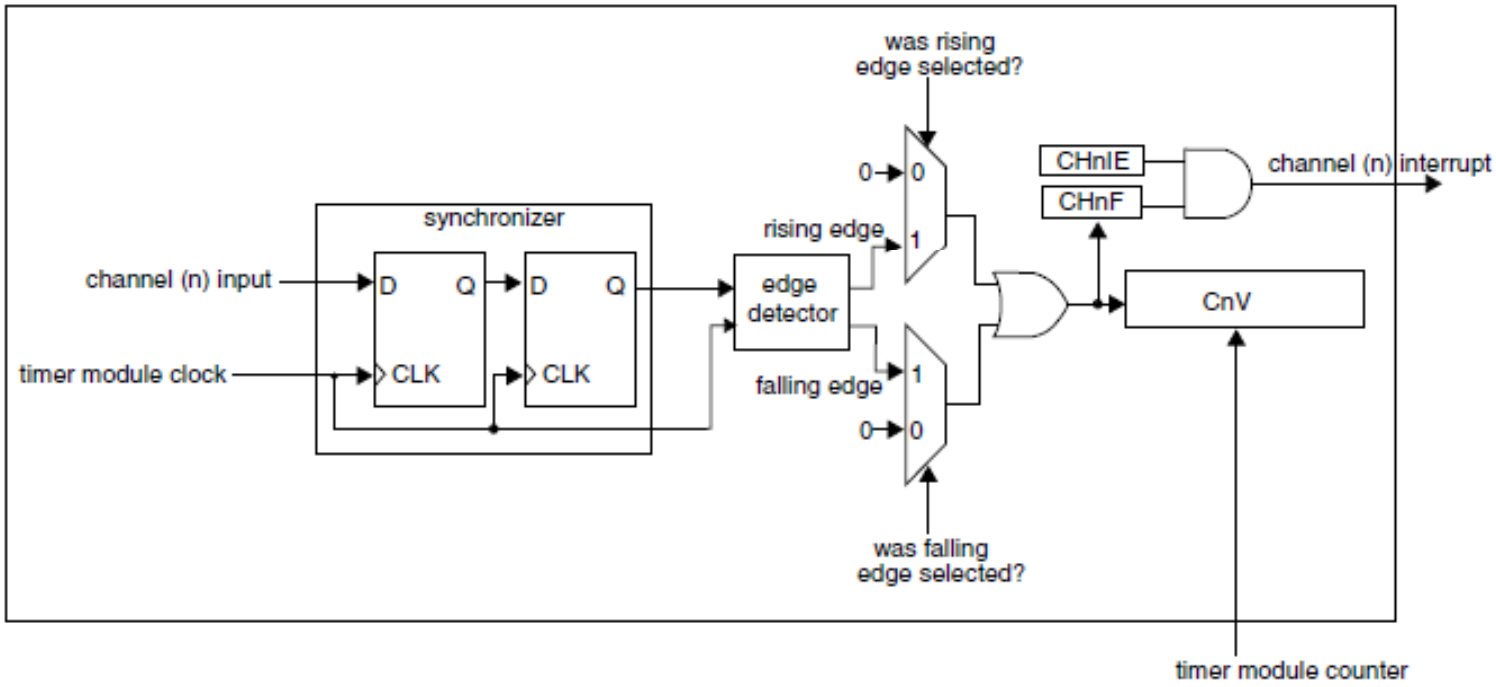
Modes of Operation - Counter

- Up-Down Counting (CPWMS = 1)
  - The value of zero is loaded into the TPM counter, and the counter increments until the value of MOD is reached, at which point the counter is decremented until it returns to zero and the up-down counting restarts.
  - The TPM period when using up-down counting is 2 × MOD × period of the TPM counter clock.
  - The TOF bit is set when the TPM counter changes from MOD to (MOD – 1).



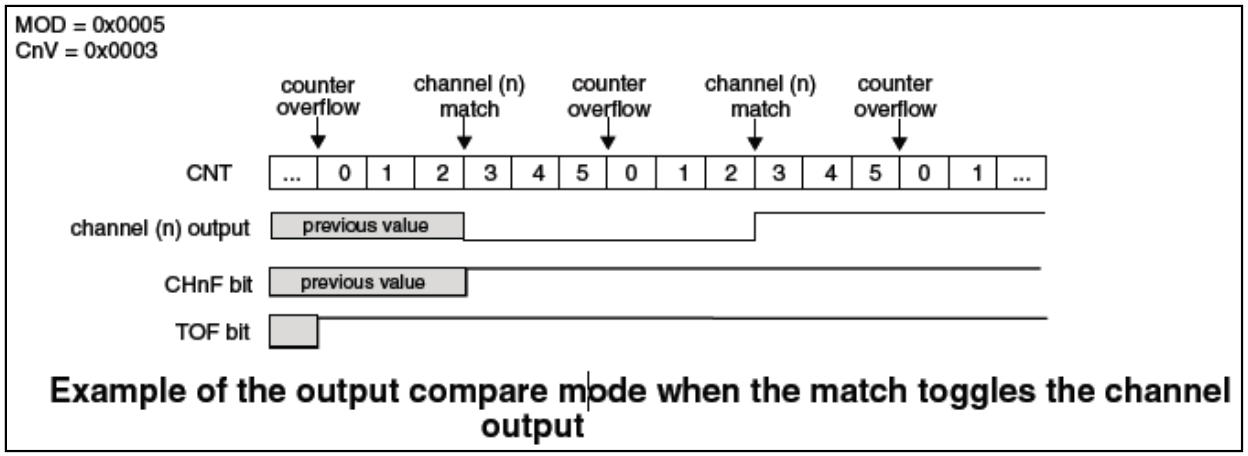
Modes of Operation - Input Capture Mode

- The input capture mode is selected when (CPWMS = 0), (MSnB:MSnA = 0:0), and (ELSnB:ELSnA ≠ 0:0).



Modes of Operation – Output Compare Mode

- The output compare mode is selected when (CPWMS = 0), and (MSnB:MSnA = 0:1)

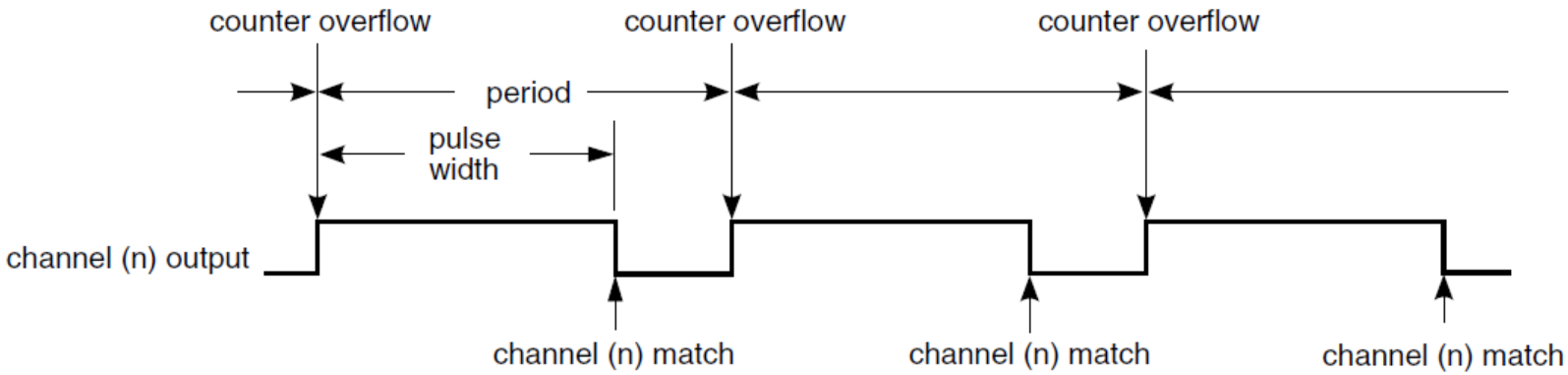


Example of the output compare mode when the match toggles the channel output

- In output compare mode, the TPM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnV register of an output compare channel, the channel (n) output can be set, cleared, or toggled.

Modes of Operation – Edge-Aligned PWM (EPWM) Mode

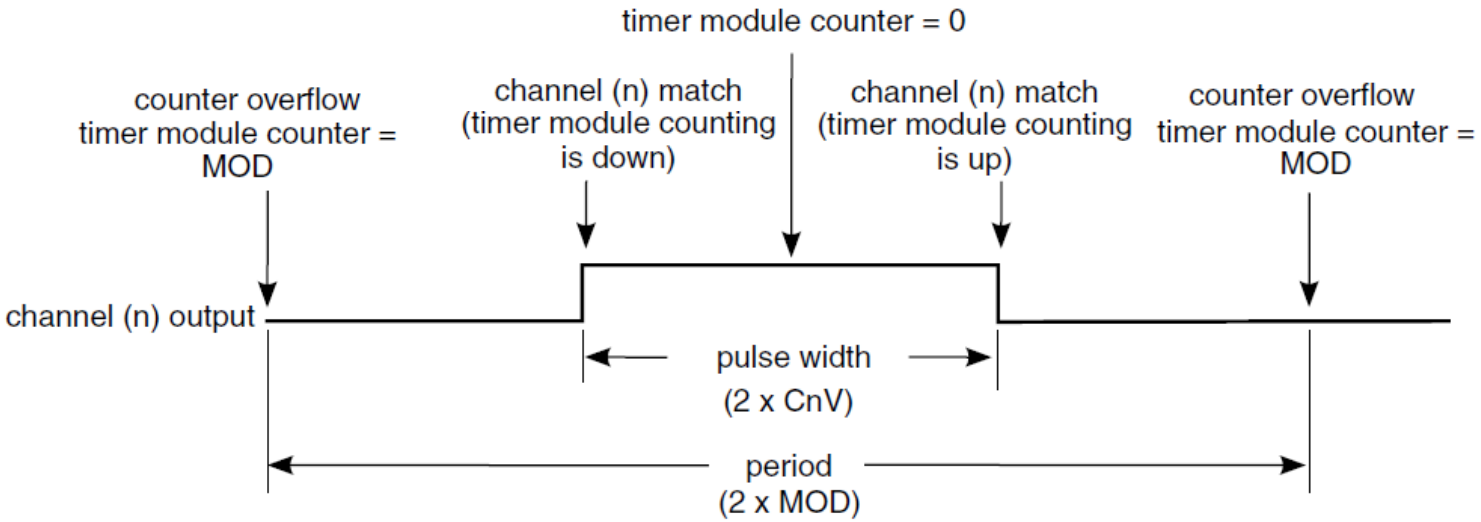
- The edge-aligned mode is selected when (CPWMS = 0), and (MSnB:MSnA = 1:0). The EPWM period is determined by (MOD + 0x0001) and the pulse width (duty cycle) is determined by CnV



[ELSnB:ELSnA = 1:0] High-true pulses (clear Output on match, set Output on reload)

Modes of Operation – Center-Aligned PWM (CPWM) Mode

- The center-aligned mode is selected when (CPWMS = 1) and (MSnB:MSnA = 1:0)
- The CPWM pulse width (duty cycle) is determined by 2 × CnV and the period is determined by 2 × MOD



[ELSnB:ELSnA = 1:0] High-true pulses (clear Output on match-up, set Output on match-down)

Hands-On

- Timer Overflow Interrupt
- Output Compare
- PWM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