Introduction to Ethernet-capable Processors for Automotive

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FAE - Automotive
Ethernet

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SECURE CONNECTIONS
FOR A SMARTER WORLD

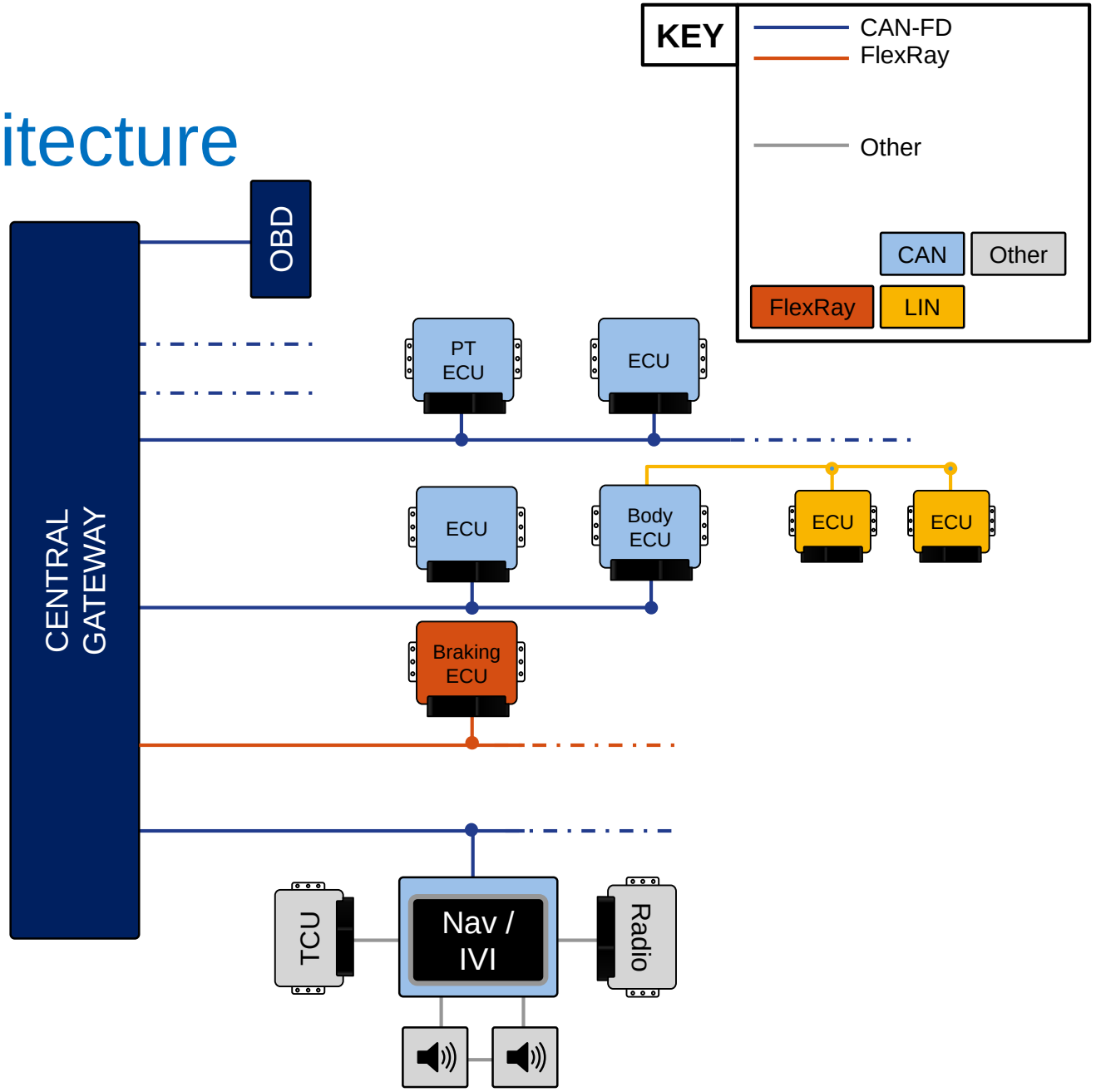
Agenda

- Introduction
- Ethernet in Automotive
- OSI model
- FEC and ENET Ethernet Blocks
- Device Specific Ethernet implementation
  - S32K, S32x and MPC57xx and i.MX
- DPAA-based Ethernet Blocks
- Device Specific Ethernet implementation
  - QorIQ Layerscape Series for Automotive
- Switches and PHYs
- Closing Remarks and Summary

Gateway Evolution - Architectures

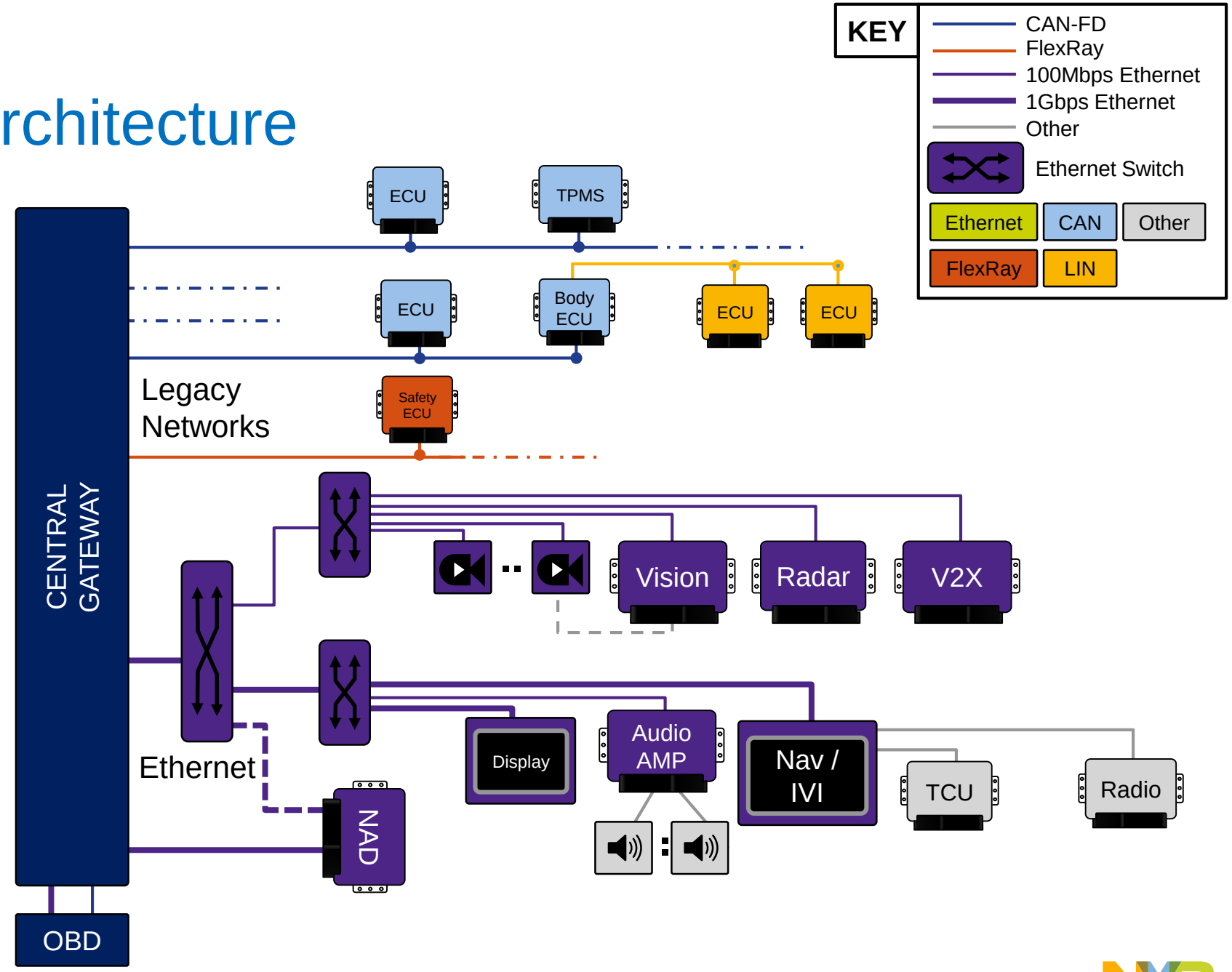
CAN Central Gateway Architecture

- Legacy Automotive Networks
  - Typically 3-8 CAN networks
  - Typically 1-2 FlexRay networks
- Increased bandwidth
  - but, small compared to consumer / networking world
  - Proprietary protocols for higher bandwidth (e.g. MOST)
- Physical Isolation
  - Functional domains
  - Safety / Non-safety
- Gateway role
  - Firewall internal traffic
  - Protocol translation



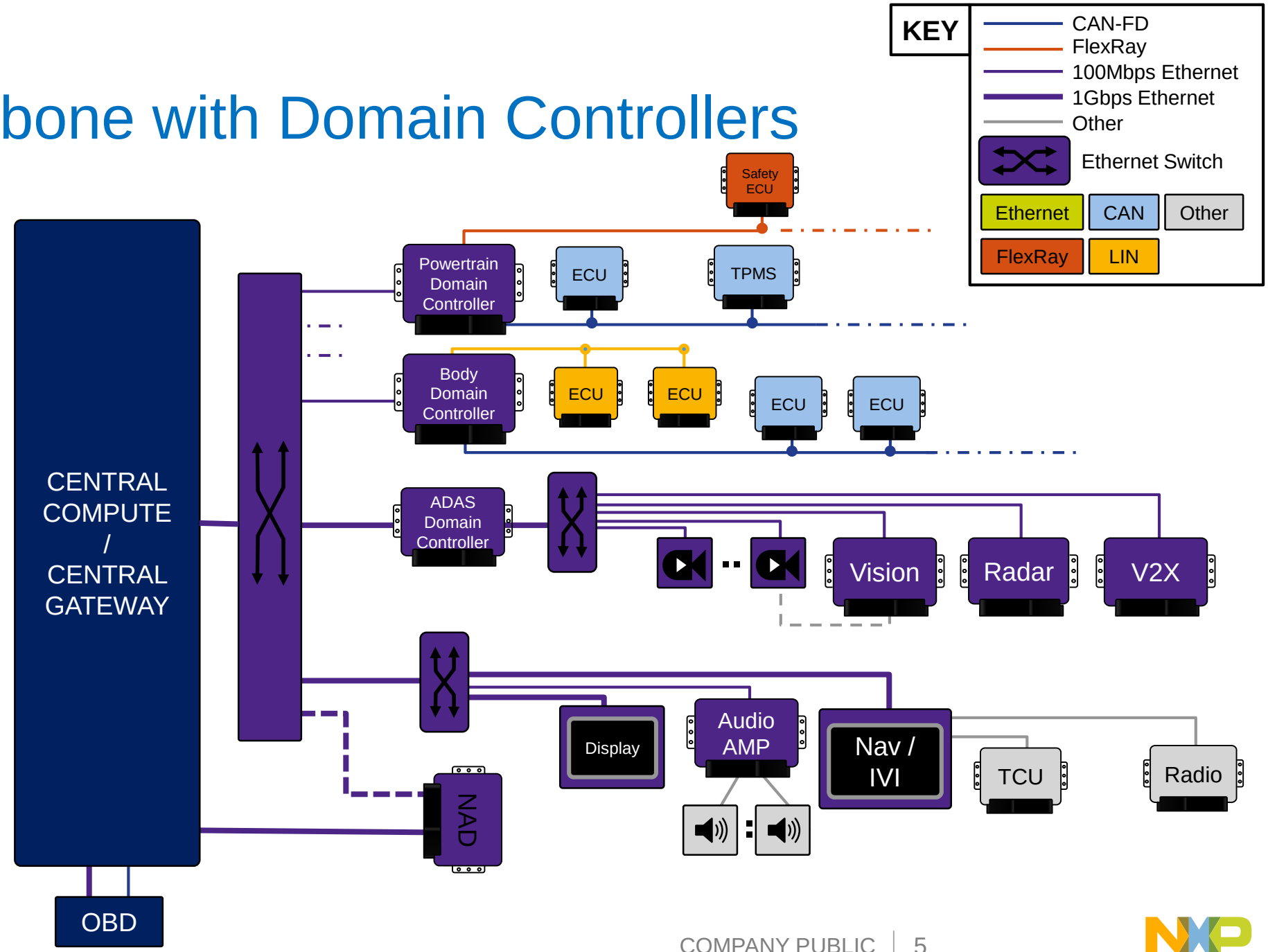
Hybrid Ethernet Architecture

- Legacy + Ethernet Networks
  - CAN, FlexRay & Ethernet
- High-bandwidth Data
  - 100Mbit →1Gbit Ethernet
  - ADAS and Infotainment drive higher data rates
  - Improved ECU program time in factory
- Gateway role
  - Firewall internal & external
  - Efficient protocol translation
  - ECU consolidation
  - New apps & services



Ethernet Backbone with Domain Controllers

- **Ethernet Backbone with Domain Controllers**
  - ECU consolidation
  - Distributed gateway
- Central Compute
  - Strategy / Decision making
  - Distributed vs Centralized



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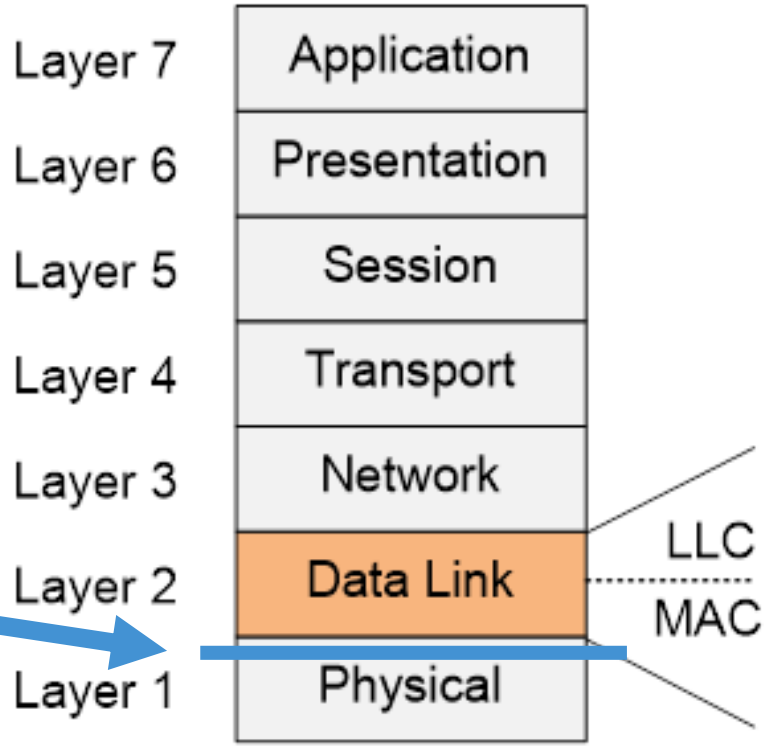
A quick visit of the OSI model

xMII - Media Independent Interface



Industry Standard interface definition sitting effectively between The Data Link Layer and the Physical Layer

- MII, MII-Lite, RMII, GMII, RGMII, SGMII, 7-wire

LLC = Logical Link Control

MAC = Media Access Control

10/100BASE-T1 PHY

- Standardized in IEEE 802.3bw-2015 Clause 96, the data is transmitted over a **single copper pair**, 3 bits/states per symbol (PAM3).
- It supports **only full-duplex**, transmitting in both directions simultaneously.
- The twisted-pair cable is required to support 66 MHz, with a maximum length of 15 m.
- No specific connector is defined.
- The standard is intended for **automotive applications** or when Fast Ethernet is to be integrated into another application. It has been developed as BroadR-Reach before IEEE standardization.[9]

PAM3 = Pulse-amplitude Modulation with 3 bits/states per symbols (+1, 0, -1)
http://www.ieee802.org/3/cg/public/May2017/Graber_3cg_08a_0517.pdf

1000BASE-T1

- IEEE 802.3 standardized 1000BASE-T1 in IEEE Std 802.3bp-2016.
- It defines **Gigabit Ethernet over a single twisted pair** for automotive and industrial applications.
- It includes cable specifications for **15 meters (type A)** or **40 meters (type B)** reach.
- The transmission is done using PAM-3 at 750 MBd.
- The cable must be capable of transmitting 600 MHz for 1000BASE-T1 (as opposed to 66MHz for 100BASE-T1) – needs better guaranteed signal integrity properties

Summary of 2 wire PHY characteristics

Comparison of twisted pair based Ethernet Physical transport layers (TP-PHYs)[20]

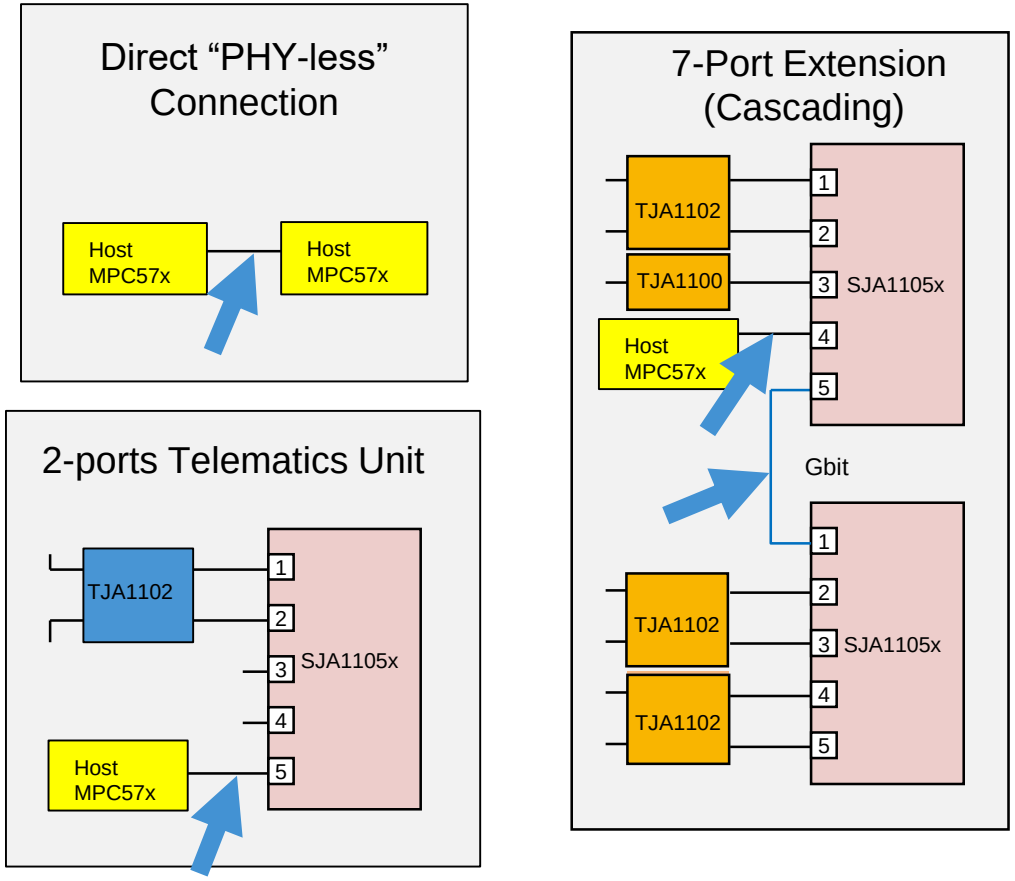
Name	Standard	Status	Speed (Mbit/s) [A]	Pairs required	Lanes per direction	Bits per hertz [B]	Line code	Symbol rate per lane (MBd)	BW[C] (MHz)	Max distance (m)	Cable req. [D]	Cable rating (MHz)	Usage
100BASE-T1	802.3bw-2015 (CL96)	Current	100	1	1	3	PAM-3 4B/3B	66.66...	33.33...	15	Cat 5e	100	Automotive IoT & M2M
1000BASE-T1	802.3bp-2016	Current	1000	1	1	2.66...	PAM-3 80B/81B RS-FEC	750	375	40	Cat 6A	500	Automotive IoT & M2M

Note: select table rows from public Wiki page

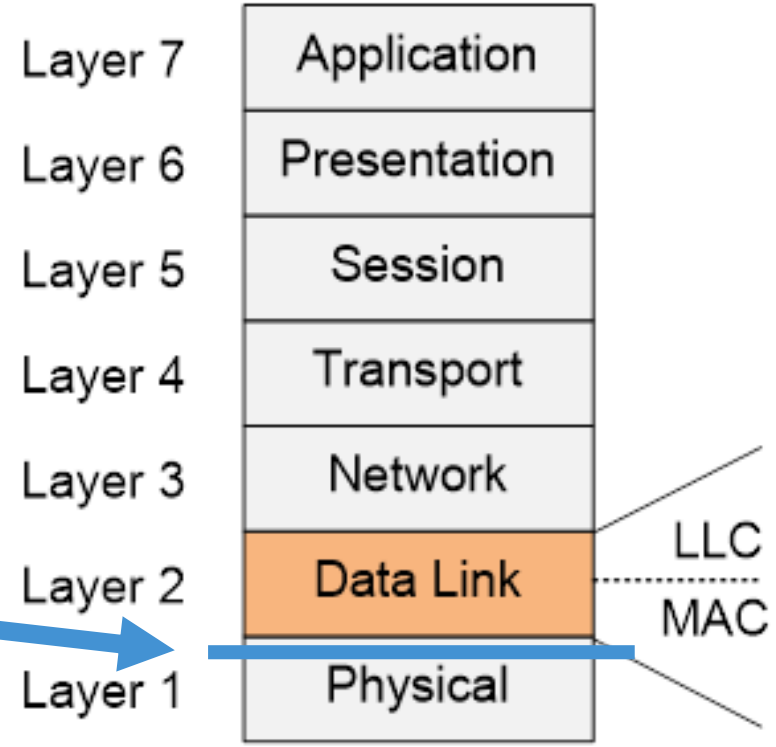
Link: https://en.wikipedia.org/wiki/Ethernet_over_twisted_pair

“PHY-less” connections to a switch or another CPU

- Direct xMII to xMII connections
- No separate (external) PHY device

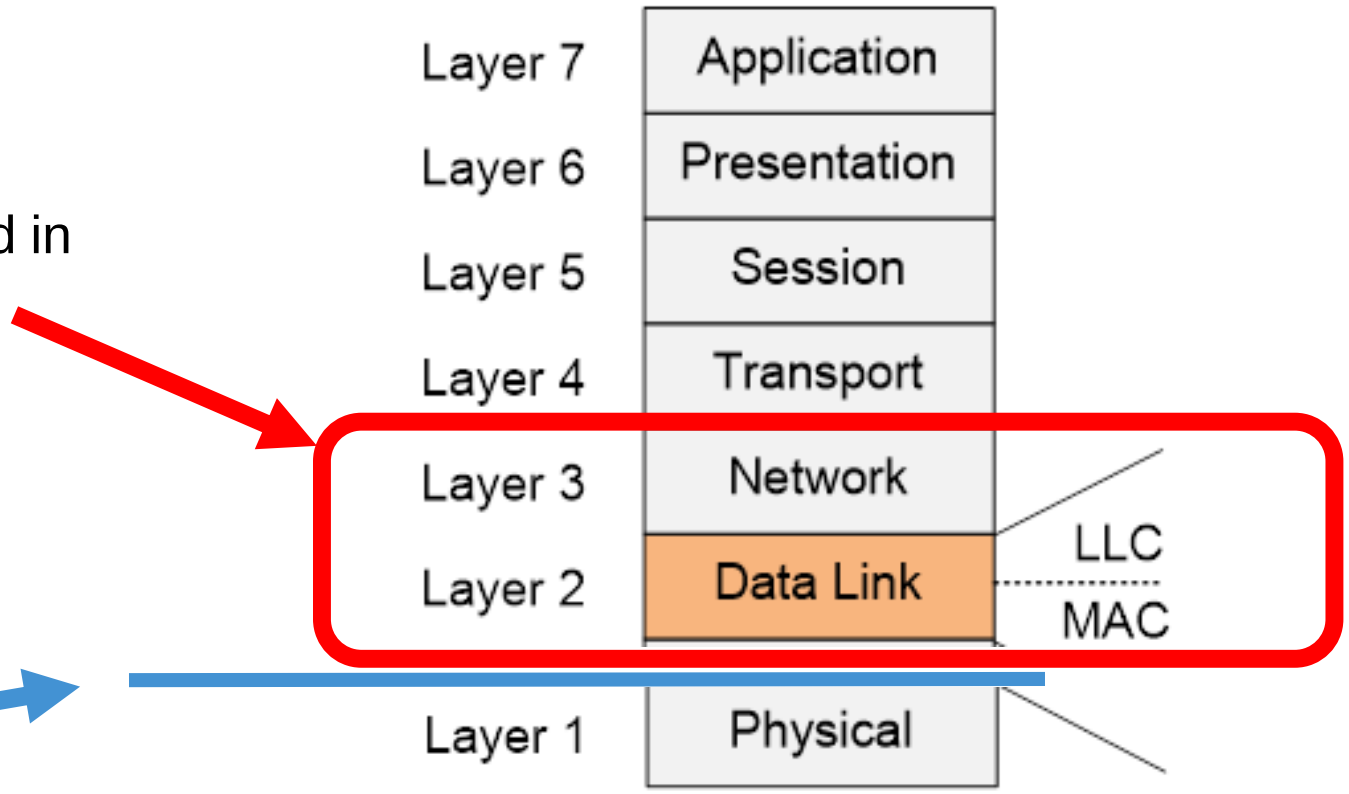


xMII - Media Independent Interface



The Ethernet Block

The Ethernet blocks in this session are generally focused in this part of the OSI model



xMII - Media Independent Interface

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FEC

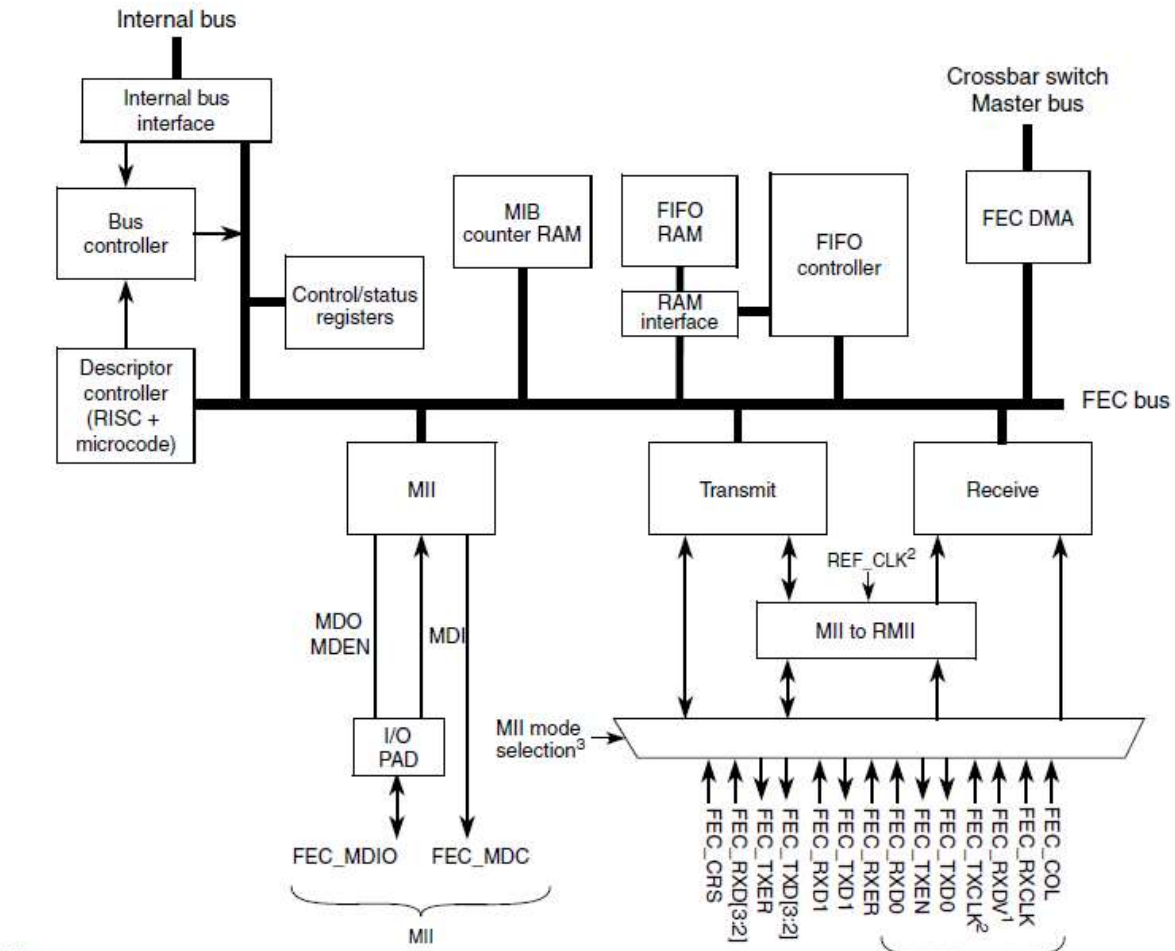
10/100Mb Fast Ethernet Controller

FEC (Fast Ethernet Controller) - Introduction

- The Fast Ethernet Controller (FEC) is a communication controller that supports 10 and100 Mbps Ethernet/IEEE 802.3 networks.
- An external transceiver interface and transceiver function are required to complete the interface to the media.
- These are the different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver.
  - The FEC supports the 10/100 Mbps MII-Lite, 10/100 Mbps reduced MII, and the 10 Mbps-only 7-wire interface.

FEC Block Diagram

- The FEC is implemented with a combination of hardware and microcode.
- The off-chip (Ethernet) interfaces are compliant with industry and IEEE 802.3 standards.



Notes:

1. FEC_RXDV in RMII mode generates RXDV and CRS.
2. FEC_TXCLK in RMII mode is the reference clock for the RMII; the RMII supplies the FEC's receive and transmit clocks depending upon the assertion of RCR[RMII_10T].
3. Interface selection is chip-specific; see the chapter that describes how modules are configured and connected.

FEC Features

- The FEC incorporates the following features:
- For interface selection options, see the chip-specific FEC information.
  - 100-Mbps IEEE 802.3 MII-Lite
  - 10-Mbps IEEE 802.3 MII-Lite
  - 100-Mbps reduced media independent interface (RMII)
  - 10-Mbps reduced media independent interface (RMII)
  - 10-Mbps 7-wire interface (industry standard)
- IEEE 802.3 full duplex flow control
- Programmable max frame length supports IEEE 802.1 VLAN tags and priority

FEC Features (continued)

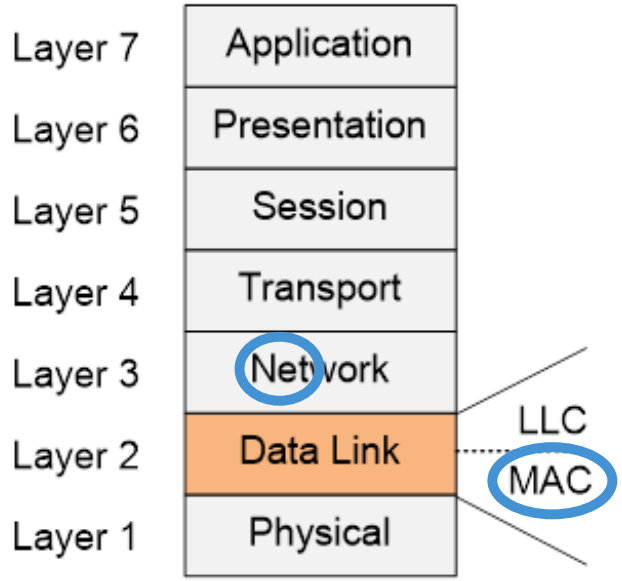
- Support for full-duplex operation (200 Mbps throughput) with a minimum internal bus clock rate of 50 MHz
- Support for half-duplex operation (100 Mbps throughput) with a minimum internal bus clock rate of 25 MHz
- Retransmission from transmit FIFO following a collision (no processor bus utilization)
- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no processor bus utilization)
- Address recognition
  - Frames with broadcast address may be always accepted or always rejected
  - Exact match for single 48-bit individual (unicast) address
  - Hash (64-bit hash) check of individual (unicast) addresses
  - Hash (64-bit hash) check of group (multicast) addresses
  - Promiscuous mode

ENET

10/100Mb or 10/100/1000 Mb Ethernet Interface

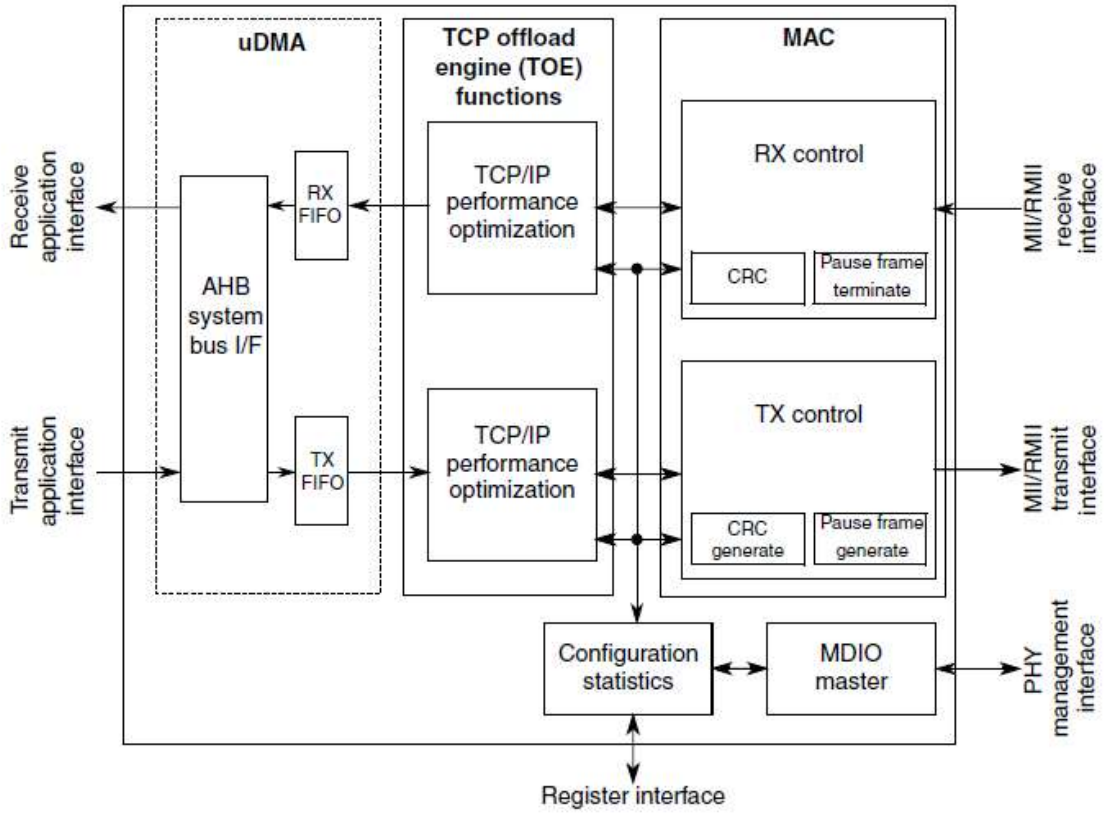
ENET - Introduction

- May be 10/100Mb or 10/100/1000Mb
- The MAC-NET core, in conjunction with a 10/100/1000-Mbit/s MAC, implements layer 3 network acceleration functions.
- These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP, and ICMP, providing wire speed services to client applications.

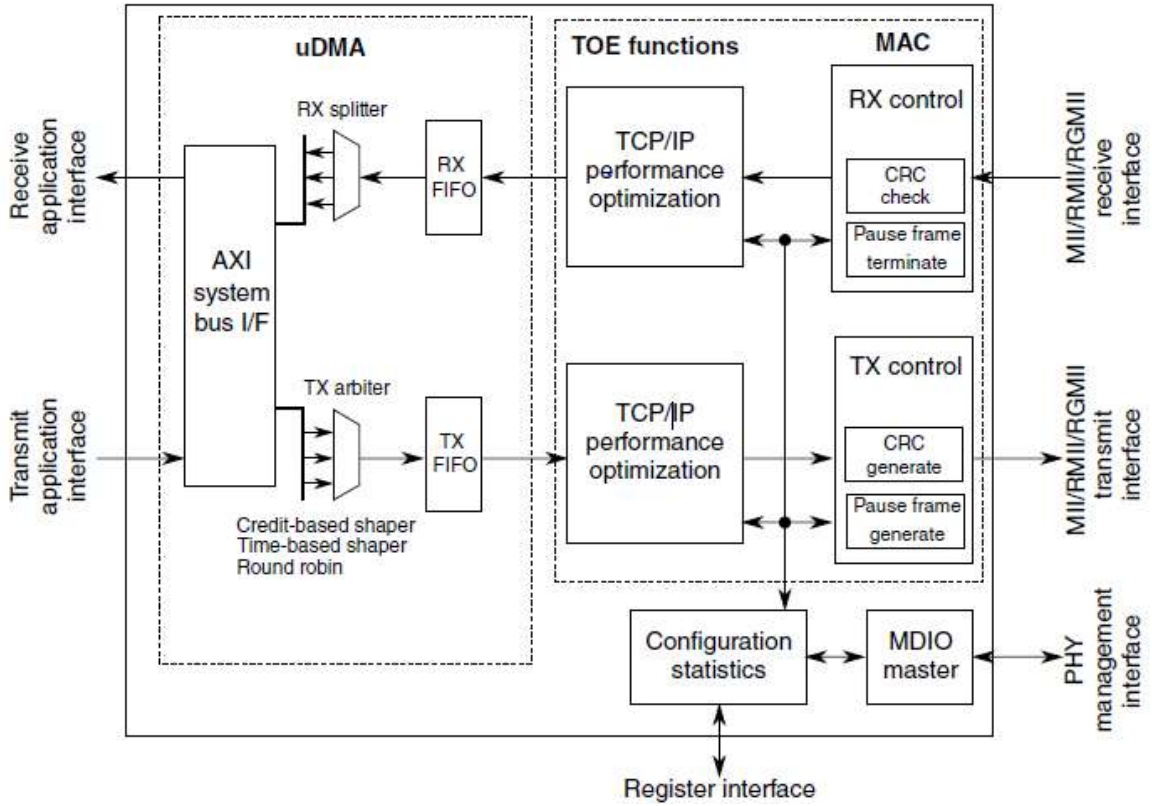


ENET - Ethernet MAC-NET core + MAC block diagram

10/100Mb ENET



10/100/1000Mb ENET



ENET - Overview

- Dual or triple speed implementations
- Half-duplex and full-duplex
- Fully programable MAC operation
- Offload acceleration
- Programmable Embedded FIFO
- Magic Packet Detection
- uDMA
- IEEE1588 support

ENET - Ethernet MAC features

(NOTE: Most items apply to both 10/100Mb and 10/100/1000Mb implementations)

- Implements the **full 802.3 specification** with preamble/SFD generation, framepadding generation, CRC generation and checking
- Supports zero-length preamble
- **Dynamically configurable to support 10/100-Mbit/s and gigabit operation**
- **Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation**
- **Supports gigabit full-duplex operation**
- Compliant with the AMD **magic packet detection** with interrupt for node remote power management
- Seamless interface to commercial ethernet PHY devices via one of the following:
  - a 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz.
  - a 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz.
  - a 2-bit Reduced MII (RMII) operating at 50 MHz.
  - a (double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz. → Applies to Gb Interfaces
  - Simple 64-bit FIFO user-application interface

ENET - Ethernet MAC features (continued 1 of 4)

- **CRC-32 checking at full speed** with optional forwarding of the frame check sequence (FCS) field to the client
- **CRC-32 generation** and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- **In full-duplex mode**:
  - Implements automated pause frame (802.3 x31A) generation and termination, providing flow control without user application intervention
  - Pause quanta used to form pause frames — dynamically programmable
  - **Pause frame generation** additionally controllable by user application offering flexible traffic flow control
  - Optional forwarding of received pause frames to the user application
  - Implements **standard flow-control mechanism**
- **In half-duplex mode: provides full collision support**, including jamming, backoff, and automatic retransmission
- Supports VLAN-tagged frames according to IEEE 802.1Q

ENET - Ethernet MAC features (continued 2 of 4)

- **Programmable MAC address**: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- **Programmable promiscuous mode** support to omit MAC destination address checking on receive
- **Multicast and unicast address filtering** on receive based on 64-entry hash table, reducing higher layer processing load
- **Programmable frame maximum length** providing support for any standard or proprietary frame length

ENET - Ethernet MAC features (continued 3 of 4)

- **Statistics indicators** for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels
- Provides separate status word for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information
- Multiple **internal loopback** options
- MDIO master interface for PHY device configuration and management supports two programmable MDIO base addresses, and standard (IEEE 802.3 Clause 22) and extended (Clause 45) MDIO frame formats
- **Supports legacy FEC buffer descriptors**

ENET - Ethernet MAC features (continued 4 of 4)

(NOTE: Items on this page mostly apply to Gb interfaces)

- **Interrupt coalescing** reduces the number of interrupts generated by the MAC, reducing CPU loading
- **Traffic-shaping bandwidth distribution** supports credit-based and round-robin-based policies. Either policy can be combined with time-based shaping.
- AVB (**Audio Video Bridging**, IEEE 802.1Qav) features:
  - Credit-based bandwidth distribution policy can be combined with time-based shaping
  - AVB endpoint talker and listener support
  - Support for arbitration between different priority traffic (for example, AVB class A, AVB class B, and non-AVB)
- **Receive frame parser** enables flexible Ethernet frame pattern matching in order to finally accept or reject a frame.

ENET - IP protocol performance optimization features

(NOTE: Applies to both 10/100Mb and 10/100/1000Mb implementations)

- **Operates on TCP/IP and UDP/IP and ICMP/IP protocol data or IP header only**
- **Enables wire-speed processing**
- Supports IPv4 and IPv6
- Transparent passing of frames of other types and protocols
- Supports VLAN tagged frames according to IEEE 802.1q with transparent forwarding of VLAN tag and control field
- Automatic IP-header and payload (protocol specific) checksum calculation and verification on receive
- Automatic IP-header and payload (protocol specific) checksum generation and automatic insertion on transmit configurable on a per-frame basis
- Supports IP and TCP, UDP, ICMP data for checksum generation and checking

ENET - IP protocol performance optimization features (continued)

- Supports full header options for IPv4 and TCP protocol headers
- Provides IPv6 support to datagrams with base header only — datagrams with extension headers are passed transparently unmodifed/unchecked
- Provides statistics information for received IP and protocol errors
- Configurable automatic discard of erroneous frames
- Configurable automatic host-to-network (RX) and network-to-host (TX) byte order conversion for IP and TCP/UDP/ICMP headers within the frame
- Configurable padding remove for short IP datagrams on receive
- Configurable Ethernet payload alignment to allow for 32-bit word-aligned header and payload processing
- Programmable store-and-forward operation with clock and rate decoupling FIFOs

ENET - IEEE 1588 features

(NOTE: Applies to both 10/100Mb and 10/100/1000Mb implementations)

- **Supports all IEEE 1588 frames**.
- Allows reference clock to be chosen independently of network speed.
- Software-programmable precise time-stamping of ingress and egress frames
- Timer monitoring capabilities for system calibration and timing accuracy management
- **Precise time-stamping of external events** with programmable interrupt generation
- **Programmable event and interrupt generation** for external system control
- Supports hardware- and software-controllable timer synchronization.
- **Provides a 4-channel IEEE 1588 timer**. Each channel supports input capture and output compare using the 1588 counter.

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S32K1xx Series

32-bit General Purpose Automotive Microcontrollers

S32K148 Processor Block Diagram

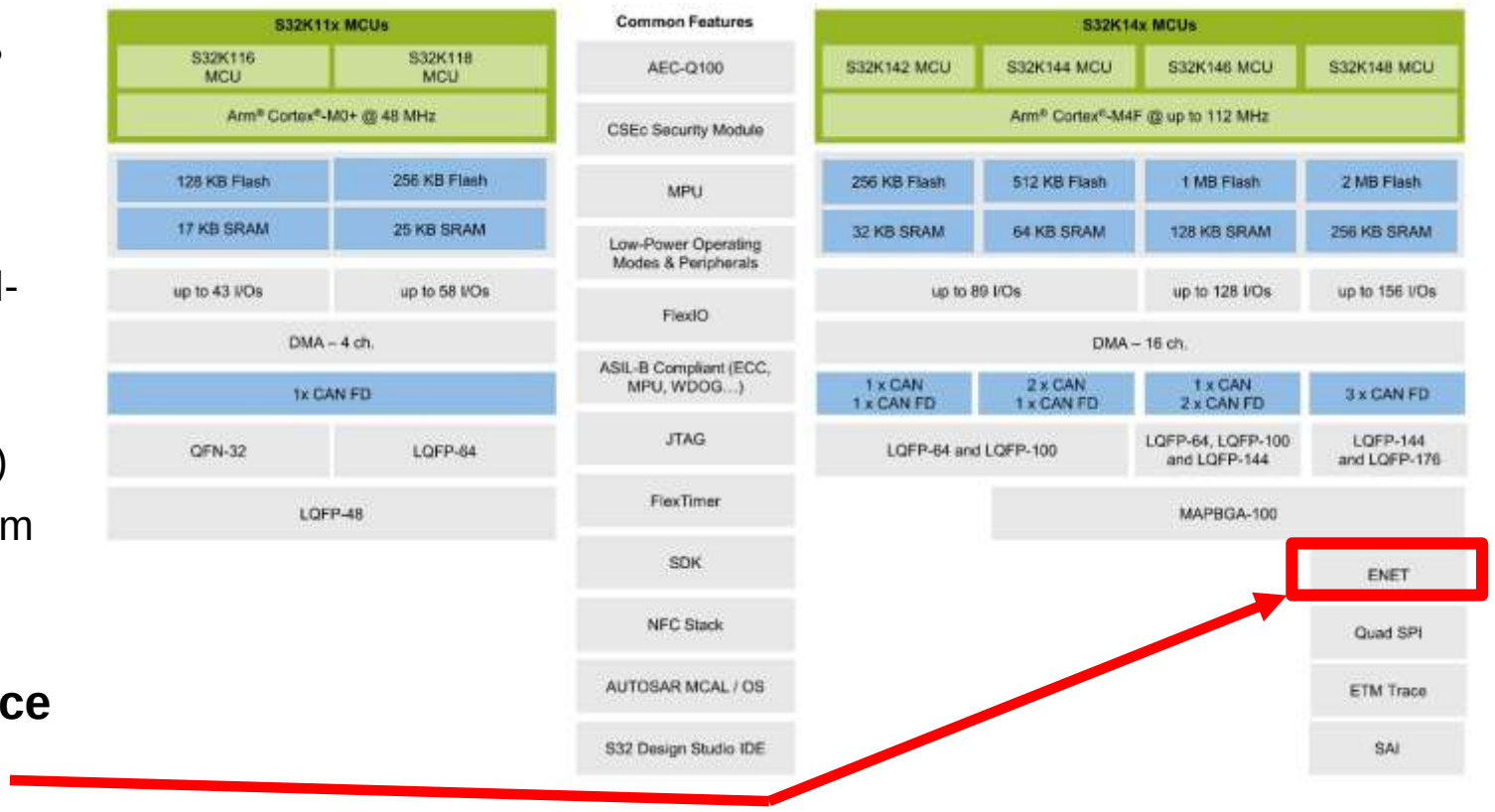
Target Application - **Automotive Sensor Fusion Systems**

Features

- 32-bit Arm Cortex-M4F core with FPU, up to 112 MHz (HSRUN) and 80 MHz (Normal RUN)
- Up to 2 MB code flash memory and 64 KB FlexMem
- Up to 256 KB SRAM
- Integrated clocking architecture
- Analog modules providing precision mixed-signal capabilities
- Power Management Controller (PMC)
- Wide operating voltage ranges (2.7–5.5 V)
- Ambient operating temperature ranges from –40 °C to 125

- **1x 10/100Mb ENET Ethernet Interface**

NOTE: Only S32K148 has an Ethernet Interface. All other S32K1xx series do not have (ENET) Ethernet capabilities.



S32K1xx - Summary Table of Ethernet Capability

Part Number	Description	Supported Ethernet Rate	Ethernet MAC	Supported Media Interface	Hardware Acceleration
S32K148	General Purpose Microcontroller	1x 10/100Mb	ENET (MAC-NET core + MAC)	MII, MII-Lite, RMII	Layer 3 IP, TCP, UDP, and ICMP
…	…	…	…	…	…
S32Kxxx					

MII-Lite = MII without the CRS and COL signals

S32 Platform

World’s First Fully Scalable Automotive Computing Architecture

NXP's Next Generation

S32x Automotive Processing Platform

World's First Fully Scalable Computing Architecture Meets the Challenges

- Industry leading performance and scalability across multiple application domains
- Reliable automotive-grade technology platform
- Common hardware and software delivers safety, security, and over-the-air updates

Performance 10X

Software Reuse Up to 90%

Safe ASIL-D Fault-Tolerant

Secure End-to-end throughout car

OTA Fault recovery rollbacks

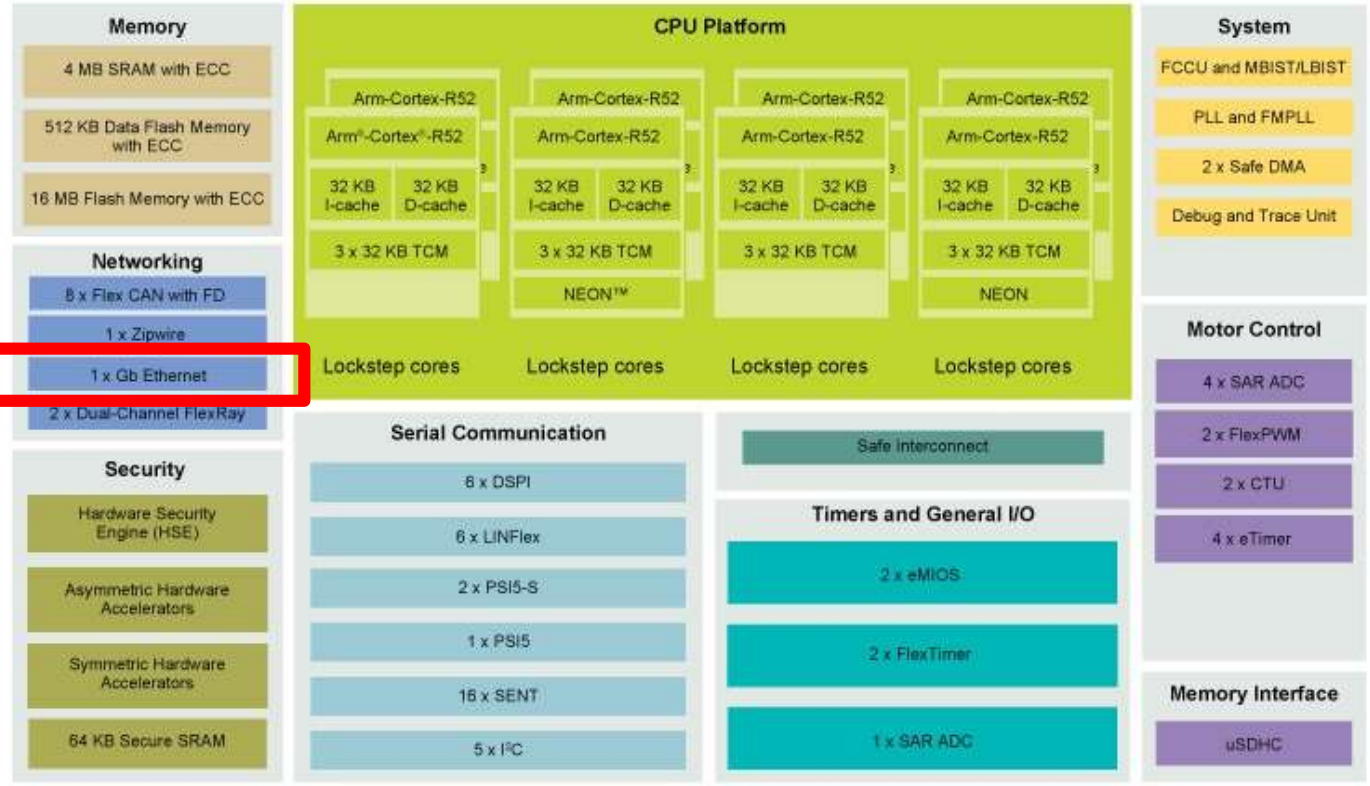
Arm Cortex®-M, -R and -A cores on common platform

S32S24 Processor Block Diagram

Features

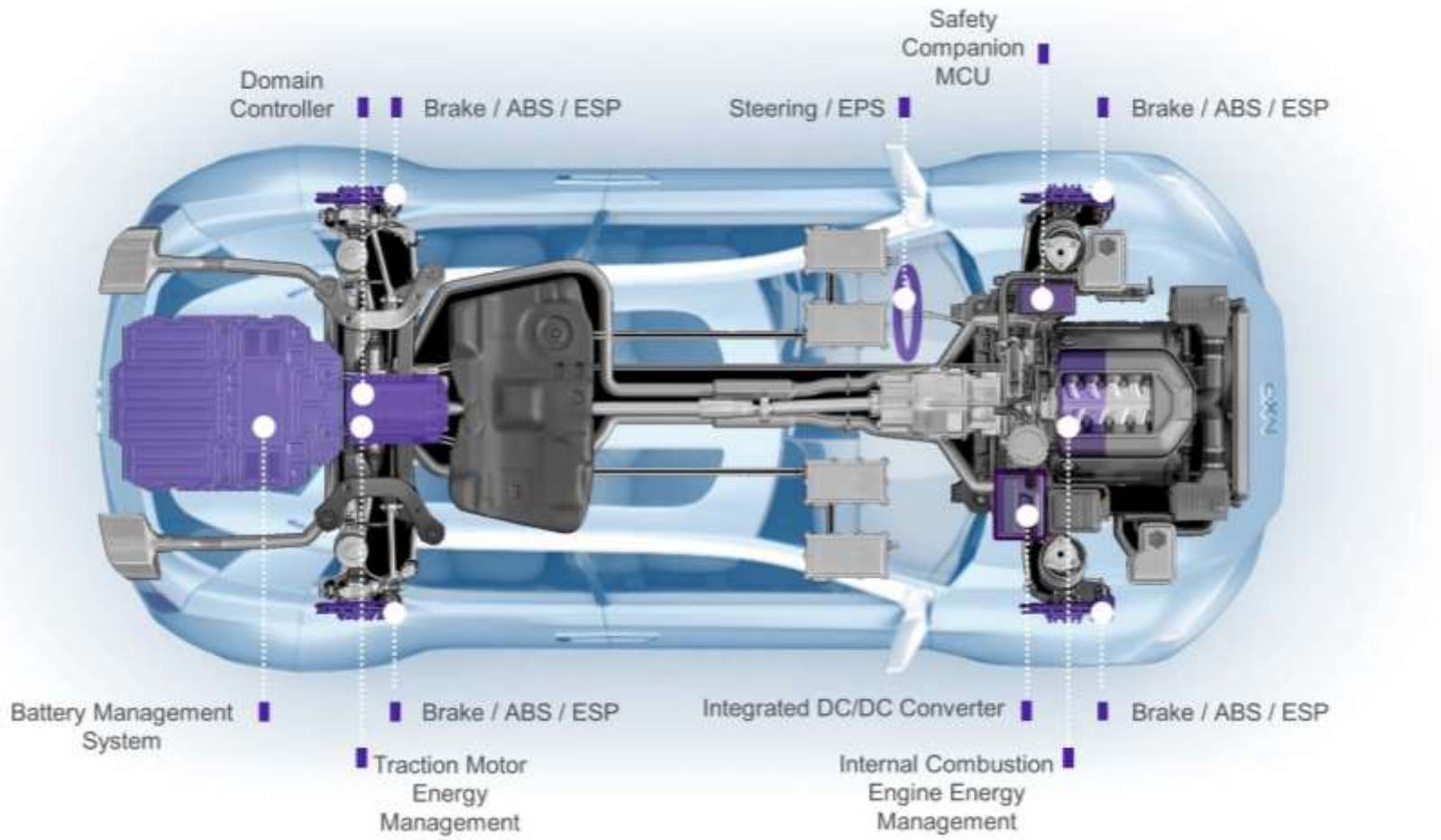
- 4 x Arm-R52 cores in lockstep (8 cores total), operating at 800 MHz
- Large integrated flash memory (up to 64 Mbytes)
- On-the-Fly, Over-the-Air update capability with zero processor downtime
- Advanced safety functionality and fault recovery to **support ASIL-D applications**
- Hardware Security Engine supporting public and private key encryption
- **AEC-Q100 Grade 1** device with support up to -40 to 150º C (junction)
- Preproduction

The first product release from the S32 Automotive Processing Platform



1x 1Gb ENET Ethernet Interface

S32S Target Applications - Safety Microcontroller

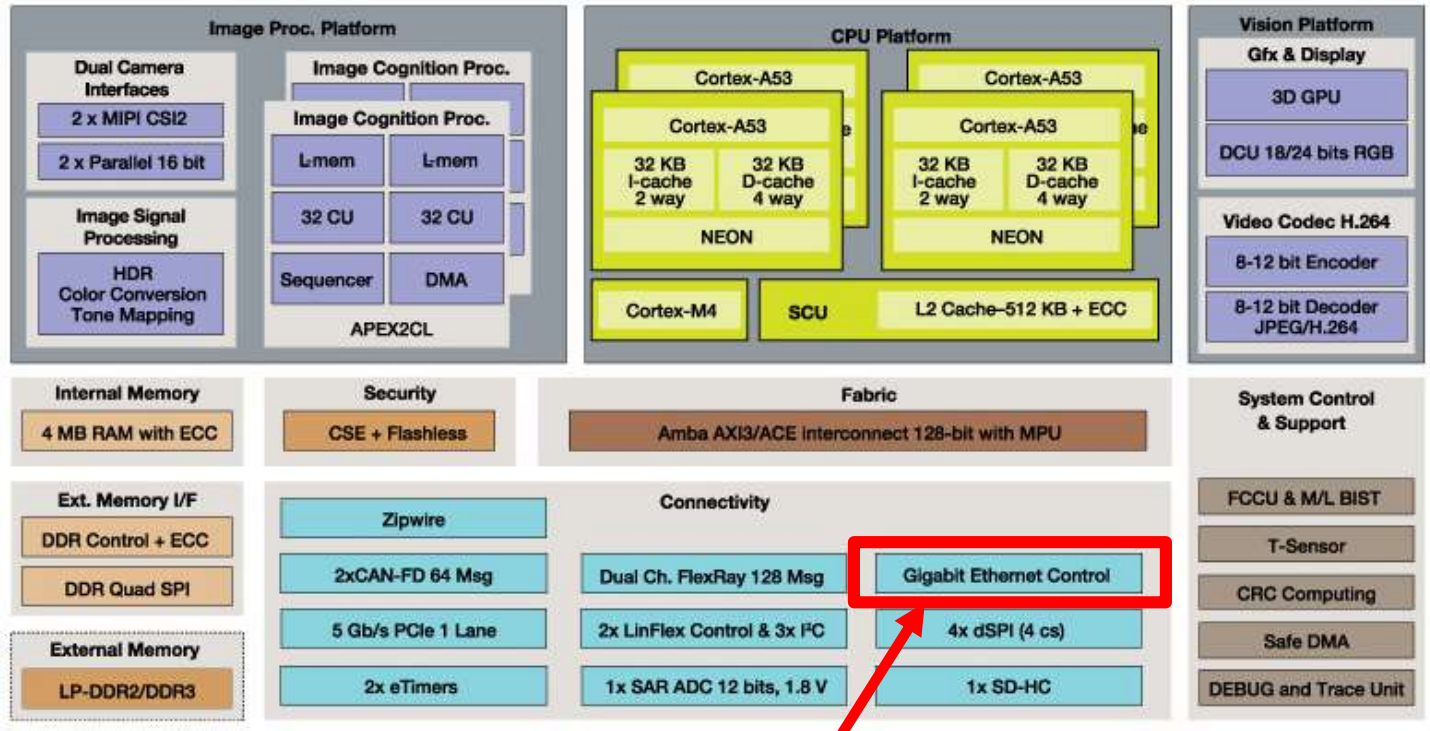


- **Active Suspension**
- **Braking and Stability Control**
- **Electric Power Steering (EPS)**
- **Hybrid and Electric Vehicle Powertrain**

S32V234 Processor Block Diagram

Vision Processor for Front and Surround View Camera, Machine Learning and Sensor Fusion Applications

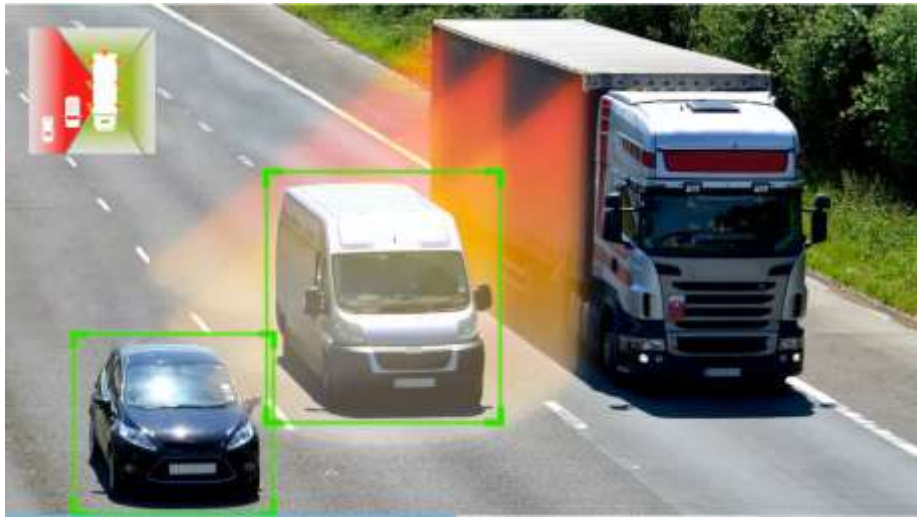
- **Automotive Vision Systems**
- **Front View Camera**
- Intelligent Roadside Unit
- Smart Rear View Camera
- Surround View & Sense Park Assist System
- Surround View Park Assist System
- High-end Automotive Sensor Fusion Systems



1x 1Gb ENET Ethernet Interface

S32V234 Processor Features

- **Quad Arm® Cortex®-A53** cores running up to 1GHz, Plus M4 core up to 133 MHz
- **Dual APEX-2 vision accelerator cores** enabled by OpenCL™, APEX-CV and APEX graph tool
- Supports ISO 26262 functional safety up to **ASIL-C**, IEC 61508 and DO 178 applications
- **3D GPU** (GC3000) with OpenCL 1.2 EP 2.0, OpenGL ES 3.0, OpenVG 1.1
- Hardware security encryption on CSE2
- Embedded image sensor processing (ISP) for HDR, color conversion, tone mapping, etc. enabled by ISP graph tool
- MIPI CSI2 and parallel image sensor interfaces
- 4 MB on-chip system RAM with end-to-end ECC
- DRAM controller support for DDR3 / DDR3L / LPDDR2
- -40 to 125 °C (junction temperature) operation
- 621 FC-BGA 17 mm x 17 mm, 0.65 mm pitch



More Ethernet capable S32x platform devices to come…

1 Based on publicly available competitor roadmap performance statements.
2 Based on analysis of existing NXP software code in existing customers' applications, NXP expects that software reuse will be significant both within domains and across vehicle domains at up to 90 and more than 40 percent respectively.

S32x - Summary Table of Ethernet Capability

Part Number	Description	Supported Ethernet Rate	Ethernet MAC	Supported Media Interface	Hardware Acceleration
S32S24	Safety Microcontroller	1x 10/100/1000Mb	ENET (MAC-NET core + MAC)	MII, MII-Lite, RMII, RGMII	Layer 3 IP, TCP, UDP, and ICMP
S32V234 Dual and Quad core variants	Vision Processor	1x 10/100/1000Mb	ENET (MAC-NET core + MAC)	MII, MII-Lite, RMII, RGMII	Layer 3 IP, TCP, UDP, and ICMP
…	…	…	…	…	…
S32x	More target applications…	More ports…	More capabilities…	More media interfaces…	More acceleration…

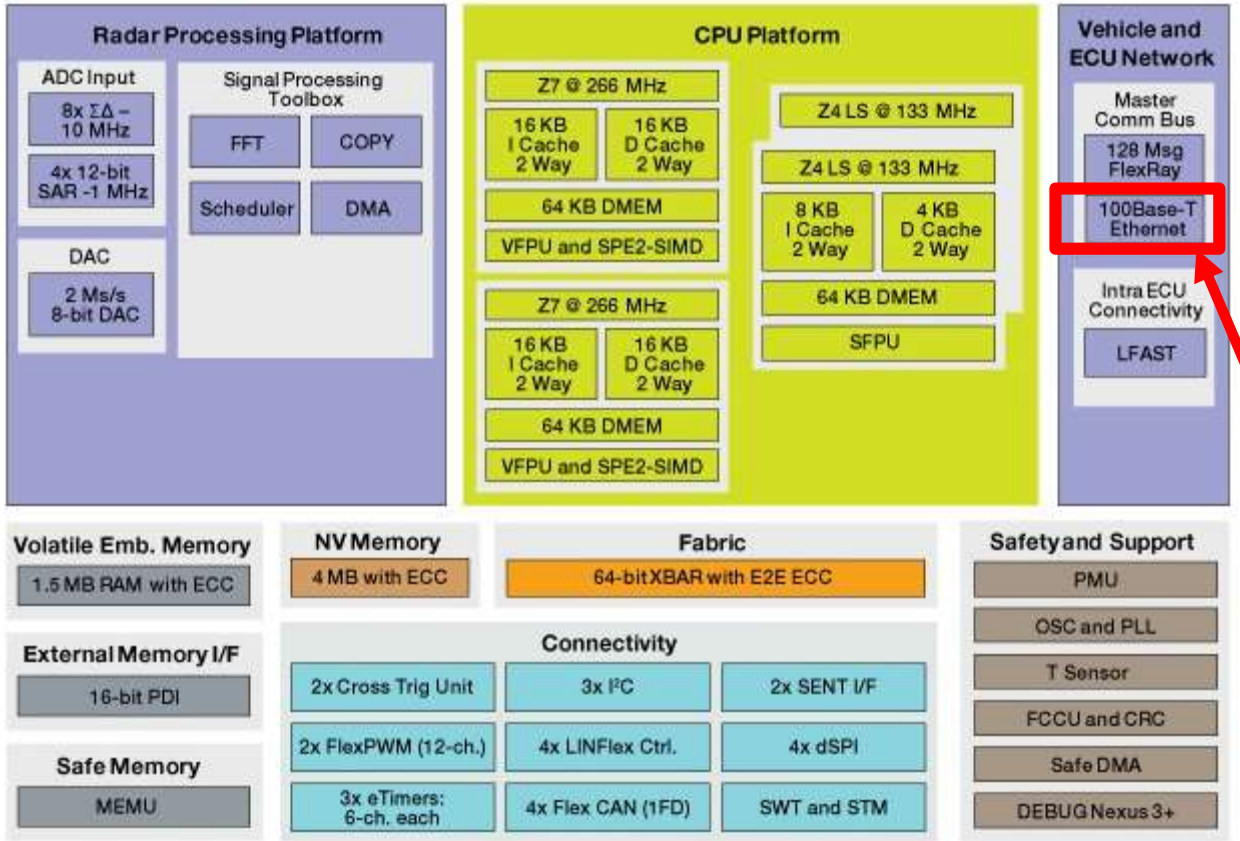
MII-Lite = MII without the CRS and COL signals

MPC57xx Series

Ultra-Reliable MPC57xx 32-bit Automotive and Industrial Microcontrollers (MCUs)

MPC577xK Block Diagram

Ultra-Reliable MPC577xK MCU for Automotive ADAS & Industrial Radar Applications



Target Applications

- Automotive Radar Systems
- Automotive Vision Systems
- Surround View Park Assist System
- Electrical Stability Control (ESC)
- Higher-end Electrical Power Steering (EPS)
- Airbag and sensor fusion applications

Features

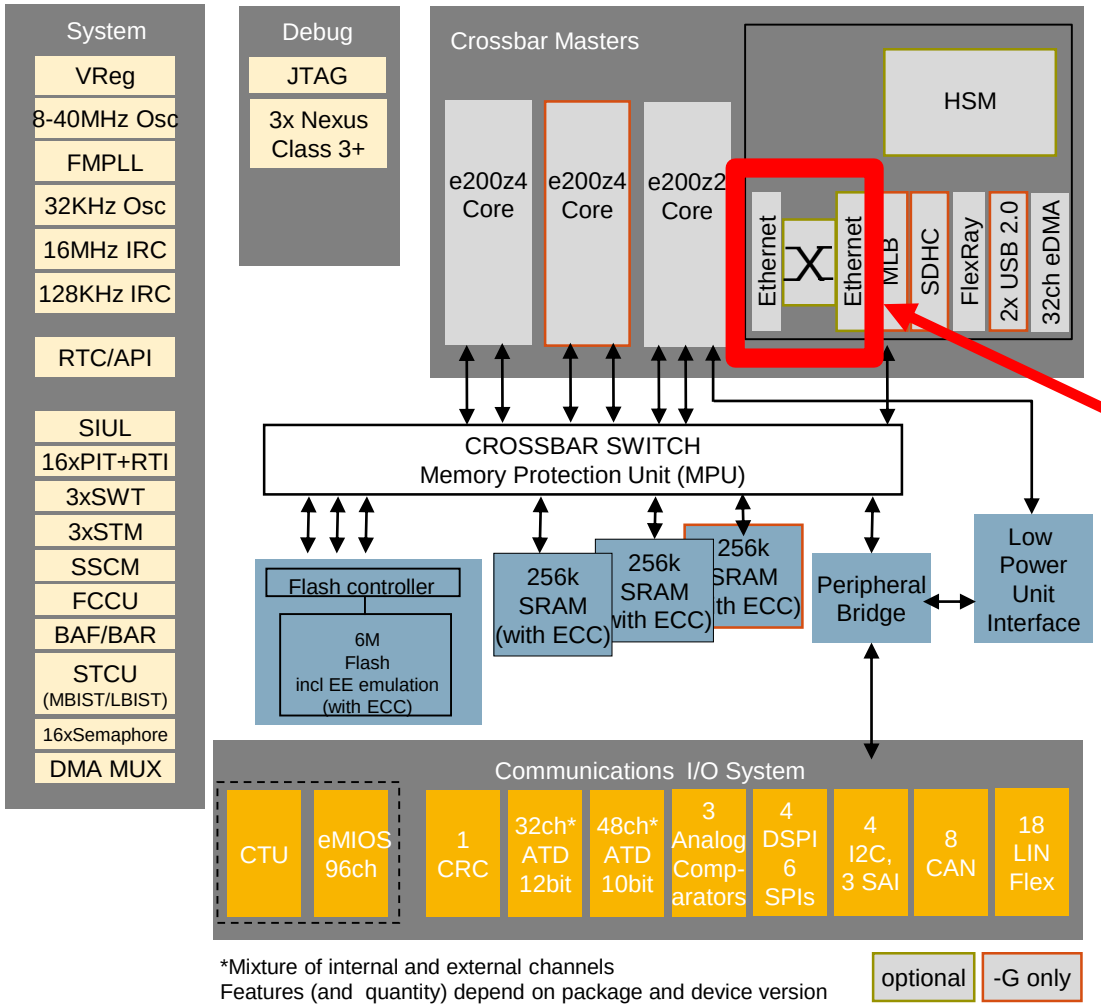
- Processing cores: 2 x e200z7 (266MHz)
- Functional Safety core2: e200z4 in lockstep (133MHz)
- NVM: 4 MB with ECC
- SRAM: 1.5 MB with ECC
- External memory support: 16-bit PDI
- FlexRay, LFAST, CTU, IIC, SENT, FlexPWM, LinFlex, dSPI, eTimers, CAN-FD, SWT, STM

1x 10/100Mb ENET Ethernet

MPC574xB/C/G – Ultra-Reliable MCUs for Automotive & Industrial Control and Gateway

Target Applications

Central Gateway, Infotainment Gateway, Battery Management, High-end Control Module



*Mixture of internal and external channels
Features (and quantity) depend on package and device version

Key Characteristics

- 2x e200z4 + 1x z2 cores, FPU on z4 cores
- 160 MHz max for z4s and 80 MHz on z2
- HSM Security Module option supports both SHE and EVITA low/medium standard
- Media Local Bus supports MOST communication
- 2 x USB 2.0 (1 OTG and 1 Host module) support interfacing to 3G modem and infotainment domain
- Up to 2x Ethernet 10/100 Mbps RMII, MII, +1588, AVB (with optional Ethernet switch)
- CAN module optionally supports CAN FD
- SDHC provides standard SDIO interface
- Low Power Unit provides reduced CAN, LIN, SPI, ADC functionality in low power mode
- Designed to ISO26262 process for use in ASIL B
- -40 to +125C (ambient)
- 3.0V to 5.5V

Up to 2x ENET Ethernet interfaces with optional Switch

Packages

100 BGA, 176 LQFP, 256 BGA, 324 BGA

SPC57xx	44B - 46B	44C - 46C	46G - 48G
Cores	1	2	3
Flash	1.5-3M	1.5-6M	3-6M
RAM	-512k	-768k	-768k
Eth/FR/ML /SD/USB	1/1/0/0/0	1/1/0/0/0	1/1/1/1/2 2/1/1/1/2

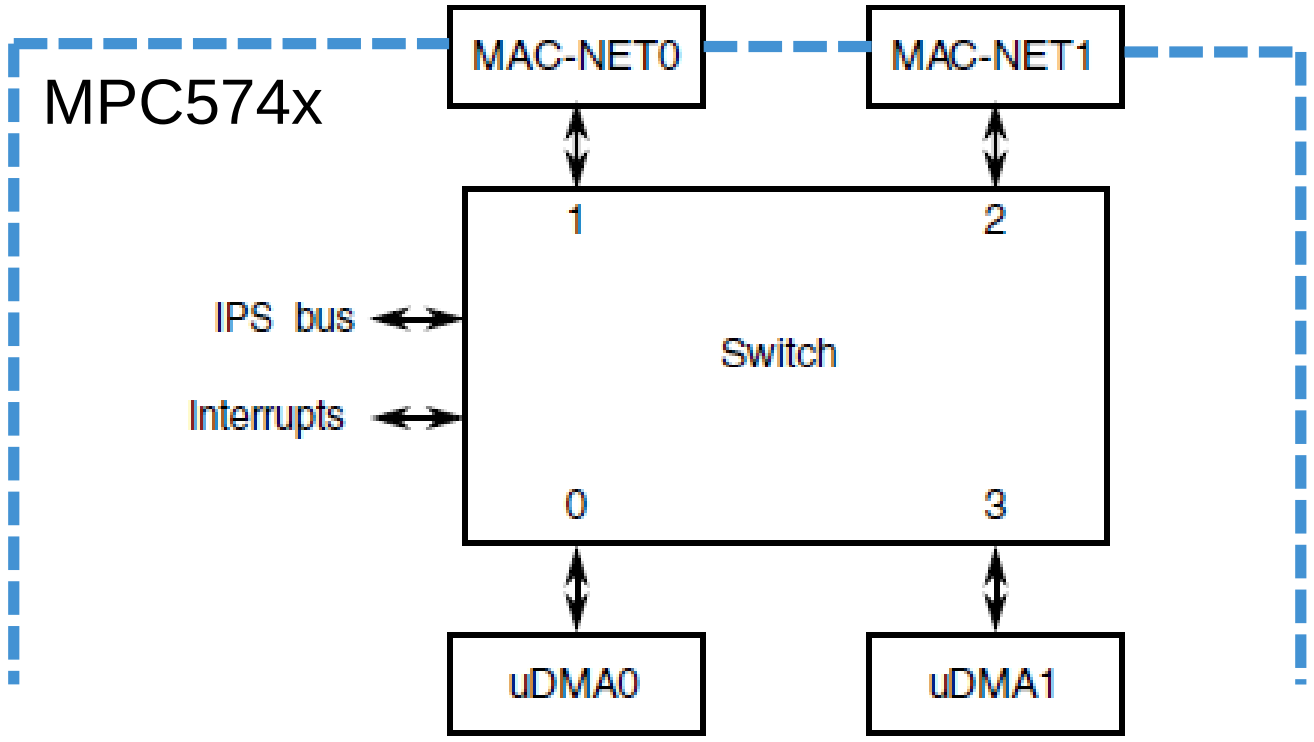
Full MPC574xB/C/G Family Feature Overview

	Single Core			Dual Core					Triple Core		
	MPC5744B	MPC5745B	MPC5746B	MPC5744C	MPC5745C	MPC5746C	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
Core	z4	z4	z4	z4 + z2	z4 + z2	z4 + z2	z4+z2	z4+z2	z4 + z4 + z2	z4 + z4 + z2	z4 + z4 + z2
FPU	Yes	Yes	Yes	Yes on z4	Yes on z4	Yes on z4	Yes on z4	Yes on z4	Yes on z4	Yes on z4	Yes on z4
Max Speed (MHz)	160	160	160	160 + 80	160 + 80	160 + 80	160 + 80	160 + 80	160 + 160 + 80	160 + 160 + 80	160 + 160 + 80
Flash Size	1.5M	2M	3M	1.5M	2M	3M	4M	6M	3M	4M	6M
DataFlash	Emulated up to 64k	Emulated up to 64k	Emulated up to 64k	Emulated up to 128k	Emulated up to 128k	Emulated up to 128k	Emulated up to 128k	Emulated up to 128k	Emulated up to 192k	Emulated up to 192k	Emulated up to 192k
RAM	192k	256k	384k (512k option)	192k	256k	384k (512k option)	512k	768k	768k	768k	768k
Security Module	HSM Option	HSM Option	HSM Option	HSM Option	HSM Option	HSM Option	Optional	Optional	Optional	Optional	Optional
MBIST/LIBIST	MBIST	MBIST	MBIST	MBIST	MBIST	MBIST	LBIST/MBIST	LBIST/MBIST	LBIST/MBIST	LBIST/MBIST	LBIST/MBIST
DMA	32-ch	32-ch	32-ch	32 ch	32 ch	32 ch	32 ch	32 ch	32 ch	32 ch	32 ch
MPU	16	16	16	16	16	16	24	24	32	32	32
ADC	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 32ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 32ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 32ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 32ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 32ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 32ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 64ch external	1x12 bit (32 channels) 1x10-bit ADC (48 channels) 64ch external	1x12 bit (32 channels) 1x10 bit ADC (48 channels) 64ch external	1x12 bit (32 channels) 1x10 bit ADC (48 channels) 64ch external	1x12 bit (32 channels) 1x10 bit ADC (48 channels) 64ch external
Analog Comparators	3	3	3	3	3	3	3	3	3	3	3
Timers/PWM	4ch System Timer 16ch x PIT Up to 64eMIOS channels	4ch System Timer 16ch x PIT Up to 64eMIOS channels	4ch System Timer 16ch x PIT Up to 64eMIOS channels	4ch System Timer 16ch x PIT Up to 64eMIOS channels	4ch System Timer 16ch x PIT Up to 64eMIOS channels	4ch System Timer 16ch x PIT Up to 64eMIOS channels	4ch x System Timer 16ch x PIT Up to 96eMIOS channels	4ch x System Timer 16ch x PIT Up to 96eMIOS channels	4ch x System Timer 16ch x PIT Up to 96eMIOS channels	4ch x System Timer 16ch x PIT Up to 96eMIOS channels	4ch x System Timer 16ch x PIT Up to 96eMIOS channels
CTU	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FlexRay 2.1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Ethernet	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
2nd Ethernet + Switch	No	No	No	No	No	No	optional	optional	optional	optional	optional
MLB	No	No	No	No	No	No	No	No	Yes	Yes	Yes
USB	No	No	No	No	No	No	No	No	Yes	Yes	Yes
SDHC	No	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
LINFlex	12	12	12	16	16	16	16	16	18	18	18
SPI	6	6	6	8	8	8	10	10	10	10	10
CAN	6	6	6	8	8	8	8	8	8	8	8
CAN FD	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs	Optional Feature on all CANs
I2C	4	4	4	4	4	4	4	4	4	4	4
SAI / I2S	3	3	3	3	3	3	3	3	3	3	3
MLB	No	No	No	No	No	No	No	No	1	1	1
USB 2.0	No	No	No	No	No	No	No	No	2 (OTG + Host)	2 (OTG + Host)	2 (OTG + Host)
Additional features	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit	Low power Unit
Debug	JTAG + Nexus 3+ (z4)	JTAG + Nexus 3+ (z4)	JTAG + Nexus 3+ (z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)	JTAG + Nexus 3+ (z2+z4)
Packages	176 LQFP 256 MAPBGA 100 MAPBGA 324 MAPBGA (debug only)	176 LQFP 256 MAPBGA 100 MAPBGA 324 MAPBGA (debug only)	176 LQFP 256 MAPBGA 100 MAPBGA 324 MAPBGA (debug only)	176 LQFP 256 MAPBGA 100 MAPBGA 324 MAPBGA (debug only)	176 LQFP 256 MAPBGA 100 MAPBGA 324 MAPBGA (debug only)	176 LQFP 256 MAPBGA 100 MAPBGA 324 MAPBGA (debug only)	176LQFP 256 MAPBGA 324 MAPBGA	176LQFP 256 MAPBGA 324 MAPBGA	176LQFP 256 MAPBGA 324 MAPBGA	176LQFP 256 MAPBGA 324 MAPBGA	176LQFP 256 MAPBGA 324 MAPBGA

Note: Datasheets on the web are pending an update to reflect this latest line-up.

MPC574x Integrated Ethernet Switch

- The Ethernet Switch (ESW) provides optional Layer 2 Ethernet switching between the connected Ethernet MACs and the SoC.



MPC574xB/C/G Ethernet Blocks

- 2 Modes of operation
- Can be configured to operate as a 3-port switch (switch mode) or as two independent ports (passthrough mode)

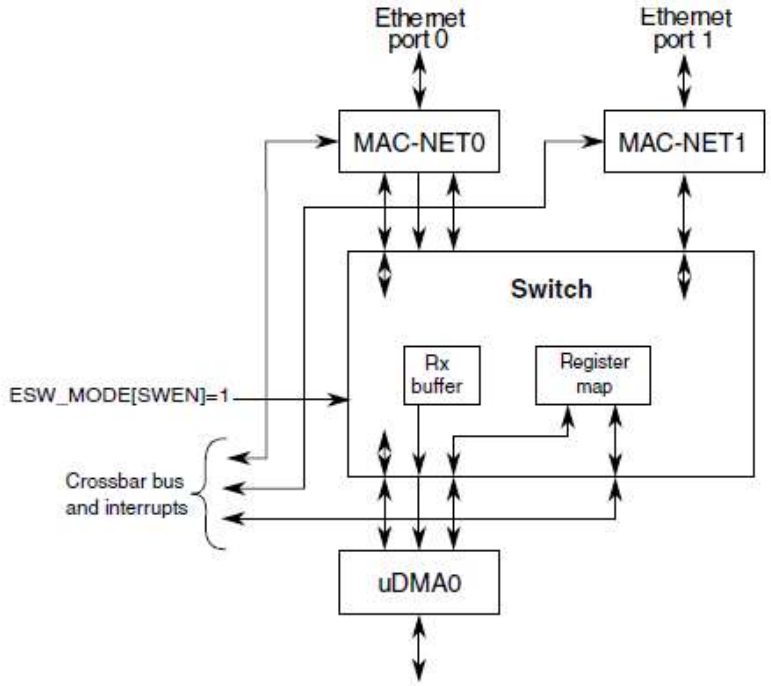


Figure 41-3. Switch Mode Configuration Overview

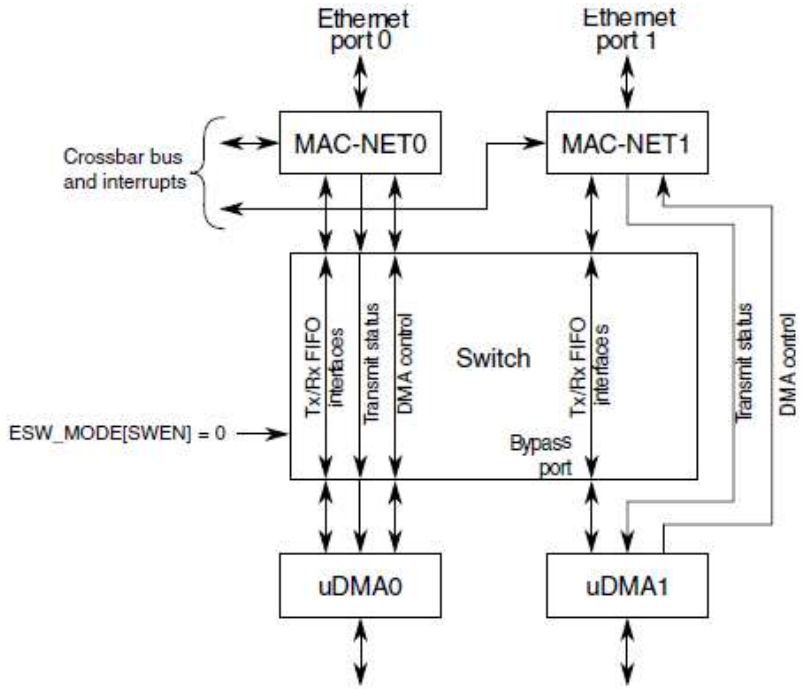


Figure 41-2. Passthrough Mode Configuration Overview

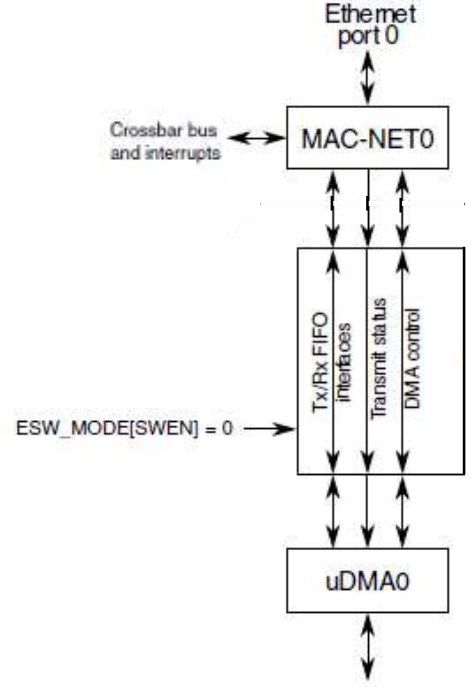


Figure 41-2. Passthrough Mode **Single Port**

uDMA = unified DMA

MPC574xB/C/G Ethernet Blocks

- 2 Modes of operation
- Can be configured to operate as a 3-port switch (switch mode) or as two independent ports (passthrough mode)

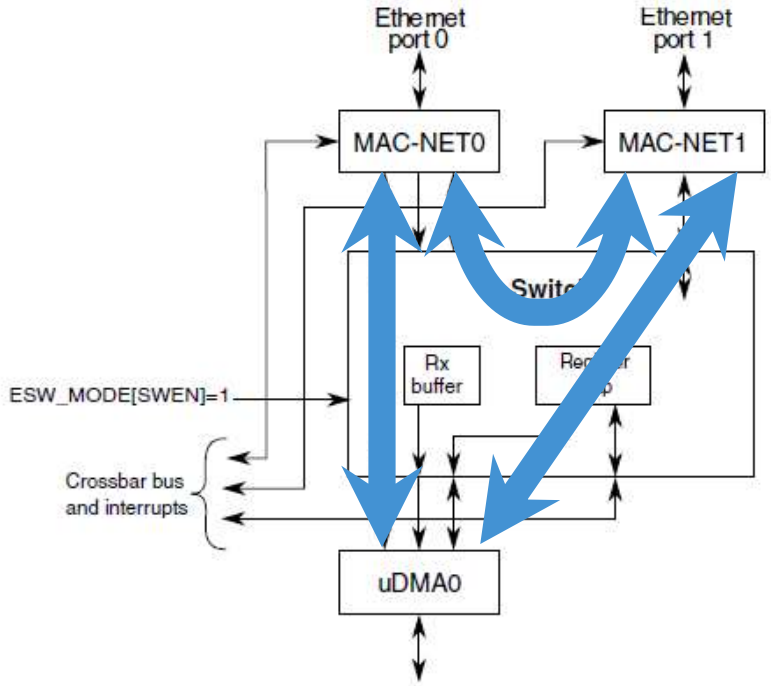


Figure 41-3. Switch Mode Configuration Overview

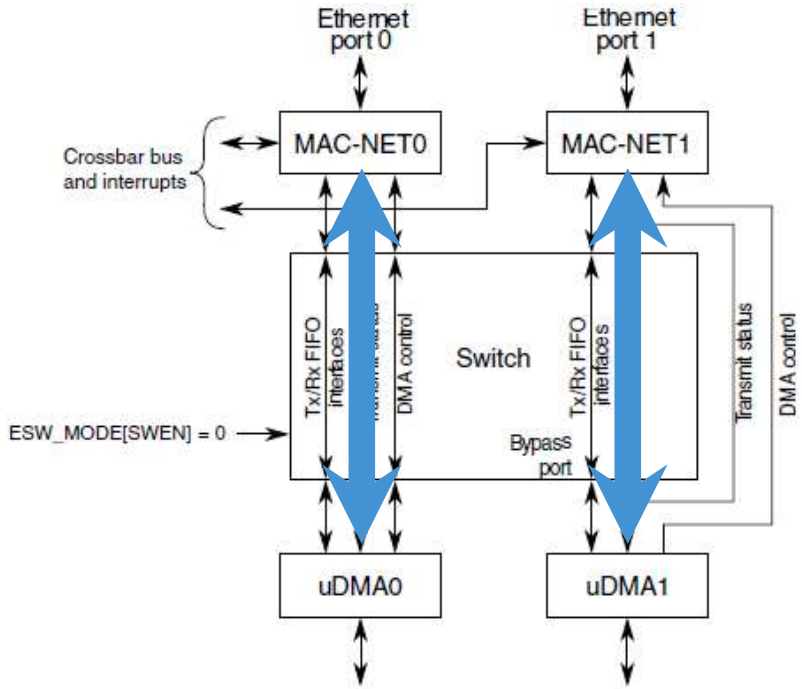


Figure 41-2. Passthrough Mode Configuration Overview

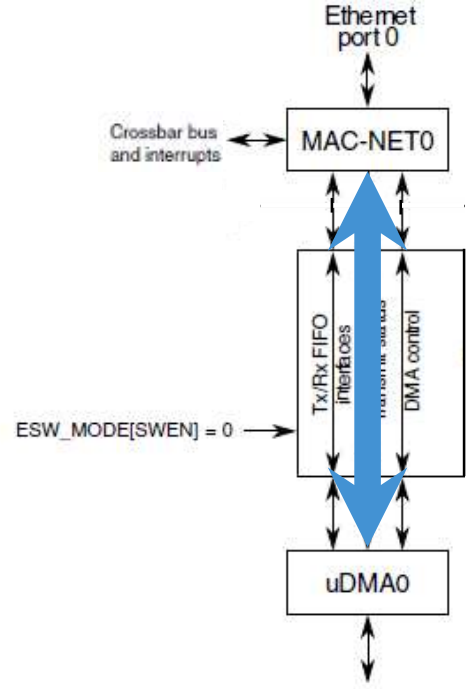


Figure 41-2. Passthrough Mode **Single Port**

uDMA = unified DMA

Additional MPC574x Integrated Switch Features

- Integrated Ethernet switch engine **compatible with 10/100 MAC-NET core**
- **Filters and forward traffic at wire-speed on all ports**
- Per-queue tail-drop congestion management
- Implements hardware switching look-up mechanism providing a learning capacity of up to 2K MAC addresses
- Supports configurable VLAN switching when MAC address lookup should be omitted
- **Classification and priority assignment** based on port number, MAC address, IPv4
- DiffServ code point field, IPv6 Class of Service and VLAN Priority (IEEE802.1q)
- Efficient output queue frame buffering with shared Frame buffer of 24 Kbyte
- Each port implements **four priority queues** with configurable weighted round-robin selection

Additional MPC574x Integrated Switch Features (continued)

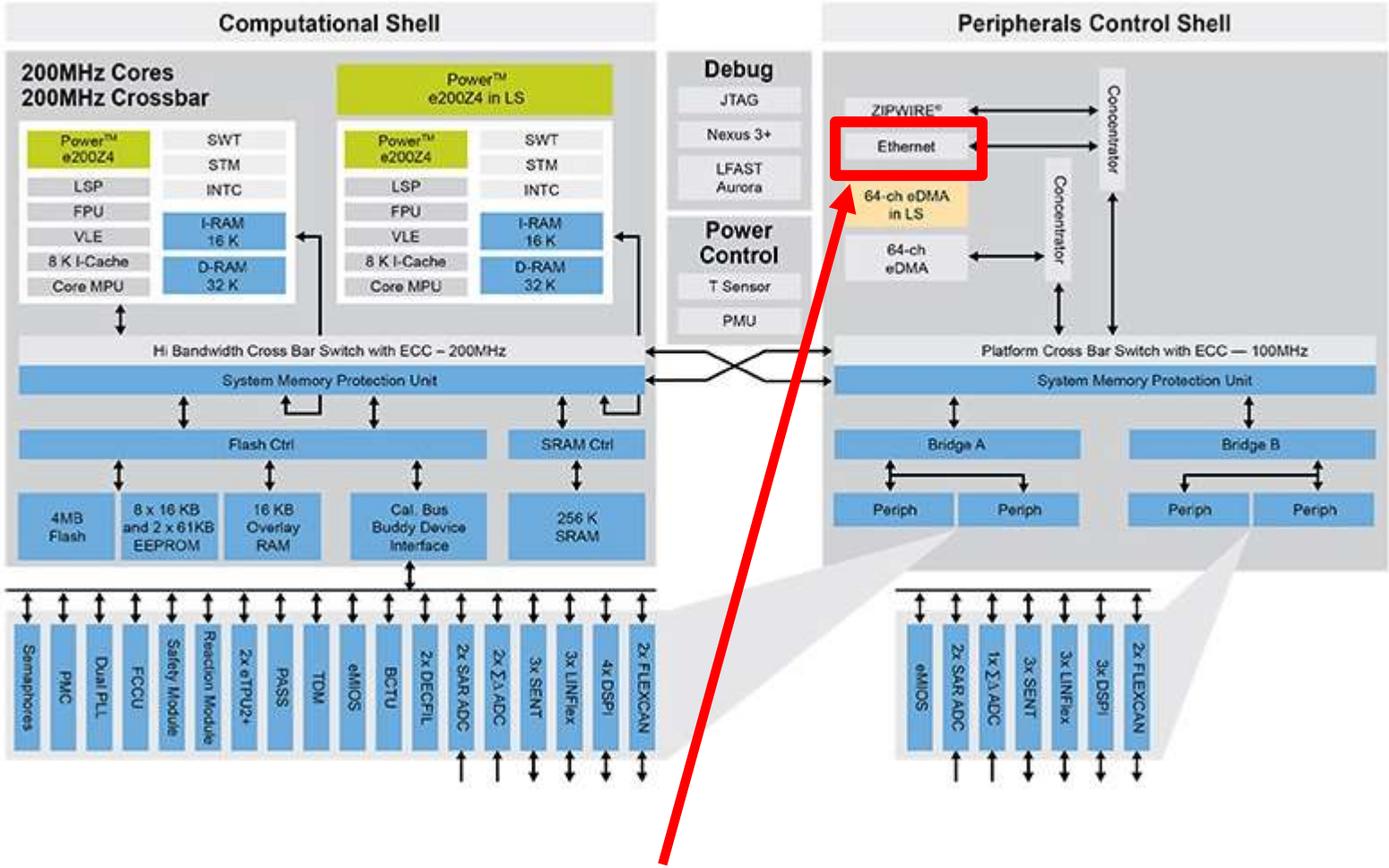
- **Support Ethernet multicast and broadcast** with flooding control to avoid unnecessary
- duplication of frames
- **Programmable multicast destination port mask** to restrict frame duplication for individual multicast addresses
- **Multicast and broadcast resolution with VLAN domain filtering** providing a strict separation of up to 32 VLANs
- IP snooping with programmable protocol and port number registers
- Programmable ingress and egress VLAN tag addition, removal and manipulation supporting single and double-tagged VLAN frames
- Event and status signals which can monitor port activity, severe error conditions, or any user-specific event
- Static or dynamic (learning, aging) switching tables
- Support for **IEEE 1588** precise time-stamping applications
- Supports aggregation and redundant backplane applications

MPC5746R: Automotive & Industrial Engine Management MCU

Target Applications
Engine control units (ECU)
Electric DC motor control
Ethernet connectivity
Safety critical applications

Features

- Two independent 200MHz Power Architecture® z4 cores
- Single 200MHz z4 core in Lockstep with one of the main cores
- 4M Flash
- 320kB total SRAM
- 2 eTPU+ timers with 64 channels
- eMIOS timer with 32 channels
- Ethernet 10/100
- 4 Sigma Delta and 3 SAR ADC converters
- Built to support functional safety (ISO 26262/ASIL-D)
- 252 MAPBGA, 176 LQFP and 144 LQFP packages
- -40 to 125C Ta Operation

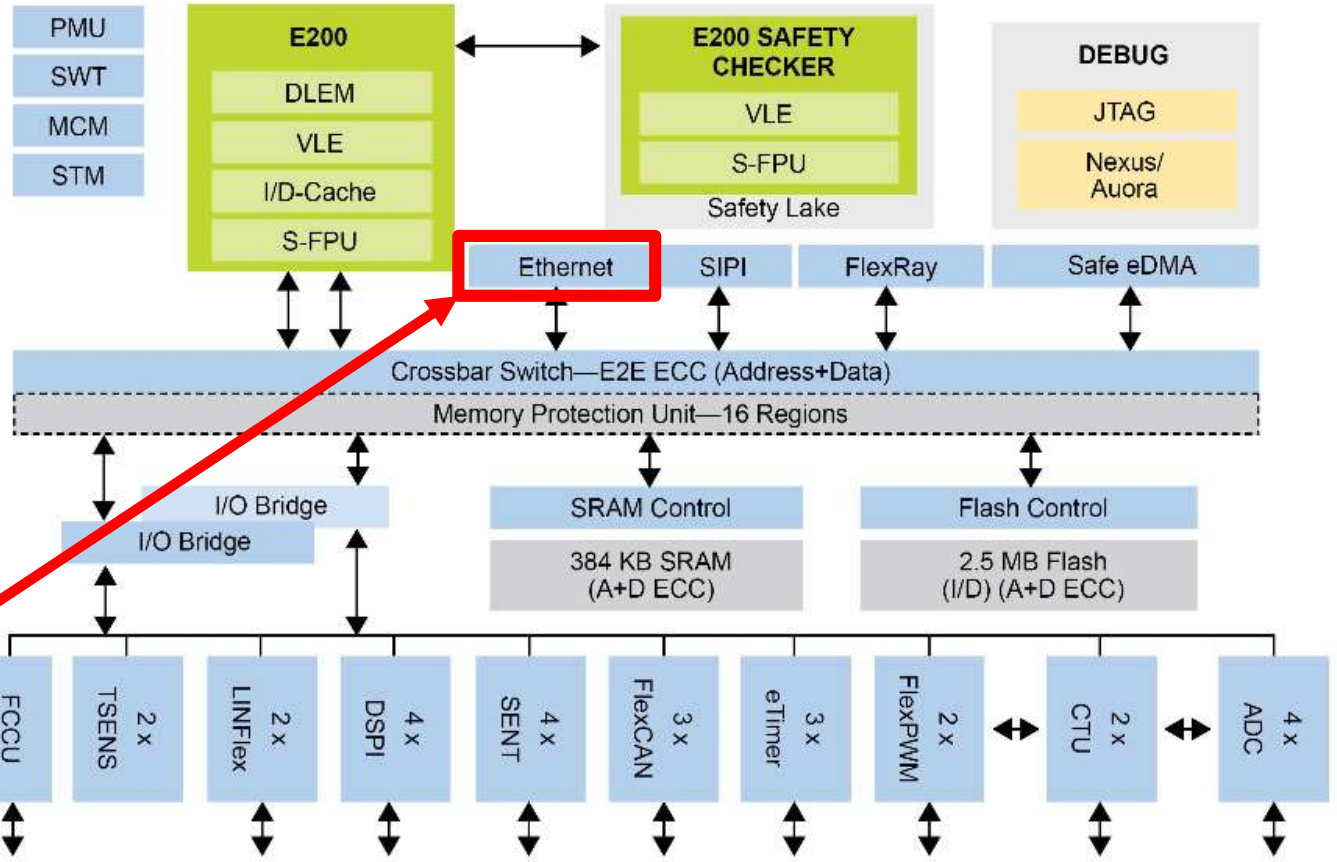


1x Ethernet FEC 10/100Mb

MPC574xP - Ultra-Reliable MPC574xP MCU for Automotive & Industrial Safety Applications

Target Applications:

- Automotive Radar Systems
- Hybrid and Electric Vehicle Power Inverter
- Electric power steering (EPS)
- Airbag system
- Safety domain control
- Safety motor controller
- Active driver assistance system
- Adaptive cruise control
- Braking and stability control
- Active suspension



1x 10/100Mb ENET Ethernet

MPC574xP - Features

Main Feature

- 2 x e200z4 in delayed lockstep operating up to 200 MHz
- Embedded floating point unit
- Built to support functional safety (ISO 26262 / ASIL D)
- 32-channel eDMA in delayed lockstep
- 4 x 12 bit analog-to-digital converters (ADC), each with 16 channels
- Ultra-Reliable MCUs
- Memory Capability
  - Up to 2.5 MB flash memory w/ error code correction (ECC)
  - Up to 384 KB of total SRAM w/ECC

- Communication Protocols
  - 3 x FlexCAN
  - 2 x LINFlexD
  - 4 x DSPI
  - 4 x SENT
  - LFAST SIPI support
  - Dual-channel FlexRay™ controller
  - Ethernet
- Additional Features
  - Aurora debug and trace support
  - 144-pin LQFP package
  - 257-pin PBGA package

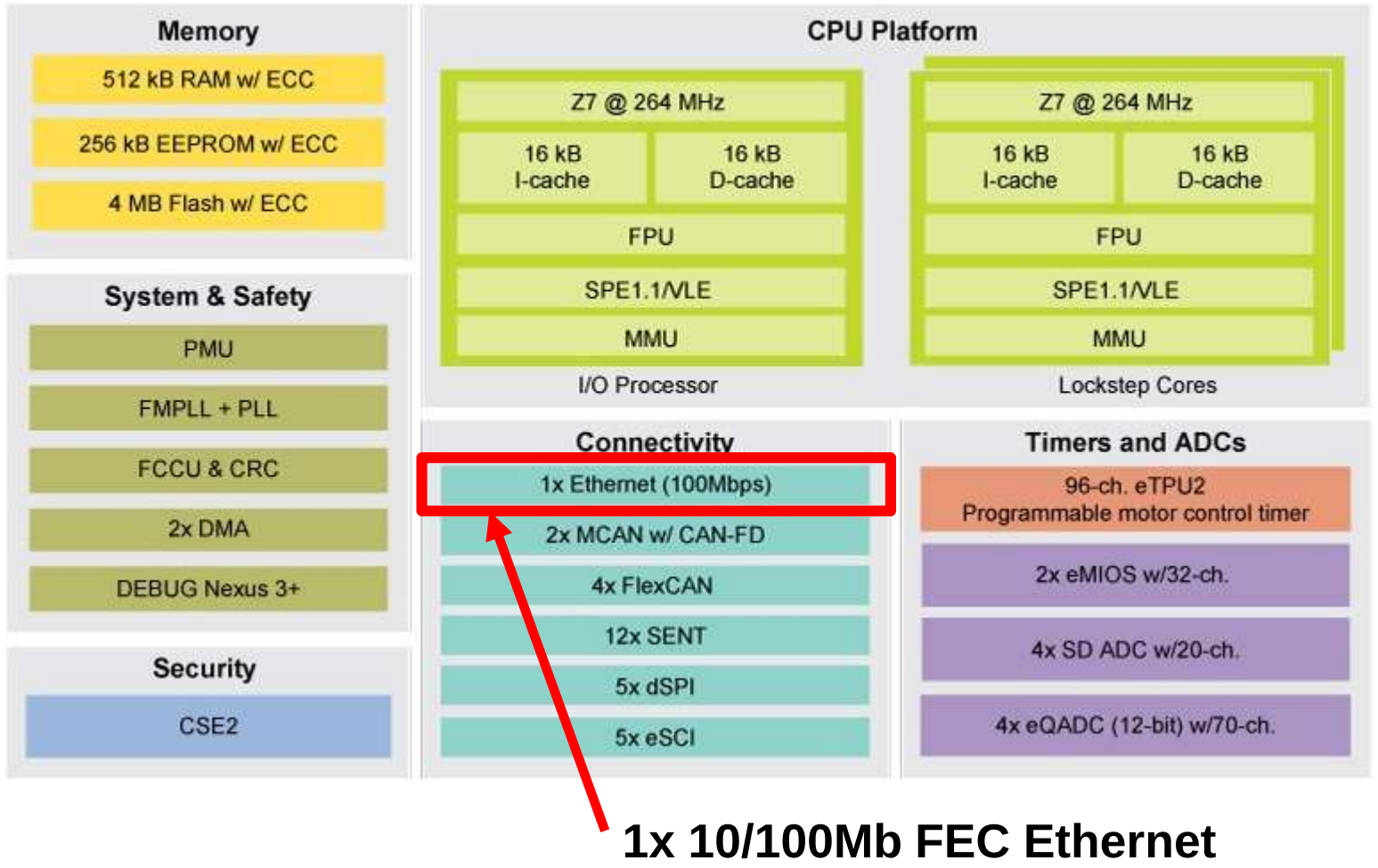
MPC5775B and MPC5775E Microcontrollers for Battery Management Systems (BMS) and Inverter Applications

Target Applications

Battery Management System
Hybrid and Electric Vehicle Power Inverter
Hybrid and Electric Vehicle Powertrain
Hybrid and Electric Traction Motors
Battery Management Systems (BMS)
Engine Control Units (ECU)
Safety Critical Applications

Features

- 2 x Power Architecture z7 cores with 264 MHz on MPC5775E and 220 MHz on MPC5775B MCUs
- 1 x z7 core in lockstep with one of the main cores, with 264 MHz on MPC5775E and 220 MHz on MPC5775B MCU
- 4 MB Flash, 512 KB SRAM
- CSE hardware security module that supports SHE protocol specification and AES-128 encryption
- 10/100Mbps Ethernet module
- 2 x CAN-FD modules and 4 x FlexCAN modules
- 3 x eTPU2 timer modules on MPC5775E MCU
- 4 x Sigma Delta modules on MPC5775E MCU
- Up to 70 ch eQADC and 32 ch eMIOS

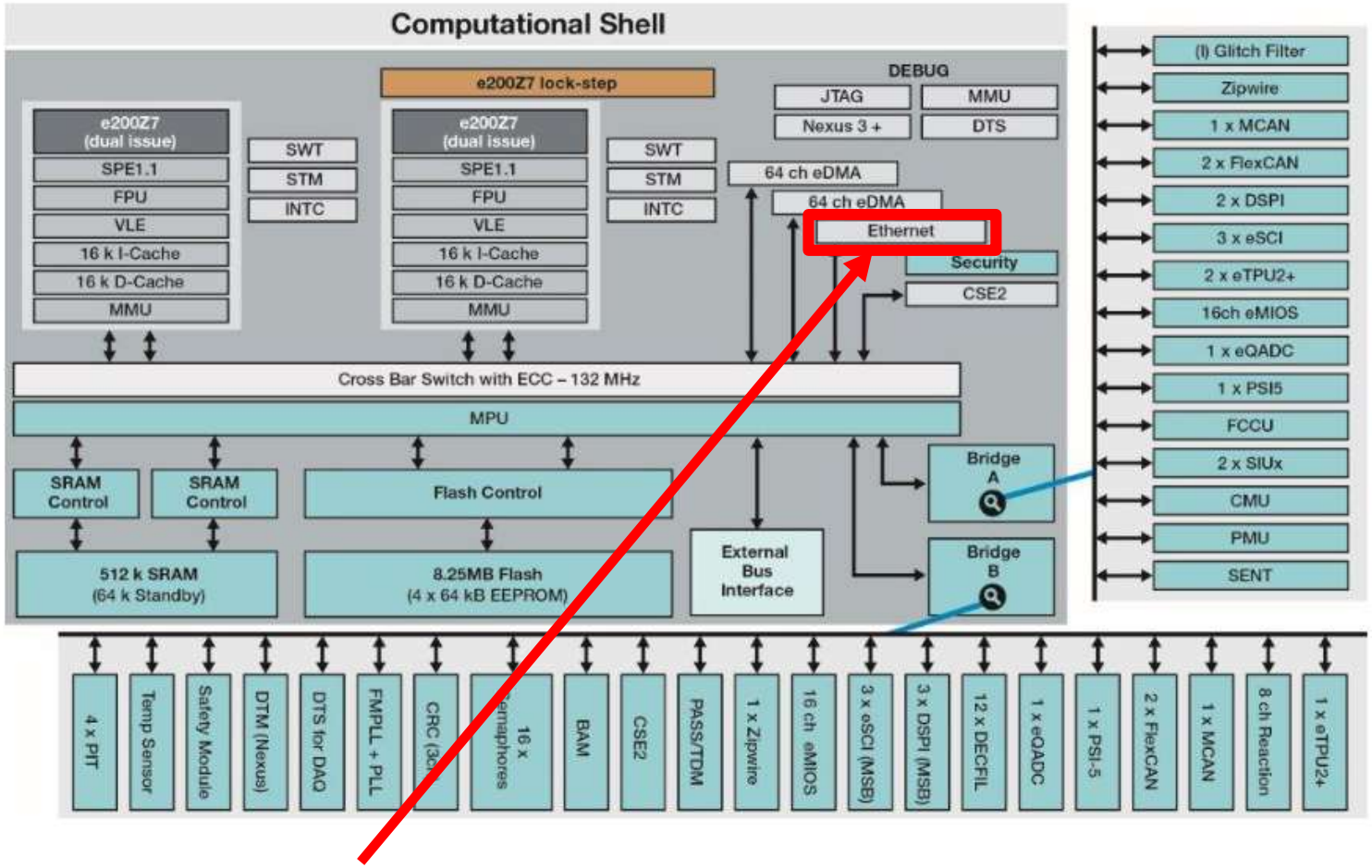


MPC5777C: Ultra-Reliable MPC5777C MCU for Automotive Engine Management

Target Applications
Safety Critical Applications
Engine Control Units (ECU)
Electric DC motor control
Ethernet Connectivity

Features

- Two independent 264MHz Power Architecture z7 cores
- Single 264MHz z7 core in Lockstep with one of the main cores
- 8M Flash
- 512kB total SRAM
- 3 eTPU2 timers with 96 channels
- eMIOS timer with 32 channels
- Ethernet 10/100
- 4 Sigma Delta and 4 eQADC converters
- Built to support functional safety (ISO 26262/ASIL-D)
- 416 and 516 BGA
- -40 to 125C Ta Operation



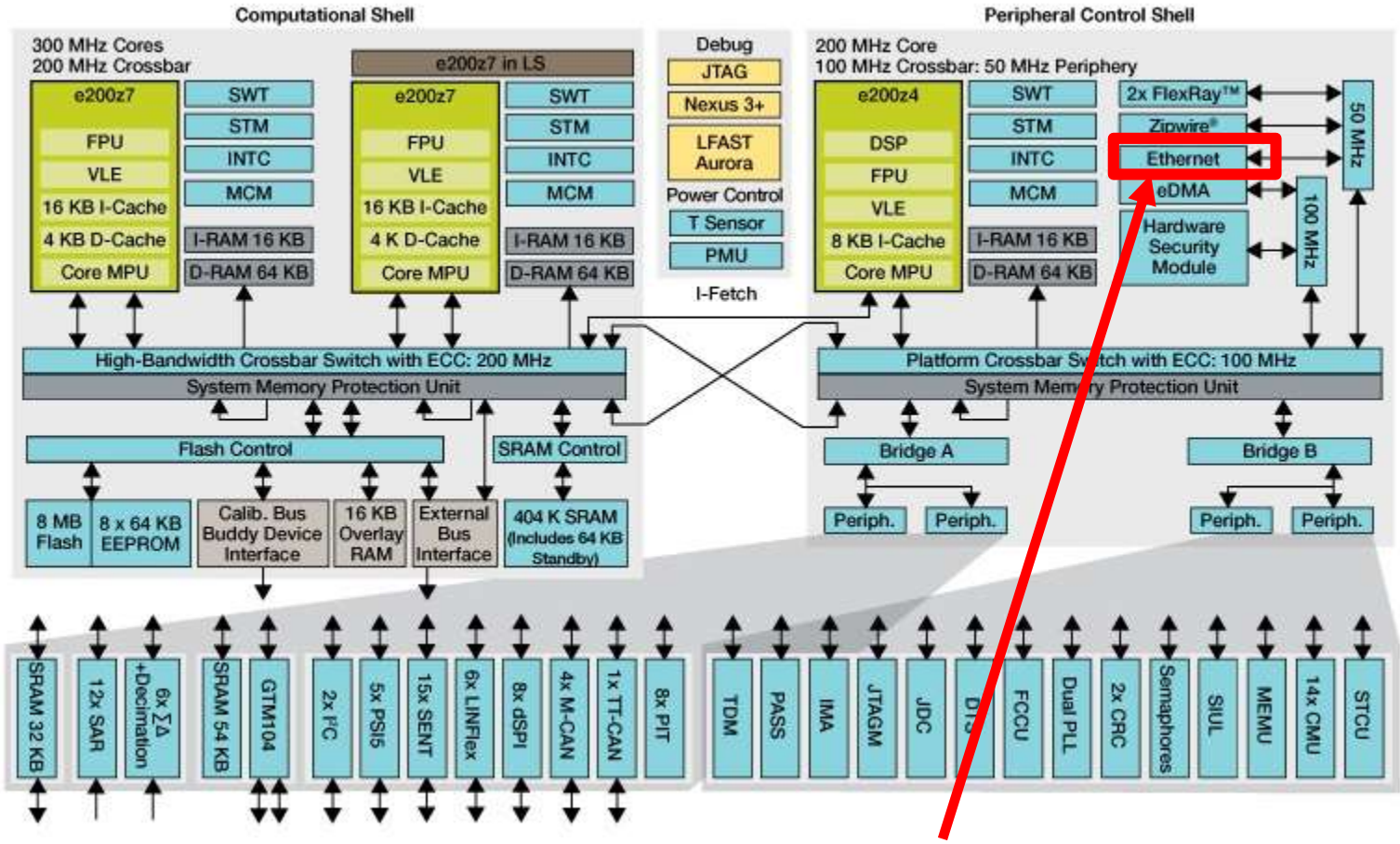
1x 10/100Mb FEC Ethernet

MPC5777M: Ultra-Reliable MPC5777M MCU

Automotive & Industrial Engine Management

Target Applications

- Engine control units (ECU)
- Electric DC motor control
- Critical functional safety



1x 10/100Mb FEC Ethernet

MPC5777M: Ultra-Reliable MPC5777M MCU for Automotive & Industrial Engine Management

Main Features

- Two independent e200z7 cores operating up to 300 MHz
- Single 300 MHz e200z7 core for delayed lockstep
- Single e200z4 I/O core operating up to 200 MHz
- On-chip DSP and floating point unit (on I/O core)
- Built to support functional safety (ISO 26262 /ASIL-D)
- 248-channel general timer module (GTM104)
- Up to 128-channel eDMA
- Up to 84-channel analog-to-digital converters (ADC)
- Includes 10 x ΣΔ ADC converters
- High-speed Nexus Aurora debug and trace support
- 416-pin PBGA package
- 512-pin PBGA package

- Memory Capability
  - 8 MB flash memory with error code correction (ECC)
  - Up to 596 KB of total SRAM with ECC
- Communication Protocols
  - Ethernet controller (FEC)
  - 4 x M-CAN and 1 x TT-CAN
  - 6 x LINFlex
  - 8 x dSPI and 2 x IIC
  - 5 x PSI-5 and 15 x SENT
  - Zipwire® support
  - 2 x dual-channel FlexRay™ controller
- Additional Features
  - Hardware Security Module (HSM)
  - Tamper Detection Module (TDM)

MPC57xx - Summary Table of Ethernet Capability

Part Number	Description	Supported Ethernet Rate	Ethernet MAC	Supported Media Interface	Hardware Acceleration
MPC577xK	32-bit MCU for ADAS Applications - PREPRODUCTION	1x 10/100Mb	ENET (MAC-NET core + MAC)	MII, MII-Lite, RMII	Layer 3 IP, TCP, UDP, and ICMP
MPC574xB-C-G	Ultra-Reliable MCUs for Automotive & Industrial Control and Gateway	Up to 2x 10/100Mb (with optional 3port switch)	ENET (MAC-NET core + MAC)	ENET0: MII, MII-Lite, RMII ENET1: MII-Lite only	Layer 3 IP, TCP, UDP, and ICMP + Switching
MPC5746R	Automotive & Industrial Engine Management MCU	1x 10/100Mb	FEC (hardware and microcode)	MII-Lite, RMII, 7-wire (7-wire → 10Mb only)	Layer 2
MPC574xP	Ultra-Reliable MPC574xP MCU for Automotive & Industrial Safety Applications	1x 10/100Mb	ENET (MAC-NET core + MAC)	MII, MII-Lite, RMII	Layer 3 IP, TCP, UDP, and ICMP
MPC5775B-E	MPC5775B/E for Battery Management Systems and Inverter Applications	1x 10/100Mb	FEC (hardware and microcode)	MII-Lite, RMII	Layer 2
MPC5777C	Ultra-Reliable MPC5777C MCU for Automotive & Industrial Engine Management	1x 10/100Mb	FEC (hardware and microcode)	MII-Lite, RMII	Layer 2
MPC5777M	Ultra-Reliable MPC5777M MCU for Automotive & Industrial Engine Management	1x 10/100Mb	FEC (hardware and microcode)	MII, RMII, 7-wire (7-wire → 10Mb only)	Layer 2

MII-Lite = MII without the CRS and COL signals

MAC57D5xx Series

Ultra-Reliable Multi-Core Arm®-based MCU for Clusters and Display Management

MAC57D5xx Processor Block Diagram

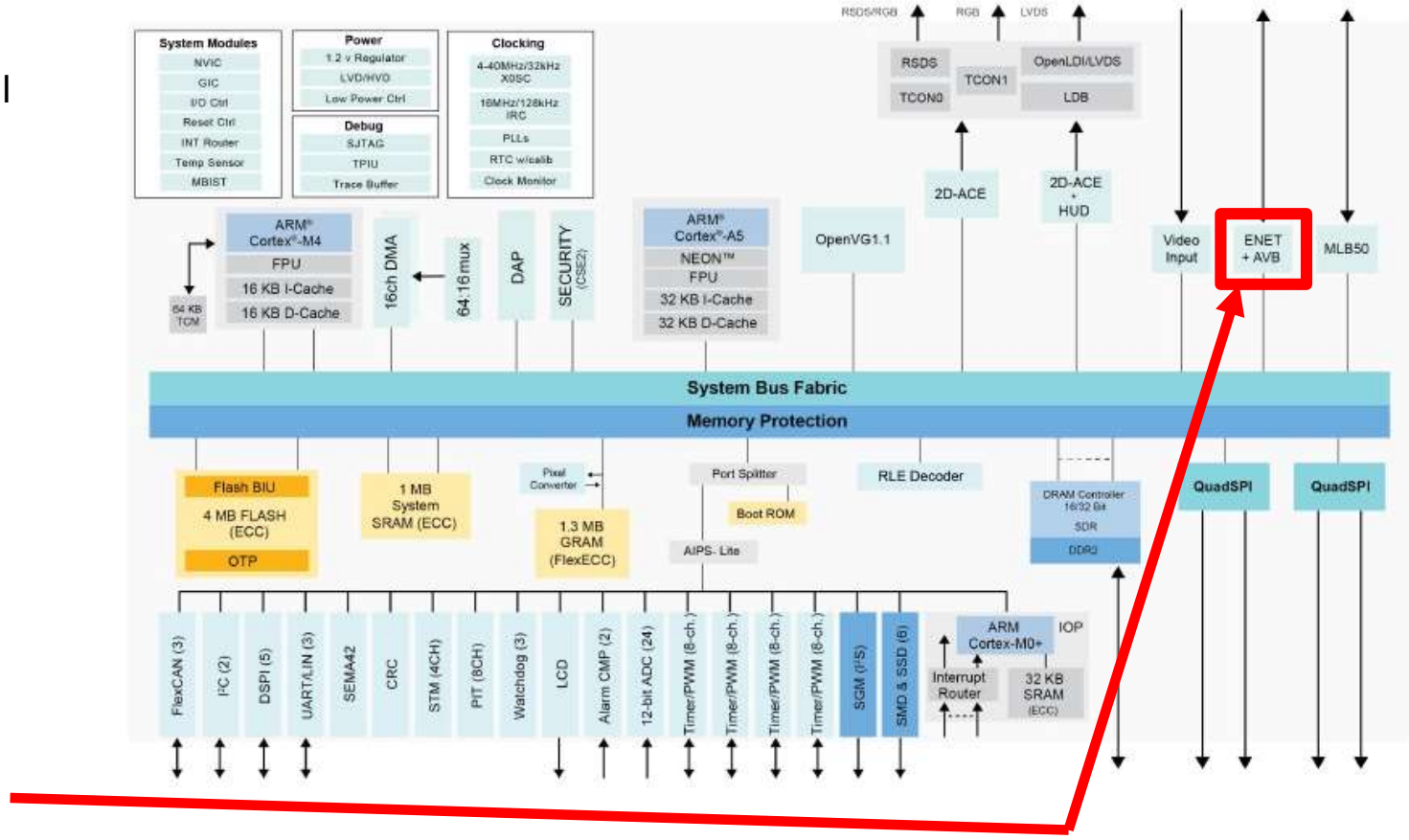
Features

- Arm-based multi-core architecture platform
  - Arm Cortex-A5, 32-bit CPU (application processor)
  - Arm Cortex-M4, 32-bit CPU (vehicle processor)
  - Arm Cortex-M0+, 32-bit CPU (I/O processor)
- Intelligent stepper motor drive with stepper stall detect
- Low-power mode peripheral management
- Supports 2 x WVGA displays
- On-the-fly Head Up Display (HUD) warping engine
- Functional safety and security compliant
- Ethernet 10/100 + AVB (ENET)
- Autonomous real time clock (self calibrating)
- QuadSPI Flash Controller utilizing the new Centered Read Strobe feature
- Ultra-Reliable MCUs

- **1x 10/100Mb ENET Ethernet Interface**

Target Application:

- Clusters and Display Management
- Heads-up display
- Multifunction display



MAC57D5xx - Summary Table of Ethernet Capability

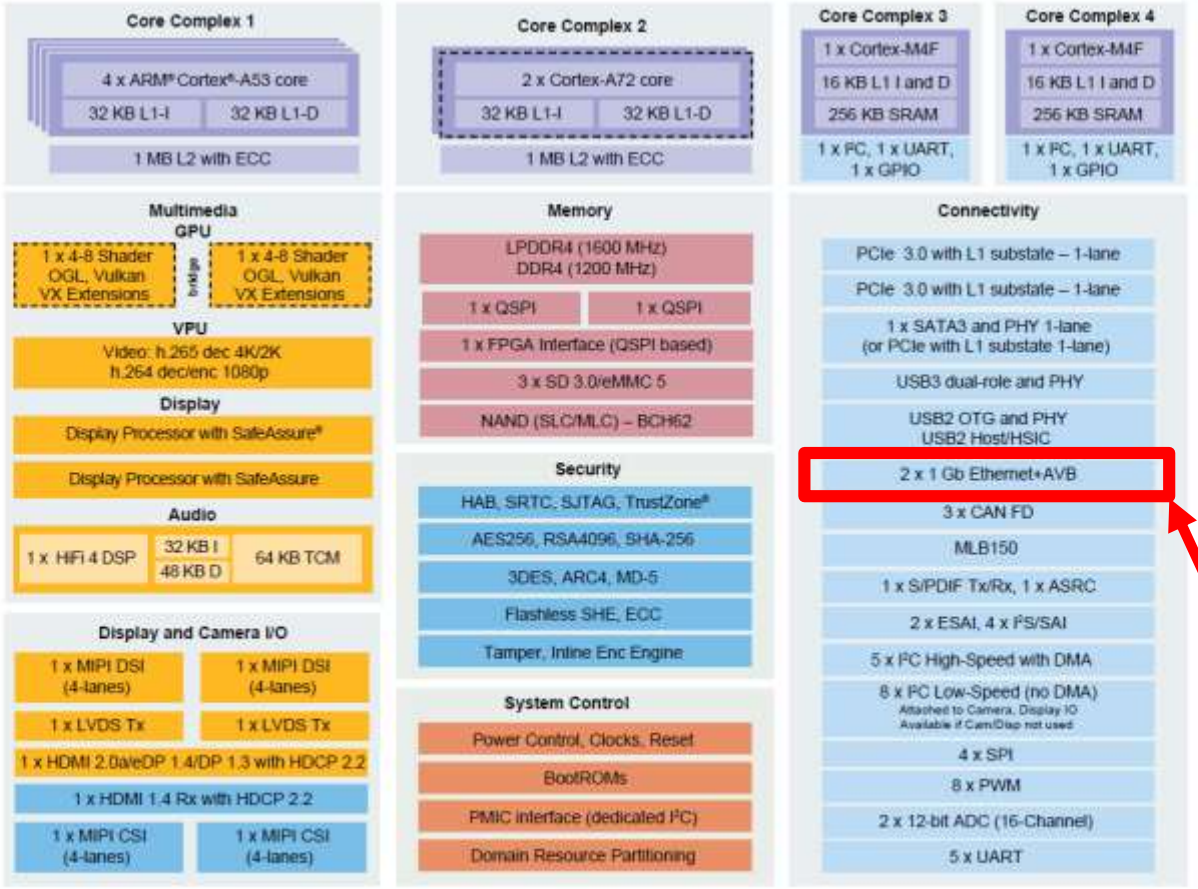
Part Number	Description	Supported Ethernet Rate	Ethernet MAC	Supported Media Interface	Hardware Acceleration
MAC57D5xx	Clusters and Display Management	1x 10/100Mb	ENET (MAC-NET core + MAC)	MII, MII-Lite, RMII	Layer 3 IP, TCP, UDP, and ICMP
…	…	…	…	…	…

MII-Lite = MII without the CRS and COL signals

i.MX 8

Virtualization, Vision, 3D Graphics, 4K Video

i.MX 8 Family Block Diagram



Target Applications:
Automotive infotainment
Instrument cluster
Head unit
Heads-up display (HUD)
Rear seat entertainment
Full digital electronic cockpit (eCockpit)

i.MX 8 FAMILY—DIFFERENTIATED FEATURES

Feature	i.MX 8QuadMax	i.MX 8QuadPlus	i.MX 8Quad
ARM® Core	2 x ARM Cortex®-A72	1 x Cortex-A72	–
ARM Core	4 x Cortex-A53	4 x Cortex-A53	4 x Cortex-A53
ARM Core	2 x Cortex-M4F	2 x Cortex-M4F	2 x Cortex-M4F
DSP Core	HiFi 4 DSP	HiFi 4 DSP	HiFi 4 DSP
GPU	2 x GC7000XSVX	2 x GC7000Lite/XSVX	2 x GC7000Lite/XSVX
PCIe 3.0	1 x PCIe (2-lane)*	1 x PCIe (1-lane)	1 x PCIe (1-lane)

*2-lane PCIe can act as 2 x 1-lane PCIe

2x 10/100/1000Mb ENET Ethernet Interface

Available on certain product families Note: Accessing muxable controller's full capabilities is dependent upon board component choices.

i.MX 8 - Summary Table of Ethernet Capability

Part Number	Description	Supported Ethernet Rate	Ethernet MAC	Supported Media Interface	Hardware Acceleration
i.MX8QuadMax	Infotainment and Displays	2x 10/100/1000Mb	ENET (MAC-NET core + MAC)	MII-Lite, RMII, RGMII	Layer 3 IP, TCP, UDP, and ICMP
i.MX8QuadPlus	Infotainment and Displays	2x 10/100/1000Mb	ENET (MAC-NET core + MAC)	MII-Lite, RMII, RGMII	Layer 3 IP, TCP, UDP, and ICMP
i.MX8DualMax	Infotainment and Displays	2x 10/100/1000Mb	ENET (MAC-NET core + MAC)	MII-Lite, RMII, RGMII	Layer 3 IP, TCP, UDP, and ICMP
…	…	…	…	…	…
i.MX8 Lower-end family members	Infotainment and Displays	1x 10/100/1000Mb 1x 10/100Mb	ENET (MAC-NET core + MAC)	MII-Lite, RMII, RGMII	Layer 3 IP, TCP, UDP, and ICMP

MII-Lite = MII without the CRS and COL signals

Agenda

- Introduction
- Ethernet in Automotive
- OSI model
- FEC and ENET Ethernet Blocks
- Device Specific Ethernet implementation
  - S32K, S32x and MPC57xx and i.MX
- **DPAA-based Ethernet Blocks**
- Device Specific Ethernet implementation
  - QorIQ Layerscape Series for Automotive
- Switches and PHYs
- Closing Remarks and Summary

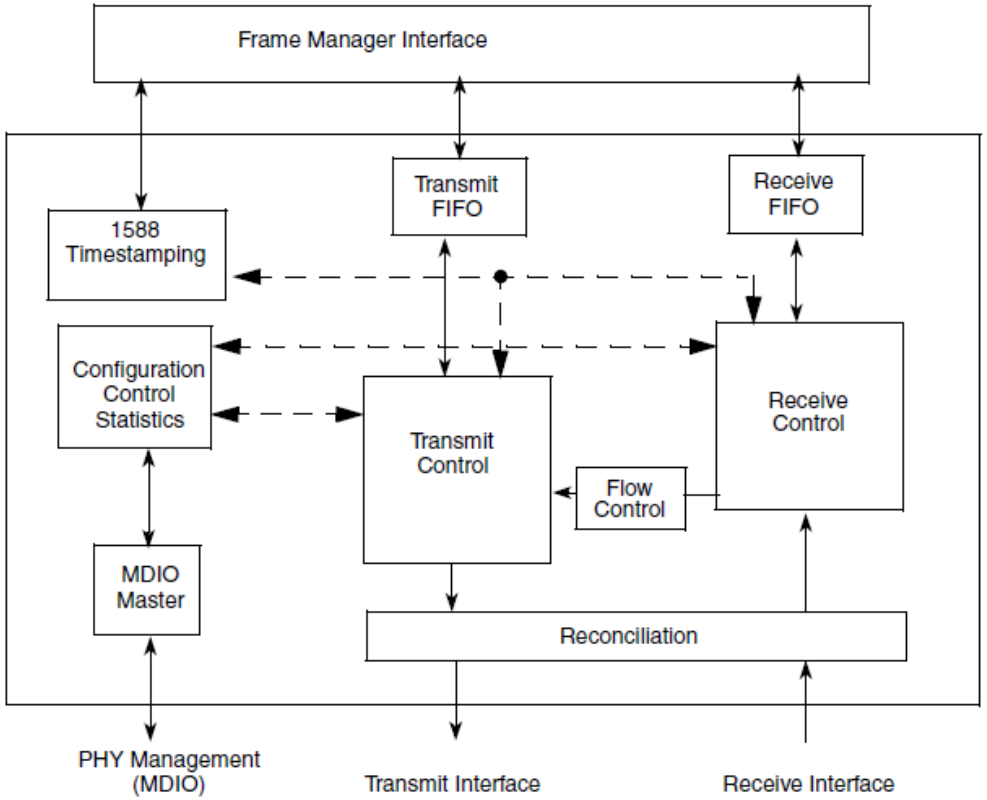
DPAA Based Ethernet Blocks

DPAA, mEMAC, RGMII and SERDES

mEMAC (multi-rate Ethernet MAC) Block Diagram and Features

Features:

- **Full MAC layer and reconciliation sub-layer implementation compliant with IEEE 802.3ae Specification**
- EEE (Energy Efficient Ethernet) 10G interface and MII/GMII signaling according to the IEEE802.3az specification
- **Lane, data alignment, PHY error and local/remote fault signaling handled by the reconciliation sub-layer**
- CRC-32 checking with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- **8 MAC address comparison on receive and one MAC address overwrite on transmit for NIC applications.**



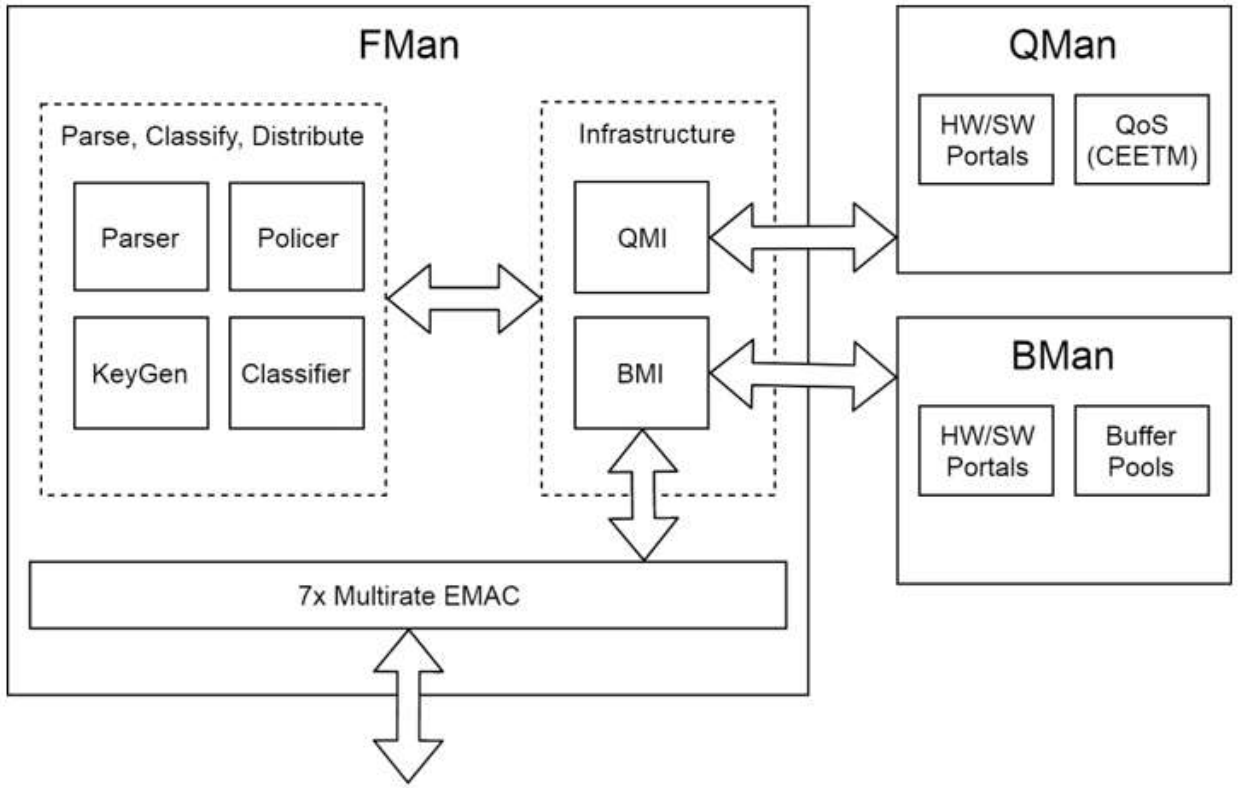
mEMAC Features (continued 1 of 2)

- **Selectable promiscuous frame receive mode** and transparent MAC address forwarding on transmit
- **Multicast address filtering** with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Ethernet pause frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- **Priority Flow Control (PFC) frame support** allowing 8 classes for higher layer congestion management
- **Magic packet detection**
- Programmable frame maximum length providing support for any frame up to 32K (for example, Jumbo frame or any tagged frame)

mEMAC Features (continued 2 of 2)

- Receive detection of VLAN tagged frames according to IEEE 802.1Q and double VLAN Tags (Stacked VLANs)
- Dynamic inter packet gap (IPG) calculation for WAN applications
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications
- **Clock and data rate decoupling with programmable asynchronous FIFOs**
- 802.3 basic and mandatory managed Objects statistic counters and IETF Management Information
- Database (MIB) package (RFC2665) and Remote Network Monitoring (RMON) counters
- Programmable Clause 22 and Clause 45 MDIO Master interface for PHY device configuration and management
- **Interrupt generation for error and Normal events**
- The Ethernet MAC controller **IEEE 1588 timestamping support** includes these features:
  - Precise time-stamping of ingress frames and egress frames

DPAA High Level Block Diagram on LS1043A



FMAN Aggregate Performance

Device	FMan frequency MHz	FMan aggregate rate Mpps @packet size = 64 bytes	FMan aggregate rate Gbps @ packet size = 1518 bytes
LS1043A	500	6.02	13.06

Device	FMan frequency MHz	FMan aggregate rate Mpps	FMan aggregate rate Gbps
LS1046A	700	32	22

FMAN Features

The FMan includes the following features:

- Supports Ethernet network interfaces (see the SerDes chapter of the ***QorIQ LS1043A*** *Reference Manual* for available configurations)
  - 5x 1-Gbps Ethernet interfaces
  - 1x 1/2.5-Gbps Ethernet interfaces
  - 1x 1/2.5/10-Gbps Ethernet interface
- Supports Ethernet network interfaces (see the SerDes chapter of the ***QorIQ LS1046A*** *Reference Manual* for available configurations)
  - 4x 1-Gbps Ethernet interfaces
  - 1x 1/2.5-Gbps Ethernet interfaces
  - 2x 1/2.5/10-Gbps Ethernet interface

FMAN Features (continued 1 of 5)

- MDIO for each Ethernet controller
- MDIO for PHY management:
  - Some of the Ethernet controller MDIO are connected to the SoC interface for PHY management
  - In FMan_v3, Dedicated MDIO control for PHY management
- **Interfaces with the Queue Manager (QMan)**
  - Dequeues/Enqueues frame descriptors (FD) from/to the QMan
  - Supports drop on tail-drop/wred per the QMan response
  - Supports transmit pause frame due to queue congestion state
  - Supports priority based flow control message pass from Ethernet MAC to QMan.

FMAN Features (continued 2 of 5)

- **Interfaces with the Buffer Manager (BMan)**
  - Allocates/Deallocates frames buffers
  - Supports transmit pause-frame due to buffer pools depletions
- **Packet parsing at wire speed**
  - Parsing of standard headers using hardware
  - Parsing of non-standard headers using soft examination sequences
- **Classification**
  - Custom classifier using internal tables
- **Policing**
  - Policing functionality based on classification result
  - RFC4115 and RFC2968
  - See the applicable device reference manual for each SoC for exact number of policer profiles

FMAN Features (continued 3 of 5)

- **Distribution**
  - Distributes to frame queues (FQs) according to custom classifier
  - Statistical distribution to FQs based on extracted key
- Storage Profile selection
  - Storage profile selection per physical port
  - Storage profile selection after distribution function evaluation or after custom classifier.
- Offline port
  - Supports Parse classify distribute (PCD) function on frames extracted frame descriptor (FD) from the QMan
  - Supports frame copy or move from a storage profile to an other.
- **FMan internal memory** (see the applicable device reference manual for the size)
  - Packet buffering (Tx/Rx FIFOs)
  - Custom classifier table
  - Frames internal context

FMAN Features (continued 4 of 5)

- **Statistics**
- **Port virtualization**
  - Separate programming model for each port in a different 4 KB region
  - Functional separation of resources for each port by management programming
  - Virtual Storage profile selection after classification or distribution function evaluation.
  - Different isolation context identifier (ICID) (in FMan_v3) per virtual storage profile
- Supports the following host commands through the QMan:
  - Debug
  - Statistics read/write
  - Configuration
- **Error reporting** through the following:
  - The QMan using the FD
  - Interrupts

FMAN Features (continued 5 of 5)

- Independent Ethernet mode
  - Does not use QMan and BMan for enqueueing and buffer allocation (i.e. ‘independent’)
  - Use of Ethernet native interface
  - Buffer descriptor (BD) ring programming model
  - Up to 100-Mbps rate per port, if more than one port is running (in independent or normal mode)
  - Up to 1 Gbps, provided that no other ports are active, either Ethernet or offline (applicable for boot loader), and that the FMan frequency is set to 500 MHz or higher
- Configurable pipeline architecture
  - Allows for the configuration of packet flow through the FMan on a per port basis
  - Classification results can modify the packet flow
  - Operational mode bits, on a per queue basis, can modify the flow

LS1043A SERDES Configuration Table

SRDS_PRTCL_S1 RCW[128:143]	A	B	C	D	PLL Mapping
0000	Unused				
1555	xfi.m9	PCIe#1 (x1)	PCIe#2 (x1)	PCIe#3 (x1)	1222
2555	sg.m9 (2.5G)	PCIe#1 (x1)	PCIe#2 (x1)	PCIe#3 (x1)	1222
4555	qs.m1,2,5,6	PCIe#1 (x1)	PCIe#2 (x1)	PCIe#3 (x1)	1111
4558	qs.m1,2,5,6	PCIe#1 (x1)	PCIe#2 (x1)	SATA	2221
1355	xfi.m9	sg.m2	PCIe#2 (x1)	PCIe#3 (x1)	1222
3333	sg.m9	sg.m2	sg.m5	sg.m6	1111
3558	sg.m9	PCIe#1 (x1)	PCIe#2 (x1)	SATA	2221
3555	sg.m9	PCIe#1 (x1)	PCIe#2 (x1)	PCIe#3 (x1)	1111
1460	xfi.m9	qs.m1,2,5,6	PCIe#3 (x2)		1222
2460	sg.m9 (2.5G)	qs.m1,2,5,6	PCIe#3 (x2)		1222
2255	sg.m9 (2.5G)	sg.m2 (2.5G)	PCIe#2 (x1)	PCIe#3 (x1)	1122
3333	sg.m9	sg.m2	sg.m5	sg.m6	1111
2233	sg.m9 (2.5G)	sg.m2	sg.m5	sg.m6	1122
2533	sg.m9 (2.5G)	PCIe#1 (x1)	sg.m5	sg.m6	1222
9960	PCIe#1 (x1)	PCIe#2 (x1)	PCIe#3 (x2		2222
2233	sg.m9 (2.5G)	sg.m2	sg.m5	sg.m6	1122
2533	sg.m9 (2.5G)	PCIe#1 (x1)	sg.m5	sg.m6	1222
	RESERVED				

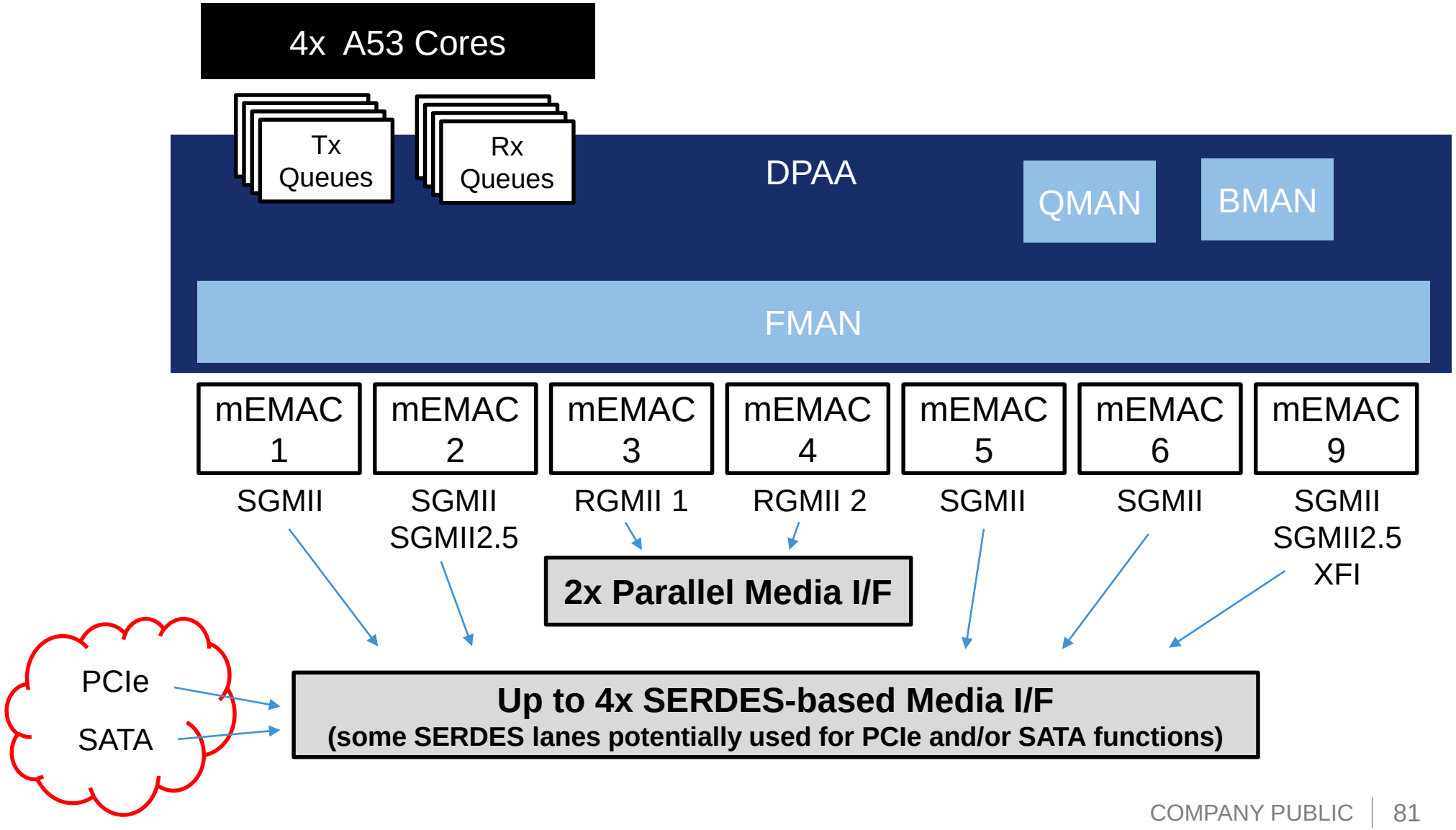
LS1043A RGMII Configuration Table

- MAC Assignment to RGMII

MAC	RGMII 1 Gbps	SGMII 1 Gbps	SGMII 2.5 Gbps	XFI 10 Gbps
1	-	Y	-	-
2	-	Y	Y	-
3	Y	-	-	-
4	Y	-	-	-
5	-	Y	-	-
6	-	Y	-	-
9	-	Y	Y	Y
Notes: RGMII Interfaces: MAC3 and MAC4 are used for EC1 and EC2 interfaces respectively.				

On LS1043A…

7 mEMACs, 4 shared (serial) SERDES Lanes, 2 Parallel xMII



Agenda

- Introduction
- Ethernet in Automotive
- OSI model
- FEC and ENET Ethernet Blocks
- Device Specific Ethernet implementation
  - S32K, S32x and MPC57xx and i.MX
- DPAA-based Ethernet Blocks
- **Device Specific Ethernet implementation**
  - **QorIQ Layerscape Series for Automotive**
- Switches and PHYs
- Closing Remarks and Summary

QorIQ Layerscape Series

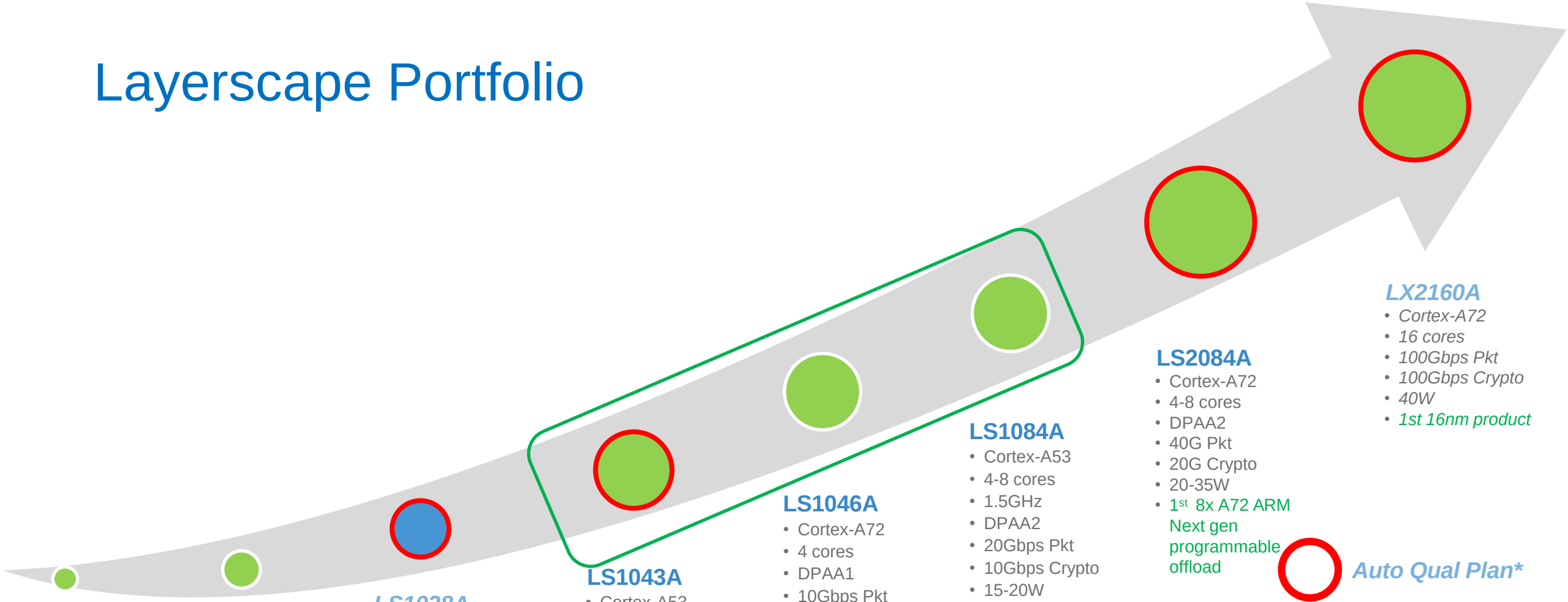
High Performance ARM-based Networking and Security

with Automotive Qualifications

Layerscape in Automotive

- **Highest CPU and IO performance SoCs in NXP**
- **Scalability –** 1-16 ARM core SoCs
- **Quality & Longevity** – Best quality available in high performance processing. Many devices already on 15 year longevity program.
- **Safety –** We've demonstrated safety for mil/aero and other critical infrastructure applications. Working to prove ASIL-B equivalence with auto-centric collateral (FMEDA, Safety Manual).
- **Security –** Secure Boot, Secure Debug, Hardware Enforced Partitioning & Virtualization
- **Software –** SDKs with a very PC-like look & feel. Broad support in Linux, history of working with WindRiver, GHS, and QNX.

Layerscape Portfolio



LS1012A
- Cortex-A53
- 800MHz
- 2Gbps Packet
- 1Gbps Crypto
- 1-2W
- Lowest power 64-bit ARM

LS1021A
- Cortex-A7
- 2 cores
- 1GHz
- 2Gbps Pkt
- 1Gbps Crypto
- 2W

LS1028A
- *Cortex-A72*
- *2 cores*
- *5Gbps Pkt*
- *5Gbps Crypto*
- 4-9W
- *1st with TSN switch*
- *Integrated GPU*

LS1043A
- Cortex-A53
- 2-4 cores
- 10Gbps Pkt
- 5Gbps Crypto
- 4-8W
- 1st 64-bit ARM processor

LS1046A
- Cortex-A72
- 4 cores
- DPAA1
- 10Gbps Pkt
- 10Gbps Crypto
- 8-15W
- 1st Value Tier A72 ARM

LS1084A
- Cortex-A53
- 4-8 cores
- 1.5GHz
- DPAA2
- 20Gbps Pkt
- 10Gbps Crypto
- 15-20W
- 1st 8x A53 ARM Next gen programmable offload

LS2084A
- Cortex-A72
- 4-8 cores
- DPAA2
- 40G Pkt
- 20G Crypto
- 20-35W
- 1st 8x A72 ARM Next gen programmable offload

LX2160A
- *Cortex-A72*
- *16 cores*
- *100Gbps Pkt*
- *100Gbps Crypto*
- *40W*
- *1st 16nm product*

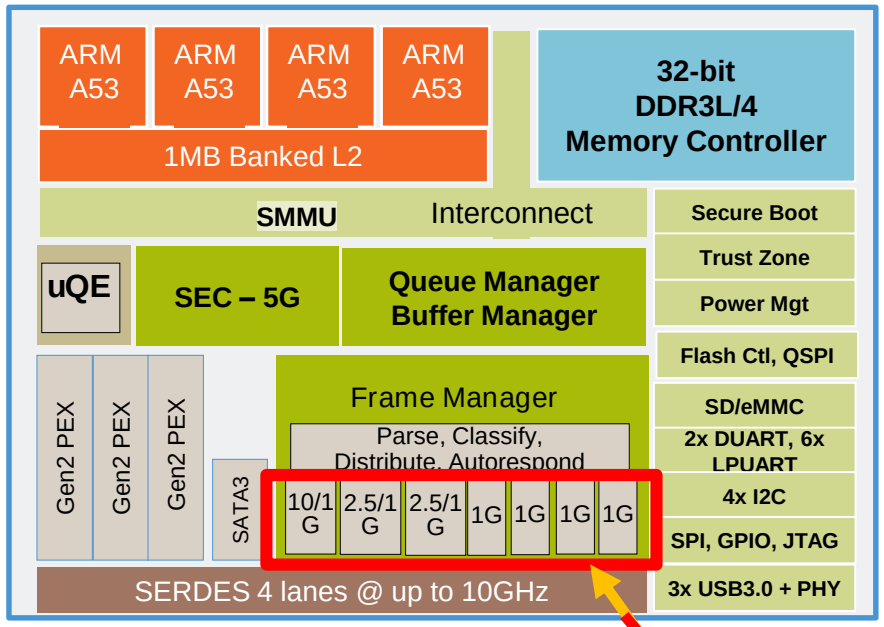
Auto Qual Plan*

In Development

Pin Compatible

* Additional products can be auto qualified with business justification

QorIQ Layerscape LS1043ACE (Grade 3)



Ethernet Interfaces

Major Milestone	Schedule
Engineering Samples Rev 1.1	Completed / October 4, 2016
Networking/Telecom Qualification	Completed / January 25, 2017
AECQ100 grade 3 Qual on Rev 1.1	Complete / Sept 12, 2017
PPAP Completion	June 2018

Auto Quality

- AEC Q100 Grade 3 (105 Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Process & Package

- 28HPM, ~4-8W Thermal Max @ 105C
- 23x23mm, Unlidded FCBGA, .8mm pitch (780 pins)

Performance

- ARM A53 x 4 @ up to 1.6GHz (LS1023A: 2 cores)
  - 19.5K DMIPS
  - SpecInt2k6 – 5.95, Rate -15
  - Neon SIMD in all CPUs
- 1x36b (including ECC) DDR3L/4 up to 1.6GT/s
  - 6.4GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen2 controllers
  - Multiple Ethernet MACs (up to 10G)

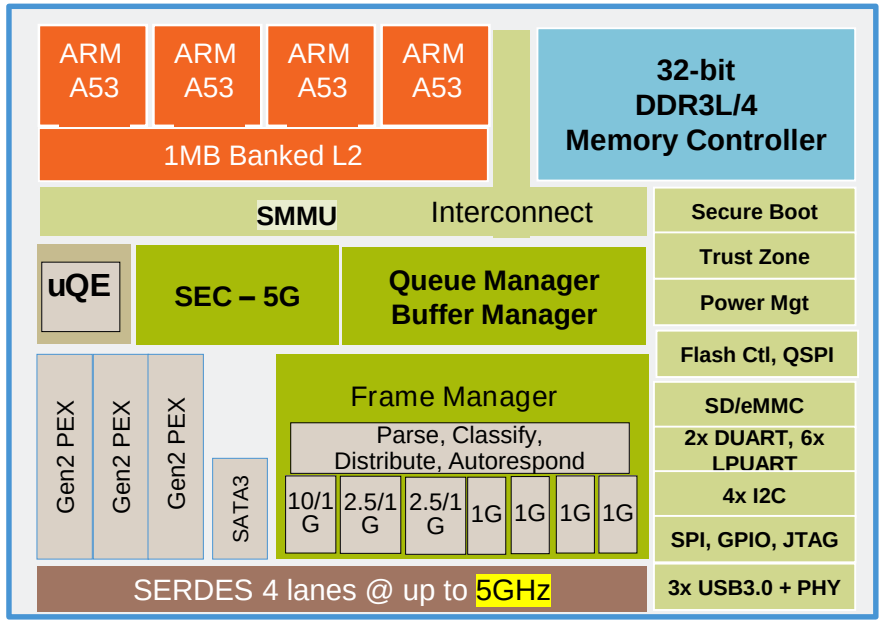
Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security

- 5Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

QorIQ Layerscape LS1043ABE (Grade 2)



Major Milestone	Schedule
Engineering Samples	Completed / May 2018
AECQ100 grade 2 Qual	On schedule / Oct, 2018
Grade 2 PPAP Completion	On schedule / December 2018

Performance

- ARM A53 x 4 @ up to 1.4GHz (LS1023A: 2 cores)
  - SpecInt2k6 – 5.2, Rate -13.1
  - SpecInt2k6 – 5.95, Rate -15
  - Neon SIMD in all CPUs
- 1x36b (including ECC) DDR3L/4 up to 1.6GT/s
  - 6.4GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen2 controllers
  - Multiple Ethernet MACs (up to 2.5G)

Auto Quality

- AEC Q100 Grade 2 (125 Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Process & Package

- 28HPM, up to 9W Thermal Max @ 125C
- 23x23mm, Unlidded FCBGA, .8mm pitch (780 pins)

Security

- 5Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

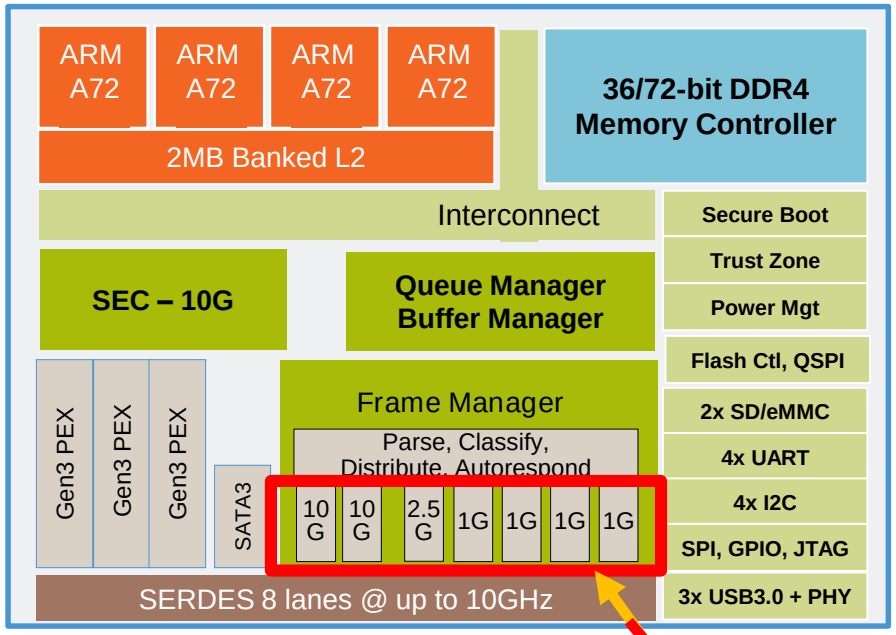
LS1043 SERDES Options

LS1043 SERDES (4 lanes)

	Grade 3				Grade 2
	Serdes 1				
	0	1	2	3	
SERDES Prot	A	B	C	D	
0000	unused	unused	unused	unused	
1555	XFI	PCIe 1	PCIe 2	PCIe 3	
2555	SGMII 2.5G	PCIe 1	PCIe 2	PCIe 3	
4555	QSGMII	PCIe 1	PCIe 2	PCIe 3	
4558	QSGMII	PCIe 1	PCIe 2	SATA	
1355	XFI	SGMII 1G	PCIe 2	PCIe 3	
2355	SGMII 2.5G	SGMII 1G	PCIe 2	PCIe 3	
3335	SGMII 1G	SGMII 1G	SGMII 1G	PCIe 3	
3355	SGMII 1G	SGMII 1G	PCIe 2	PCIe 3	
3358	SGMII 1G	SGMII 1G	PCIe 2	SATA	
3558	SGMII 1G	PCIe 1	PCIe 2	SATA	
3555	SGMII 1G	PCIe 1	PCIe 2	PCIe 3	
7000	PCIe 1				
9998	PCIe 1	PCIe 2	PCIe 3	SATA	
6058	PCIe 1		PCIe 2	SATA	
1455	XFI	QSGMII	PCIe 2	PCIe 3	
2455	SGMII 2.5G	QSGMII	PCIe 2	PCIe 3	
2255	SGMII 2.5G	SGMII 2.5G	PCIe 2	PCIe 3	
3333	SGMII 1G	SGMII 1G	SGMII 1G	SGMII 1G	
1460	XFI	QSGMII	PCIe 3		
2460	SGMII 2.5G	QSGMII	PCIe 3		
3460	SGMII 1G	QSGMII	PCIe 3		
3455	SGMII 1G	QSGMII	PCIe 2	PCIe 3	
9960	PCIe 1	PCIe 2	PCIe 3		
2233	SGMII 2.5G	SGMII 2.5G	SGMII 1G	SGMII 1G	
2533	SGMII 2.5G	PCIe 1	SGMII 1G	SGMII 1G	

- Rows with green right edge are supported on grade 2 version.
- Rows with black right edge are only supported on grade 3 version.

QorIQ Layerscape LS1046A



Status: In Production (Networking/Telecom)
Full Auto qual: If requested, ~6mos after MOU
Auto Production: Immediately upon qual completion

Auto quality

- AEC Q100 Grade 3 (105 Tj) - achievable, qual plan with MOU
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Process & Package

- 28HPM, ~8-15W Thermal Max @ 105C
- 23x23mm, Lidded FCBGA, .8mm pitch (780 pins)

Performance

- ARM A72 x 4 @ 1.8 GHz
  - 42.9K DMIPS
  - SpecInt2k6 – 13.3, Rate -37.4
  - Neon SIMD in all CPUs
- 1x36/72b (including ECC) DDR4 up to 2.1GT/s
  - 16.8GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen3 controllers
  - Multiple Ethernet MACs (up to 10G)

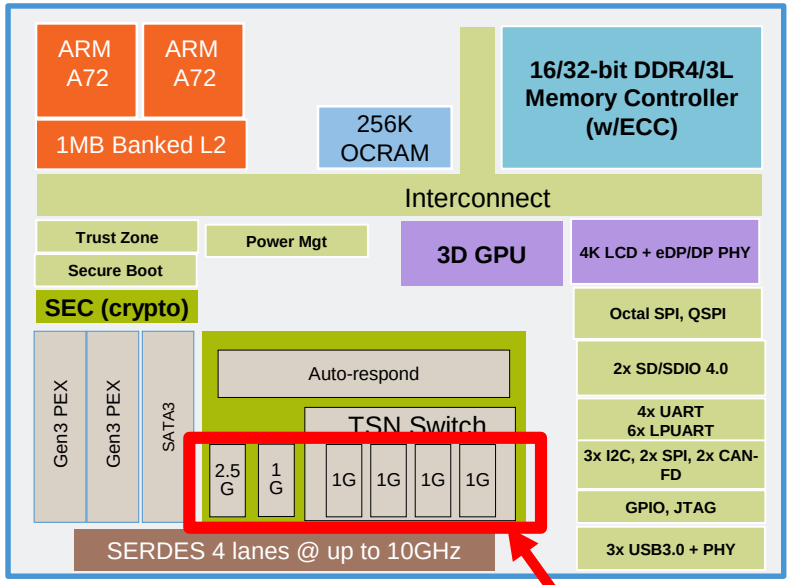
Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security

- 10Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Layerscape LS1028A



Ethernet Interfaces

Samples: **Q3 2018**
Full Auto qual: **Q2 2019**
Auto Production: **Q2 2019**

Auto quality

- AEC Q100 Grade 3, supports 125 Tj
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Process & Package

- 28HPM, 1.3GHz ~9W @ 105C; 800MHz ~4.5W @ 105C
- 17x17mm, FCBGA, .75mm pitch (448 pins)

Performance

- ARM A72 x 2 @ 1.3 GHz
  - ~15.4K DMIPS
  - SpecInt2k6 – 9.4, Rate -16.9
  - Neon SIMD in all CPUs
- 1x16/32b (with ECC) DDR4/3L up to 1.6GT/s
  - 6.4GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen3 controllers
  - Multiple Ethernet MACs (up to 2.5G)

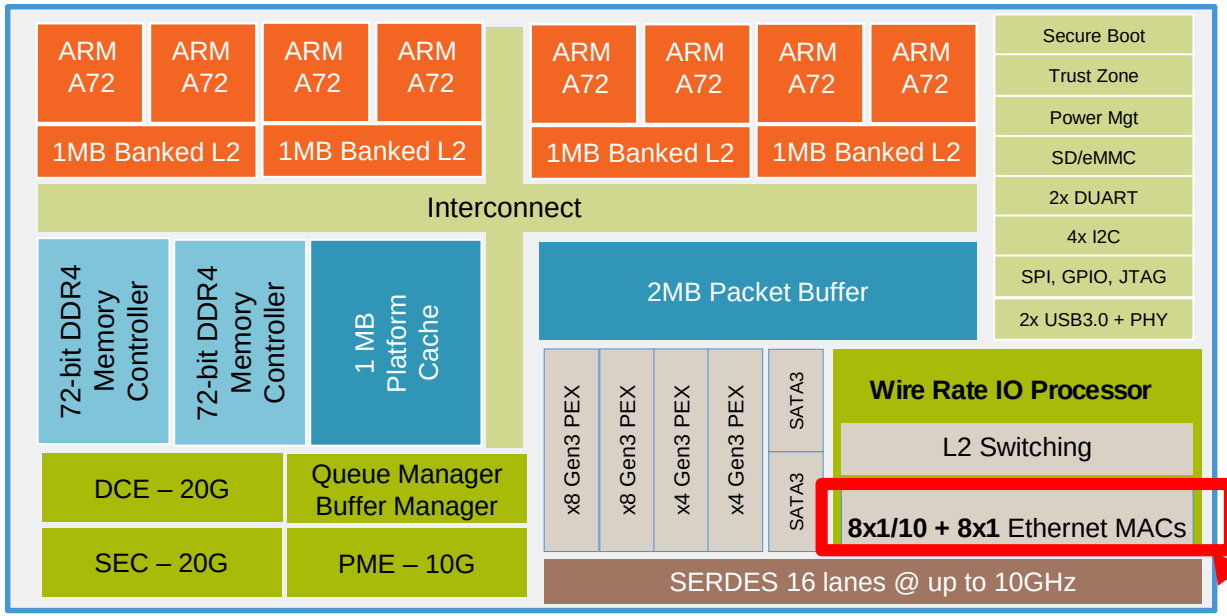
Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security

- 5Gbps Crypto Acceleration
- IPsec, SSL, Sign/Verify
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Layerscape LS2084A



Major Milestone	Schedule
Samples (Production Rev)	Dec 2017
Networking/Telecom Qualification	March 2018
AECQ100 grade 3 Qual on production rev	Nov 2018
PPAP Completion	Dec 2018

Auto Quality

- AEC Q100 Grade 3 (105C Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Performance

- ARM A72 x 8 @ 2.0 GHz
  - 95.3K DMIPS
  - SpecInt2k6 – 14.5, Rate -83.4
  - Neon SIMD in all CPUs
- 2x72b (including ECC) DDR4 up to 2.1GT/s
  - 33.6GB/s memory BW
- High Speed IO
- Multiple PCIe Gen3 controllers
- Multiple Ethernet MACs (up to 10G)

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Process & Package

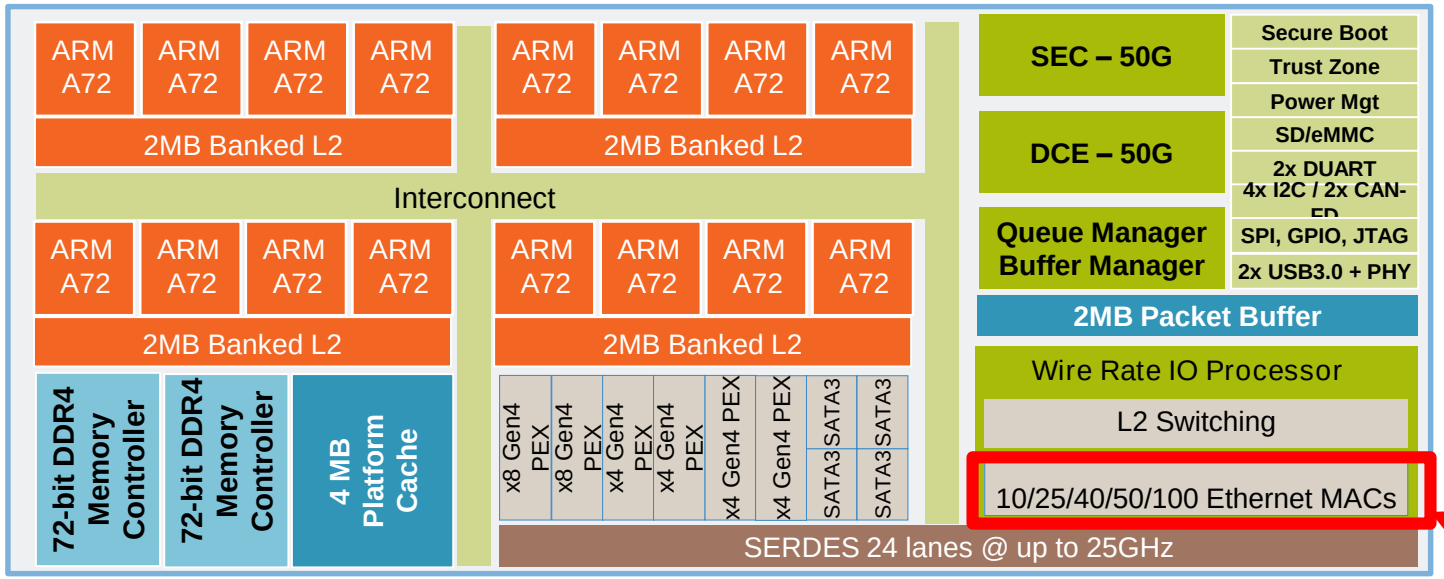
- 28HPM, ~40W Thermal Max @ 105C
- 37.5 x 37.5 mm, lidded FCBGA, 1mm pitch, 1292 pins

Ethernet Interfaces

Security

- 20Gbps Crypto Acceleration
- MACSEC, IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Layerscape LX2160A



Ethernet Interfaces

Samples:	March 2018
Full Auto qual:	Q1 2020
Production:	Q1 2020

Auto quality

- AEC Q100 Grade 3 (105 Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Performance

- ARM A72 x 16 @ 2.2 GHz
  - ~210K DMIPS
  - SpecInt2k6 – 16, Rate -183
  - Neon SIMD in all CPUs
- 2x72b (including ECC) DDR4 up to 3.2GT/s
  - 51GB/s memory BW
- High Speed IO
- Multiple PCIe Gen4 controllers
- Multiple Ethernet MACs (up to 100G)

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Process & Package

- 16nm FinFET Compact, ~40W Thermal Max @ 105C
- 40x40mm, Lidded FCBGA, 1mm pitch (1517 pins)

Security

- 50Gbps Crypto Acceleration
- MACSEC, IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Remaining QorIQ Layerscape family

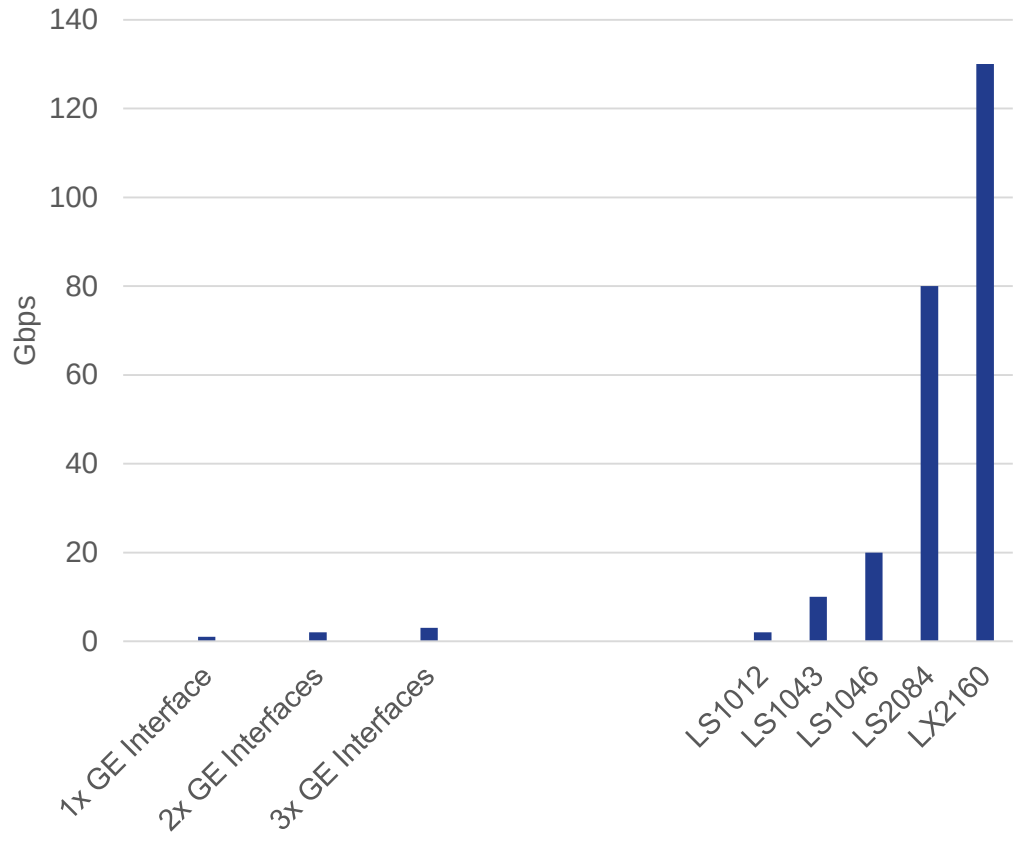
- Other Layerscape devices can also be auto qualified (grade 3) with business justification.

- Some exceptions, but in general, devices that pass the telecom qualification process will pass automotive qualification process at least to Grade3.

QorIQ Layerscape - Summary Table of Ethernet Capability

Part Number	Description	Supported Ethernet Rate	Ethernet MAC	Supported Media Interface	Hardware Acceleration
LS1043A	Gateway, TCU. General Purpose Processing	6x 1Gb 2x 2.5Gb 1x 10Gb 1x 4Gb	FMAN mEMAC	RGMII, SGMII, QSGMII, XFI	DPAA Parse, classify, police, soft switching
LS1046A	Gateway, TCU. General Purpose Processing	7x 1Gb 3x 2.5Gb 2x 10Gb 1x 4Gb	FMAN mEMAC	RGMII, SGMII, QSGMII, XFI	DPAA Parse, classify, police, soft switching
LS2084A	ADAS, Central Processor	6x 1Gb 4x 2.5Gb 8x 10Gb 2x 4Gb	WRIOP mEMAC	RGMII, SGMII, QSGMII, XFI	DPAA2 Parse, classify, police, soft switching
LS1028A	Gateway, AVB, Domain Controller	4x 1Gb 1x 2.5Gb 1x 4Gb + 4-port TSN Switch	ENETC	RGMII, SGMII, QSGMII	TSN Switching
LX2160A	ADAS, Central Processor	L2 Switching with 1G, 2.5G, 10G, 25G, 40G, 50G and 100G Ethernet + Up to two RGMII interfaces	WRIOP mEMAC	RGMII, SGMII, QSGMII, XFI	DPAA2 Parse, classify, police, soft switching

Comparative NXP ARM Packet Processing Capacity & High Speed IO



	Ethernet MAC (capable, not aggregate)			PCIe		USB	
Product	10G	2.5G	1G	Controllers	Max lanes	2.0	3.0
LS1012A	0	2	2	1x 2.0	2	1	1
LS1043A	1	2	5	3x 2.0	4	0	3
LS1046A	2	2	5	3x 3.0	8	0	3
LS2084A	8	8	8	3x 3.0	16	0	2
LX2160A	10	10	16	6x 4.0	24	0	2

Refer to product specific documents for exact features and performance

Agenda

- Introduction
- Ethernet in Automotive
- OSI model
- FEC and ENET Ethernet Blocks
- Device Specific Ethernet implementation
  - S32K, S32x and MPC57xx and i.MX
- DPAA-based Ethernet Blocks
- Device Specific Ethernet implementation
  - QorIQ Layerscape Series for Automotive
- **Switches and PHYs**
- Closing Remarks and Summary

Automotive Ethernet Switches and PHYs

NXP Ethernet Portfolio: The Auto-Native Portfolio

Flexible, Scalable Solution

TJA1100 / TJA1101

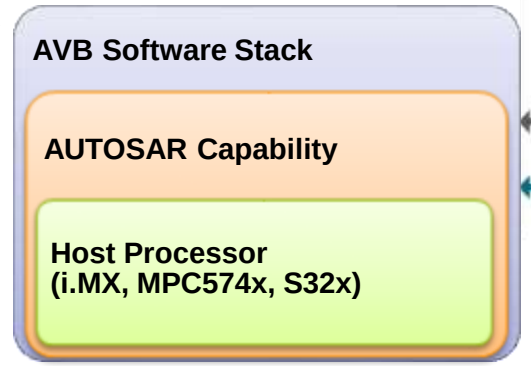
- IEEE 100BASE-T1 Compliant PHY
- Fully automotive qualified
- Enhanced Power Management to save battery life

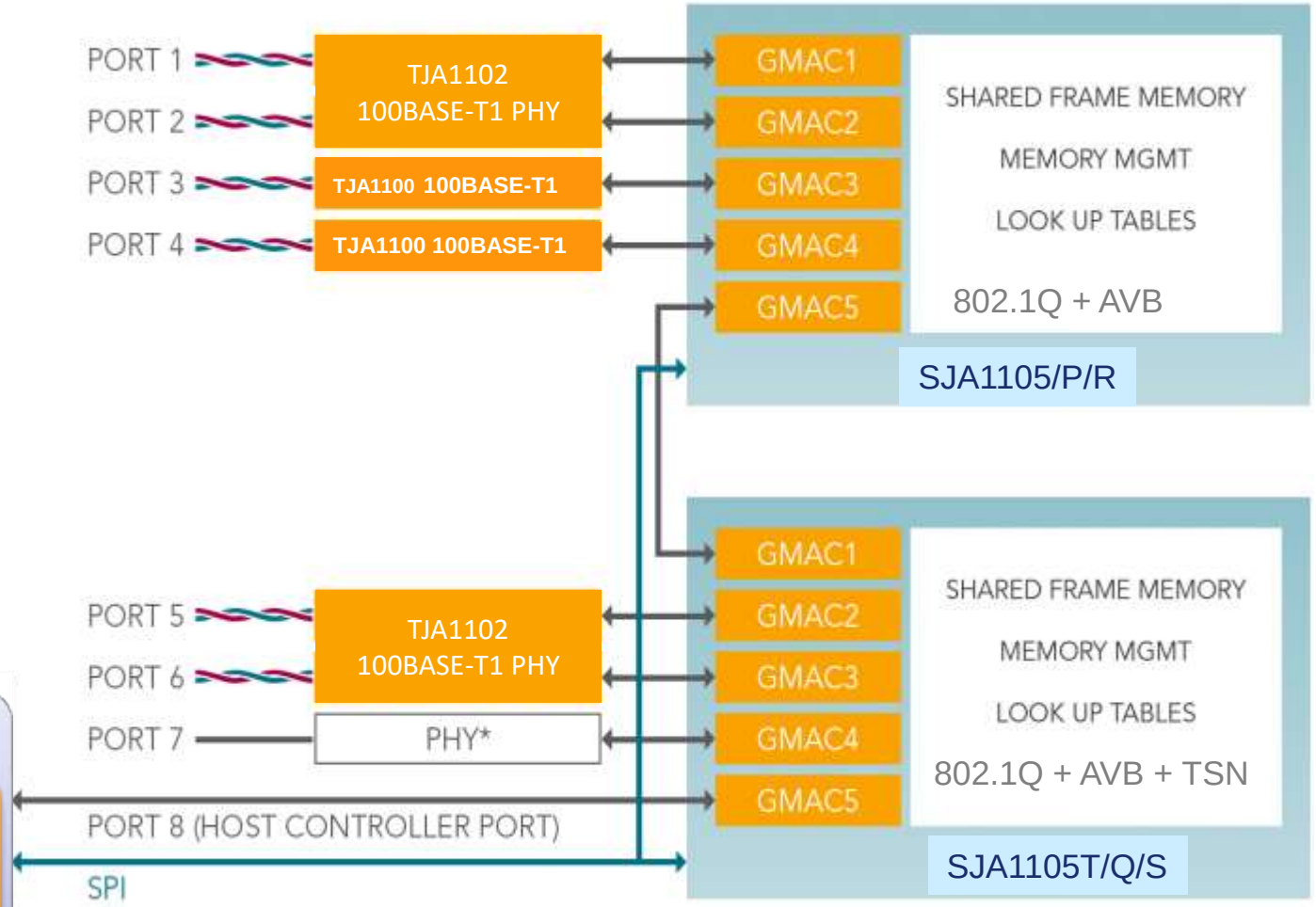
TJA1102 / TJA1102S

- Dual / Single IEEE 100BASE-T1 PHY
- Minimal external component count
- Robust automotive grade EMC and ESD
- Standardized Sleep/Wake-Up per OPEN TC10

SJA1105 /P/Q/R/S/T

- Layer 2 Store and Forward Switch family
- Supports AVB, TSN and Deterministic Ethernet
- 10/100/1000 Mbps interfaces
- MII/RMII/RGMII/SGMII Interface
- Port Mirroring and VLAN support (IEEE 802.1Q and IEEE 802.1P)





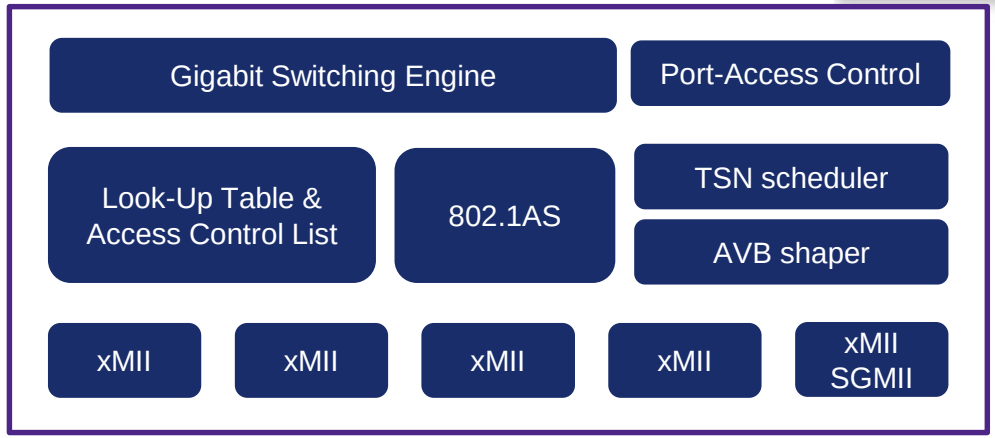
Automotive Ethernet Switch – SJA1105P/Q/R/S

Small form factor
- Non blocking gigabit architecture
- Package: LFBGA-159 (12x12 mm2)
- Temperature range: - 40 °C …+105°C

Flexible and cost optimized
- 5x Integrated (G)MACs
- MII / RMII / RGMII / SGMII interfaces
- 4x variants for optional TSN and SGMII features
  - SJA1105P / SJA1105Q / SJA1105R / SJA1105S

Advanced feature set
- Support for MAC-Address white/black listing
- IEEE 802.1X Port-Based Network Access Control
- AVB support
- Per-port and priority traffic policing
- Advanced Network debugging features

Software
- Linux drivers (released)
- NXP original AUTOSAR drivers (released)
- AVB/gPTP SW stack (beta available)



Delta from SJA1105EL/SJA1105TEL
- 1x optional SGMII interface
- Extended RGMII IO supplies (1V8, 2V5, 3V3)
- TCAM-based L2 LUT and ACL features
- Support for Q-in-Q double VLAN tagging

NXP Ethernet Switches

Features	SJA1105/ SJA1105T	SJA1105P/ SJA1105Q	SJA1105R/ SJA1105S
Package	LFBGA159 12x12mm2 0,8mm pitch		
Ports	• 5x MII/ RMII / RGMII • RGMII 2v5 IO (no internal delay line)	• RGMII 1.8/2.5/3.3V IO, with integrated delay line	• 4x MII/ RMII / RGMI • 1x SGMII
AVB/ TSN	• Full AVB Hardware Spec • TSN/Scheduled Traffic (SJA1105T only) • TSN/Per-stream policing* (*pre standard)	• TSN features on SJA1105Q only	• TSN features on SJA1105S only
Configuration	Via SPI and external host controller		
Other Features	• Hash-based look-up table (LUT) • Port/priority BW policing • Full VLAN support VLAN tag editing • Frame mirroring and diagnostic Features	• Non-conflicting address Look-up table (LUT) • LUT with extended security features • MAC address white & black-listing • Double VLAN tag support	

Features Delta Comparison

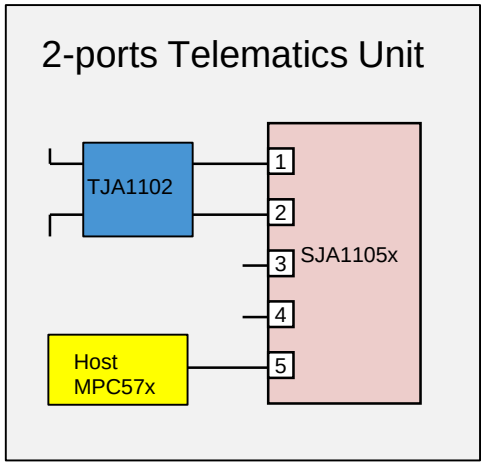
SJA1105 Series Overview

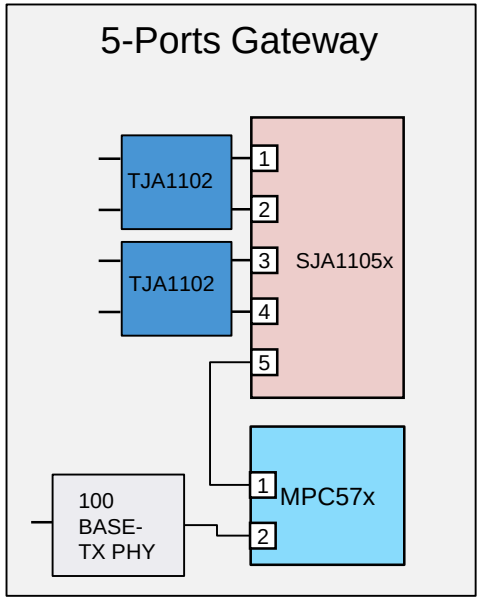
	SJA1105P IP updates (TCAM, RGMII update, Black listing, etc…)	TSN support - Time-aware shaping	SGMII interface	Pin Compatible	Software Compatible
SJA1105				●	●
SJA1105T		●		●	●
SJA1105P	●			●	○
SJA1105Q	●	●		●	○
SJA1105R	●		●	○	○
SJA1105S	●	●	●	○	○

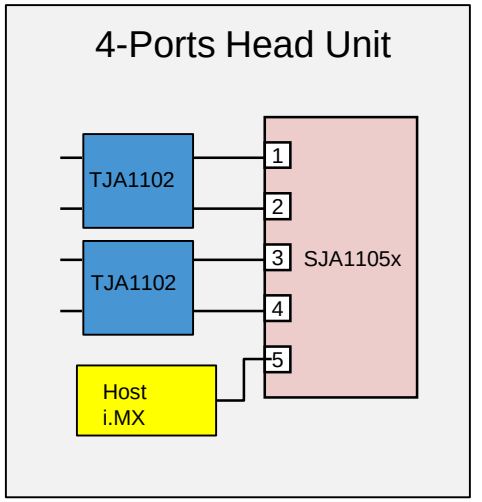
● Compatible with other black dots

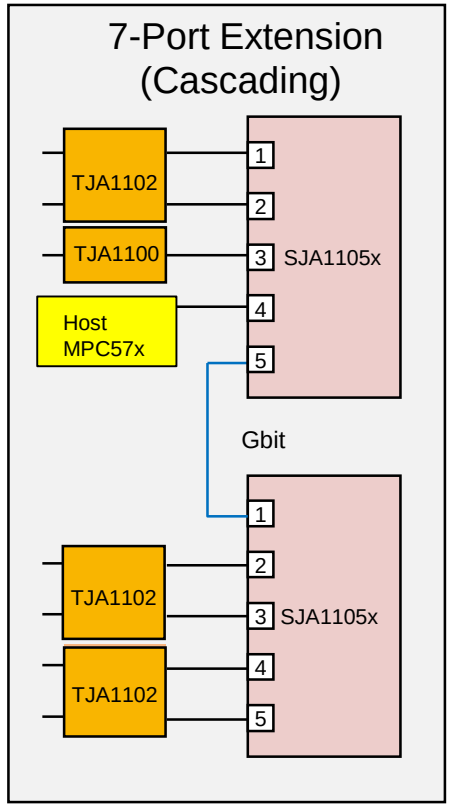
○ Compatible with other white dots

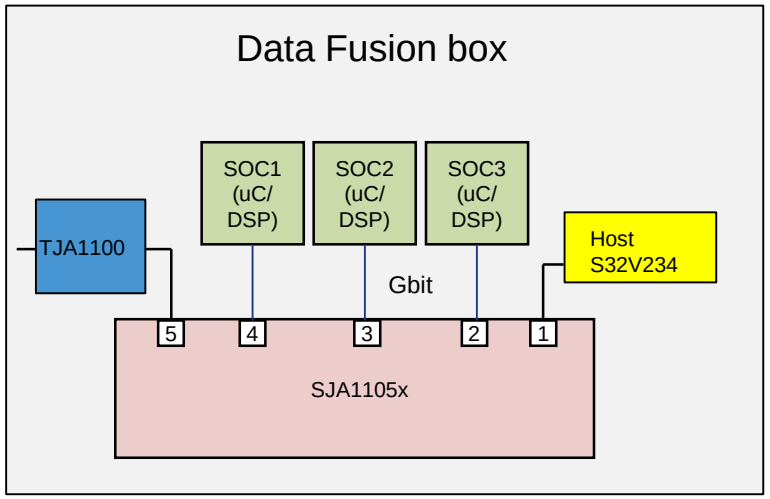
TJA110x & SJA1105x Use Cases

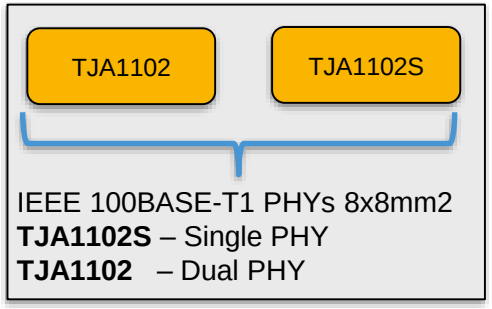


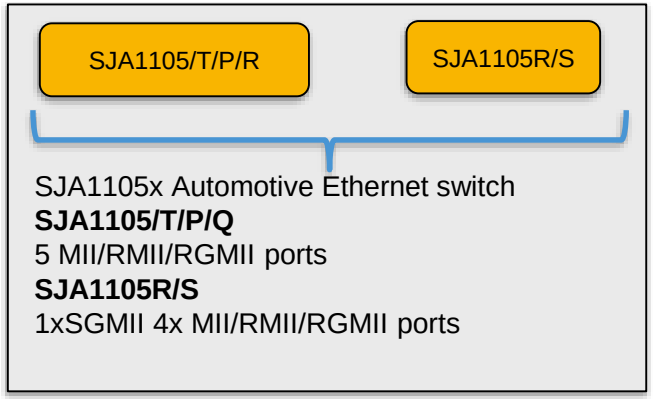












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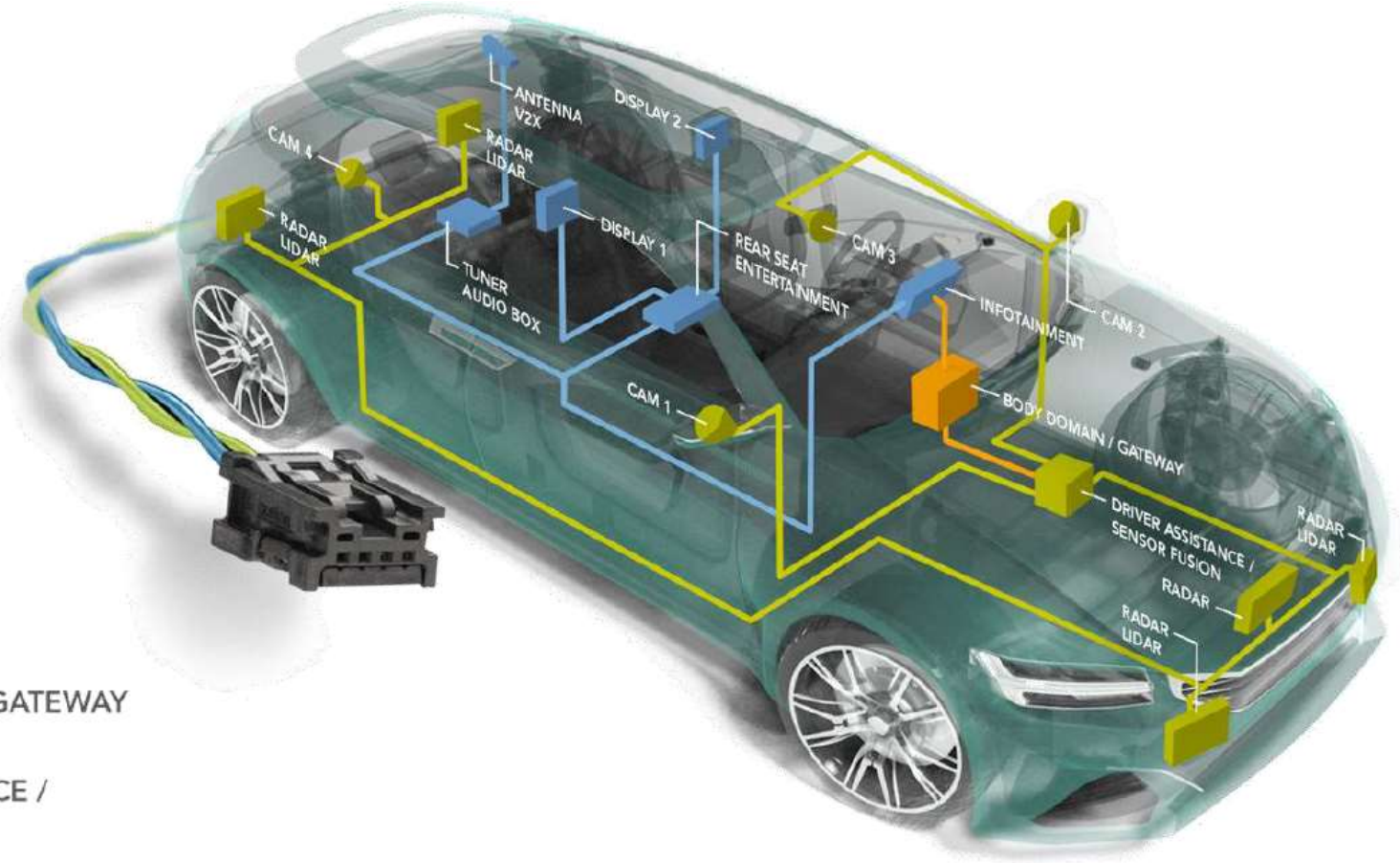
NXP has a long history with Automotive Ethernet

OPEN ALLIANCE — **CO-FOUNDER**

IEEE — **MEMBER RTPGE**
Reduced Twisted Pair Gigabit Ethernet

AVNU — **PROMOTER**

JasPar — **MEMBER**



INFOTAINMENT

BODY DOMAIN / GATEWAY

DRIVER ASSISTANCE / SENSOR FUSION

ETHERNET BACKBONE

Summary

- Long history of Automotive Ethernet
- Wide range of application specific devices with Ethernet Capability
  - 10/100Mb or 10/100/1000Mb support on most Ethernet capable devices
  - Support up to 10s or 100s of Gb on the QorIQ Layerscape family
- Auto Qualifications across the board
- Ethernet offload of layer 2 and layer 3 functions in hardware
- Expandable Ethernet capability using external Switches and PHYs
  - Adapt to wide range of vehicle networking configurations
  - Increase the number of ports
- Summary Tables of Ethernet Capability across Automotive MCUs and MPUs

Any Questions?

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