Timing & Signal Analysis
Benefits and Approaches

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Agenda

- What is a TSA?
- Traditional Approach (pTSA)
- The vTSA
- i.MX8 vTSA Tool
- pTSA vs. vTSA Demonstration with i.MX8 MEK
- Pros and Cons
- Summary

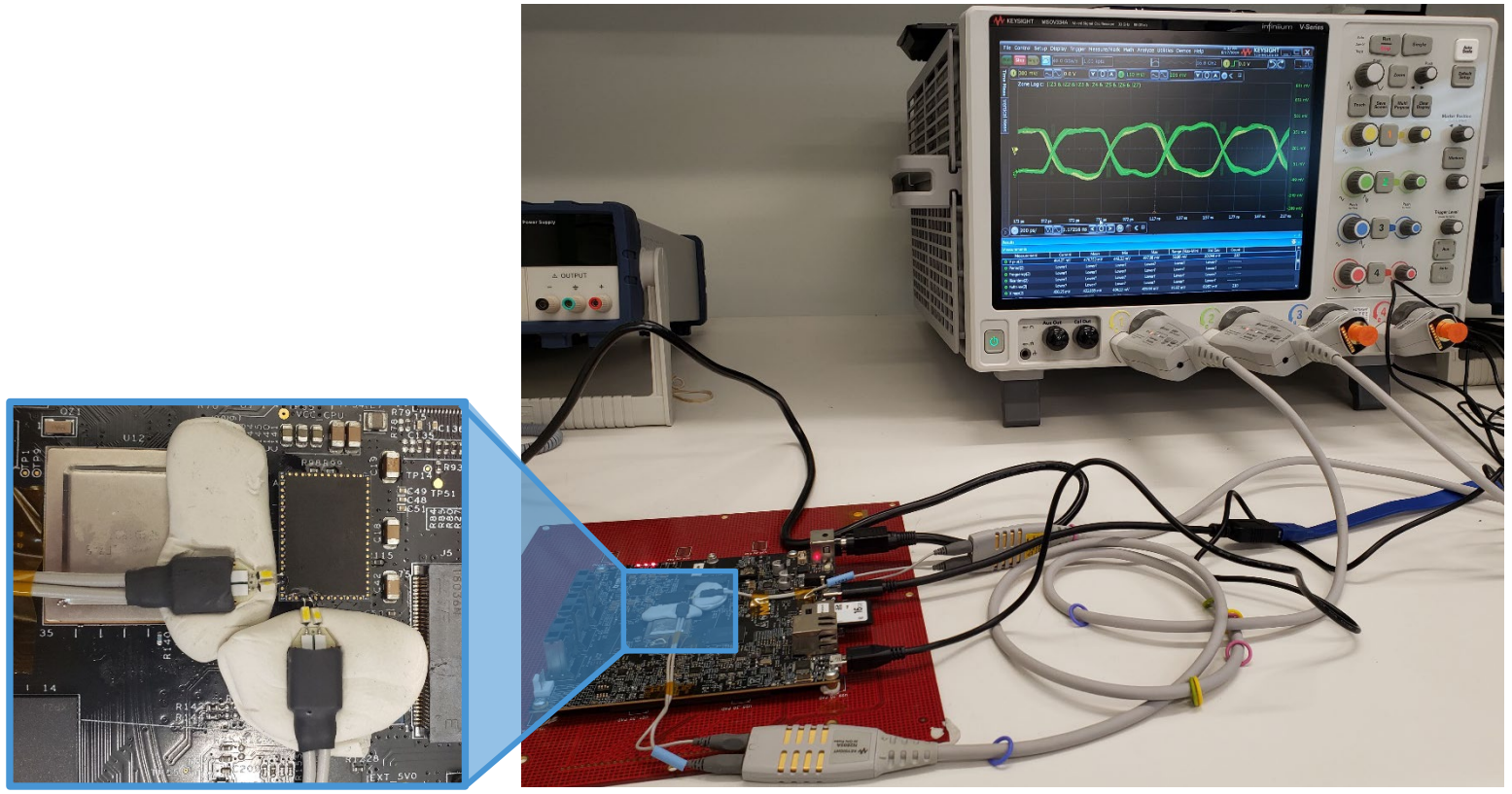
What is a TSA?

- Timing & Signal Analysis (TSA) is Micron's approach to validate that the memory interface is being operated properly and with margin in the system

- TSAs typically include measurement of the following:
  - Signaling margin
  - Critical timings vs. spec
  - Power supply ramps and levels
  - Mode register settings

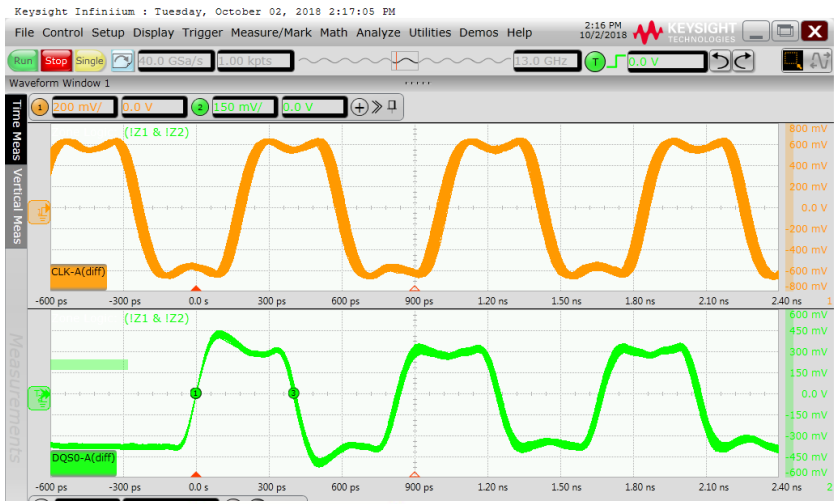
Traditional Approach – pTSA

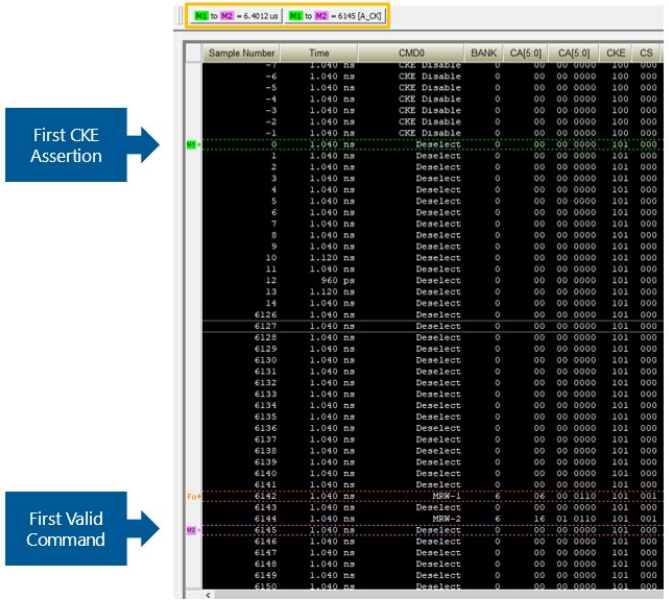
- Historically, TSAs (pTSA = physical TSA) are done by connecting test equipment to a subset of the memory interface and taking measurements
- Requirements:
  - Rework
  - Socket/interposer
  - High bandwidth oscilloscope/logic analyzer and probes



pTSA on i.MX8QXP MEK

pTSA Output





- pTSA reports typically include:
  - LA capture of initialization/calibration
  - Summary of final mode register settings
  - Detailed scope captures and measurements
  - Summary of measurements vs. spec

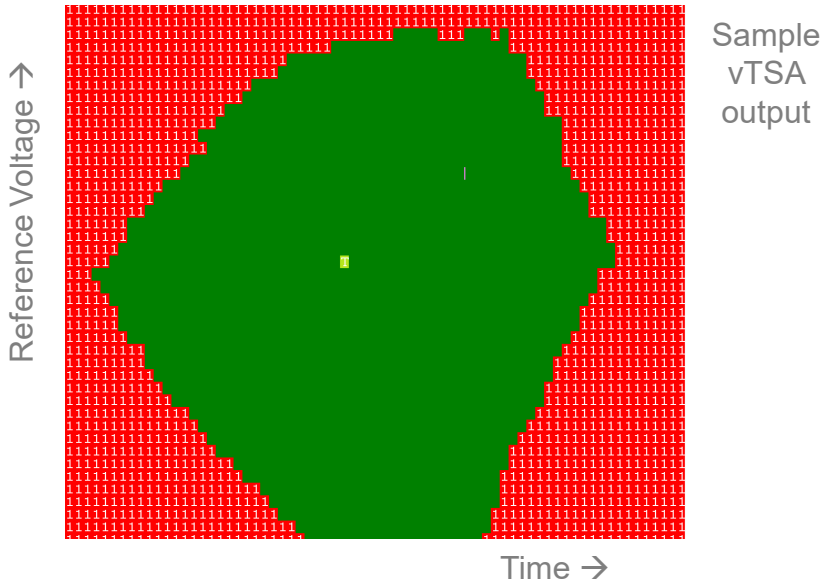
Parameter	Symbol	Limit	Spec	Measured	Unit	Tool	Signal	Remarks
Power Supply Parameters								
Core 1 power	VDD1	Min	1700	1797	mV	Oscope	-	In Spec
		Max	1950	1809	mV	Oscope	-	In Spec
		↑	↑	1799	mV	Meter	-	In Spec
Core 2 power / IO buffer power [Electrically Connected]	VDD2 / VDDQ	Min	1060	1073	mV	Oscope	-	In Spec
		Max	1170	1098	mV	Oscope	-	In Spec
		↑	↑	1088	mV	Meter	-	In Spec
Initialization and Calibration Parameters								
Maximum voltage-ramp time	tINIT0	Max	20	46.1	ms	Oscope	-	Out of Spec
Minimum RESET LOW time after voltage ramp complete	tINIT1	Min	200	68303	us	Oscope	-	In Spec
Minimum CKE low time before RESET high	tINIT2	Min	10	>> 10	ns	Oscope	@Ch.A	In Spec
Minimum CKE low time after RESET high	tINIT3	Min	2	2.51	ms	Oscope	@Ch.A	In Spec
Minimum stable clock before first CKE high	tINIT4	Min	5	>> 5	tCK	Oscope	@Ch.A	In Spec
Minimum idle time before first MRW/MRR command	tINIT5	Min	2	6.40	us	LA	@Ch.A	In Spec
ZQ calibration time	tZQCAL	Min	1	1.01	us	LA	@Ch.A	In Spec
ZQ calibration latch time	tZQLAT	Min	30	40.0	ns	LA	@Ch.A	In Spec
Clock Parameters								
Average clock cycle time	tCK(avg)	Min	535	833	ps	Oscope	CK@Ch.A	In Spec
Average clock high-level width	tCH(avg)	Min	0.460	0.496	tCK	Oscope	CK@Ch.A	In Spec
		Max	0.540	0.496			CK@Ch.A	In Spec

pTSA Pitfalls

- The pTSA approach provides direct measurement of the memory interface, but has some downsides:
  - Requires expensive test equipment
  - Connecting test equipment affects signal path – more of a concern with higher interface speed/less margin
  - Risk of damaging system during rework
  - Not feasible to measure entire memory interface
  - Take several weeks to complete

Another Approach – vTSA

- A “virtual” TSA uses the memory controller itself to test margins without test equipment
  - “Virtual” does not mean simulation!
  - Memory controllers have the ability the alter timings, voltage references, termination settings, etc. for both incoming and outgoing signals
  - “Training” is when the memory controller sweeps these parameters and finds the configuration with the most margin for operation
  - A vTSA simply logs this information for output, which provides insight into the system’s signaling margin without the need for test equipment
  - Initialization and calibration settings can be dumped to a file for analysis as well



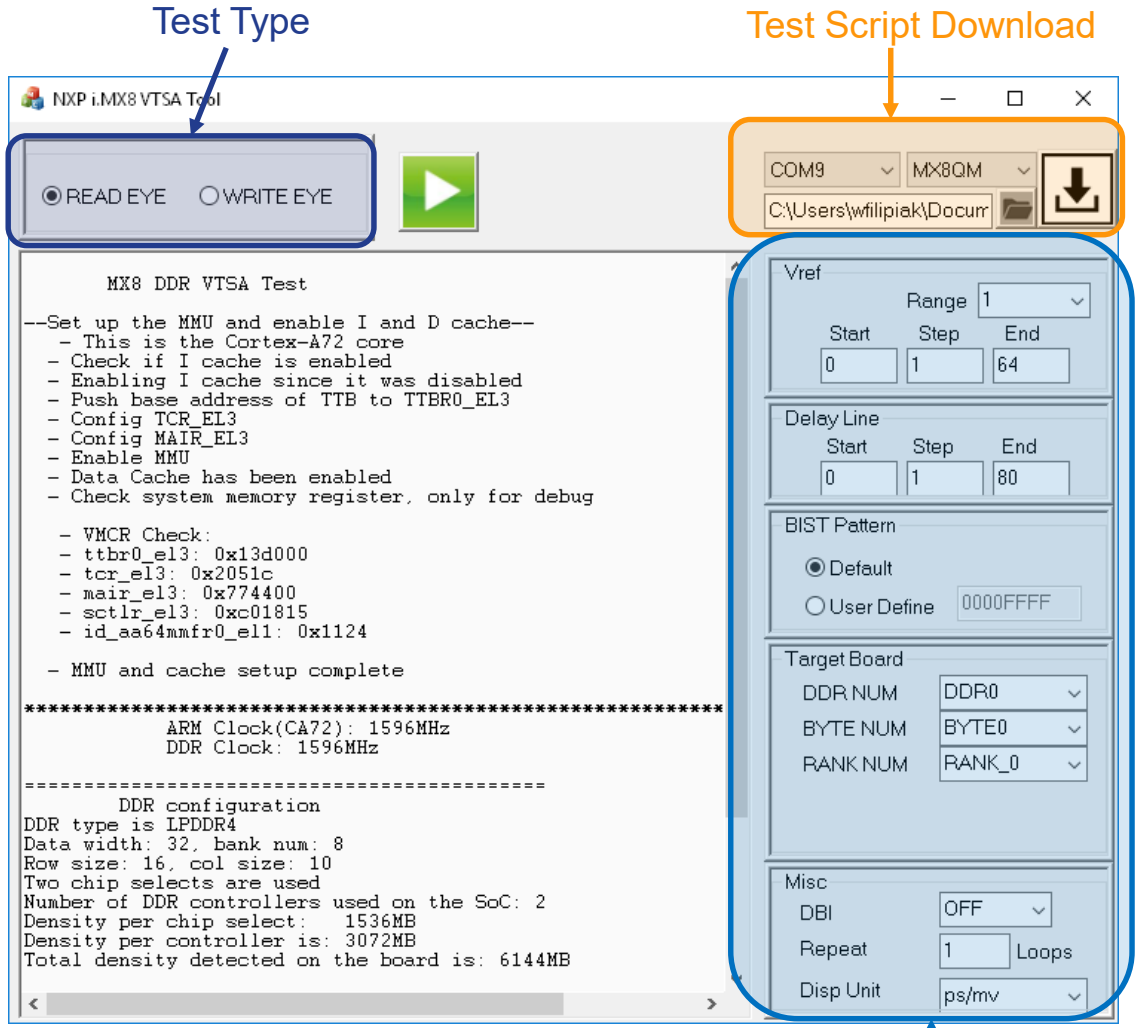
vTSA Merits

- The lack of test equipment provides a number of advantages:
  - No signal impact from socket/interposer/probes/etc.
  - No risk of destroying the board through re-work
  - Much quicker turn-around time
  - Margin information is collected across the entire memory interface, not just a subset

- Unfortunately, a vTSA cannot cover all items covered by a pTSA
  - Power supply ramps and levels
  - Clock parameters, preambles, some timing specs

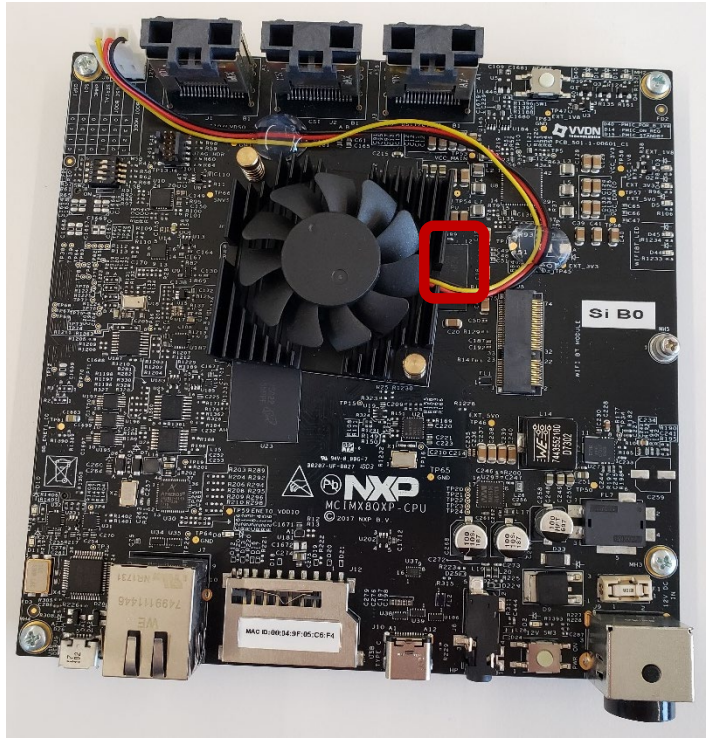
i.MX8 vTSA Support

- i.MX8 has support for vTSA!
  - Target for availability is end of 2019, early access through local FAE
  - Distributed through an NXP Community page
- Details
  - Windows PC
    - UART communication
    - USB in SDP
  - i.MX8QM: Test software runs on Cortex A72
  - i.MX8QXP: Test software runs on Cortex A35
- Windows GUI makes characterization effortless
  - Download test script through UART
  - Read/Write selection
  - Configuration settings (sweep ranges, byte/rank, pattern, etc)



i.MX8 vTSA GUI

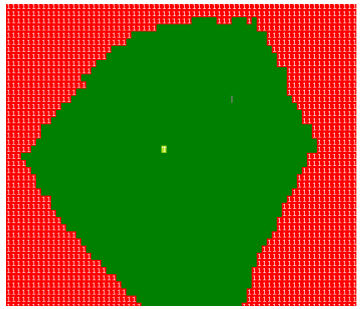
pTSA vs. vTSA Demonstration

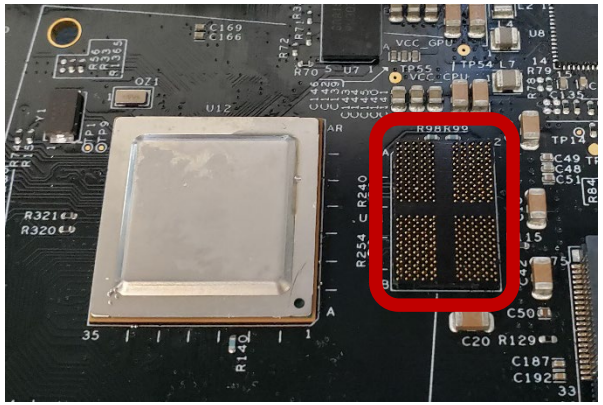


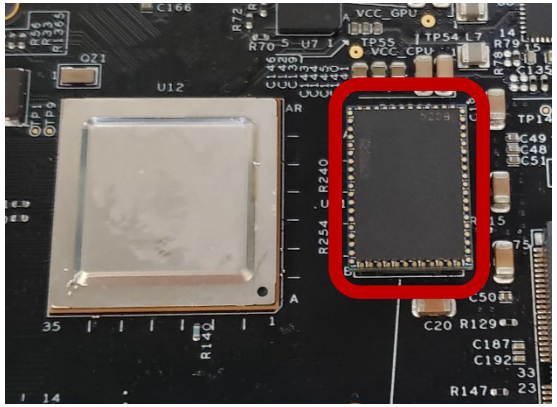
i.MX8QXP MEK

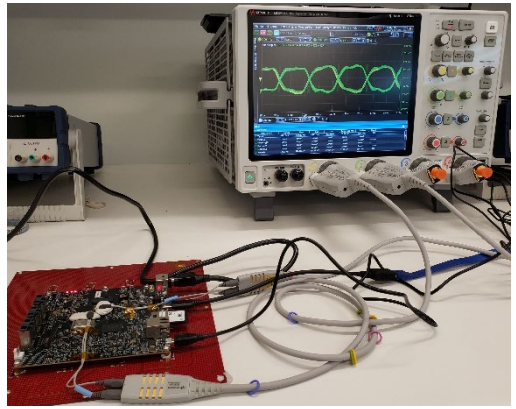
- Both pTSA and vTSA performed on an i.MX 8QuadXPlus Multisensory Enablement Kit (MEK)
  - MEK contains several Micron memory components:
    - 3GB LPDDR4 DRAM
    - 32GB eMMC 5.0
    - 512Mb QSPI NOR
  - pTSA/vTSA performed on the LPDDR4 component
    - 6 Gb die, 4 die in package
    - Dual channel/dual rank

pTSA vs. vTSA Process

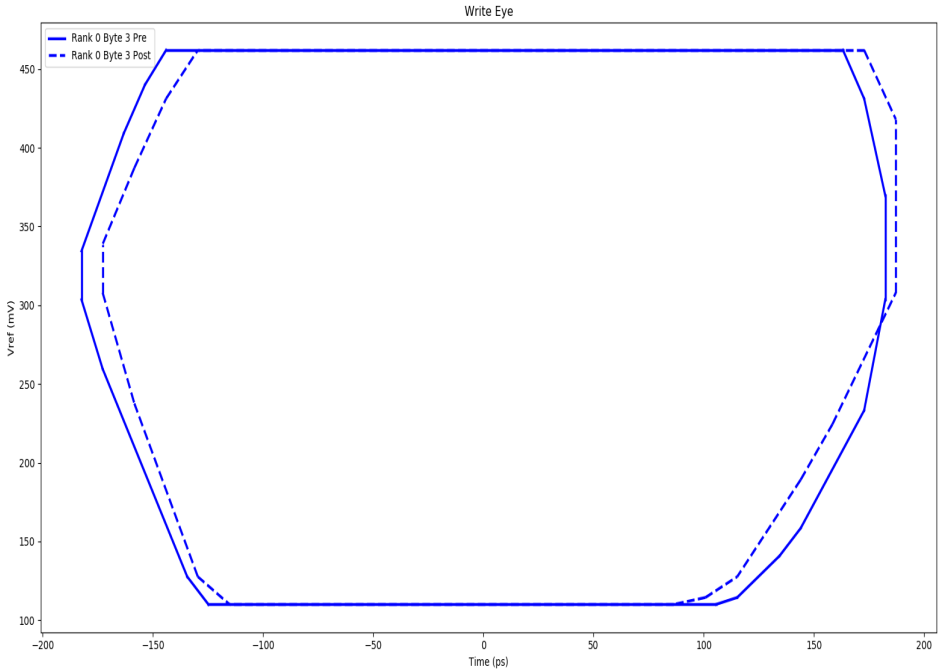








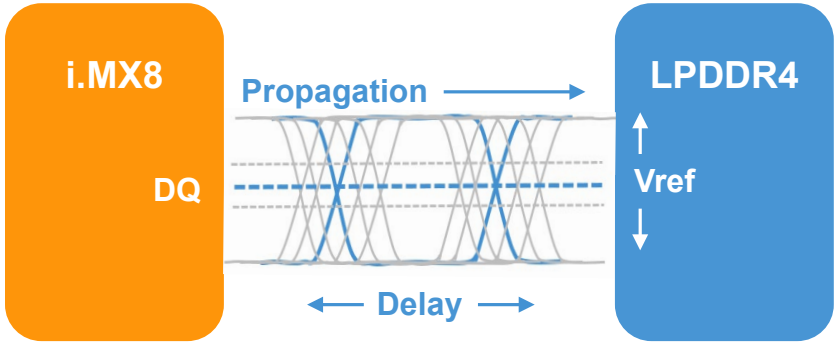
Impact of Test Equipment



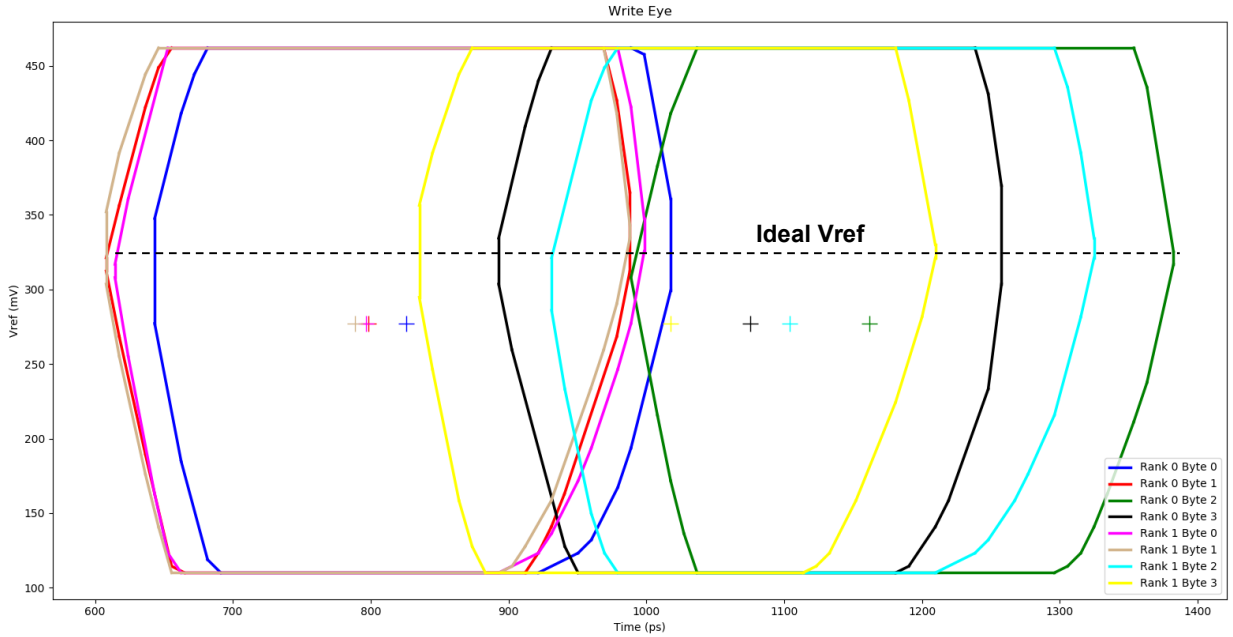
vTSA before and after test equipment attached to DRAM

- Introduction of test equipment (socket, interposer, probes) will affect signal margin
- vTSA measurements can be taken before and after test equipment is attached to study the effect on signal margin
- An example is shown here where write eye collapse can be seen due to the test equipment
  - ~5% reduction observed in this example
- For vTSA/pTSA comparison, it is important to compare apples-to-apples
  - De-embedding was chosen in this case to compare directly to vTSA results without test equipment attached

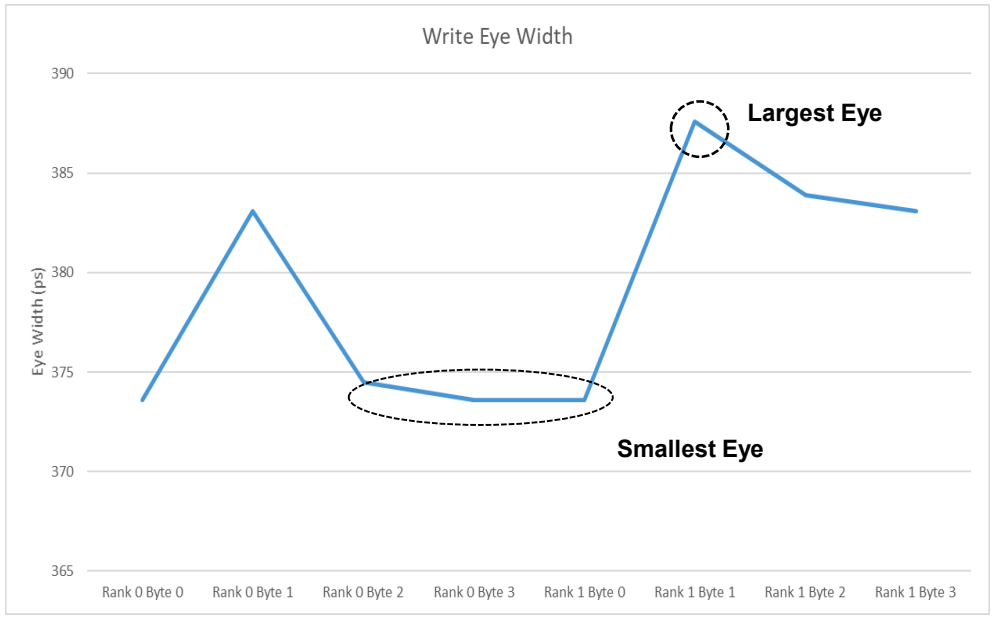
Write Eye: vTSA



- Write eye of the worst bit of each rank/byte can be shown through vTSA
- Vref range is too small to see the top/bottom of data eye
- Training chose ~275mV for Vref, which is a bit low based on the eye diagrams
- Training chose the middle of the eye in terms of delay for each rank/byte

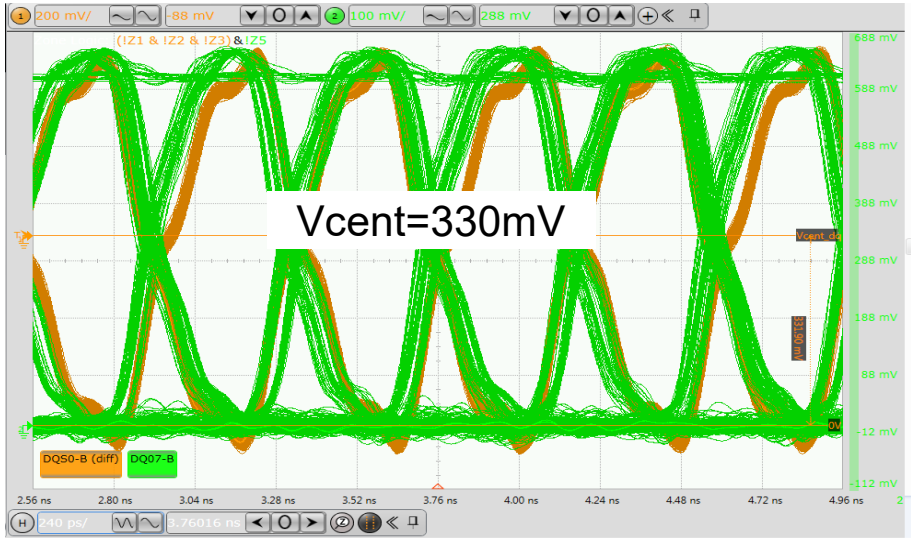


vTSA write eye across rank/byte



Write eye width across rank/byte

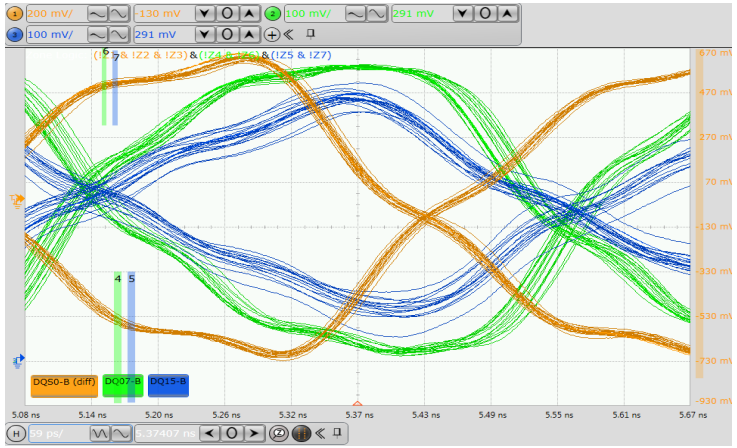
Write Eye: pTSA



Write eye of single DQ (shown against DQS)

- Not feasible to measure each rank/byte, so chose a bit from the rank/byte with the smallest eye in vTSA
  - Vcent=330mV, which is as expected from vTSA
  - Eye width is ~370ps, which agrees with vTSA
  - Eye height is ~550mV, which exceeds the available range in vTSA

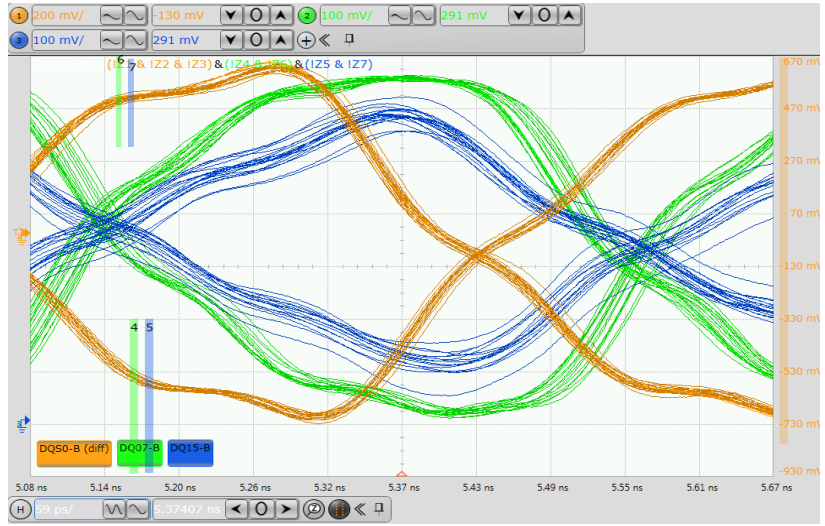
- Samples another bit from a different rank/byte with a similar eye in vTSA
  - Eye appears much smaller, which does not agree with vTSA results
  - Why? Which result should we trust?



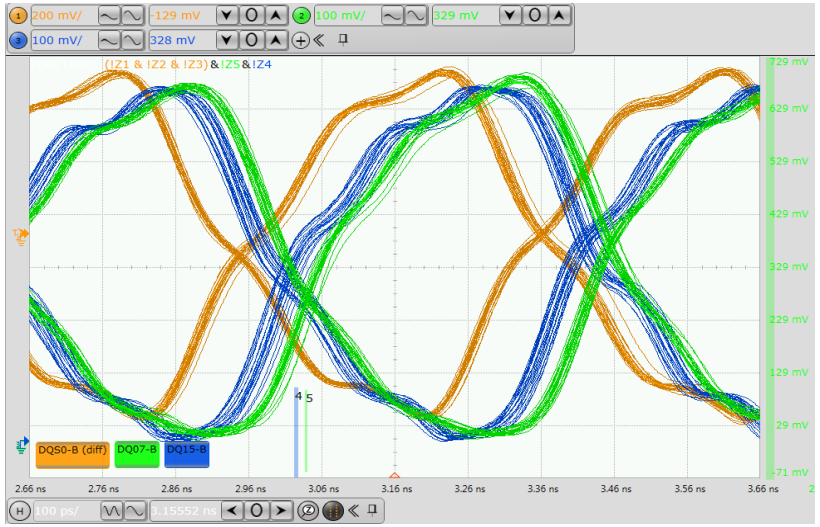
Write eye of two DQs (shown against DQS)

Write Eye: pTSA

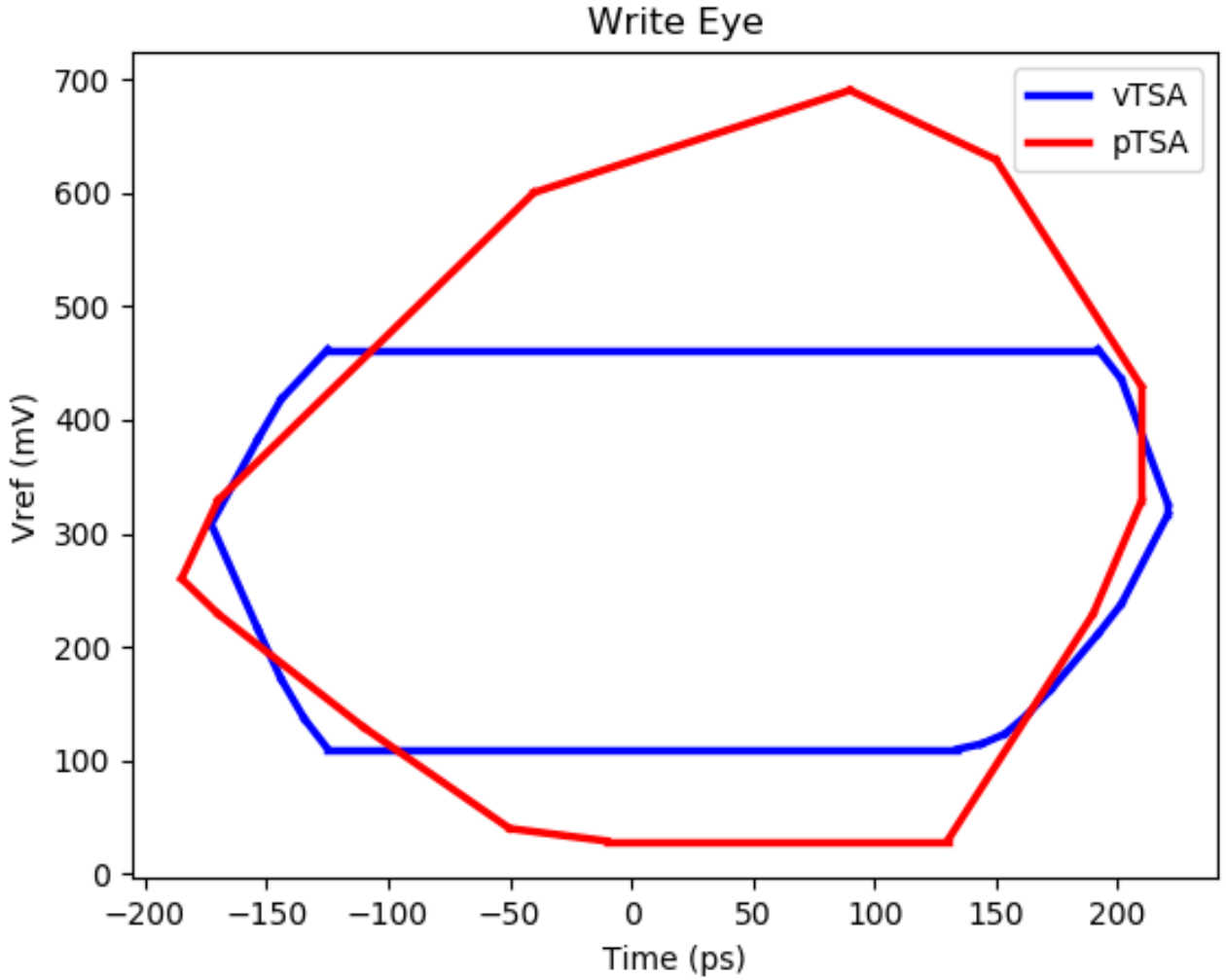
- Inspected physical setup and found poor connection to probe ground
  - Re-soldering the probe addressed this issue
  - vTSA approach avoids issues with test equipment that can result in misleading results!



Re-soldered probe GND

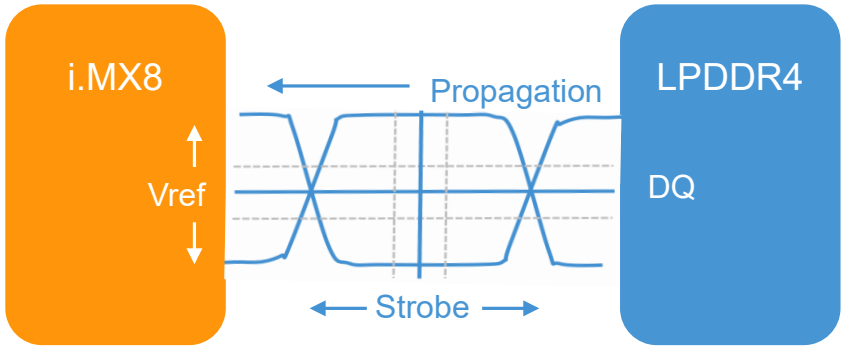


Write Eye: vTSA vs. pTSA

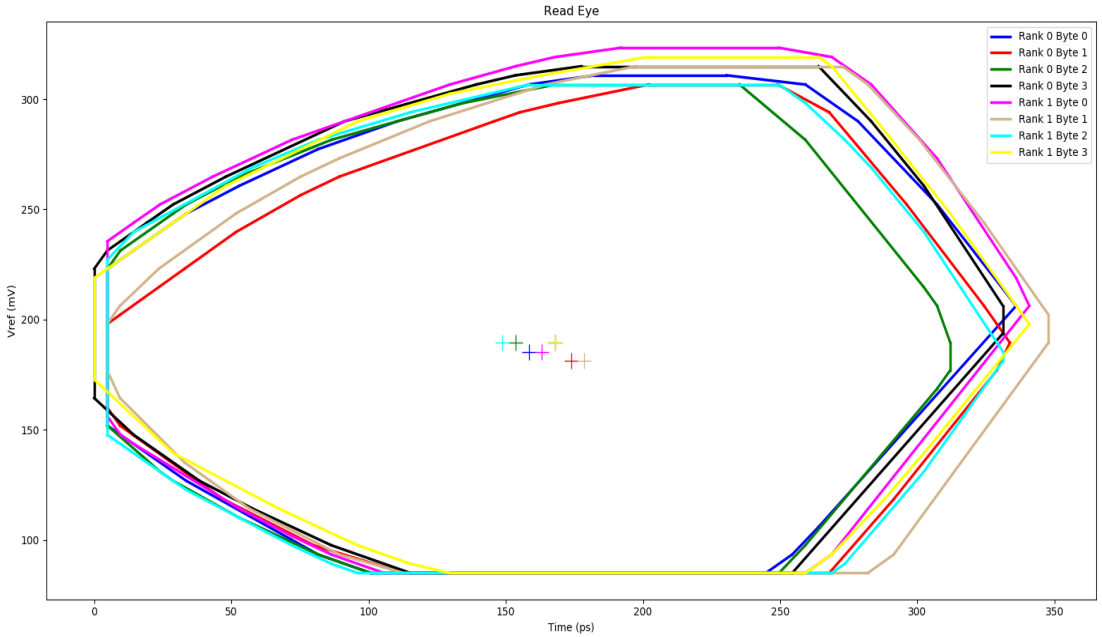


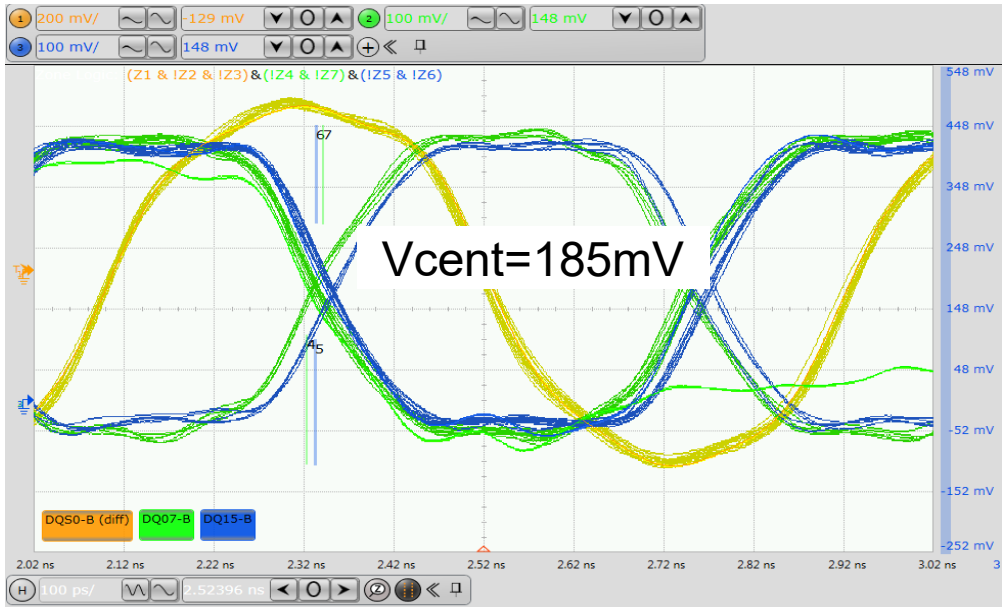
- Very good correlation seen between vTSA and pTSA in terms of write eye
  - pTSA provides more Vref range, but vTSA covers the area of interest
  - vTSA write eye data was obtained in a matter of minutes, pTSA took an entire day (for just two DQs!)

Read Eye: vTSA vs pTSA



- Read eye of the worst bit of each rank/byte can be shown through vTSA, just as in writes
- Proper pTSA measurement of read eye would be at the i.MX8, not at the output of the DRAM, so pTSA measurements of read eye are unreliable
- vTSA provides a way to characterize the read eye that is not available in a pTSA





Pros and Cons

Item	pTSA	vTSA
Equipment Required	High bandwidth scope/LA/probes Interposers/sockets	None
Accuracy	Affected by test hardware Usually measured at memory interface only	No test hardware needed Measurements at memory and SOC interface Software based
Statistical Significance	Sampled signals	Full interface
Comprehensiveness	Includes mode register settings, power supply, clock, etc. in addition to data eyes	Write/Read eyes Mode register setting output
Risk	Re-work may damage system	Low risk
Completion Time	Weeks	Days

Summary

- The vTSA approach enables accurate characterization of signaling margin of the entire memory interface very quickly and easily
  - Focus is on data eyes
  - Mode register setting output covers most of the LA work from pTSA
  - Unable to cover clock, power supply, and some timing parameters, so a hybrid approach is recommended for comprehensive coverage
- i.MX8 supports vTSA measurements, which has been demonstrated here to match pTSA results
- Come see us at our booth for a hands-on demo!