Automotive Ethernet PHY + Software

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FAE/Marketing In-Vehicle Networking

October 2018 | AMF-AUT-T3347

SECURE CONNECTIONS FOR A SMARTER WORLD

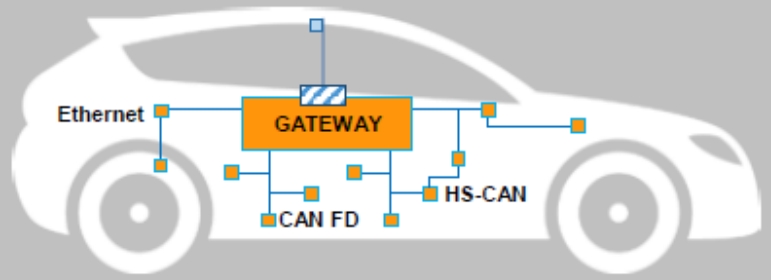
Agenda

- Automotive Networking Overview
- Introduction Automotive Ethernet / PHY
- Added Value Through PHY SW
- Software Availability
- Summary

Automotive Networking Overview

Bandwidth and Security Transforming Car Networks

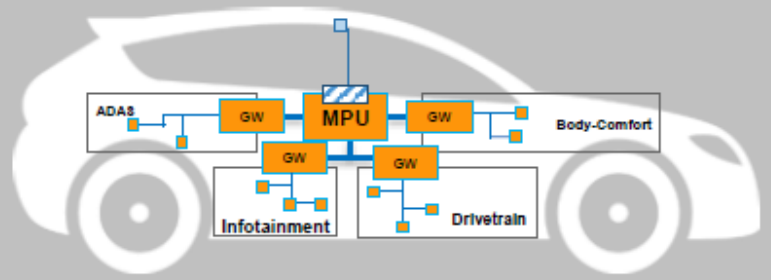
Today
Multi-Branch Network



Gateway as Hub

- Introducing layered security
- Ethernet for IVI and ADAS
- CAN FD for drivetrain
- CAN-LIN for body-comfort

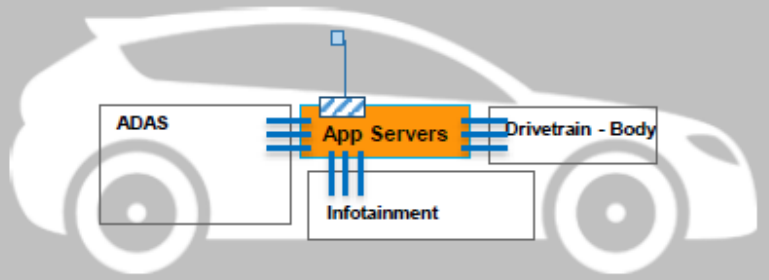
Tomorrow
Domain-Based Network



Hierarchy on Processing Duties

- Smart sensors / actuators
- Specialized domain controllers
- Central MPUs for Deep Learning
- AI-based autonomous vehicle

Tomorrow
Centralized Network

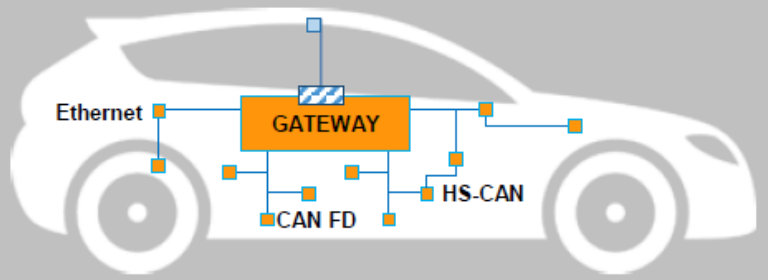


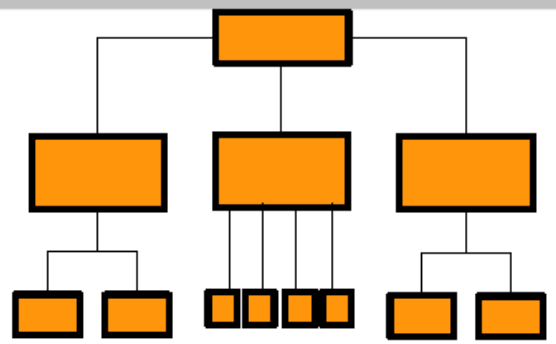
Highly Virtualized System

- Redundant central servers
- Unprocessed data highways
- Real-time cloud interaction
- AI-based autonomous vehicle

New Network Architecture Enable Autonomous Driving

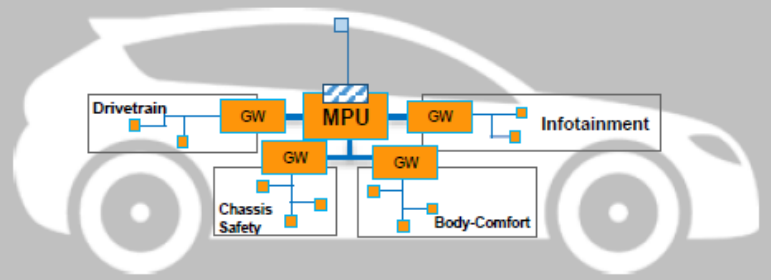
Today
Multi-Branch Network

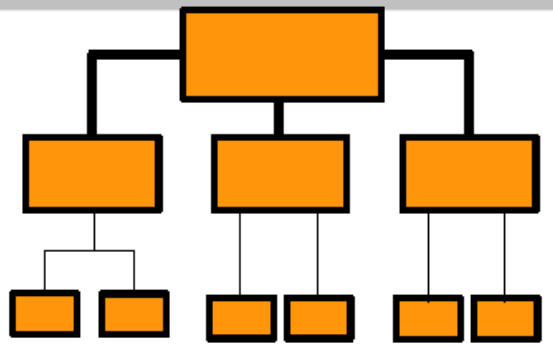




One Function per One Box
Post-processed Data on Bus

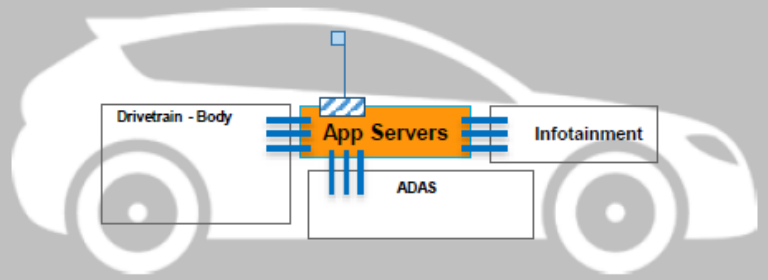
Tomorrow
Domain-Based Network

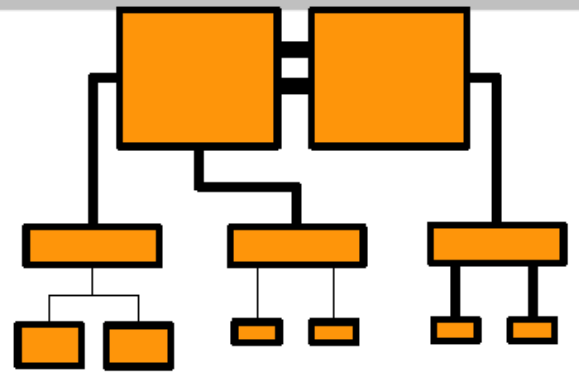




Few Functions in One Box
Un- or Pre-Processed Data

Tomorrow
Centralized Network





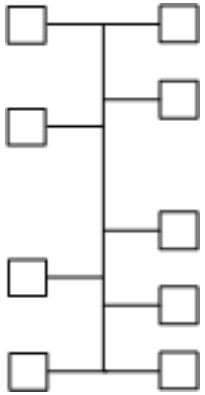
"Central Brains" replace ECUs
Un-Processed Data on Bus

Introduction Automotive Ethernet/PHY

In-Vehicle Network Topologies

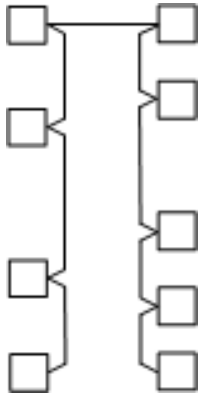
Ethernet is point-to-point, not a bus

CAN



Linear bus

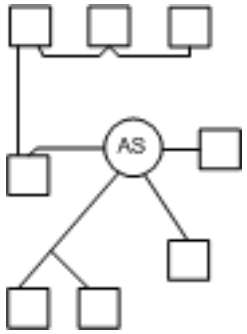
Low cost solution but
less scalable and safe



Daisy chain

Lowest cost but
difficult to implement

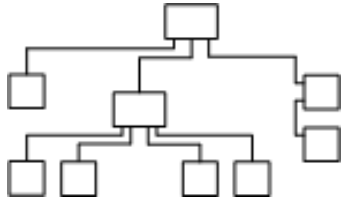
FlexRay



Star architecture

most flexible and
scalable topology,
advantages in terms of
EMC and safety

Ethernet



Tree architecture

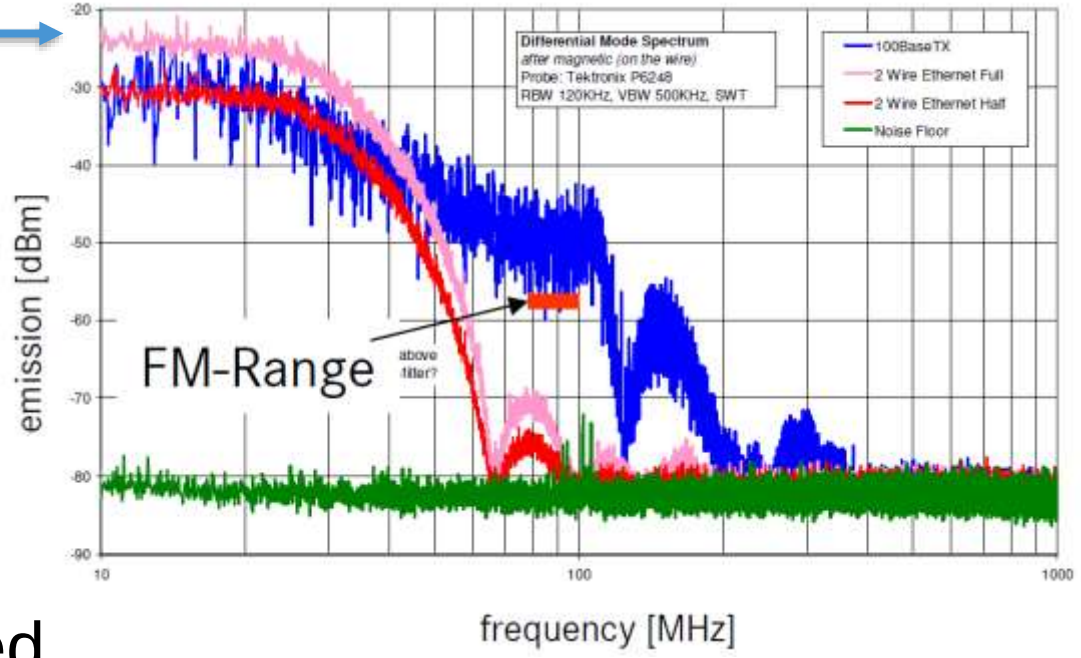
point to point
communication,
multiple switches
needed,
easy scalable

Driving Factors for Adoption of Ethernet

- Vehicle complexity and features
  - ADAS, Collision avoidance, Radar, Vision
  - Camera's, surround view
  - OTA, Module re-flash
  - V2V, Autonomous operation
- CAN & CAN FD not enough
  (Bandwidth!)

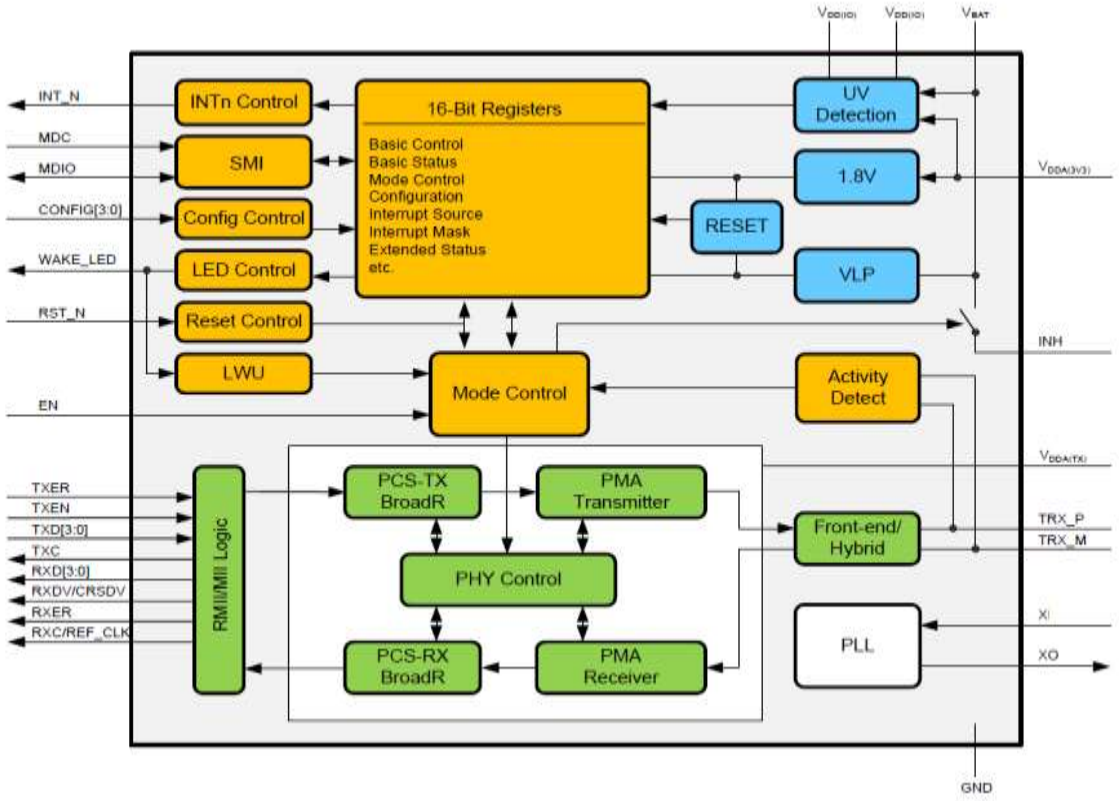
Requirements for Adoption

- Existing 100BTx solution not well suited for Automotive applications
  - Did not meet OEM EMC requirements
  - Required shielded cable, 4 wires for Tx/Rx
  - Costly implementation, magnetics
  - Still used for diagnostic service bay interface



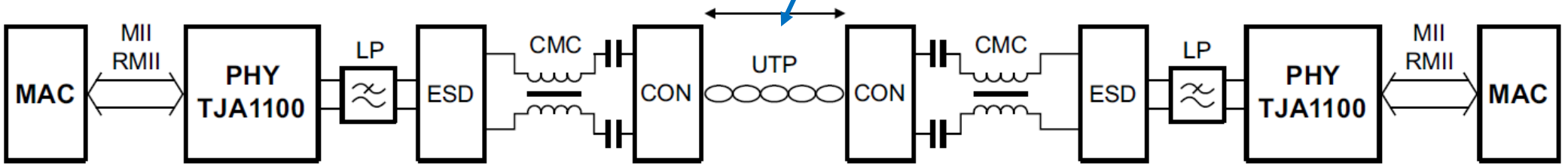
- Automotive standardized interface required
  - BroadR-Reach → OPEN Alliance → IEEE 802.3bw-2015 100BASE-T1
    → IEEE 802.3bp- 2016 1000BASE-T1
  - AEC-Q100, Automotive EMC,ESD
  - Support for Automotive low power modes

Implementing Ethernet PHY (TJA1100)



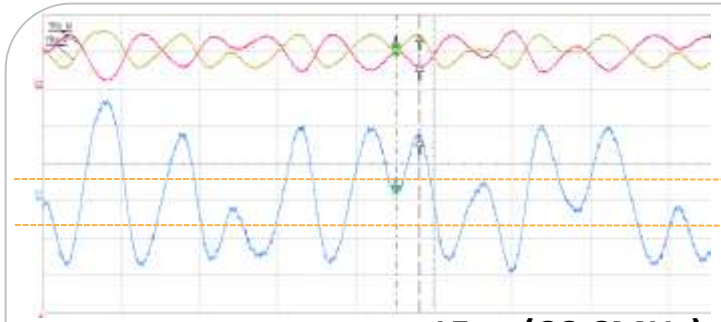
- MAC MII / RMII required
- Up to 15m link segment
- UTP reduced cable cost compared to 100BTx
- 100Ω Characteristic impedance
- Switch required for multiple nodes
- Operate with or without software intervention

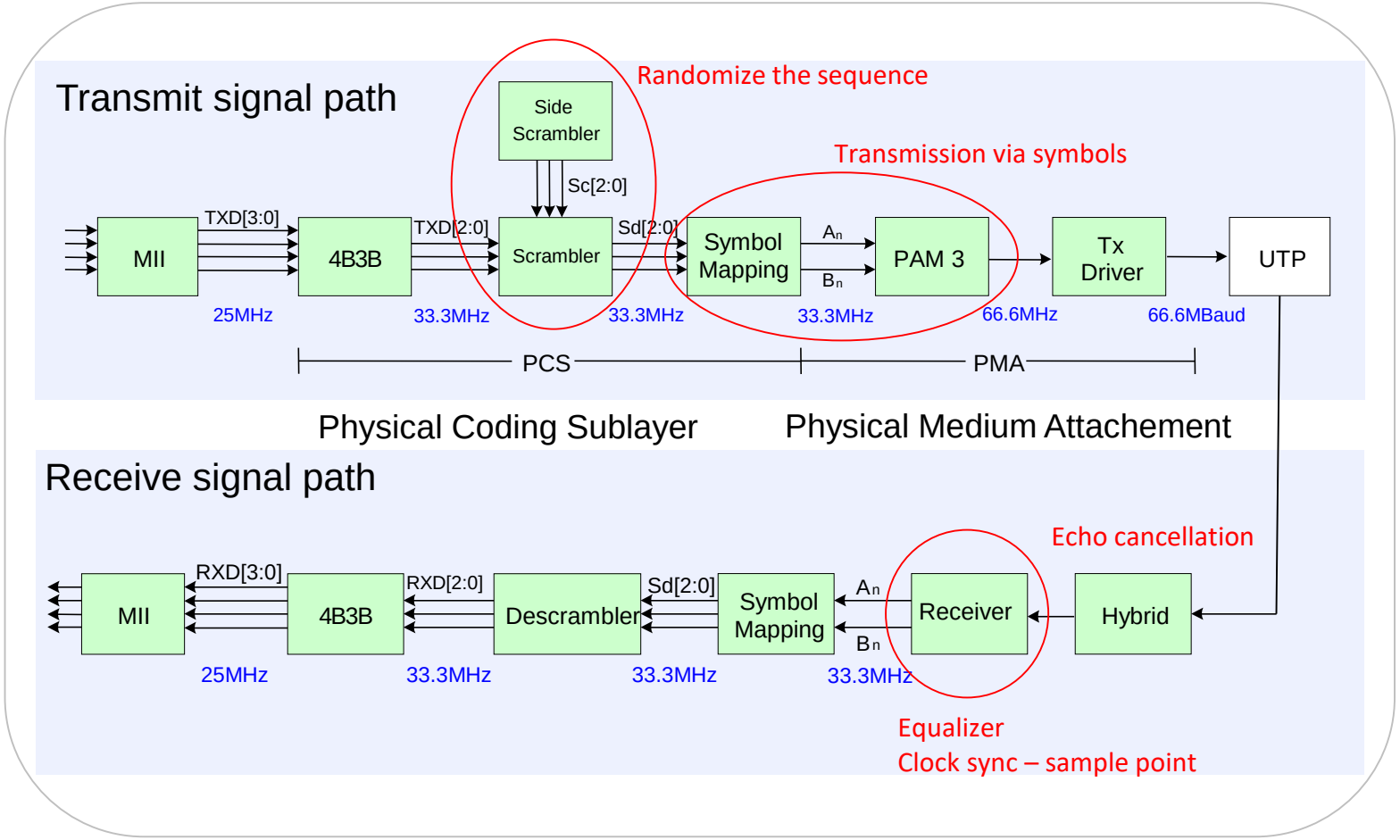
15m(Max) UTP
100Ω
4 interconnects Max



PHY Basics

- Bi-directional communication
- Symbol transmission (PAM-3)
  - Baud rate 66.6MHz
  - Data rate 100Mbps
- Permanent transmission
  - Link startup
  - Active transmission in idle
  - Synchronized link partner
- Scrambled data stream

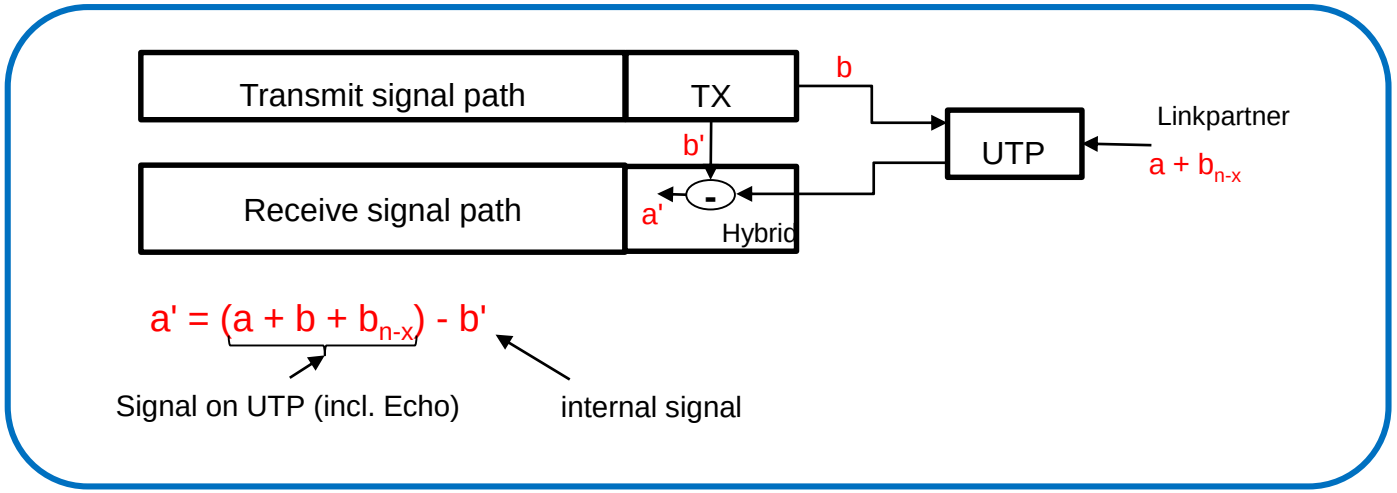


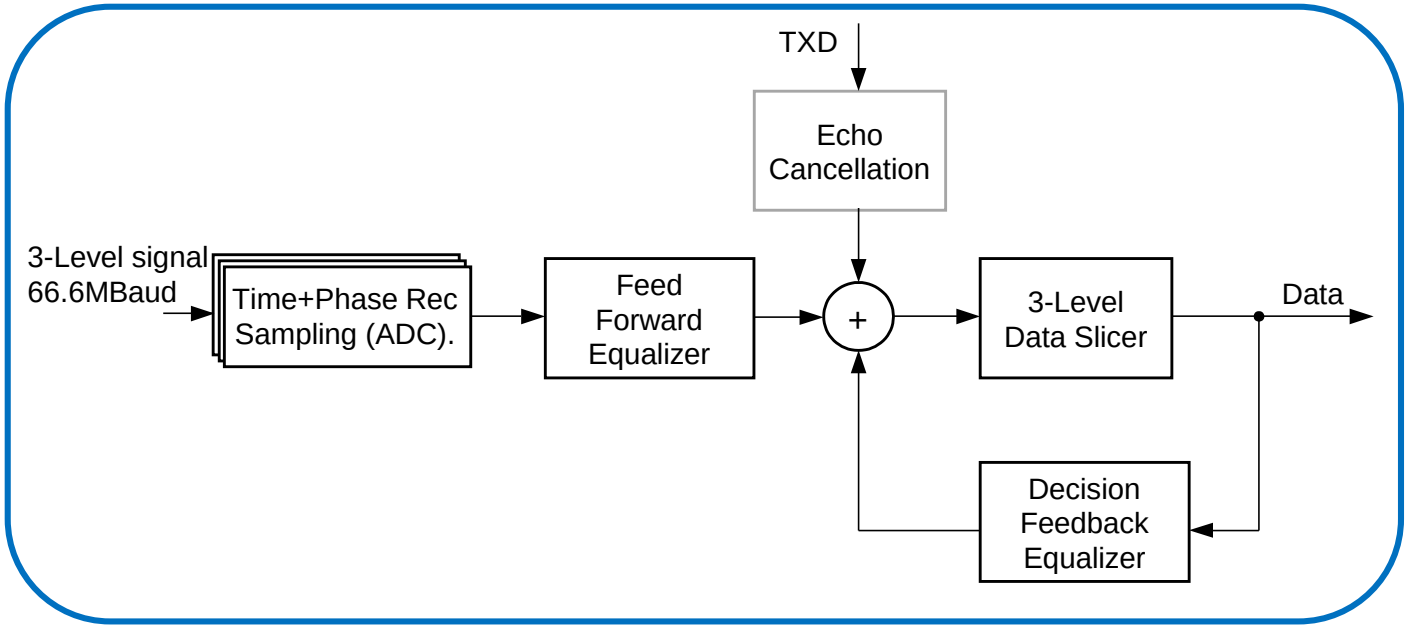


PHY Basics

Receiver

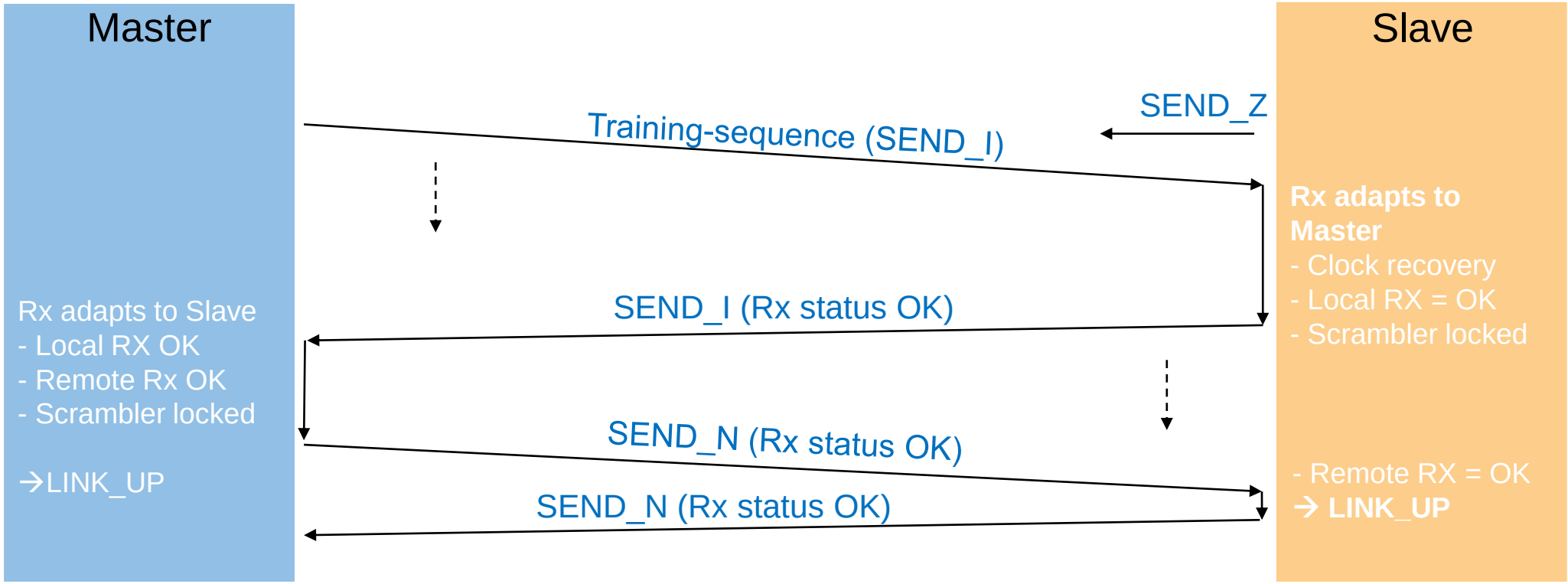
- Time + Phase recovery
- Level recovery „Slicer“
- Equalizer
- Echo canceller
- Adaptive filter loops
- needs channel within specification
- gives feedback about the channel





PHY Basics

Link startup (simplified)



- Master/Slave has only relevance for Startup and Clocking
- Faster than Autonegotiation, Link control to valid data in < 200mS
- Full duplex communication when link is established

NXP Ethernet Portfolio: The Auto-Native Portfolio

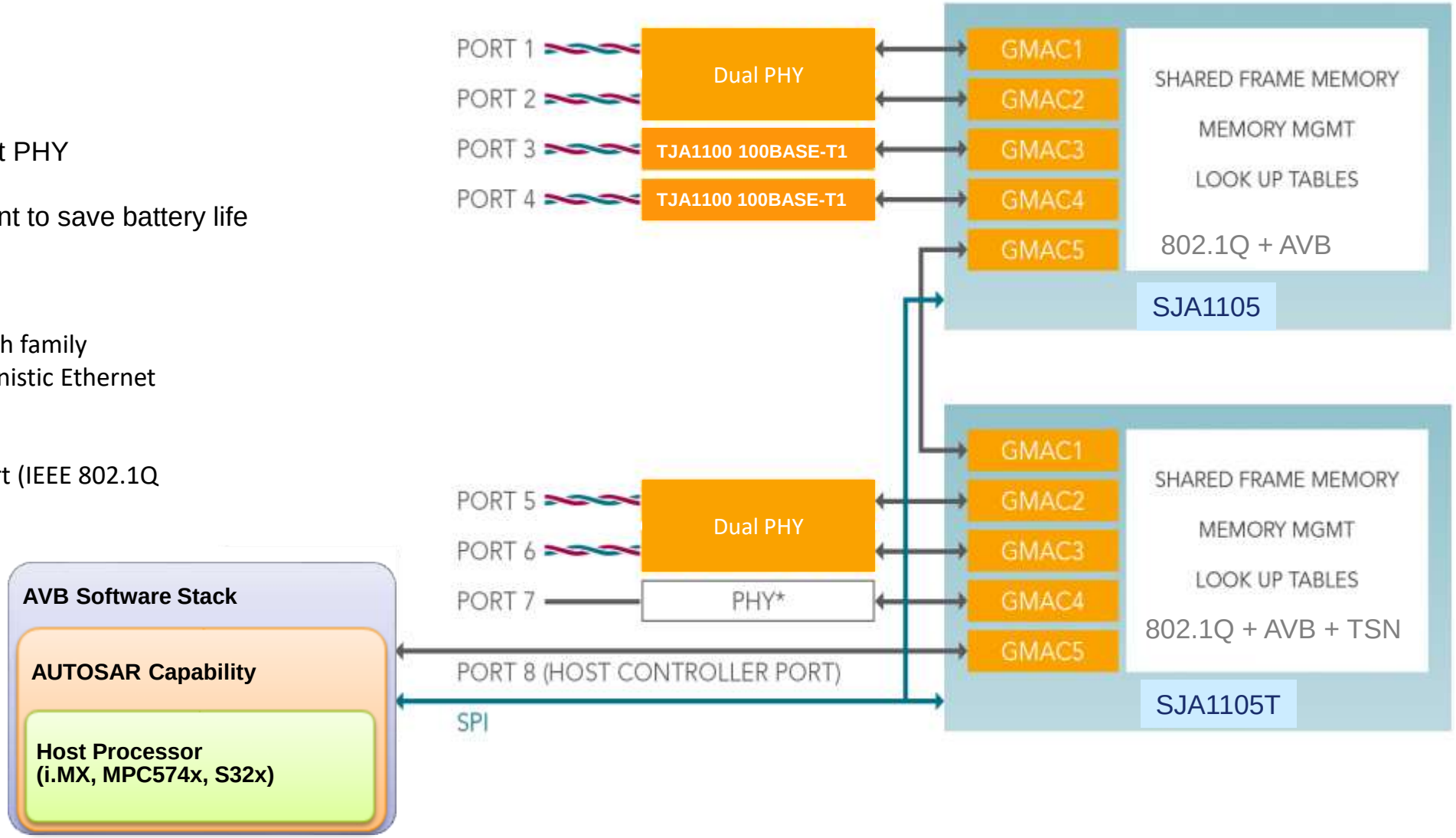
Flexible, Scalable Solution

TJA1100

- IEEE 100BASE-T1 Compliant PHY
- Fully automotive qualified
- Enhanced Power Management to save battery life

SJA1105(T)

- Layer 2 Store and Forward Switch family
- Supports AVB, TSN and Deterministic Ethernet
- 10/100/1000 Mbps interfaces
- MII/RMII/RGMII Interface
- Port Mirroring and VLAN support (IEEE 802.1Q and IEEE 802.1P)



Added Value Through PHY SW

Motivation

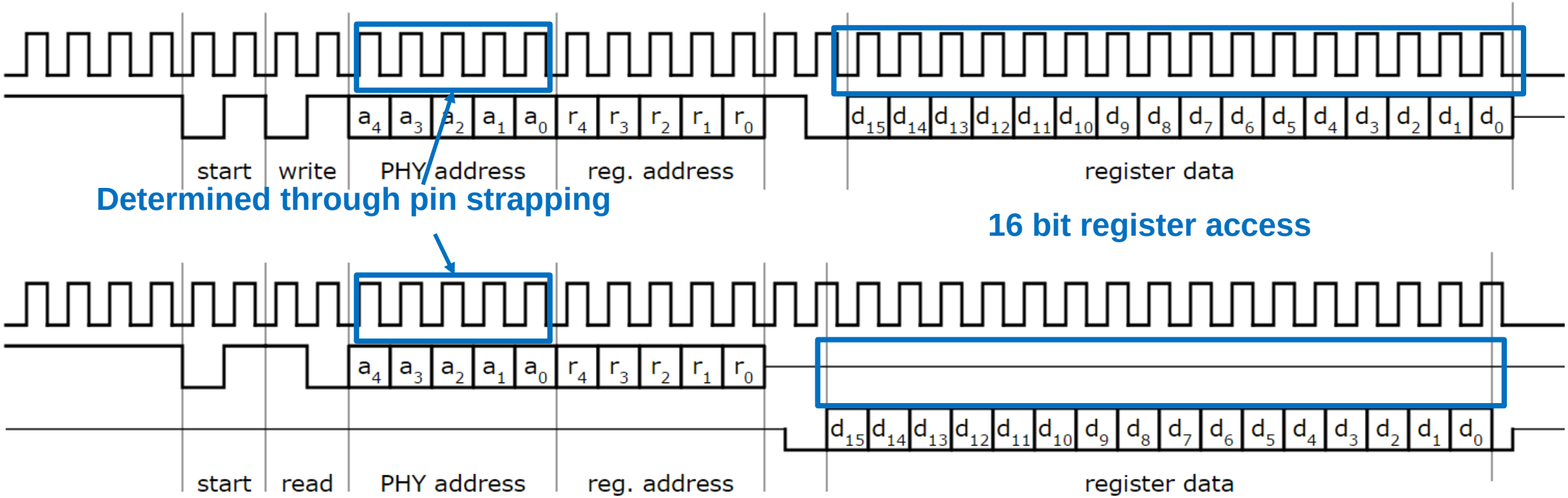
- An Ethernet PHY is functional without any software, so why bother?

- Tasks related to network management, diagnosis, fault handling require SW involvement
- Added value can be generated through e.g.:
  - Reduced wiring cost by leveraging advanced network management like wake/sleep
  - Fault prevention/aging detection through SNR, symbol errors, cable test
  - Enablement of ASIL x functional safety designs
  - Detection of tampering for enhanced security, e.g. for PNAC (Port-based Network Access Control)

How to configure/control TJA1100

- Reset and enable pin, wake-up pin, interrupt pin
- Pin strapping (Resistor strapping)
  - Master/Slave + enable/disable of PHY
  - Autonomous mode/managed mode
  - PHY Address (used for MDIO access)
  - …
- Register read/write through MDIO bus
  - Status information
  - Link control, loopback modes, test modes
  - Sleep/wake

Management Data Input/Output (MDIO)
Serial Management Interface (SMI)

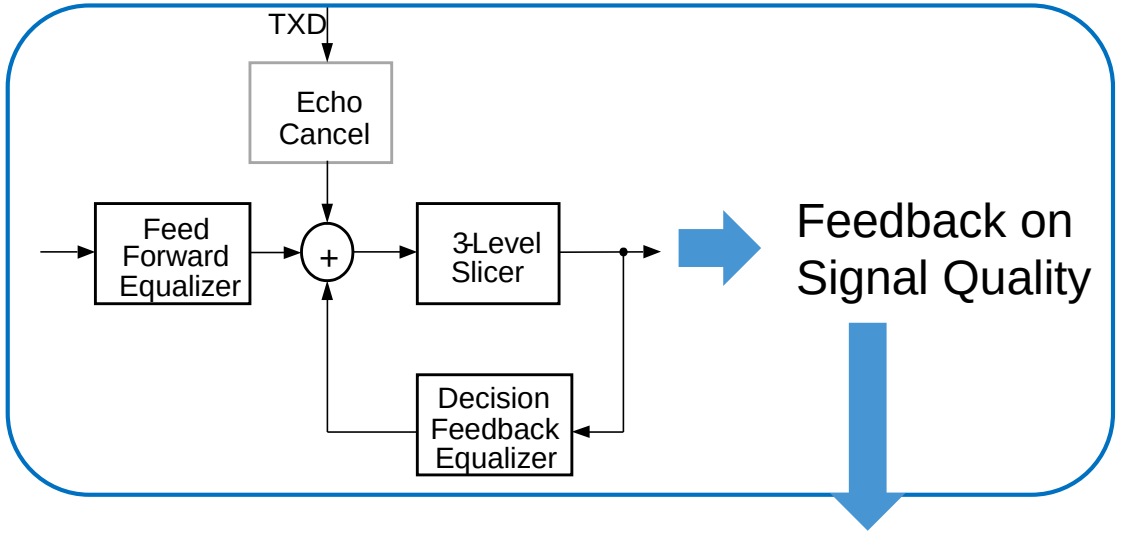


- 2 wire bus
- 32 PHY's Max
- 2.5MHz CLK Freq

PHY Diagnostics SMI

- Permanent
- Link up information
  - Scrambler/Clock sync/PLL… feedback
  - Receiver status (local and remote)
- Feedback from Equalizer – Signal Quality + Warning when limits are exceeded
- Symbol error detection
- Under-Voltage and Over-Temperature status
- On Request
- e.g. during start-up or if link failure detected
- Cable diagnostics: Open/Short detection
  - e.g. during start-up or if link failure detected
- Loop back modes – to check integrity along data flow
  - Internal, external, remote (see next slides)

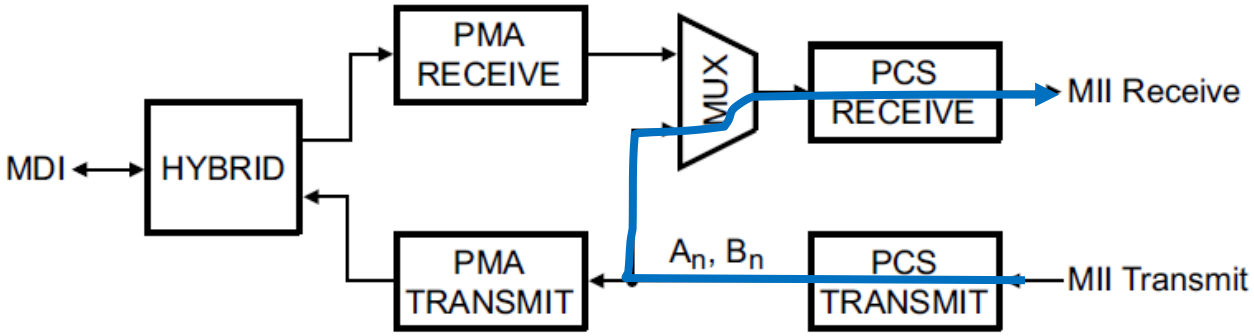
- Usage of additional PHY feedback for channel quality under discussion with OEMs



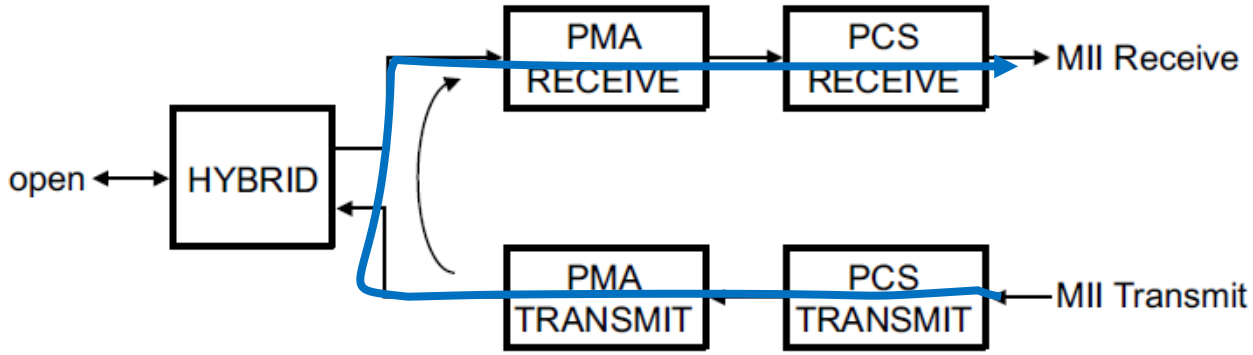
000 worse than class A (unstable link)
001 class A (unstable link)
010 class B (unstable link)
011 class C (unstable link)
100 class D (poor link; potential bit error)
101 class E (good link)
110 class F (very good link)
111 class G (very good link)

Loopback Modes (1)

Internal Loopback



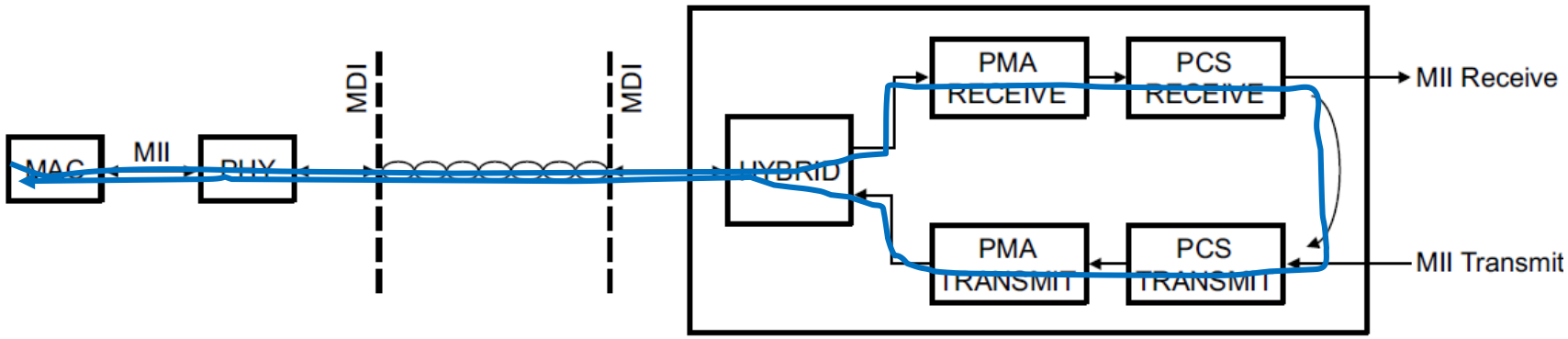
External Loopback



- Both will loop back traffic to the host connected over MII
- No physical medium needs to be attached
- Can be used for diagnosis of PHY and for (software) testing

Loopback Modes (2)

Remote Loopback



- Complete diagnosis of PHY and cable
- Requires a second PHY to be connected via a cable

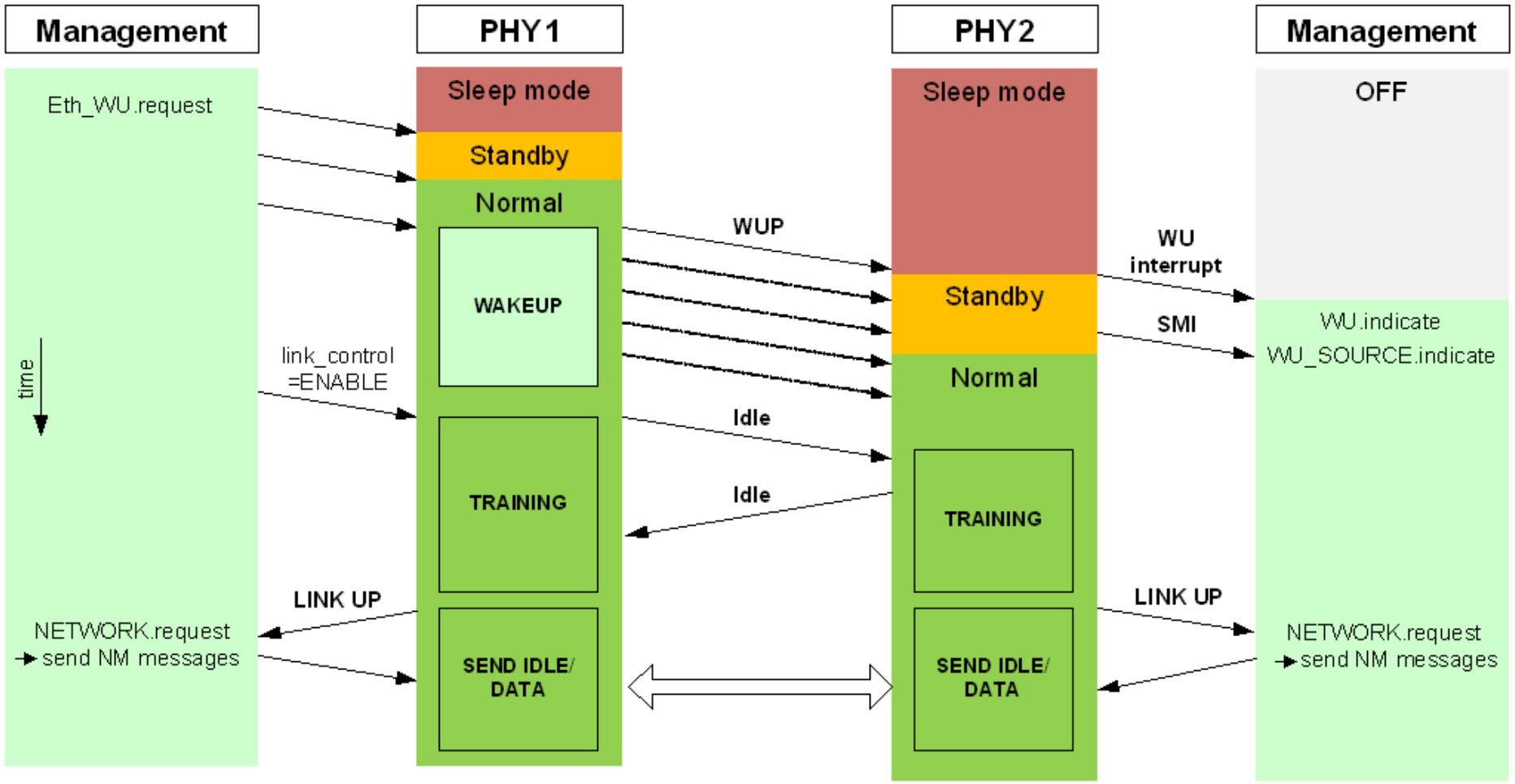
- Multiple loopback modes can be combined to locate the source of a failure

Sleep/Wake-Up: Objectives

- Enables partial networking
- No dedicated wake-up line needed
- Node/cluster wakeup within less than 200 ms
  - No microcontroller involvement in forwarding wake requests
- Sleep current consumption per port less than 10 µA
  - PHYs are directly powered through battery supply V_BAT

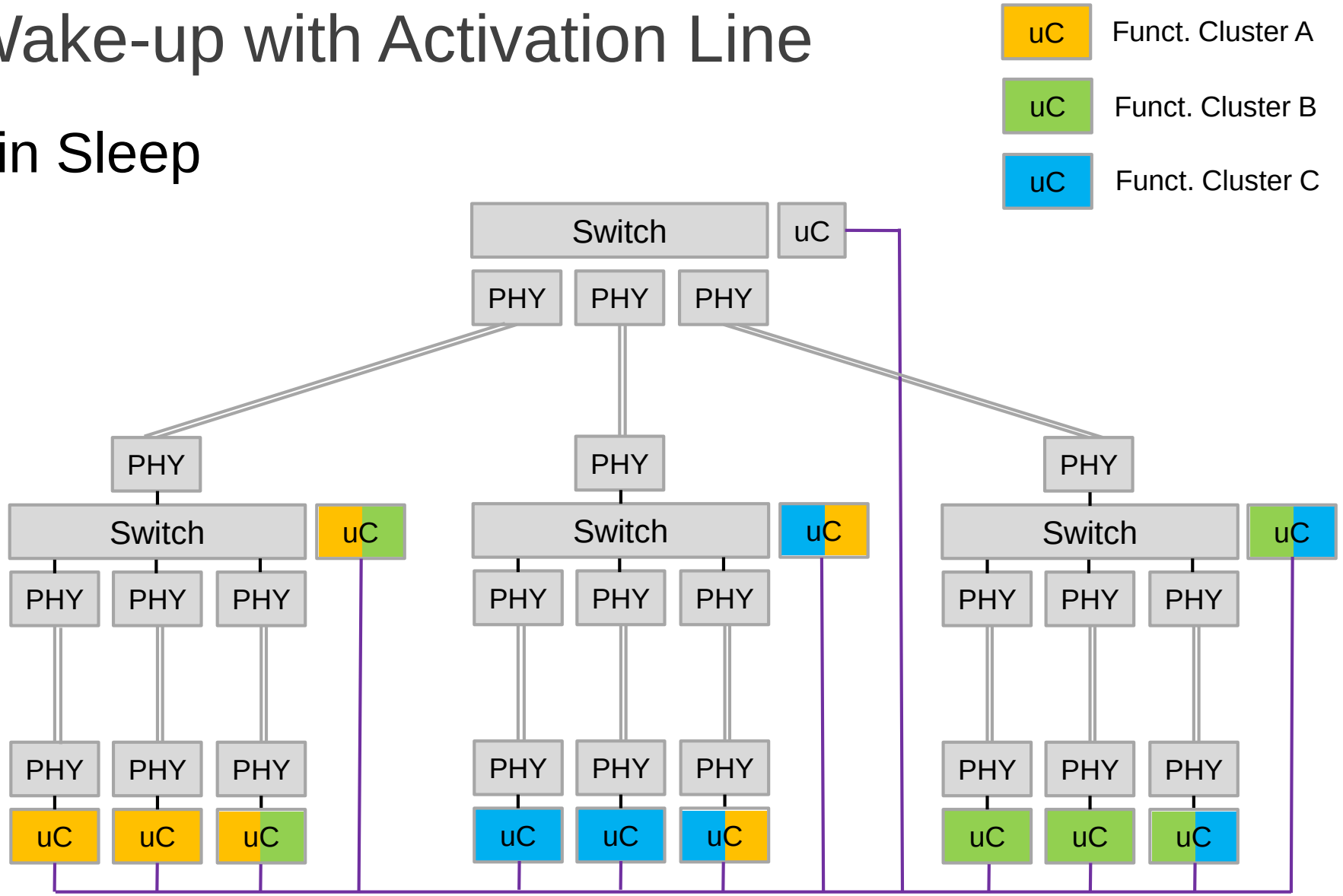
- Standardized in Open Alliance TC10, moving to ISO standard

Sleep/Wake States



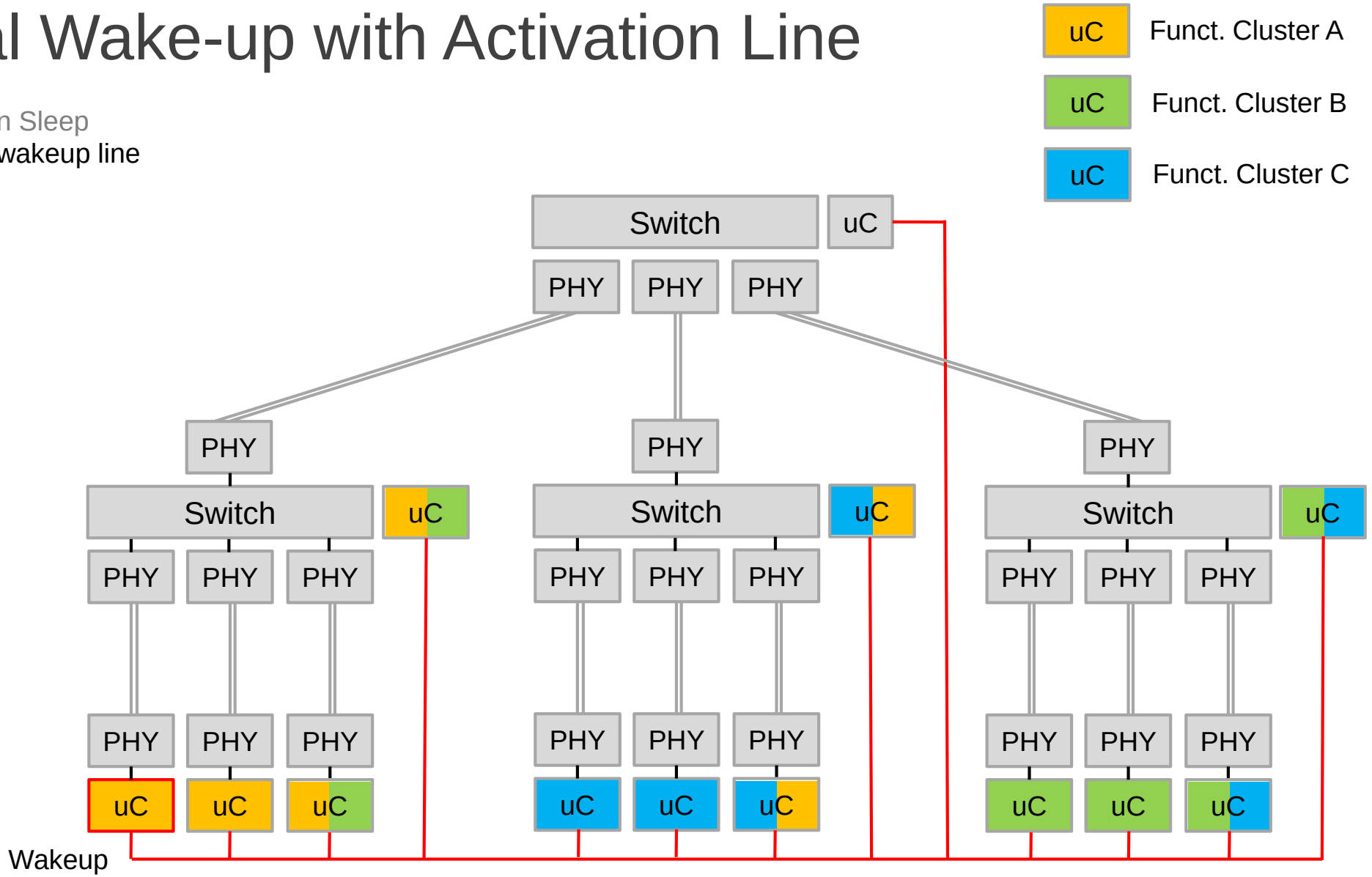
Global Wake-up with Activation Line

- System in Sleep



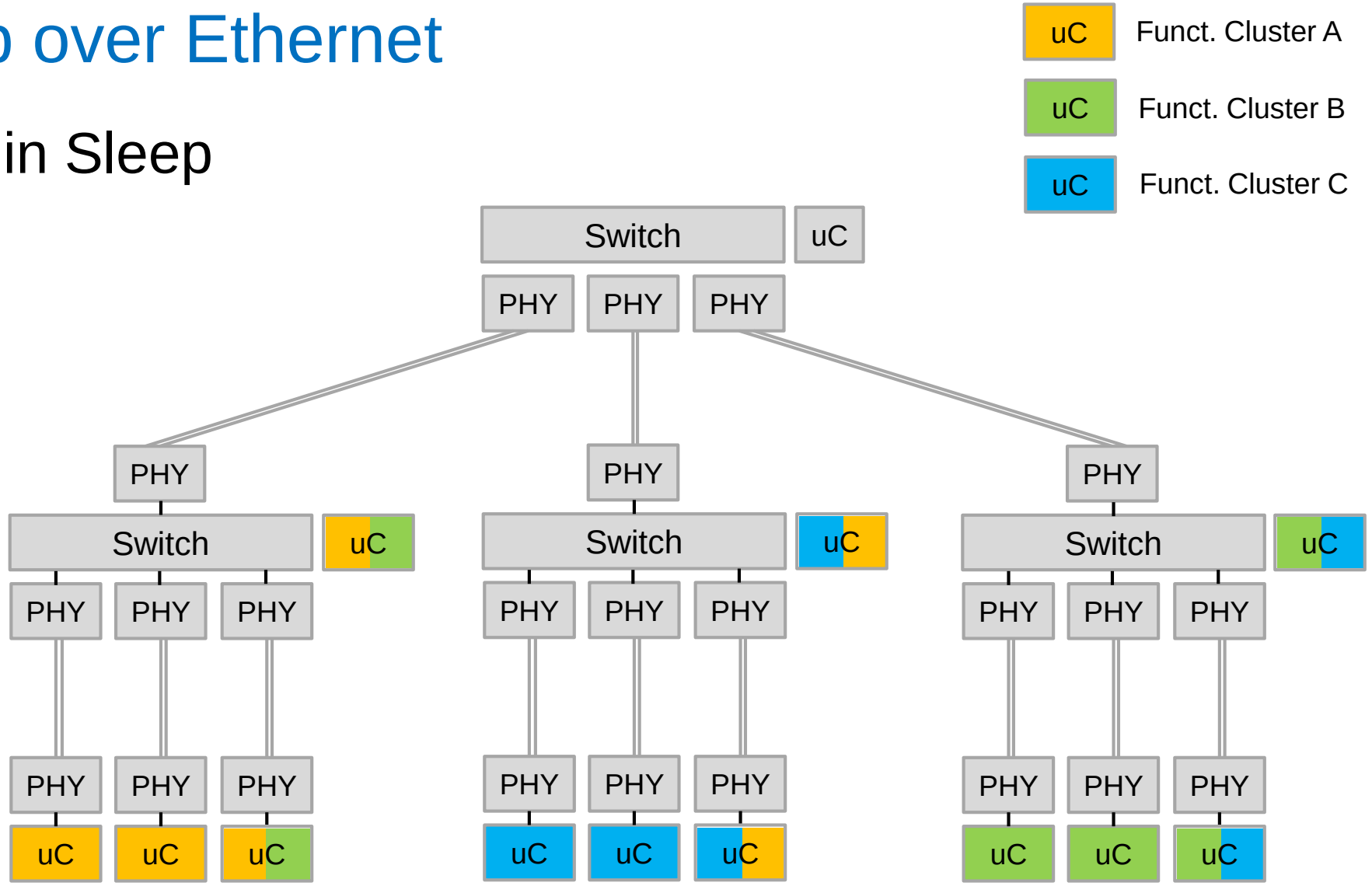
Global Wake-up with Activation Line

1. System in Sleep
2. Activate wakeup line



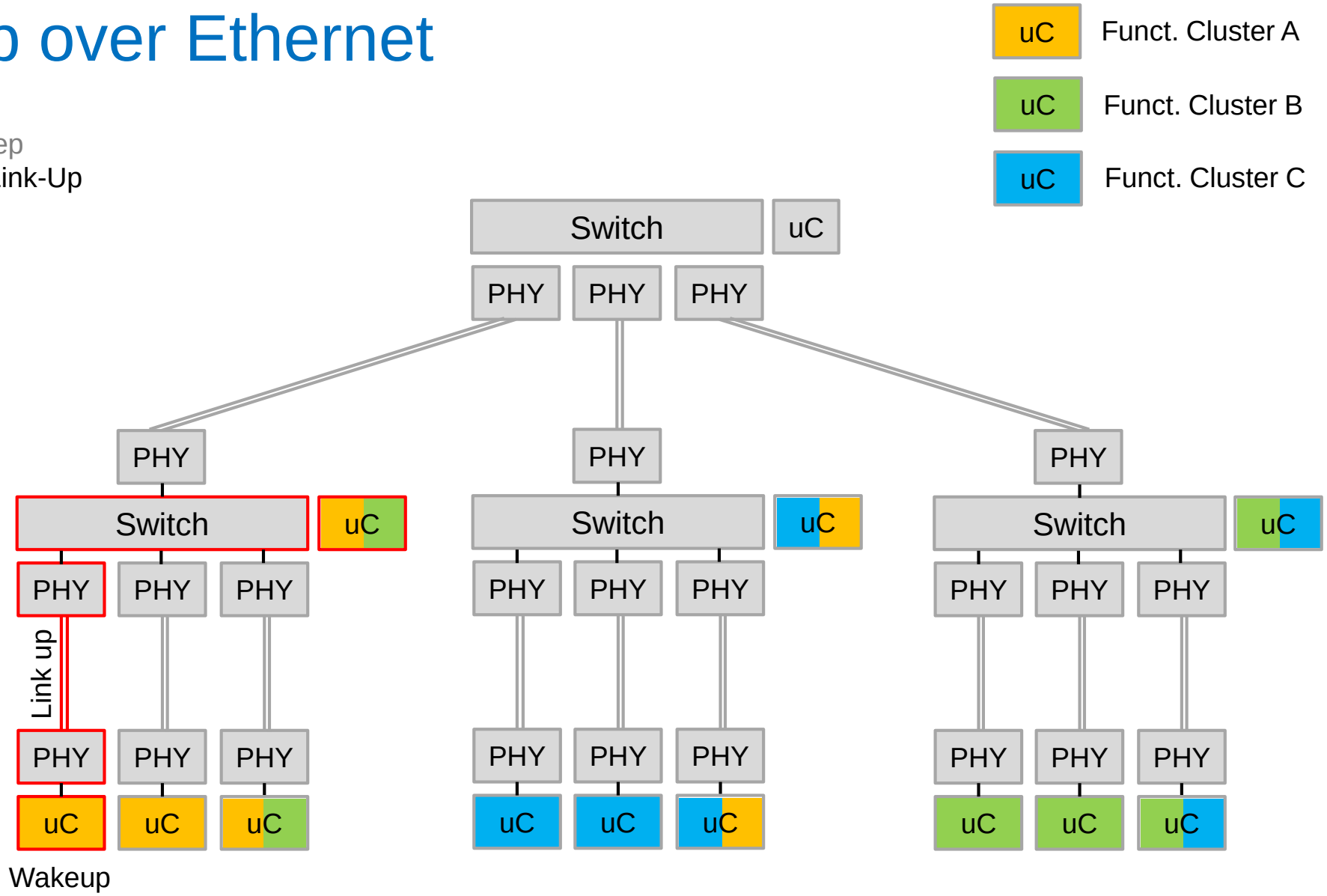
Wake-up over Ethernet

- System in Sleep



Wake-up over Ethernet

1. System in Sleep
2. Wakeup and Link-Up



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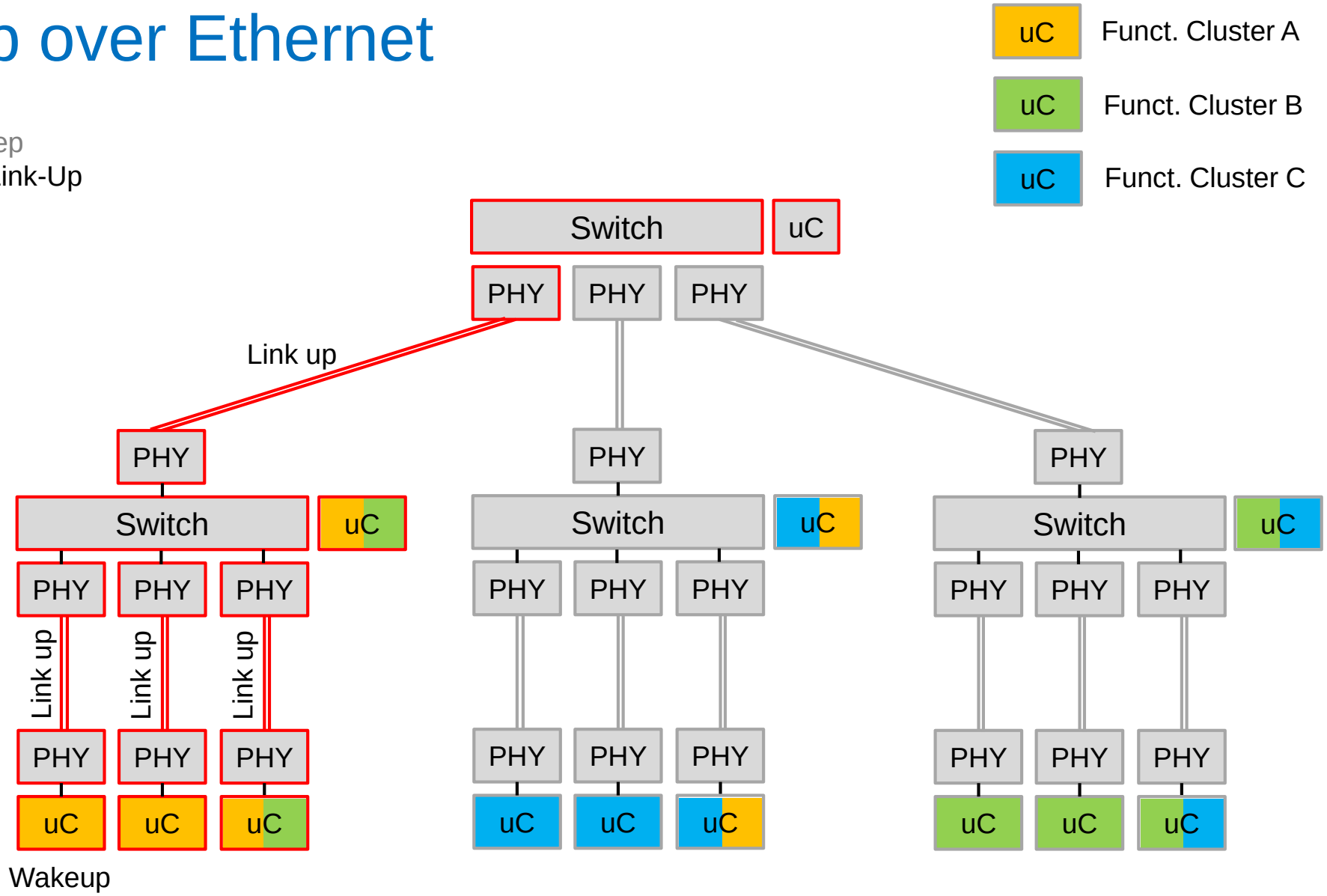

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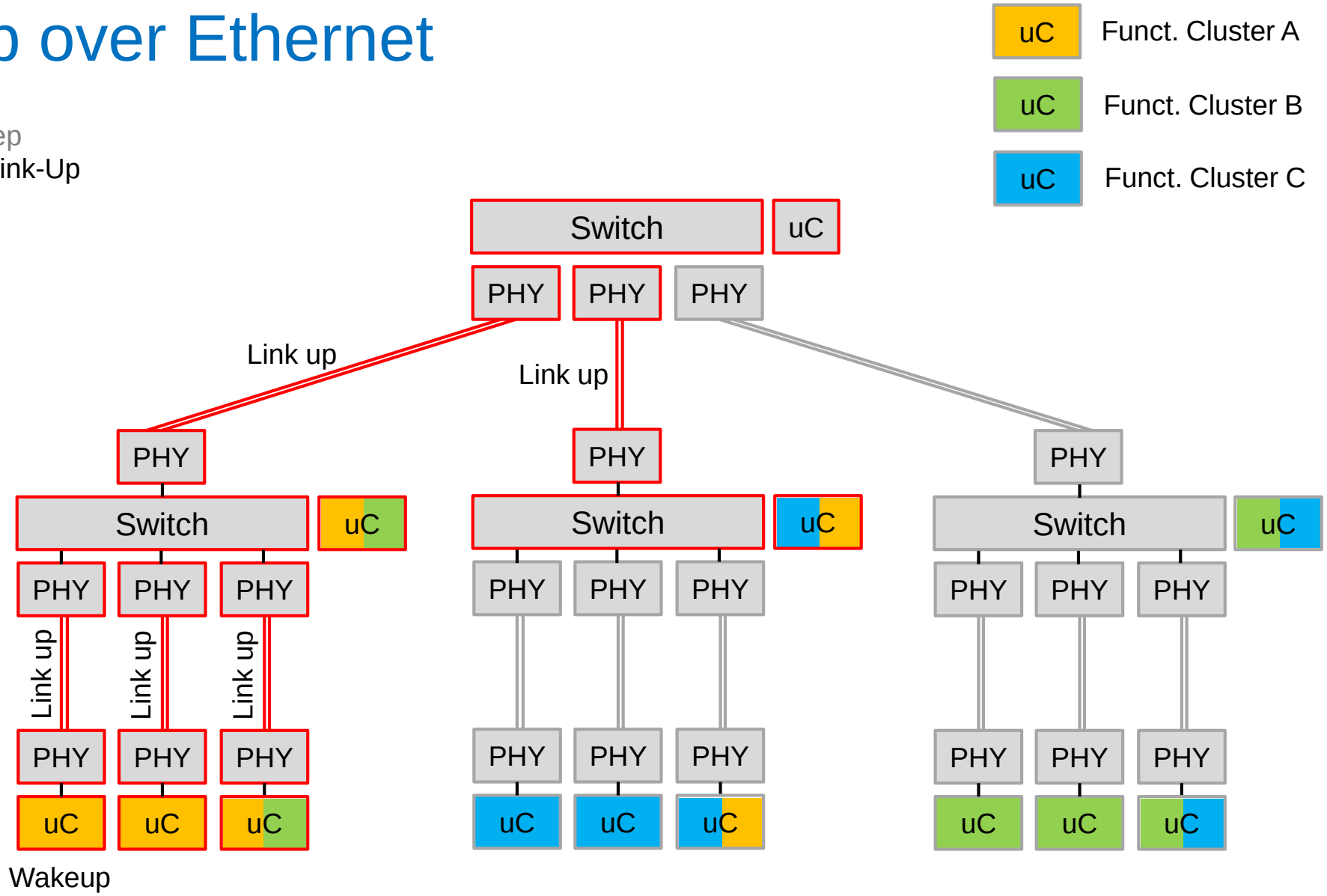

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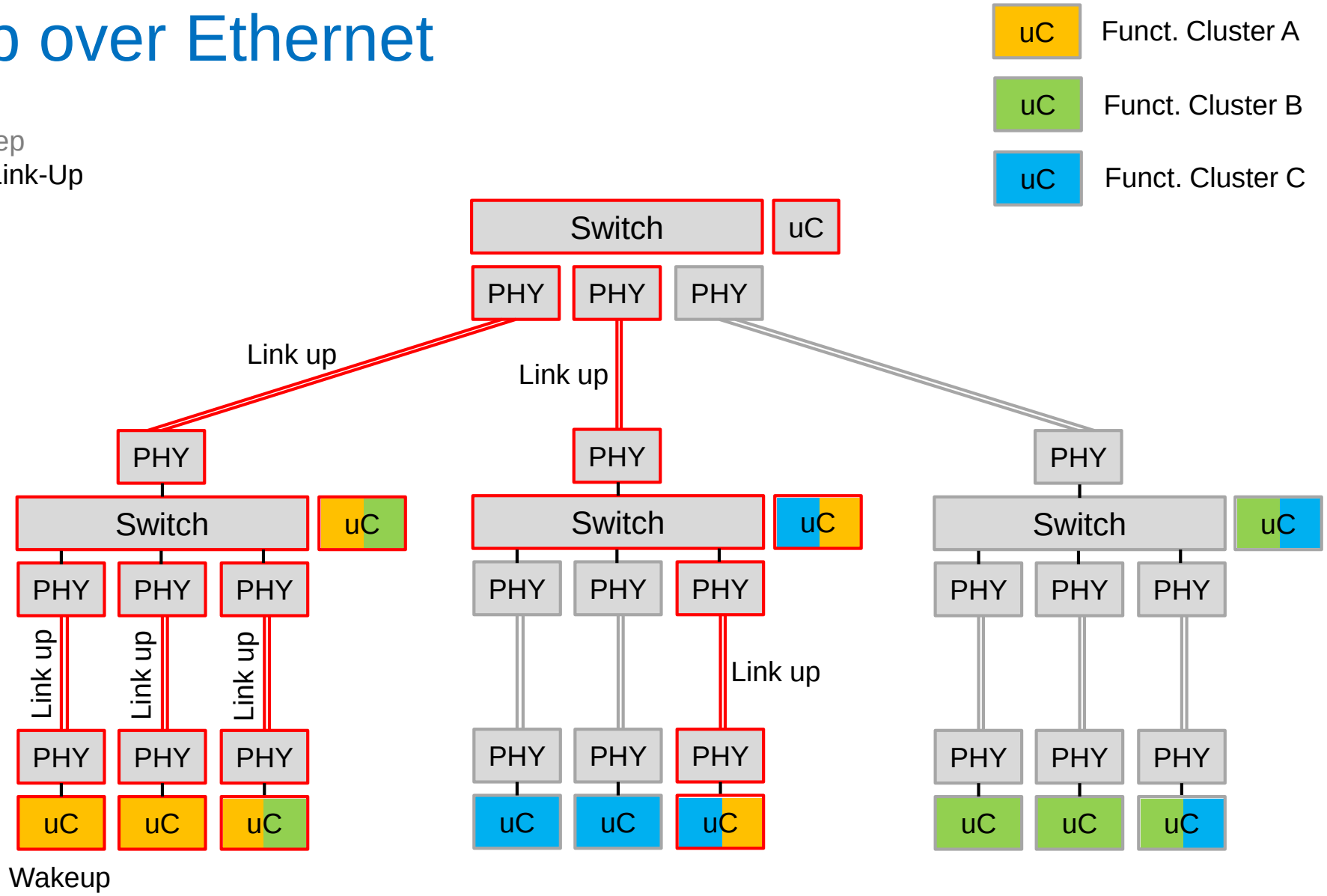
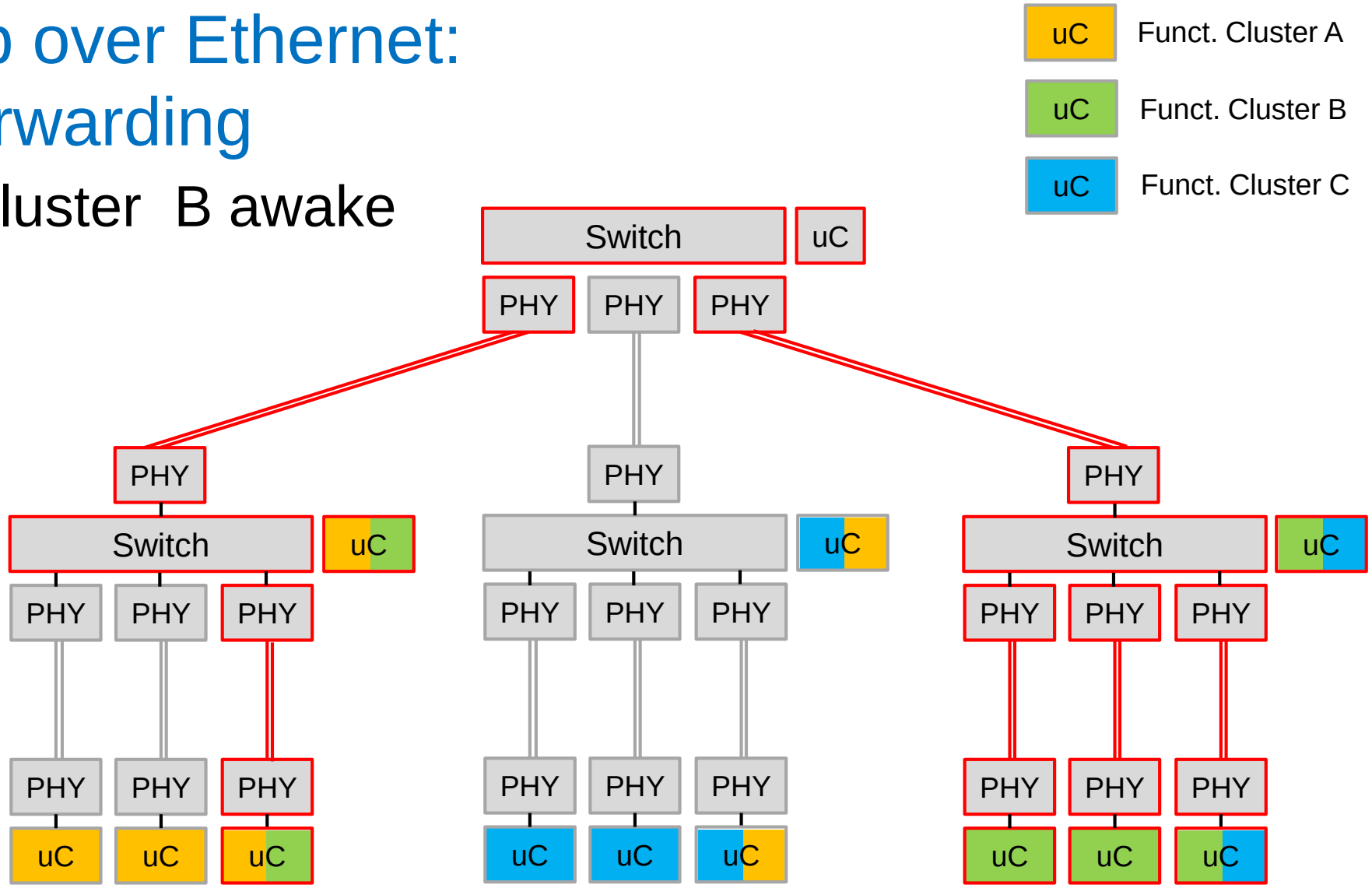
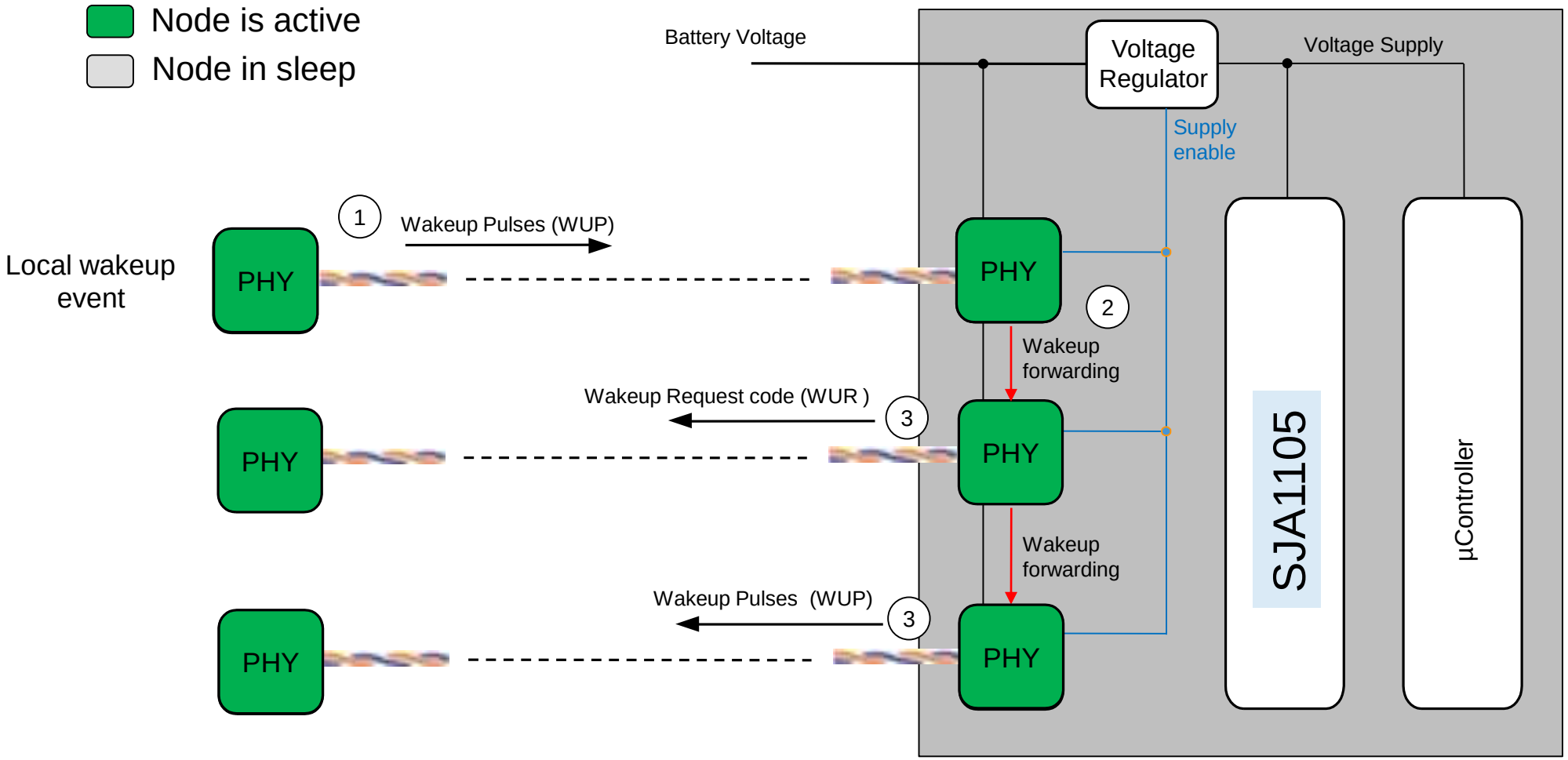


Wake-up over Ethernet: Wake forwarding

- Funct. Cluster B awake



Wake-up Forwarding - Example Implementation



Software Availability

NXP Original Software

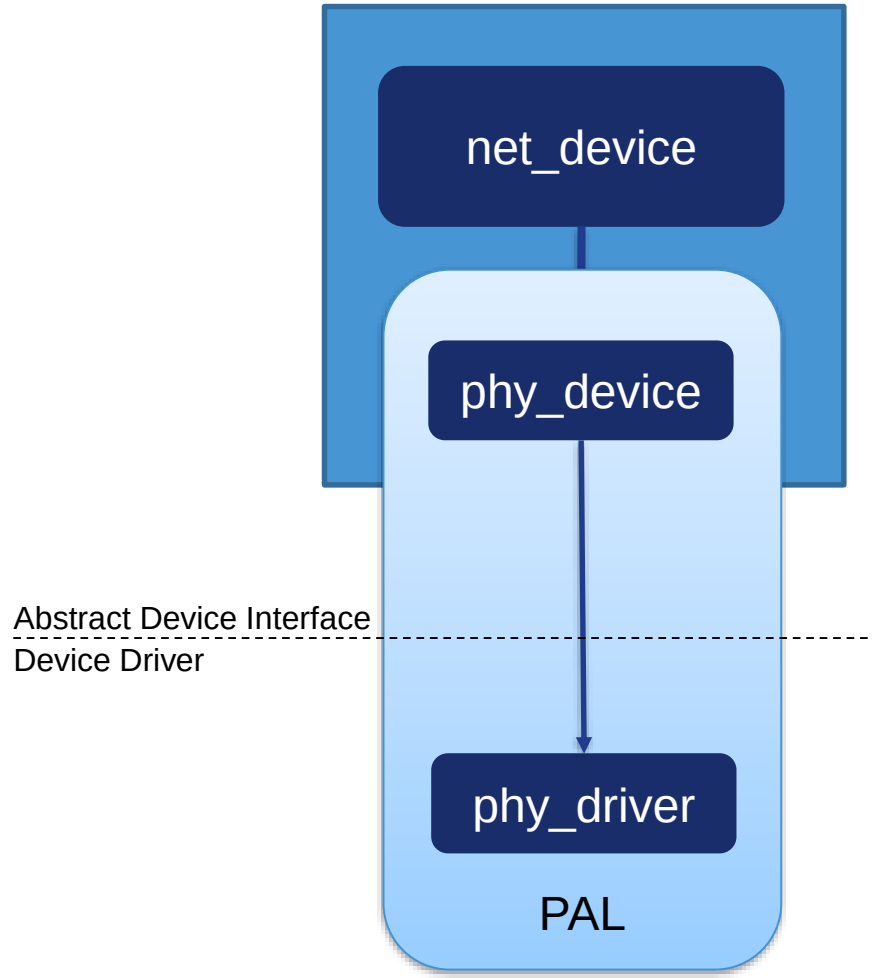
- Free Software is provided without warranty, “as is”
- Optional Licensed AUTOSAR drivers and AVB SW stack

	Low-Level Drivers	Linux Drivers	AUTOSAR Drivers	AVB Software
TJA1100	Available	Available	Via Vector	n.a.
TJA1101	Available	Available	Available	n.a.
TJA1102/ TJA1102S	Available	Available	Available	n.a.
SJA1105/ SJA1105T	Available	Available	Via Vector	Available
SJA1105P/Q/R/S	Available	Planned	In development	Planned
Comments	Free	Free	Licensed	Licensed

TJA110X Linux PHY Driver

- Single Linux driver for TJA1100 and TJA1102
- Integrates into Linux' PHY Abstraction Layer (PAL)
- Extended with automotive features
  - Support for Managed and Autonomous Mode
  - Master/Slave configuration
  - Cable Test
  - LED, Loopback and Test Modes
  - Sleep and Wakeup
- Implements polling of interrupt status register
  - Warning about and reaction to failure conditions

Download: http://bit.ly/2IrIZxz



Summary

Summary

- Car content connectivity is driving adoption
- PHY Software is not needed for Ethernet communication
- PHY Software can improve network intelligence, diagnosis/monitoring, safety, security
- Standardized frameworks exist for
  - Linux (phydev)
  - AUTOSAR (EthTrcv)
  - …

  With varying levels of automotive feature depth

IEEE 802.3 Automotive Ethernet PHY Standards Handout

	10 Mbit/s	100 Mbit/s	1000 Mbit/s	2500 Mbit/s	10 Gbit/s	Next
MAC Interface Digital/ SERDES	SNI, xMII/ SGMII OC-SGMII	xMII/ SGMII OC-SGMII	xGMII/ SGMII OC-SGMII 1000BASE-X	OC-SGMII 2500BASE-X	USXGMII XFI	?
Media Interface Single Twisted Pair	802.3cg 10BASE-T1S 15 m Point to Point 25 m Multi-Drop 10BASE-T1L 1000 m Point to Point	802.3bw-2015 100BASE-T1 15 m Point to Point	802.3bp-2016 1000BASE-T1 15 m Point to Point	802.3ch 2500BASE-T1 15 m Point to Point	802.3ch 10GBASE-T1 15 m Point to Point	?

Media Interface (PHY) Standards without an appended year are not completed yet.

Updated 6-2018

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