Effective Printed Circuit Board Design: Techniques to Improve Performance

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NXP | SECURE CONNECTIONS FOR A SMARTER WORLD

News Flash!

- We all are involved with developing products which generate, control and consume electromagnetic field energy.
- This is what we are taught:
  - Circuit theory pretends that electric energy is made up of electrons moving in the conductors.
  - Switches add conductors, and the current instantly starts to move in the loop.
  - The wires carry the energy, and the load instantly affects the flow of energy.

- Wrong!
  - Switches add new **spaces**, and the moving field carries the energy.
  - It takes time for the field energy to move into that **space**.
    - The moving field energy has no idea of what it is at the end of the new **space**.
  - Field energy moving through a **space** induces current flow in the conductors.
    - The magic here is the displacement current flowing through the dielectric at the wave front, completing the circuit.

Because You Know…

- It’s All About the Space!
  (not wires)

In Case You Already Forgot…

“All About the Space“ To the tune of Meghan Trainor’s “All about that Bass”.   http://youtu.be/WglPHiZx4Gw

Because you know it’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**... **space**... **space**... **space**

Yeah, it's pretty clear, you don’t believe it
But the wires just show, just show, where all the fields will fit
‘Cause all the energy only moves in the **space**
“Gotta put all the wires in all the right places”

I know your teacher said, it’s the conductor
We know that’s not the way, don’t listen to, the instructor
If you got fields a movin’, you got current flow
‘Cause it’s the movin’ fields that really make everything go

Yeah, your teachers they told you "don't worry about the field”
They said, “The math that they use isn’t something you wish to wield”.
You know that circuits are better, you just have to make them connect
So if that’s what you’re into, then you know what to expect

Because you know it’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**...Hey!

I'm bringing physics back
Go 'head and tell them circuit fossils that
No, I'm just saying, I know you think they're right
But I'm here to tell you...
Physics tells us that it fields in **space** that’s really outta sight

I know your teacher said, it’s the conductor that holds the key
We know that’s not the way, you’ve gotta listen to me
If you got fields that are movin’, that makes all the current flow
So you gotta take all of this in, and lose all that you know

Because you know it’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**, not wires
It’s all about the **space**
'Bout the **space**...

Changes on the Wind

What Changes?

- Smaller device geometries and higher current switching capabilities have thrust us all into the world of RF, HF, UHF and microwave energy management
- Rise times on even the lowest tech devices now exhibit gigahertz impact
- These changes directly impact product functionality and reliability

What Changes?

- IC technology was described as % shrink from Integer Design Rules
  - Circuit-based approach usually was close enough
- IC technology now described in nanometers
  - Circuit-based approach completely falls apart
- EM field (physics) based approach essential
- EMC standards have changed
  - Lower frequency compliance requirements
  - Higher frequency compliance requirements
  - Lower emissions levels allowed
  - Greater immunity required
- The playing field and the equipment have changed!
- This really is a brand new game!

What Can We Do?

- The skills required are only taught in a few universities
  - Missouri University of Science and Technology (formerly the University of Missouri-Rolla) http://www.mst.edu/
  - Clemson University http://www.cvel.clemson.edu/emc
- Our sagest mentors may not be able to help
- Nearly every rule of thumb is wrong
- To gain the skills needed, you have to actively seek them
- Industry conferences
  - PCB West
  - IEEE EMC Society events
  - EMC Week
  - Embedded Systems Conferences

  - And of course, from your favorite semiconductor supplier, NXP!

What Can We Do?

About Me: Daniel Beeker

- 38+ years experience at Motorola/Freescale/NXP designing and working with microprocessor and microcontroller development systems
- 30+ years working with automotive customers in one of the most demanding embedded control environments
- Championing the cause for increased awareness of advanced design technologies
- Used to believe in black magic, but Ralph Morrison set me straight!
- Firmly entrenched in physics-based design philosophy

What Can We Do?

- There are many “myths” and folklore about the “art” of PCB design
- Old “rules of thumb” no longer apply
- Time to update our techniques and remove the mystery

What Can We Do?

I Had an Epiphany at PCB West

- System designers do need to care about PCB design.
- Electromagnetic field behavior is not “black magic.”
- Geometry is critical.
- There are solutions that work.

Foundation of Electronics

Myths We Depended On

- Fields are invisible
- Fields are well behaved
- Fields follow the trace
- Fields avoid open spaces
- Fields are someone else’s problem
- Fields are only important in RF and power supply designs
- Fields are only for farmers

What is Electricity?

Is it volts and amperes …

or electric and magnetic fields?

(Slide compliments of Ralph Morrison, Consultant)

What is Electricity?

- Fields are basic to all circuit operation

- Volts and amperes make things practical
  - We easily can measure volts and amperes
  - More difficult to measure “E” and “H” fields

(Slide compliments of Ralph Morrison, Consultant)

What is Electricity?

Fields do all of the work

- “Current flow” is an artifact caused by moving fields, in the conductors that bound them
  - This is a result of the fields interacting with the molecules in the conductor
  - This interaction consumes some of the field energy, hence a resulting voltage drop caused by this “resistance”
  - The consumption of field energy results in increased movement of the molecules, hence is converted to “heat”!
  - The dielectric also consumes energy the same way, unless it is a vacuum.
  - Electromagnetic energy moves slower through a physical dielectric that through **space** for the same reason
    - It takes TIME for the interaction between the molecules in the dielectric, and it has to travel farther to get around them, even in air.
    - The field has to stop and shake hands with every molecule it meets!

Heresy!!

- THAT is NOT what WE were taught.
- THAT is NOT the perspective we have used our entire careers.
- How dare you contradict my professors and my mentors?
- Didn't what we are doing work for years?
- Don't I just have to connect the pins and things will work?

- …Wait a minute, then why do we have so much trouble with signal integrity and EMC??
- Maybe there IS something we are missing…

Heresy!!

- Is the song still going through your heads?
- It is “All About the **Space**!!”
- Words to live by!!
- Now let’s see what we can learn so we can understand this mystery

Maxwell's Equations

$$\oint \mathbf{E} \cdot d\mathbf{A} = \frac{q_{enc}}{\varepsilon_0}$$

$$\oint \mathbf{B} \cdot d\mathbf{A} = 0$$

$$\oint \mathbf{E} \cdot d\mathbf{s} = -\frac{d\Phi_B}{dt}$$

$$\oint \mathbf{B} \cdot d\mathbf{s} = \mu_0 \varepsilon_0 \frac{d\Phi_E}{dt} + \mu_0 i_{enc}$$

(Slide compliments of http://www.physics.udel.edu/~watson/phys208/ending2.html)

Maxwell's Equations

Maxwell *was* smart!

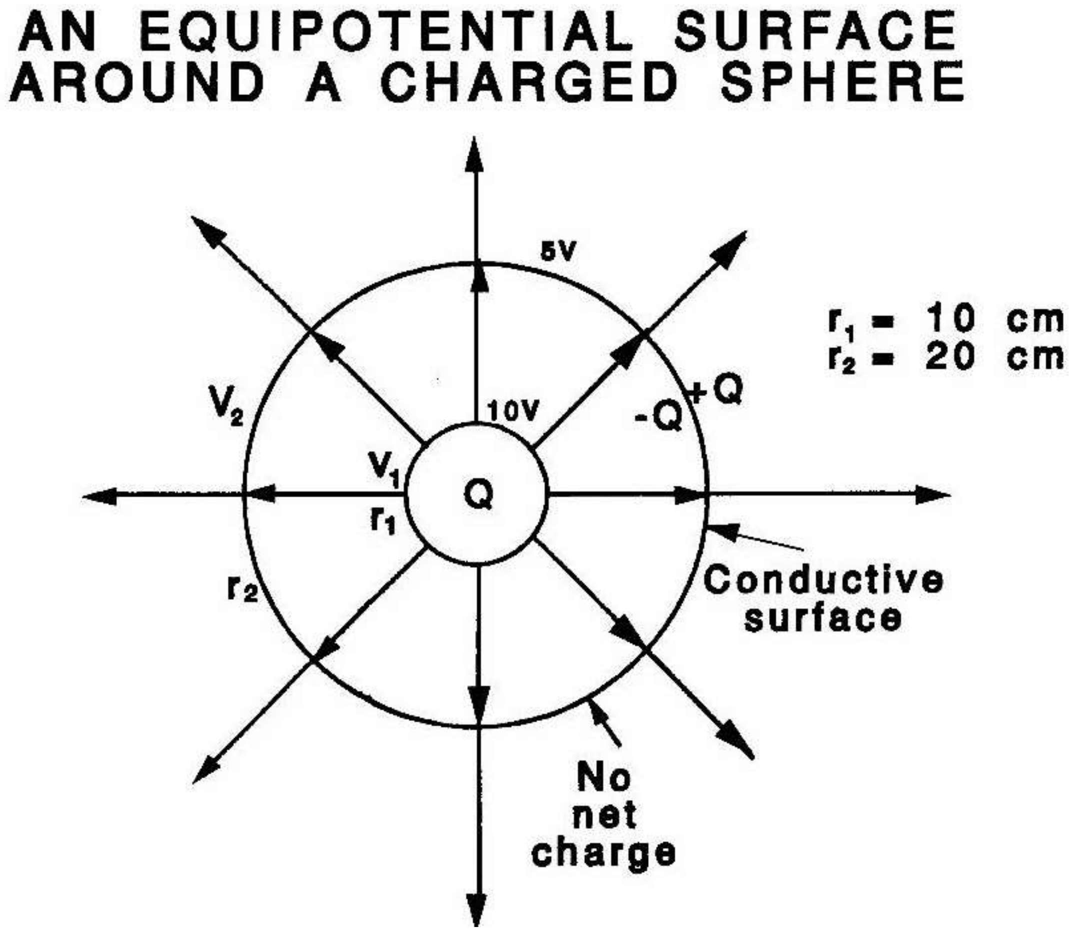
Heresy!!

- Maxwell's equations are all about the interaction between electric and magnetic fields

- There are not any electrons in them
  - No holes, either
  - If it were all about electrons moving, how would fields move through **space**???

Electromagnetic Field Behavior

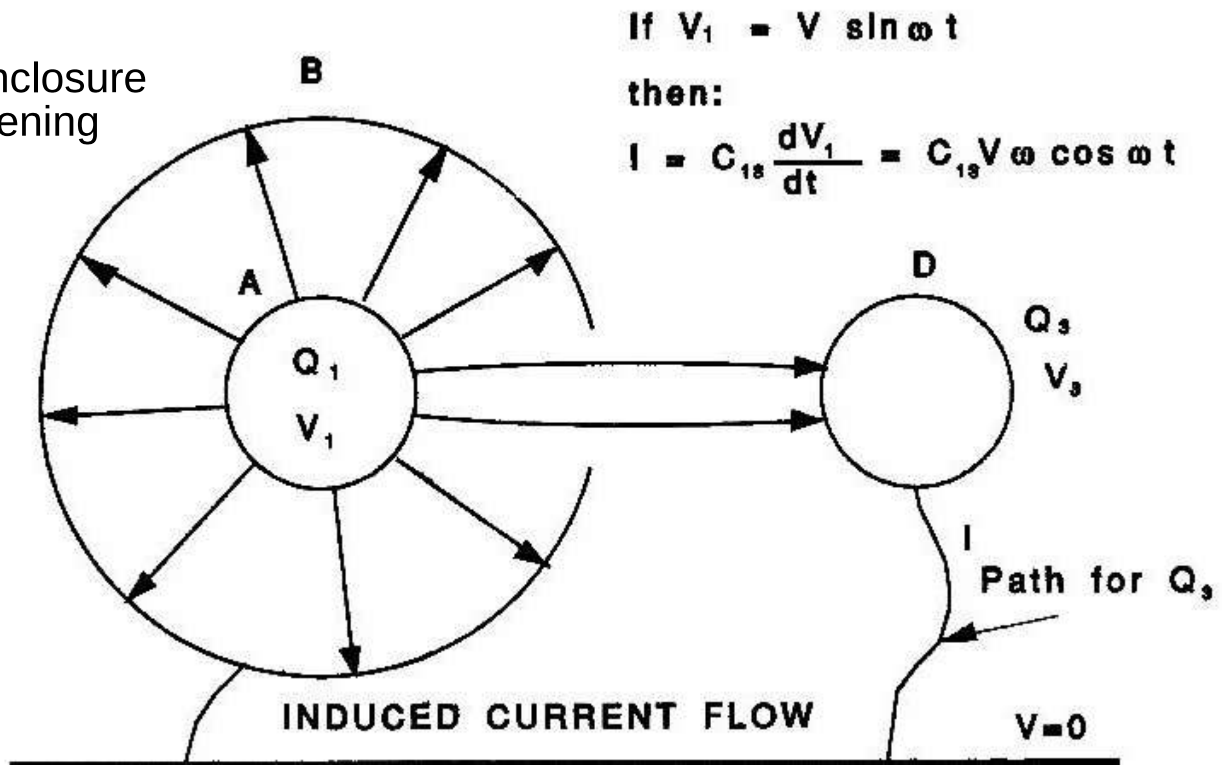
Contained Fields are Friendly!



(Slide compliments of Ralph Morrison, Consultant)

A Loose Field is Not a Friendly Field

A shielded enclosure
with an opening

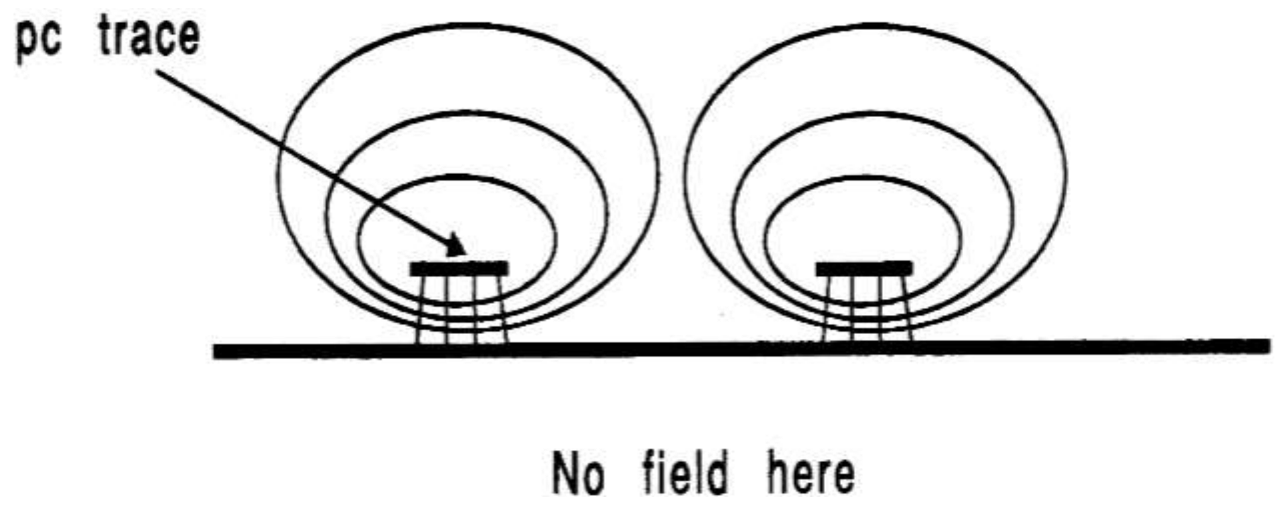


Field is not contained and looks for trouble

(Slide compliments of Ralph Morrison, Consultant)

Contained Fields are Friendly!

Fields concentrate under the traces and there is little crosstalk



Fields do not penetrate the plane

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

Energy Management

A capacitor is:

A conductor geometry that concentrates the storage of electric field energy

In a capacitor:

Field energy is stored in the **space** between the plates

Think of capacitors as lakes between two rivers

An inductor is:

A conductor geometry that concentrates the storage of magnetic field energy

In an inductor:

Field energy is stored in the **space** around wires and in gaps

Think of inductors as wire stretchers. They add travel time to the waves!

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

Why does field energy follow conductors?

- Why does water flow in a stream?
  - Same reason
- Nature follows the path that stores the least energy
- It takes less energy for fields to fill the space between traces than to fill open space

The Impedance of free space is 377 ohms

- Between conductor pairs it will be lower, so they follow the path of lowest impedance

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

Transmission lines are convenient paths for energy flow:

- Every conductor pair is a transmission line
- Trace-to-trace or trace-to-conducting plane
- The fields, and thus the energy flow, will concentrate between traces or between a trace and a conducting plane
- Draw the fields to locate the current

(Slide compliments of Ralph Morrison, Consultant)

Fields are Friendly!

Fields need to be carefully managed:

- Every connection must be treated as one conductor of a transmission line pair
- Field volumes (read "transmission line impedance") must be carefully managed
- Each discontinuity (read "change in transmission line GEOMETRY") results in reflections
- Each segment of this geometry must have enough field energy delivered to match the voltage (read "field density") from the driver
- This all takes TIME

- Yes, this is now a four-dimensional geometric design problem

What’s in the Waves

Power Supply Transmission Line Properties

- In a good design:
  - Energy is available whenever there is a demand
  - The voltage source must be reasonably constant
  - Energy must be replaced after it is used or there will be logic (signal integrity) problems
  - This is called energy management

- Local sources of energy:
  - Decoupling capacitors
  - There is also energy available from ground/power plane capacitance

- New problem: It takes time to move this energy from storage to a load

(Slide compliments of Ralph Morrison, Consultant)

How Long Does It Take?

Wave velocity

- For traces on a circuit board $v = c/\varepsilon^{1/2}$
- Where “c” is the velocity of light and “ε” is the relative dielectric constant

v = 150 mm / ns or 6”/ns

All energy is moved by wave action!

- A drop in voltage sends a wave to get more energy
- Waves reflect at discontinuities (changes in the geometry of the **space**)
- A source of voltage is a discontinuity
- Each reflected wave can carry a limited amount of energy

(Slide compliments of Ralph Morrison, Consultant)

Getting 1 Ampere to Flow

What does this mean in my circuit board?

Initial power level in a 50 Ohm line

- 5 Ohm load and 5 V source
- I = 0.1 amperes or ½ watt

Now, how do I get 1 ampere (1 *coulomb* per second)?

Even if the line is only 1/16 inch long:

- It takes 10 ps for a wave to go 1/16 inch in FR4
- It takes 20 ps for a wave to make one round trip
- It takes 30 round trips to bring current level up to near one amp
- That is 600 ps, assuming zero rise time

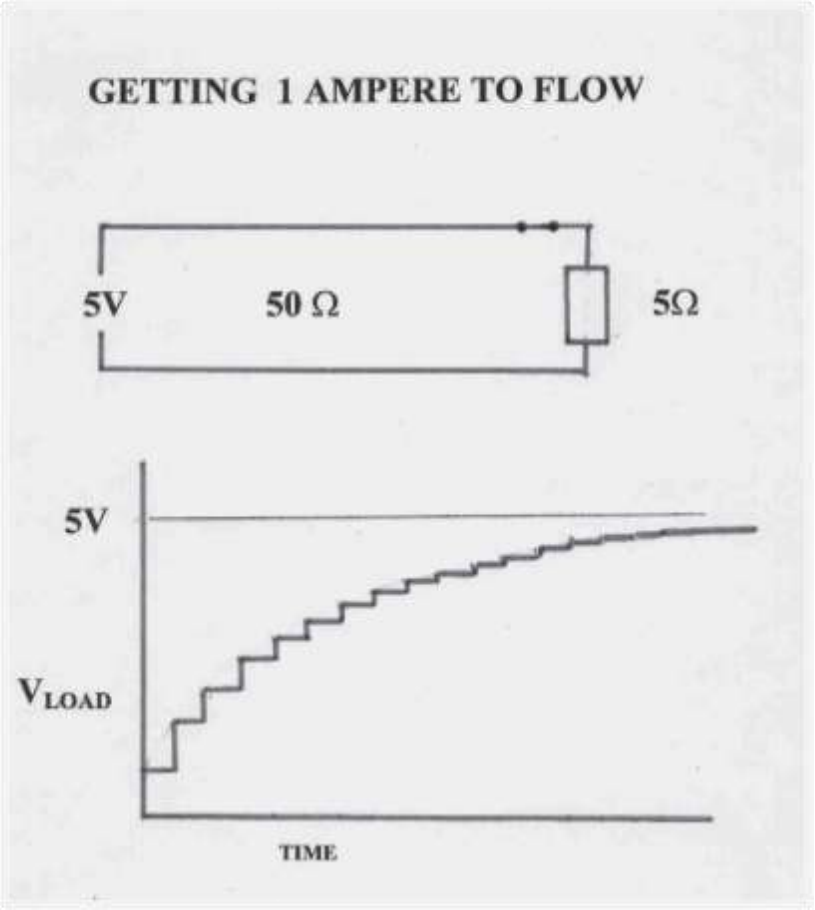
(Slide compliments of Ralph Morrison, Consultant)

Getting 1 Ampere to Flow

Note: This is not a curve, but a series of step functions.

The amplitude of the step is determined by the impedance of the transmission line.

The width of the step is determined by the length of the transmission line and a two way transition for the wave.



(Slide compliments of Ralph Morrison, Consultant)

Typical 1/16 Inch Connections

- Traces to capacitors
- Connections to IC dies
  - Lead frames and wire bonds
  - BGA interposers
- Traces to vias
- Vias to ground/power planes

- Remember, 1/16 inch is about 10 ps
  - Yes, you do care about picoseconds now!

Transmission Lines

Capacitors are short transmission lines:

- Wave action is required to move energy in and out of a capacitor
- Don’t forget the connections to the capacitor!
- Self inductance does not properly tell the story of why it takes time to supply energy
- Circuit theory does not consider time delays
- See the previous diagram!

(Slide compliments of Ralph Morrison, Consultant)

Energy Management

All energy is moved by wave action!

- When a switching element closes, the movement of the field energy into the new **space** results in a drop in the voltage (field density) of the power supply. The resulting field energy request wave travels until this request is filled or it radiates.

The only way to reduce noise in a system is to reduce this distance and provide adequate sources of electromagnetic field energy.

- Energy source hierarchy
- On-chip capacitance
- **Space** between the wire bonds
- Between layers of Substrate (BGA) or lead frame (QFP)
- Power planes if present
- Local bypass capacitors
- Field energy stored across the PCB structure
- Bulk storage capacitors
- Finally the power supply

We have to keep the field happy and contained as far up the food chain as we can, to reduce system noise.

(Slide compliments of Ralph Morrison, Consultant)

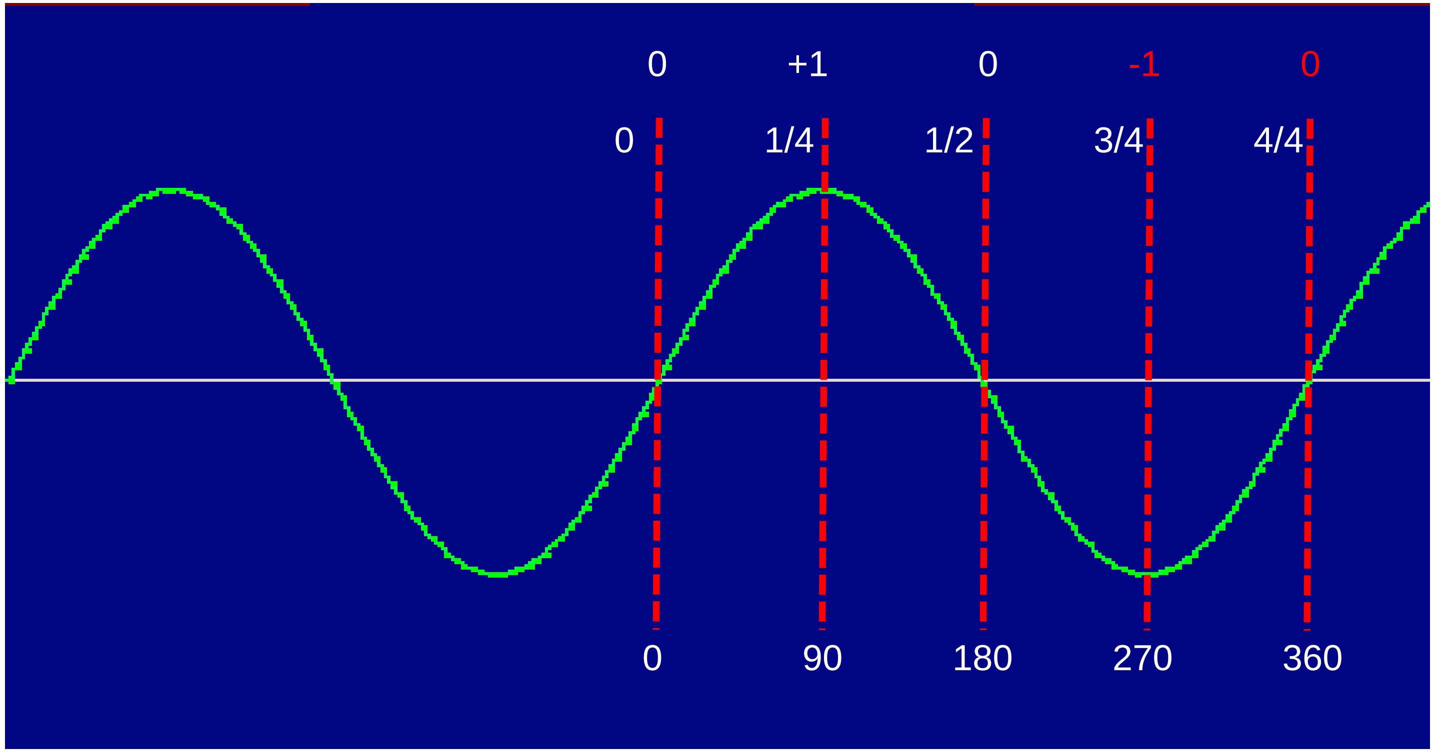
Antenna Size vs. Frequency

¼ wavelength is accepted as a good antenna size. In the Analog Domain, this is 90 degrees (0-1-0-1-0)

Frequency	¼ wave length
1 Hertz Rise time equivalent, who cares	246,000,000 feet (46,591 miles) Almost 6 times around the earth
10 Hertz Rise time equivalent, still who cares	24,600,000 feet (4,659 miles) Almost from Detroit to Honolulu
100 Hertz Rise time equivalent, .01 seconds	2,460,000 feet (466 miles) Almost from Detroit to New York
1 KHz Rise time equivalent, 1 millisecond	246,000 feet (46.6 miles) Almost from Novi to Flint
10 KHz Rise time equivalent, 100 microseconds	24,600 feet (4.659 miles) Almost from NXP Novi to Walled Lake
100 KHz Rise time equivalent, 10 microseconds	2,460 feet (0.466 miles) Almost from the NXP Novi to Meadowbrook Road
1 MHz Rise time equivalent, 1 microsecond	246 feet (0.0466 miles) Less than a football field
10 MHz Rise time equivalent, 100 nanoseconds rise time distance, 100 feet	24.6 feet Across the room
100 MHz (TTL Logic) Rise time equivalent, 10 nanoseconds rise time distance, 10 feet	2.46 feet Less than a yard
1 GHz (BiCMOS Logic) Rise time equivalent, 1 nanosecond rise time distance, 1 foot	0.246 feet (2.952 inches) Less than your finger
10 GHz (GaAs Logic) Rise time equivalent, 100 picoseconds rise time distance, 1.2 inches	0.0246 feet (0.2952 inches) Less than the diameter of a pencil
100 GHz (nanometer geometry HCMOS) Rise time equivalent, 10 picoseconds rise time distance, 0.12 inches	0.00246 feet (0.0295 inches) Half the thickness of a standard FR4 PCB

Analog Wave Perspective

- Seen as sine wave with positive and negative amplitude
- Rise time distance would be ¼ wavelength



Antenna Size vs. Frequency

¼ wavelength is accepted as a good antenna size   In the Analog Domain, this is 90 degrees (0-1-0-1-0)

Frequency	¼ Wave Length
10 MHz **HMOS** Rise time equivalent, 100 nanoseconds rise time distance, 100 feet	**24.6 feet** Across the room
100 MHz (TTL Logic) **UDR HCMOS** Rise time equivalent, 10 nanoseconds rise time distance, 10 feet	**2.46 feet** Less than a yard
1 GHz (BiCMOS Logic) **IDR HCMOS** Rise time equivalent, 1 nanosecond rise time distance, 1 foot	**0.246 feet** (2.952 inches) Less than your finger
10 GHz (GaAs Logic) **65 nm HCMOS** Rise time equivalent, 100 picoseconds rise time distance, 1.2 inches	**0.0246 feet** (0.2952 inches) Less than the diameter of a pencil
100 GHz **32 nm HCMOS** Rise time equivalent, 10 picoseconds rise time distance, 0.12 inches	**0.00246 feet** (0.0295 inches) Half the thickness of a standard FR4 PCB

Antenna Size vs. Frequency

From the previous table, a few things become apparent:

- We got away with ignoring basic physics because IC switching speeds were slow and efficient antennas had to be *huge*.
- At a switching speed of 1 nanosecond, it only takes a PCB feature (trace or slot) of 3 inches to be an efficient antenna (1/4 wave length).
- Once you cross that magic boundary of 1 nanosecond, most PCB designs are capable of providing a wonderful source of antennas.
- At 10 picosecond speeds, every structure in the system can be an good antenna.

Since TTL days:

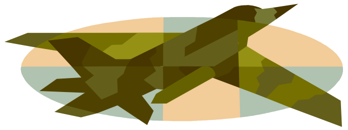
- **Four order magnitude change in switching speeds**
- **Almost no changes in PCB or system design philosophy**

Four Order Magnitude Change

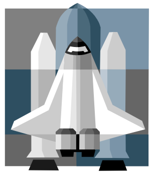
0th order: Vehicles go 6 miles an hour

1st order: Vehicles go 60 miles an hour

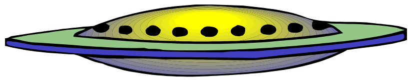
2nd order: Vehicles go 600 miles an hour



3rd order: Vehicles go 6,000 miles an hour



4th order: Vehicles go 60,000 miles an hour



Only in our industry we try to make the buggy to go fast!

Energy and Logic Signals

- The transmission of a logic signal means that field energy is sent out on a transmission line
  - Logic drivers should be treated the same as any power source
- This is true even if the line is un-terminated
  - The driver does not know what is at the end of the transmission line
  - The driver only sees a short circuit until after a reflection occurs
- This energy must be transmitted to the receiver or lost in heat or radiation – it cannot be returned to the driver

Well-Defined Transmission Lines

- Signal traces *must* be one dielectric away from the return!
  - Adjacent to planar copper
  - Adjacent to ground trace
    - Any deviation from this *must* be an engineered compromise, *not* an accident of signal routing
  - Any deviation from this *will* increase radiated emissions, degrade signal integrity and decrease immunity

- Unless a transmission line is required to be controlled impedance (*read receiver is more than 1/6th wavelength away*), the goal should be the lowest possible (practical) impedance.

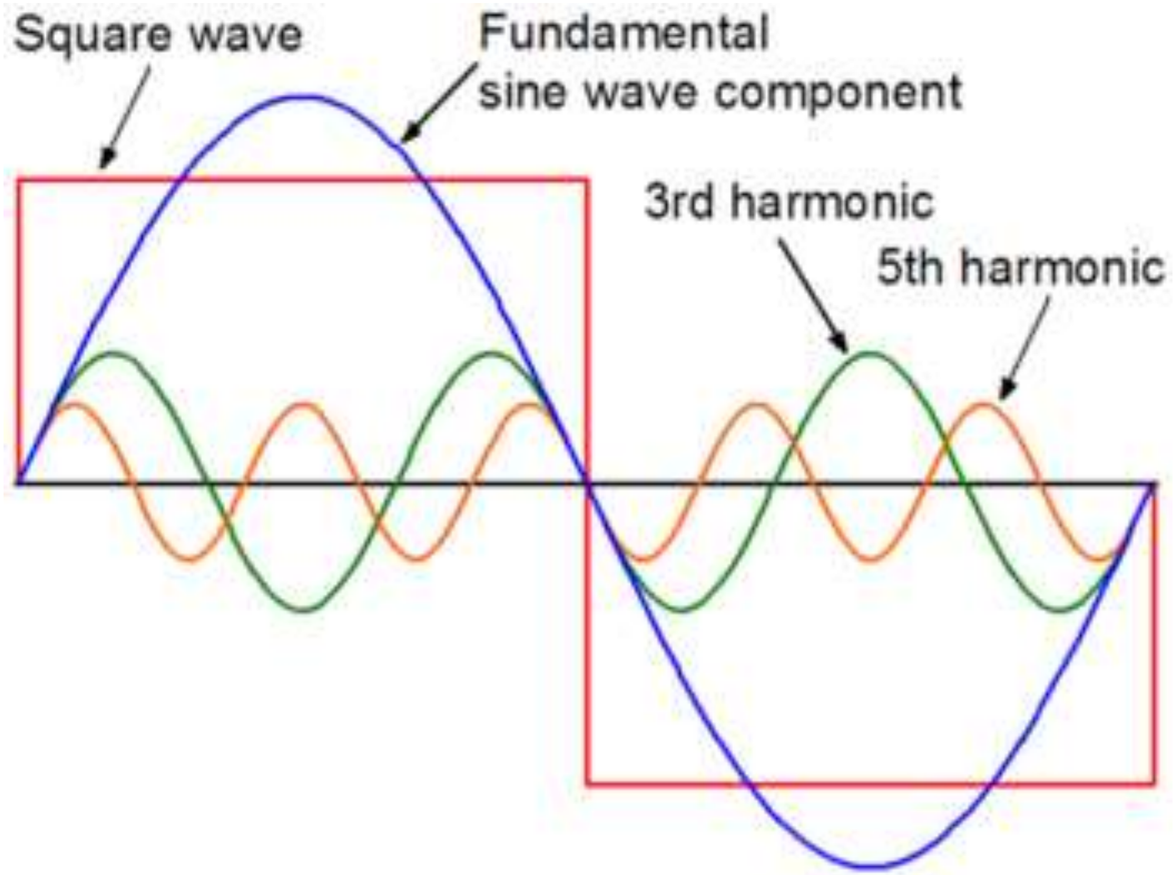
This is a very serious problem and a big change from normal board design philosophy

Well-Defined Transmission Lines

- Good news is that any discontinuity that is less than 1/6th wavelength is virtually invisible to the signal
  - Routing schemes need to be driven by the transistor geometry
- Any failure to insure that both signal and ground copper are contiguous (and adjacent) results in large discontinuities that will cause signal integrity and EMC issues
  - Vertical transitions can not be not excluded
    - This is the most common mistake made in otherwise good designs

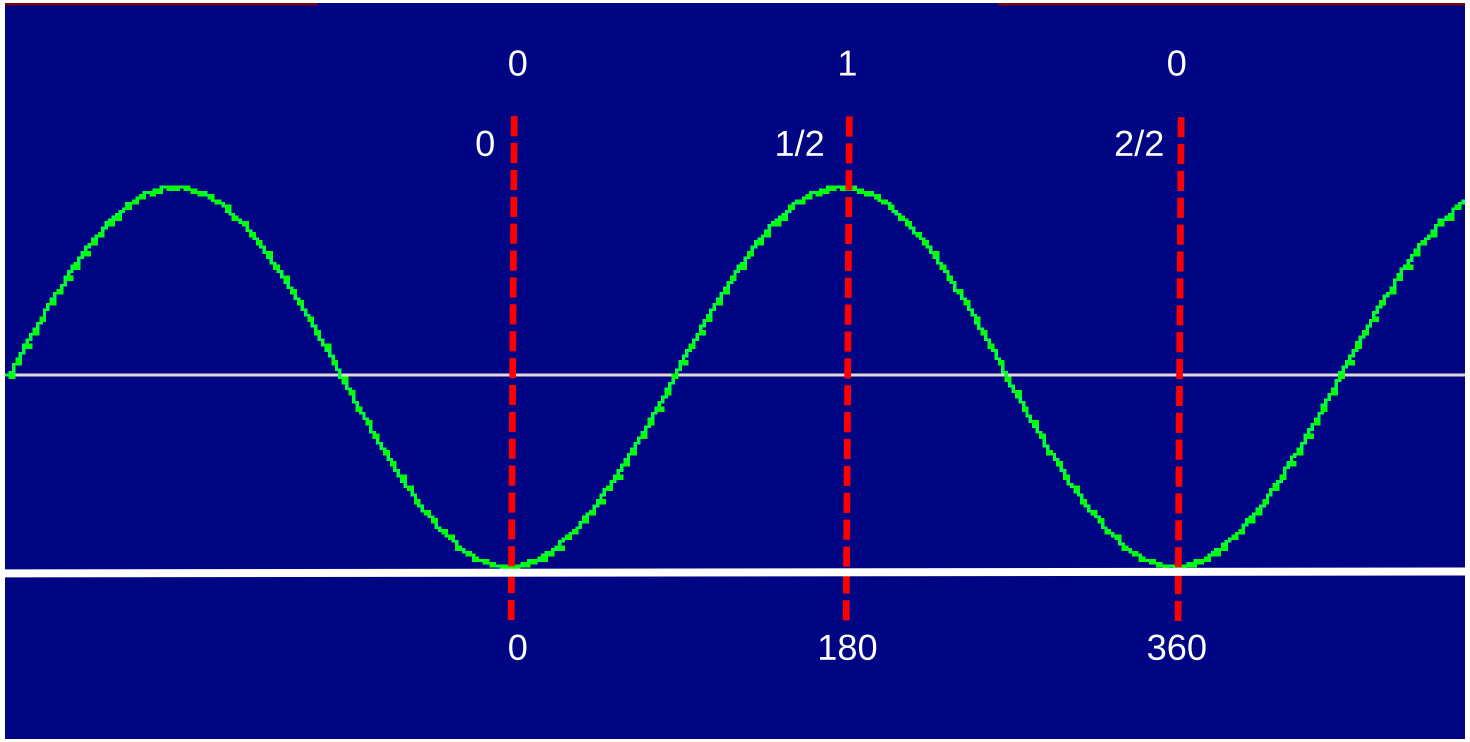
Digital Wave Perspective

Square wave is made up of an infinite number of frequencies
Design for the highest frequency the driver is capable of supporting



Digital Wave Perspective

Seen as sine wave with positive amplitude, the reference is at the lowest point
Rise time distance would be ½ wavelength



Switching Frequency vs. Lumped Distance
(Inner Layer)

Rise time distance is ½ wavelength in digital domain, or 180 degrees

Frequency	1/6 wave length
5 MHz **HMOS** Rise time equivalent, 100 nanoseconds Rise time distance, 100 feet	**16.4 feet** In the room
50 MHz (TTL Logic) **UDR HCMOS** Rise time equivalent, 10 nanoseconds Rise time distance, 10 feet	**1.64 feet** Anywhere on the board
500 MHz (BiCMOS Logic) **IDR HCMOS** Rise time equivalent, 1 nanosecond Rise time distance, 1 foot	**0.164 feet** (1.968 inches) Pretty close
5 GHz (GaAs Logic) **65 nm HCMOS** Rise time equivalent, 100 picoseconds Rise time distance, 1.2 inches	**0.0164 feet** (0.1968 inches) In the package
50 GHz **32 nm HCMOS** Rise time equivalent, 10 picoseconds Rise time distance, 0.12 inches	**0.00164 feet** (0.01968 in. or 500 µm) On the die

Wave Reflection

Reflection Coefficient

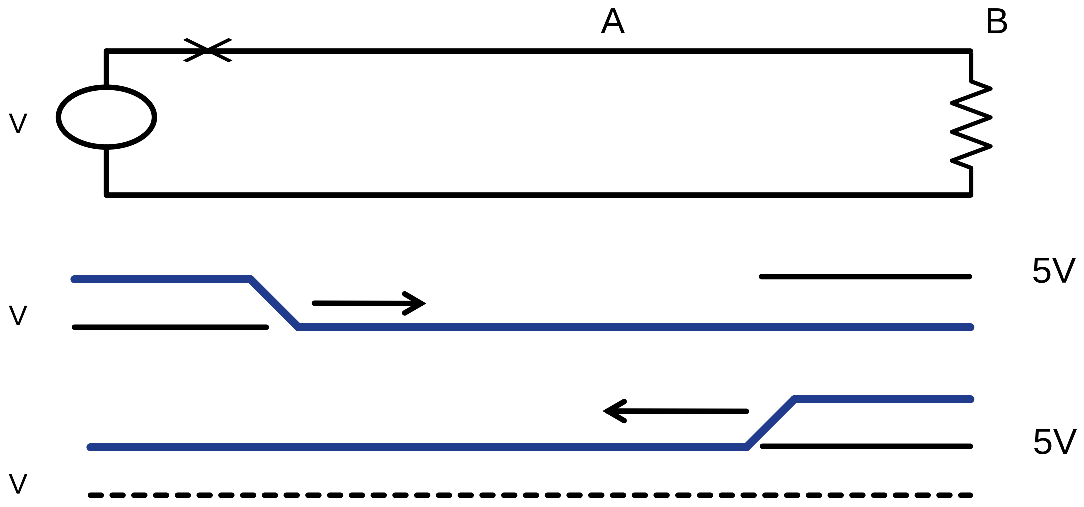
$$\text{Reflection:} \quad \rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

- When $Z_2 = Z_1$ then $\rho = 0$ or *no reflection*
- When $Z_2 > Z_1$ then $\rho > 0$ or *a positive reflection*
- When $Z_2 < Z_1$ then $\rho < 0$ or *a negative reflection*

(Slide compliments of Ralph Morrison, Consultant)

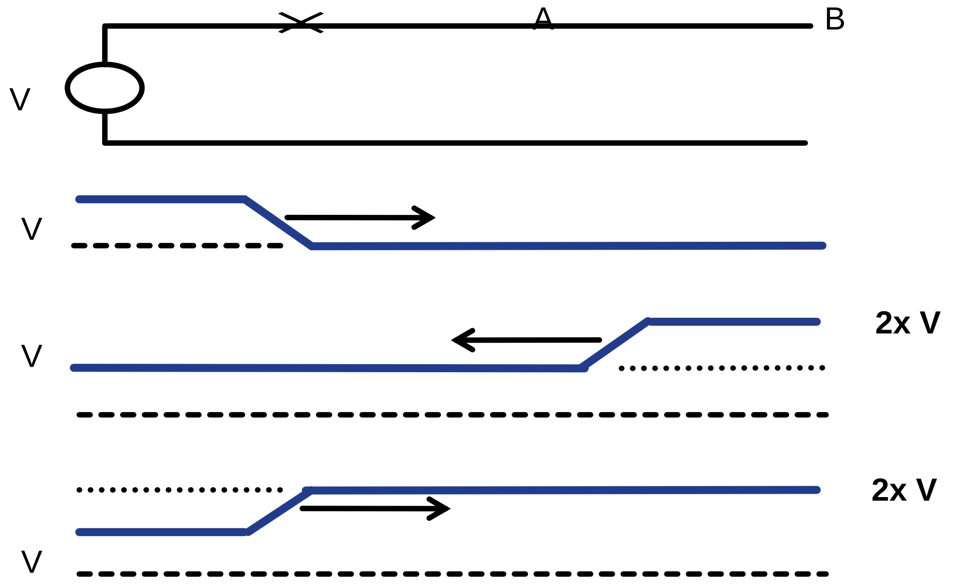
Wave on a Transmission Line

Low impedance source to high impedance load
Wave reflects and voltage doubles



(Slide compliments of Ralph Morrison, Consultant)

Second Reflection at Source



From a low impedance to a high impedance, the wave voltage is doubled and reflected. From a high impedance to a low impedance, the wave voltage is inverted and reflected.
This is called “ringing” and continues until all of the energy is either transferred to the receiver, converted to heat in the dielectric, or radiates.

(Slide compliments of Ralph Morrison, Consultant)

Rise Time Distance

Now, what does this really mean?

- Rise time distance is how far the wave travels by the time it reaches full amplitude.
- Determined by the switching speed of the output driver
- In digital circuits, this is really ½ wavelength, or 180 degrees!
- Let’s look at this from a switching speed vs. lumped distance perspective.
- Remember, lumped distances are basically the size of a discontinuity which remains invisible to the energy flow.
- To prevent problems on uncontrolled impedance transmission lines, the load must be less than 1/6 of the wavelength (67% amplitude reflection)
- The voltage developed is less than ½ of the output voltage, so the reflection is less than the output voltage
- One reflection and the transmission line is stable
- How far is that for a given switching speed?

Logic Families / Rise Time / Max Length

DEVICE TYPE	RISETIME	Max Line Length Inner (inch/mm)	Max Line Length Outer (inch/mm)
Standard TTL	5.0 ns	7.27 / 185	9.23 / 235
Schottky TTL	3.0 ns	4.36 / 111	5.54 / 141
10K ECL	2.5 ns	3.63 / 92	4.62 / 117
ASTTL	1.9 ns	2.76 / 70	3.51 / 89
FTTL	1.2 ns	1.75 / 44	2.22 / 56
BICMOS	0.7 ns	1.02 / 26	1.29 / 33
10KH ECL	0.7 ns	1.02 / 26	1.29 / 33
100K ECL	0.5 ns	.730 / 18	.923 / 23
GaAs	0.3 ns	.440 / 11	.554 / 14

(Calculated assuming a nominal Er = 4.1)

(Slide compliments of Rick Hartley, Consultant)

Energy Delivery From A Storage Device

For energy to be delivered from a storage device:

- The wave requesting the energy (observed as a dip in the power supply caused by the switching event) has to travel to the source and back to the switch.

It's a two-way trip!

Switching Frequency vs. Power Source

Frequency	1/20 Wave Length
5 MHz HMOS Rise time equivalent, 100 nanoseconds Rise time distance, 100 feet	4.92 feet Somewhere in the room
50 MHz (TTL Logic) UDR HCMOS Rise time equivalent, 10 nanoseconds Rise time distance, 10 feet	0.492 feet (5.9 inches) Somewhere on the board, should be routed as co-planar pairs
500 MHz (BiCMOS Logic) IDR HCMOS Rise time equivalent, 1 nanosecond Rise time distance, 1 foot	0.0492 feet (0.59 inches) Width of your finger, time to look at small geometry capacitors and power islands
5 GHz (GaAs Logic) 65 nm HCMOS Rise time equivalent, 100 picoseconds Rise time distance, 1.2 inches	0.00492 feet (0.059 in. or 1498.6 µm) In the package
50 GHz 32 nm HCMOS Rise time equivalent, 10 picoseconds Rise time distance, 0.12 inches	0.000492 feet (0.0059 in. or 149.86 µm) On the die

Switching Frequency vs. Power Source

- If the energy source is not inside the 1/20 wavelength distance, there will be radiated energy caused by the switching event.
- The job of the PCB designer is to minimize the amount of energy by managing the power delivery system for each type of switching event.
- As the geometry of the ICs we use continues to shrink, so does the area of effective power delivery.
- Well-defined power delivery transmission lines and small geometry, low impedance, field storage devices are essential.
- Even if they are outside of the “zone,” they can minimize the amount of radiated energy.

How to Use this Wonderful Information

Where Do We Start?

- Board outline / usually pre-determined
  - Defined by previous product
  - Customer requirements
- Placement

1. Pre-defined components / usually connectors
2. Filter components / high priority, must be as close to the pins as allowed by manufacturing
3. Power control / as close to connector involved as possible

    Voltage regulators

    Power switching devices

    See number 2 above

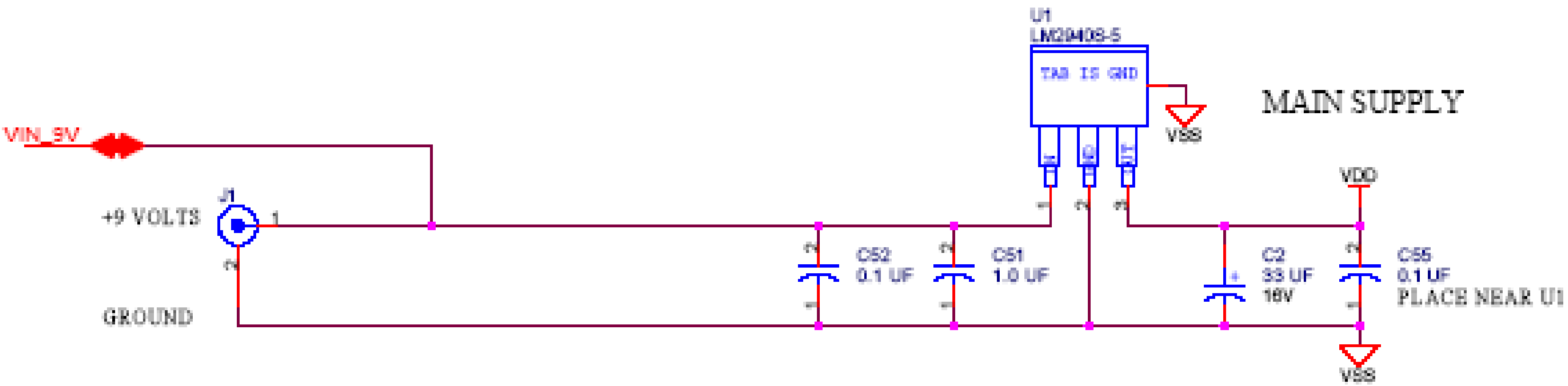
Schematics Must Be Evaluated During Layout

Arbitrary connections can be redefined to improve layout

- Unscrambling nets can result in:
  - Reduced complexity
  - Reduced trace length
  - Improved EMC performance
- Signals that are not defined to specific pins
  - GPIO on MCUs
  - A/D pins on MCUs
  - Address and data lines to memories
    - No, the memory does not care what you call each pin.
    - They are just address and data, not Addr14 or Data12

Schematics Must Be Evaluated During Layout

- Schematic is often lacking in order definition
- Capacitors must be placed in the daisy chain in the correct order



Uncontrolled Component Placement

You get to decide!

- Placement not specified by customer or company requirements
- Evaluate component domain
  - Power
  - Sensor
  - Digital IC
- Place to limit signal mixing
  - Route power only in power realm
  - Route sensor lines only where needed
  - Digital IC connections only in digital realm

Uncontrolled Component Placement

- Power realm devices must be placed near connectors
  - Shorter traces
  - Cleaner returns
  - Reduced field volumes (Yes, this is a three-dimensional consideration)
- Don’t forget their supporting cast
  - Bypass capacitors, Inductors, resistors
  - Use the largest value capacitor in the smallest package allowed by manufacturing and reliability[3]
- Digital realm devices
  - Technology (geometry) of each device
  - Function
  - Devices placed within lumped distance do not need terminating resistors
  - 1/6 wavelength of the IC switching frequency, not clock frequency (determined by IC geometry)
    - Yes, this is important to know …sometimes controlled by variable drive strength
    - For 1 ns switching speeds (500 MHz) this is about 2 inches!

[3] Comment compliments of Dr. Todd Hubing

Uncontrolled Component Placement

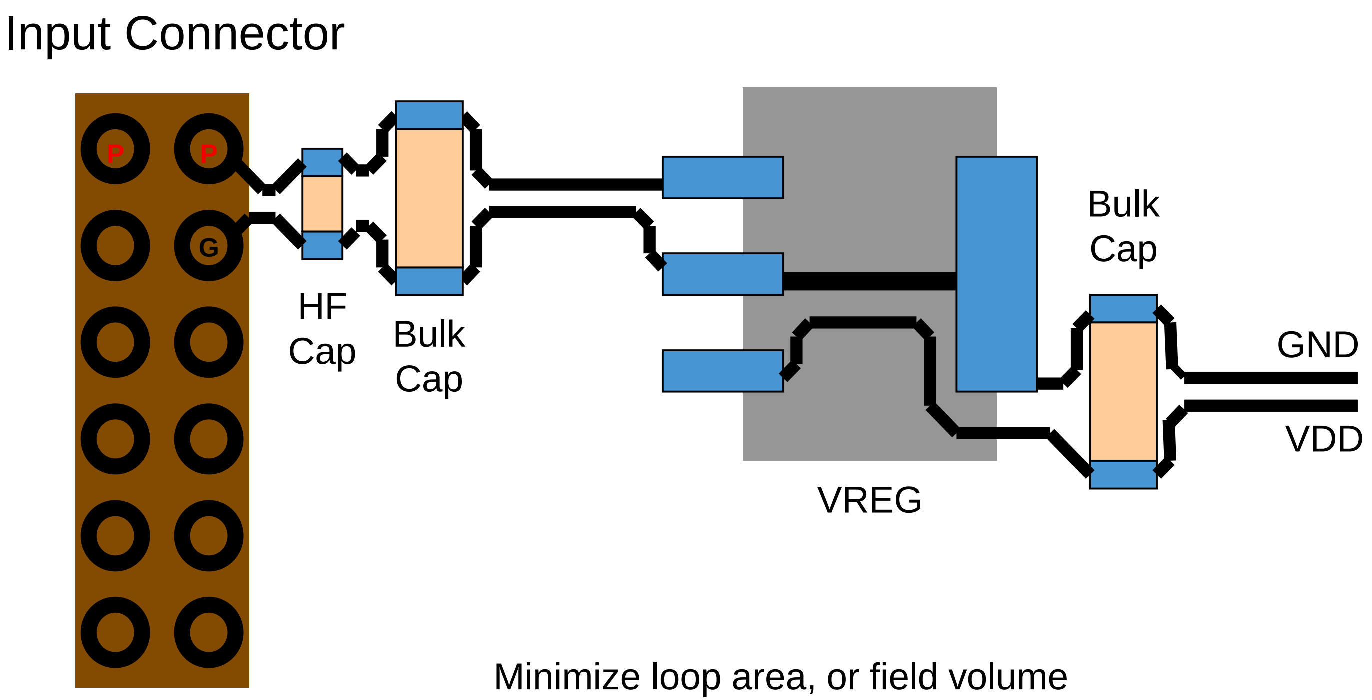
- Remember, if you do not route signals where they don't need to be, there will not be any crosstalk or interference.
- This is easier if you do not mix the parts together.
- If the traces are not near each other, there is no magic that will cause them to interfere with each other.
- Can I say this any other ways? Is this important, YES!
- Let's move on to actually routing the board…

Power Distribution

PCB ~~signal~~ Transmission Line Routing

- The first and most important job is to route the power distribution network – it is the source of all of the electromagnetic energy you will be managing on the PCB
- On low layer count boards, with no dedicated ground plane, the power lines must be routed in pairs
  - Power and ground
  - Side by side
    - Trace width determined by current requirements
    - Spaced as close as manufacturing will allow them
  - Daisy chain from source to destination, connecting to each component, then finally to target devices
- Minimize the volume of the power transmission network

PCB ~~signal~~ Transmission Line Routing



Minimize loop area, or field volume

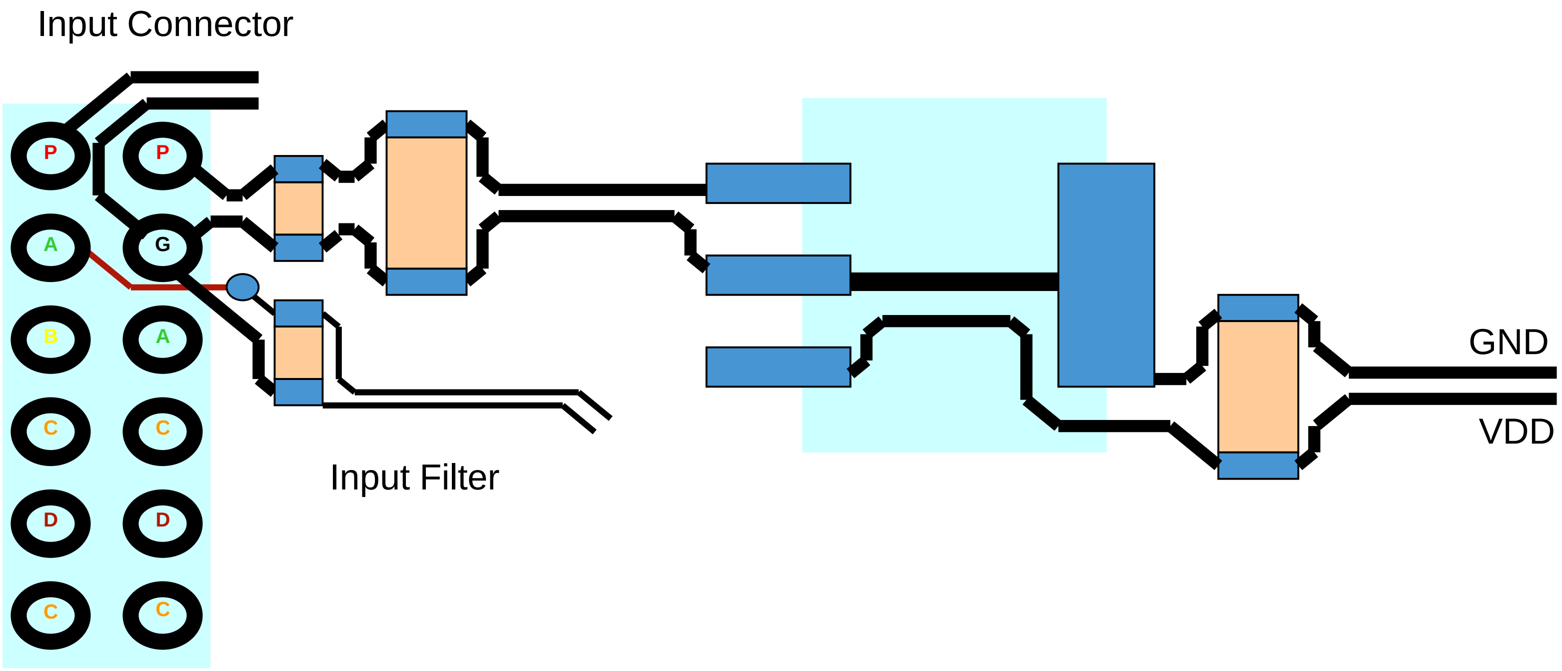
Energy flows from left to right, never the reverse!

PCB ~~signal~~ Transmission Line Routing

- Route power and ground traces as close as manufacturing allows
- Internal and customer separation requirements
- PCB fabrication limits for chosen supplier
  - Yes, you do need to know what the supplier can manufacture
  - Can have big impact on PCB cost
- Small changes in routing can have a large impact on performance
- Component placement is critical
  - Staying within lumped distance
    - Reduces component count
    - Reduces system cost
    - Improves EMC performance
    - Minimize the volume of the power transmission network

Designing Good Transmission Lines

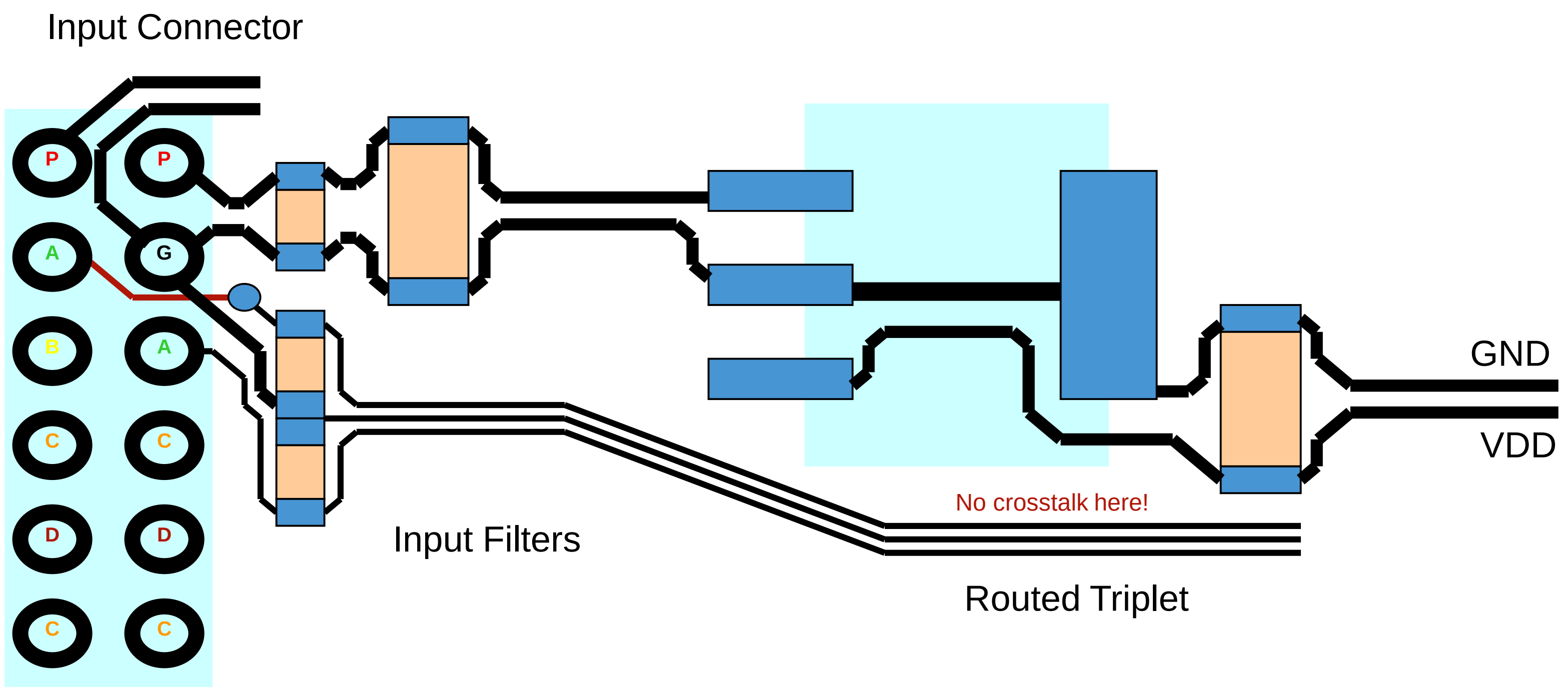
PCB ~~signal~~ Transmission Line Routing



PCB signal Transmission Line Routing

- Input filters must be placed as close as allowed to connectors
- Connections must be directly to the connector ground pins
- Route traces with well defined return path
- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing

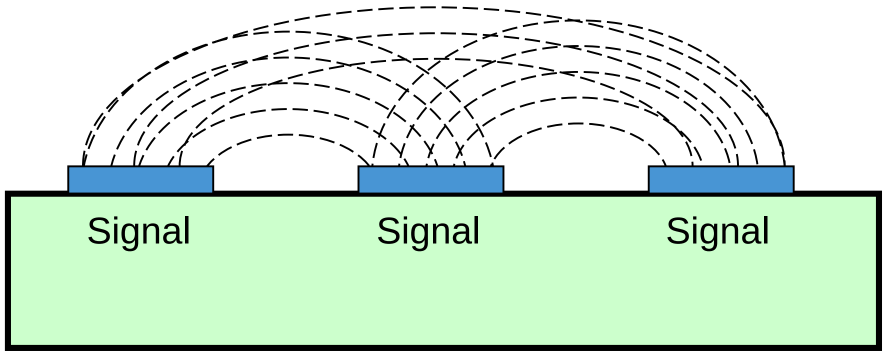


PCB ~~signal~~ Transmission Line Routing

- Routing in “triplets” (**S**-**G**-**S**) provide good signal coupling with relatively low impact on routing density
- Ground trace needs to be connected to the ground pins on the source and destination devices for the signal traces
- Spacing should be as close as manufacturing will allow
- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing

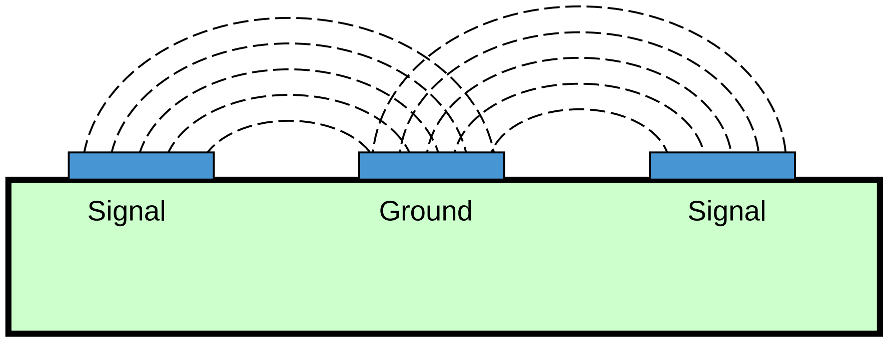
You really want to make sure that the field energy is coupling to the conductor <u>you</u> choose!



Note: All field lines actually terminate at 90 degree angles

PCB ~~signal~~ Transmission Line Routing

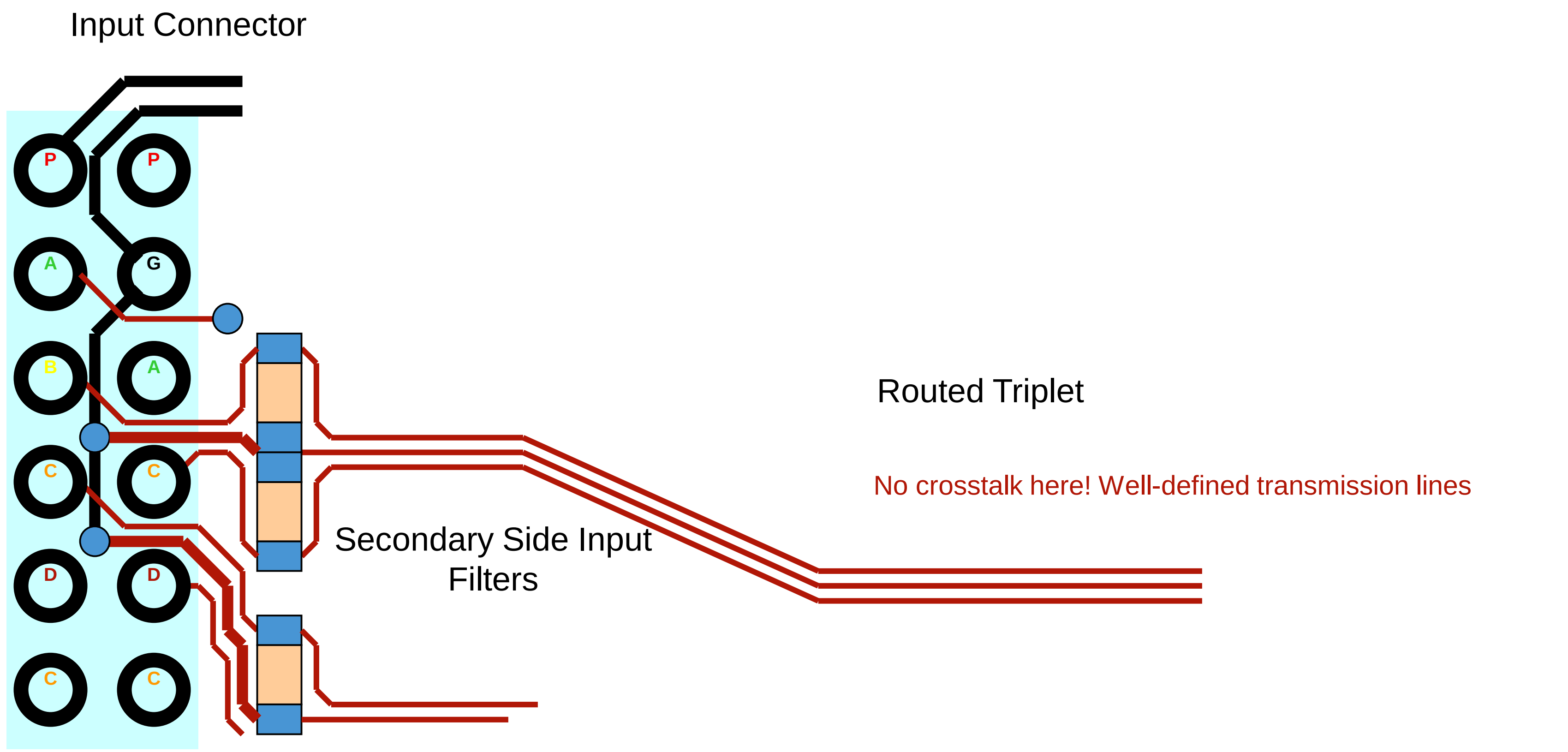
You really want to make sure that the field energy is coupling to the conductor <u>you</u> choose!



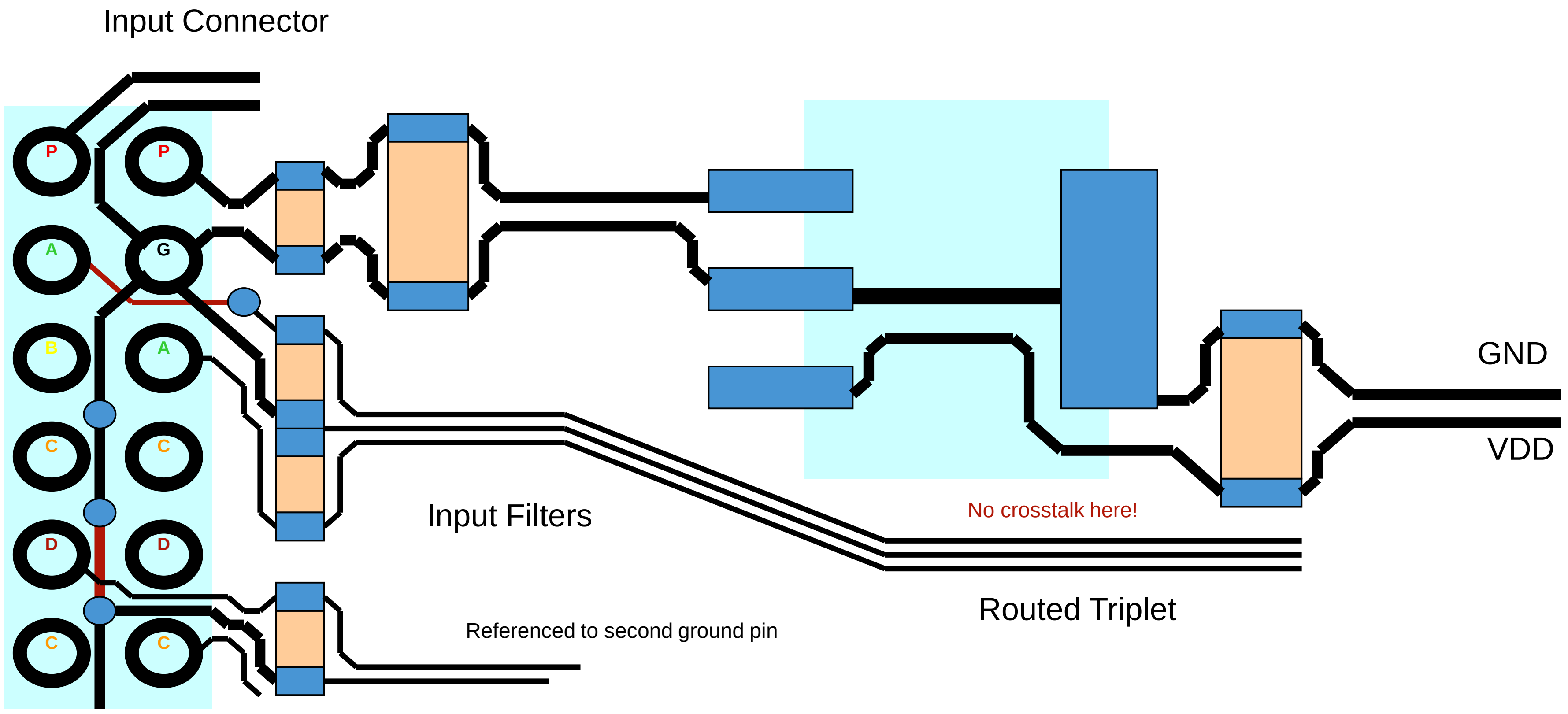
Note: All field lines actually terminate at 90 degree angles

Maybe a “triplet” makes sense?

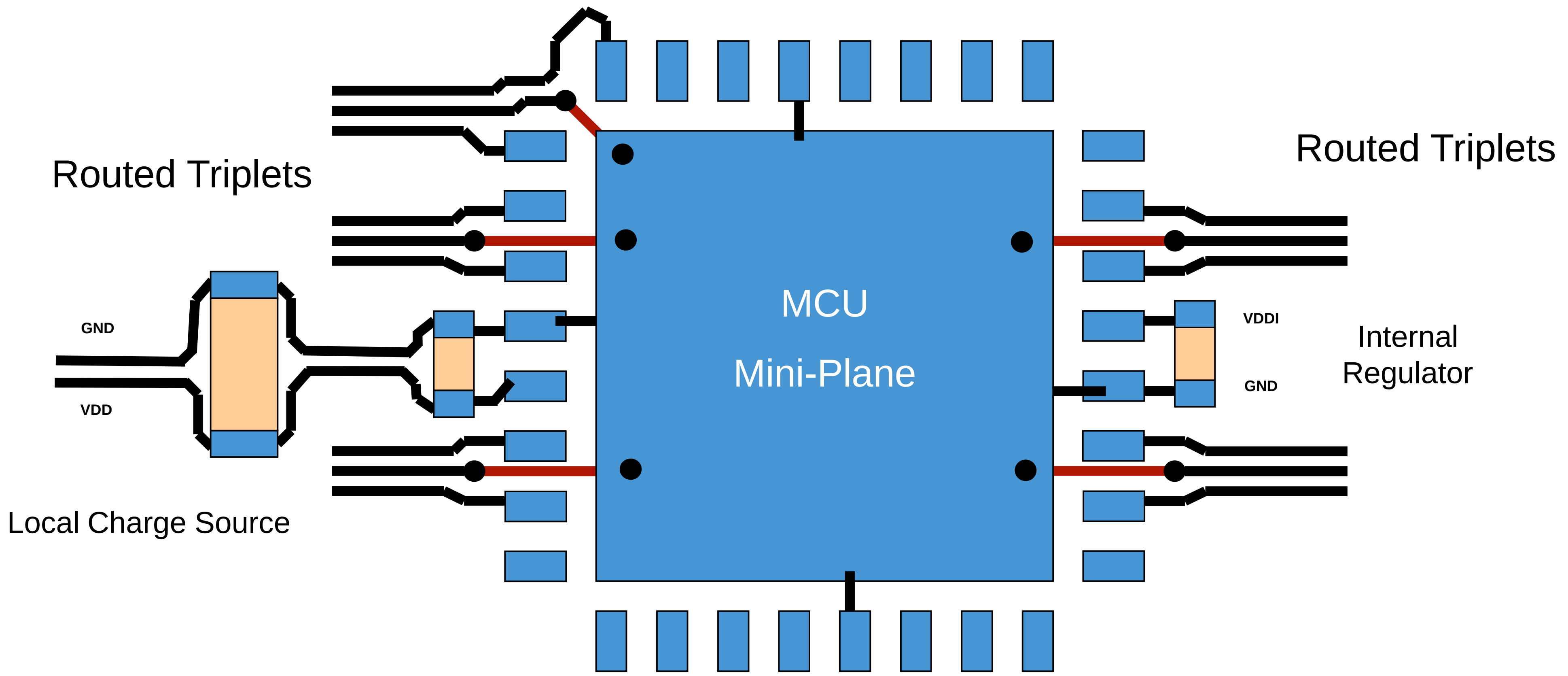
PCB ~~signal~~ Transmission Line Routing



PCB ~~signal~~ Transmission Line Routing



PCB ~~signal~~ Transmission Line Routing

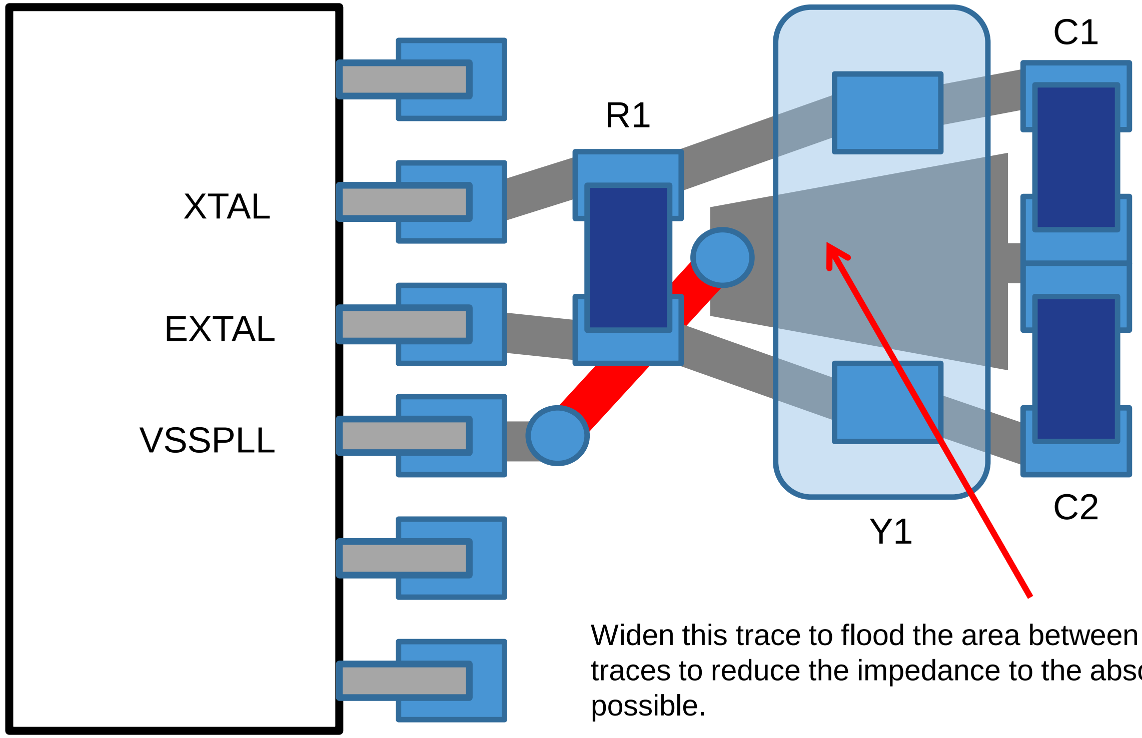


PCB ~~signal~~ Transmission Line Routing

- Lead frame and wire bonds are parts of transmission lines, too
- Mini-plane under the QFP provides improved EMC
- Triplet ground traces can be easily coupled to the mini-plane on secondary side
- In high density applications, even routing with “quints”
  (**S**-**S**-**G**-**S**-**S**) will provide some improvement
- You know where most of the field energy is going!
- Last but not least, flood everything with ground copper!
- Must be able to tie each “island” with at least two via to adjacent layer ground
- Minimize the volume of the signal transmission network

PCB ~~signal~~ Transmission Line Routing

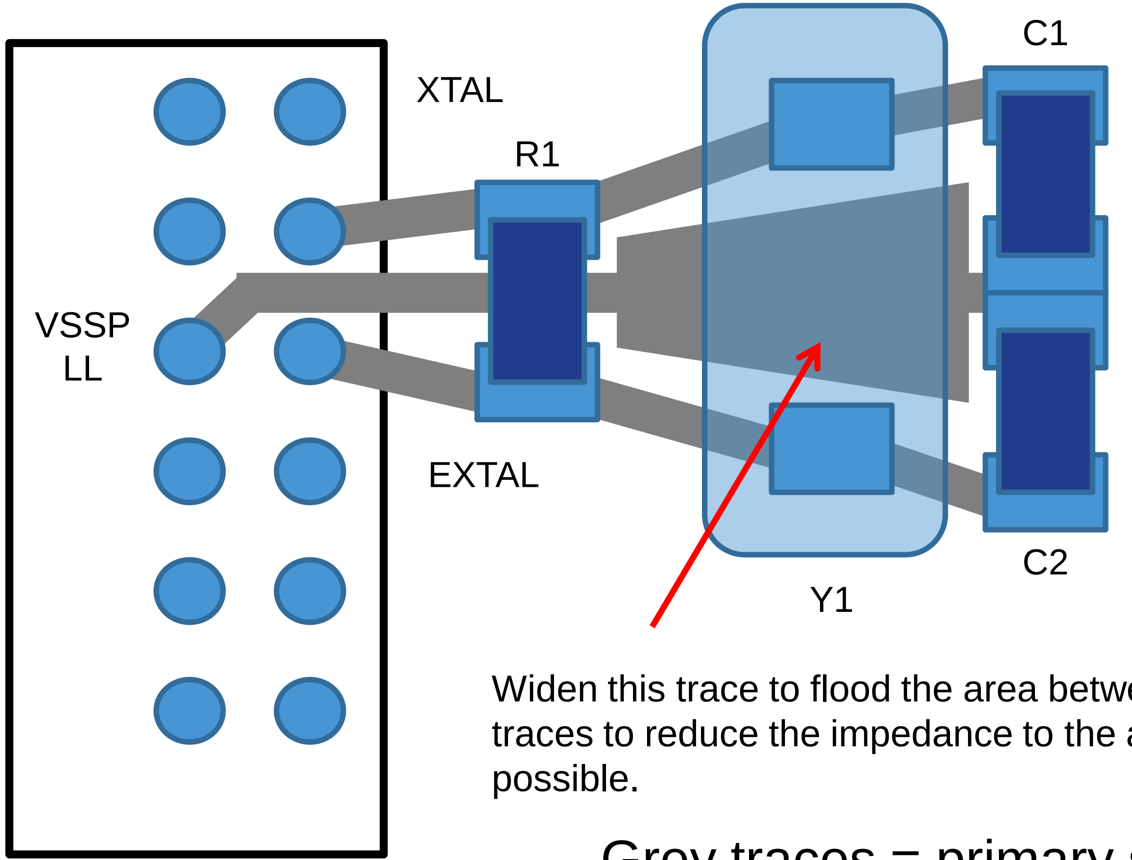
Oscillator ground must be routed to MCU pin, not tied to System Ground
Connect System Ground on the opposite side of the MCU pin



Widen this trace to flood the area between the signal traces to reduce the impedance to the absolute minimum possible.

Grey traces = primary side
Red traces = secondary side (or adjacent layer)

PCB ~~signal~~ Transmission Line Routing



Oscillator ground must be routed to MCU pin, not tied to System Ground
Connect System Ground on the opposite side of the MCU pin

Widen this trace to flood the area between the signal traces to reduce the impedance to the absolute minimum possible.

Grey traces = primary side

PCB ~~signal~~ Transmission Line Routing

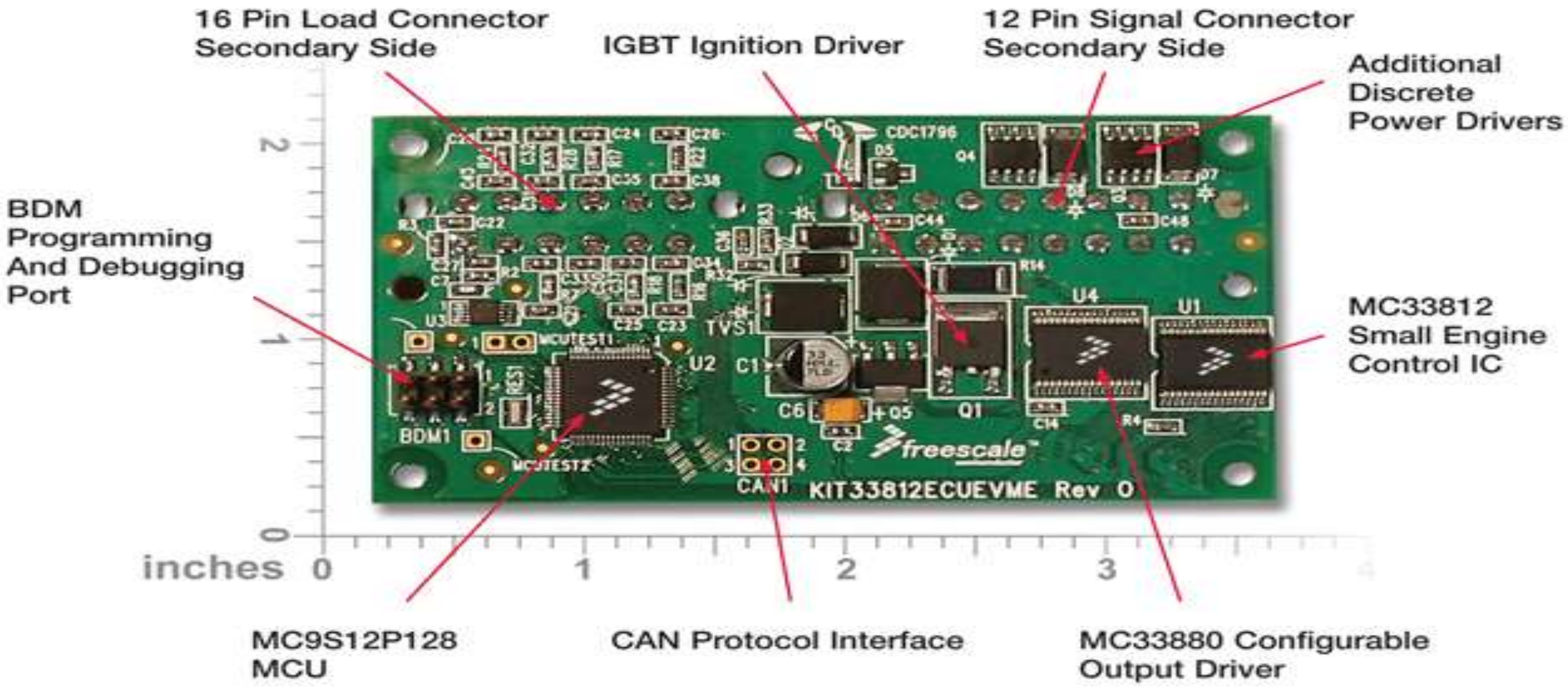
- Crystal output from MCU is the POWER source
  - Energy flows out, between the MCU output signal trace and MCU oscillator ground trace to the crystal or resonator
- Crystal becomes POWER source
  - Energy flows back, between the crystal output signal trace and the oscillator ground trace to the MCU input pin
- This is a closed loop system, and SYSTEM ground is not required
  - Lower impedance for the connecting transmission lines
  - Smaller loop area
  - Significantly improved robustness
- It is always about "Where does the energy come from?"
- This rule should be applied to the entire design
  - Ground for any signal is determined by the power source return
- Another important fact is that this is a low amplitude, low frequency, analog circuit. It is not required to be placed as close as possible to the MCU, just that it must be connected with transmission lines as described above. Moving these components can allow for placement and routing of more critical components in the area near the MCU.

Test Results

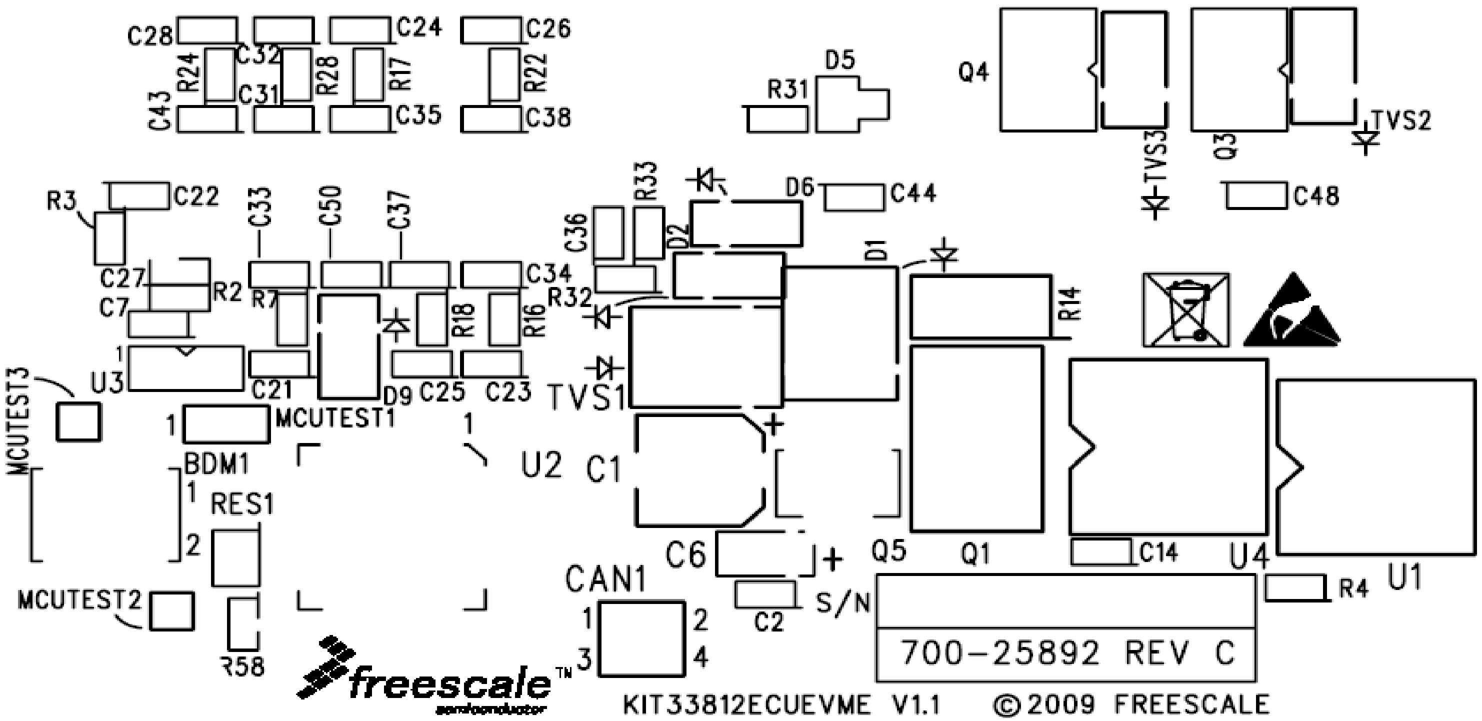
The Proof is in the Testing

- KIT33812ECUEVME Reference Design
  - Intended for motorcycle and other single/dual cylinder small engine control applications
- MC33812 analog power IC
  - Multifunctional ignition and injector driver
- MC9S12XD128 MCU
  - Designed for either the MC9S12P128 or MC9S12XD128
  - Test results are for the older, noisier MCU
- Two-layer PCB
- Business card dimensions
- Implements these design and layout concepts
  - “Smart” connector pinout
  - MCU mini-plane
  - Triplet routing
  - Maximum flooding

KIT33812ECUEVME Reference Design

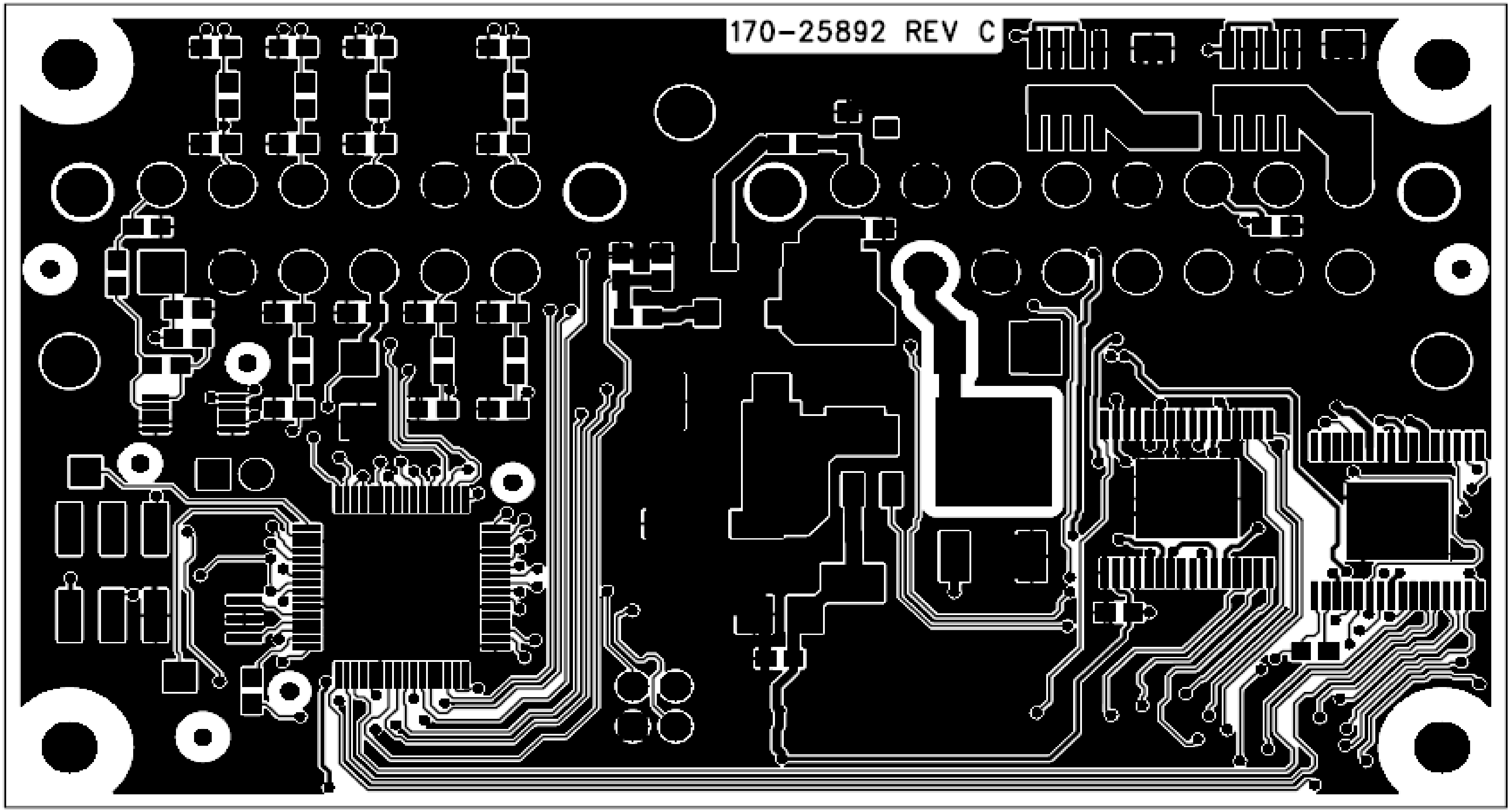


KIT33812ECUEVME Reference Design



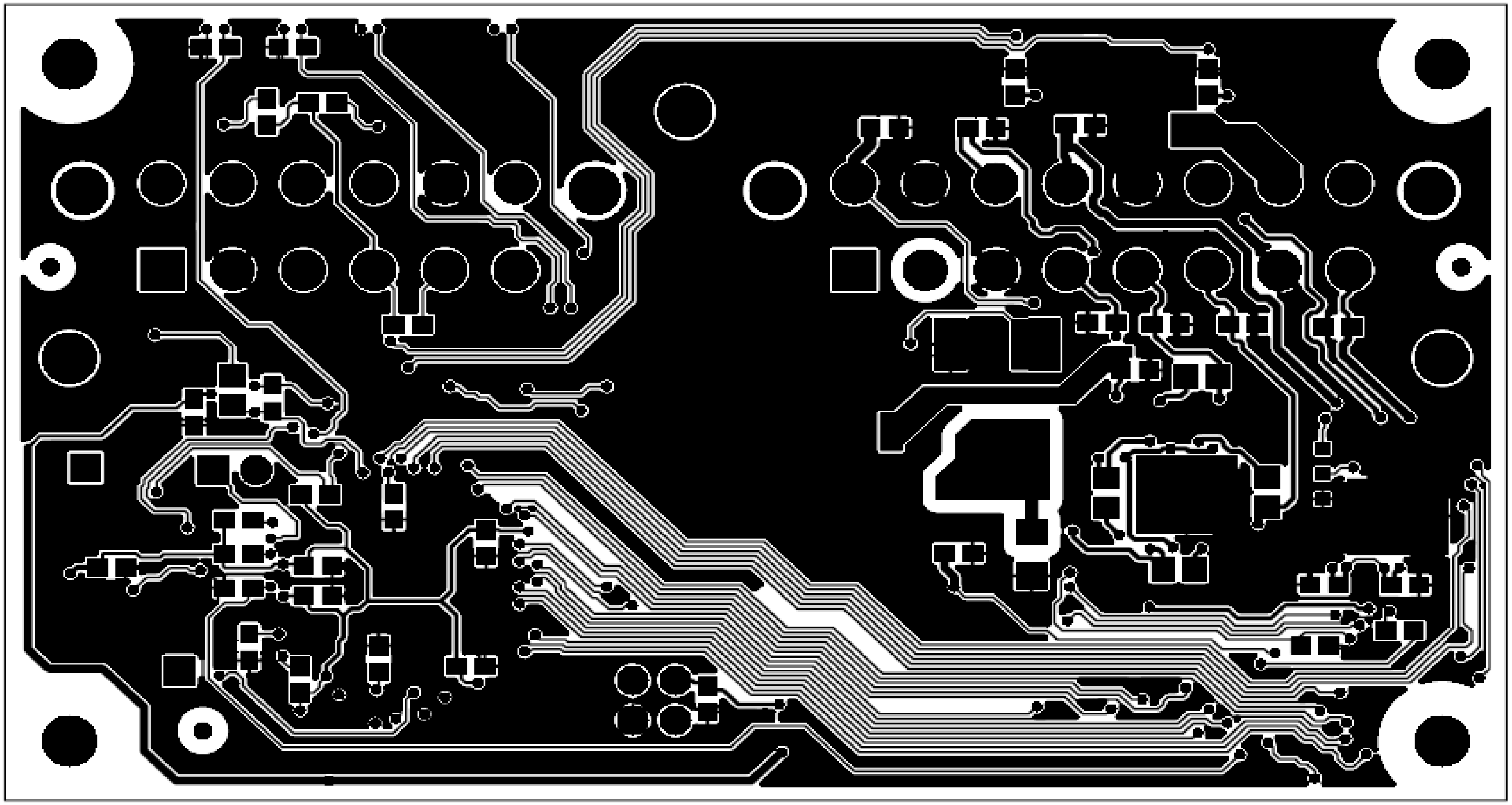
Primary Silk

KIT33812ECUEVME Reference Design



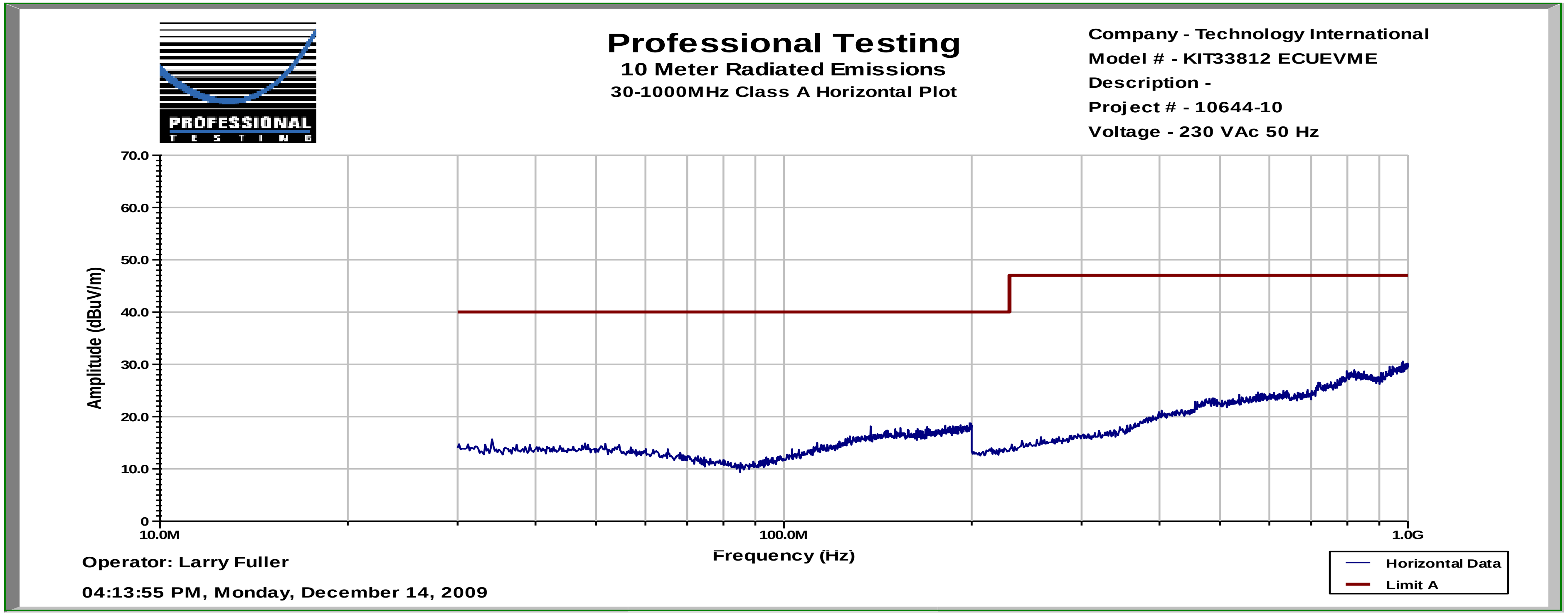
Primary Side

KIT33812ECUEVME Reference Design

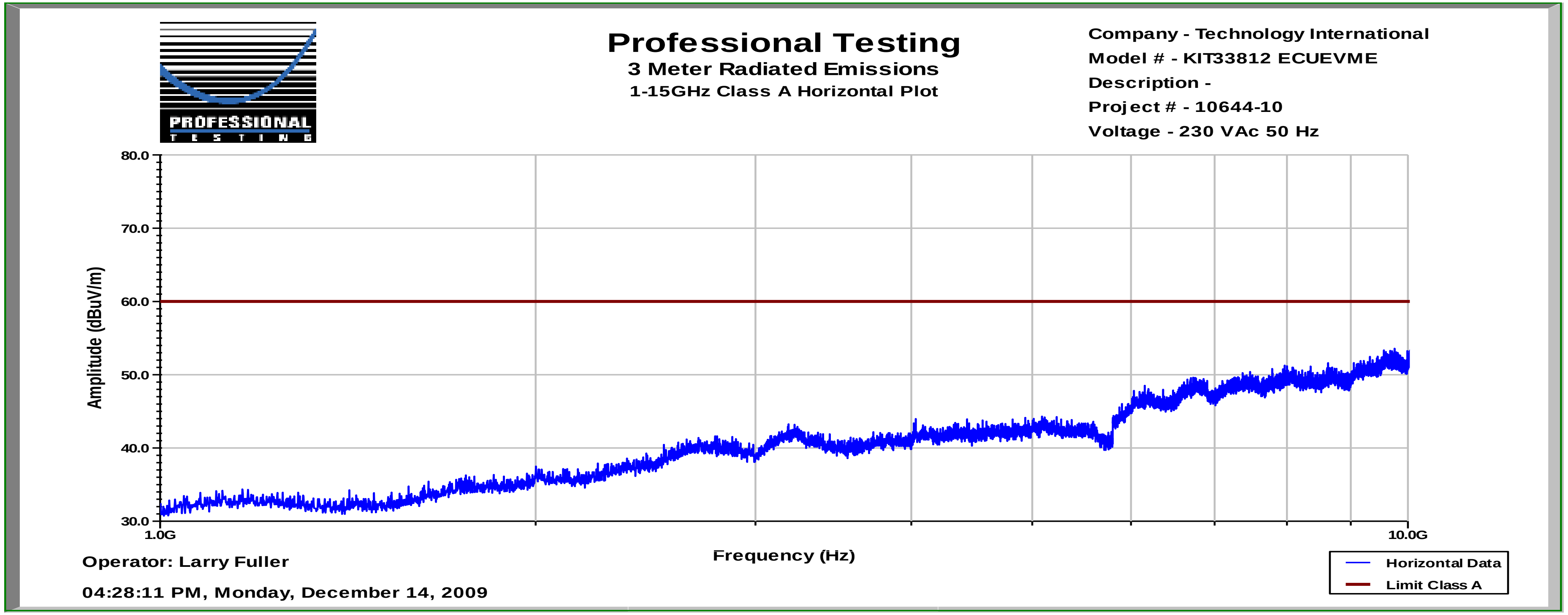


Secondary Side

KIT33812ECUEVME Reference Design



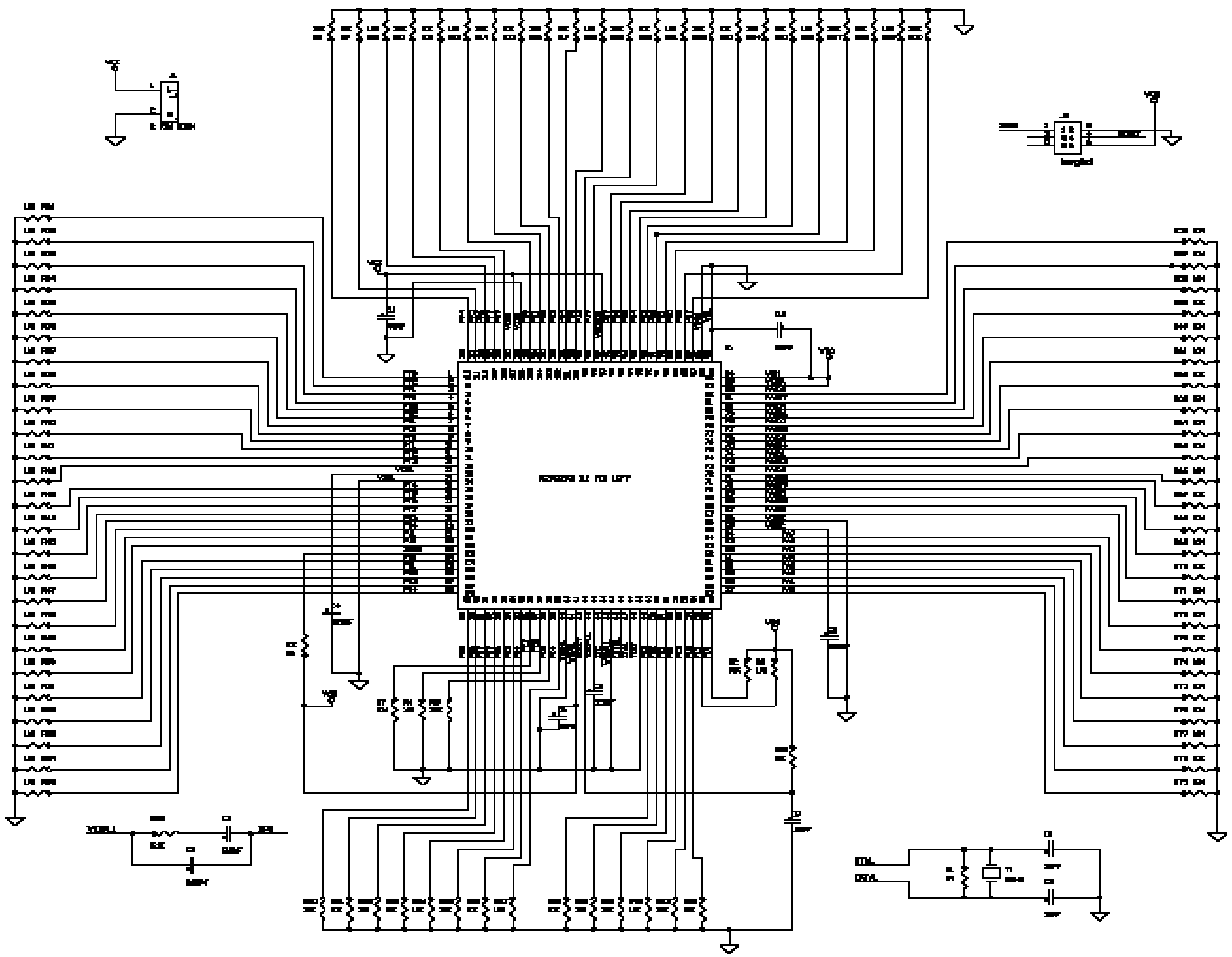
KIT33812ECUEVME Reference Design



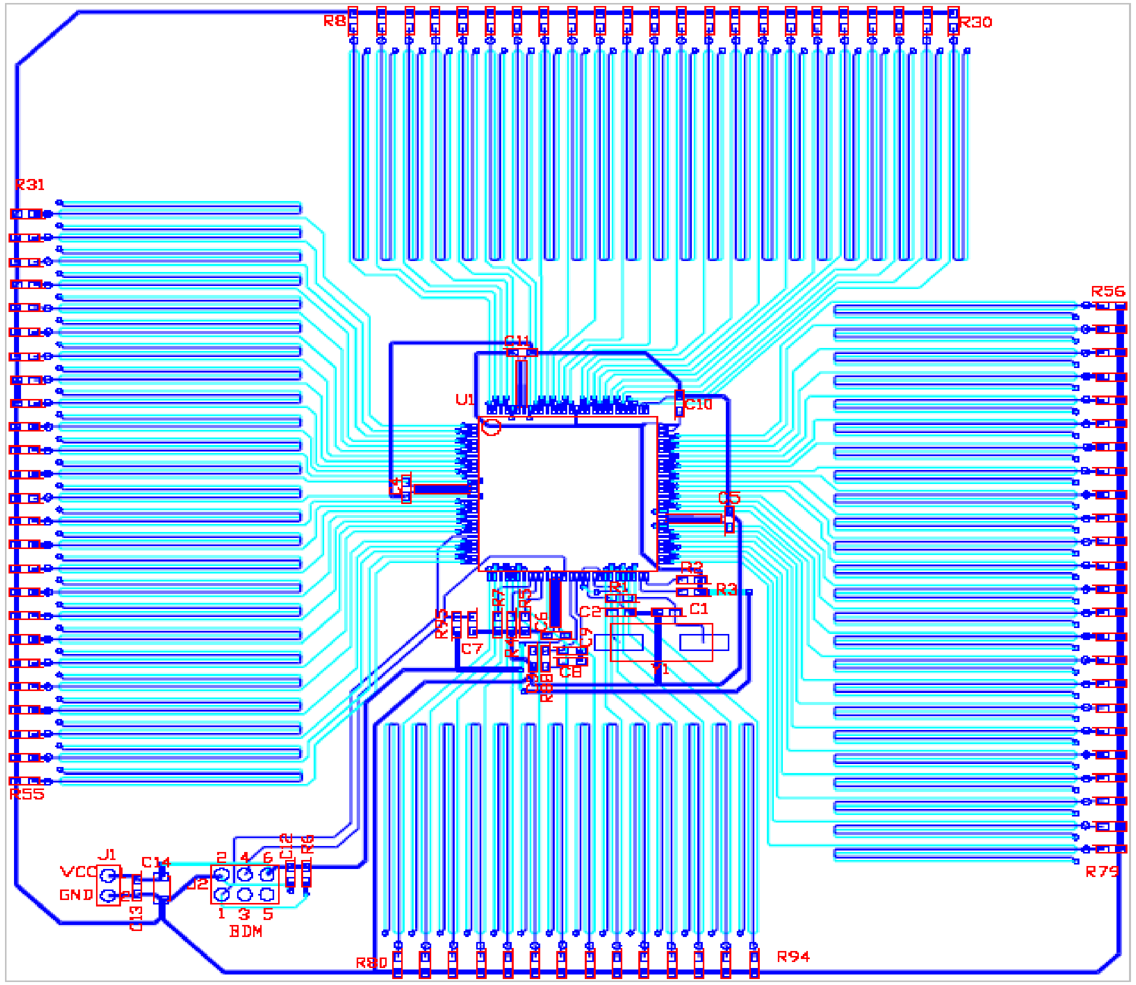
EMC Test Board

- EMC test board with no field control considered
- Two layers
- 112-pin MC9S12XD128 MCU
- All I/O lines routed to 10 K termination resistors using serpentine 6” traces
- All ground connections routed in “convenient” patterns
- Filter components placed “somewhere near”
- Line widths and spacing aimed for low cost FAB
- Software running at 40 MHz, toggling all I/O pins

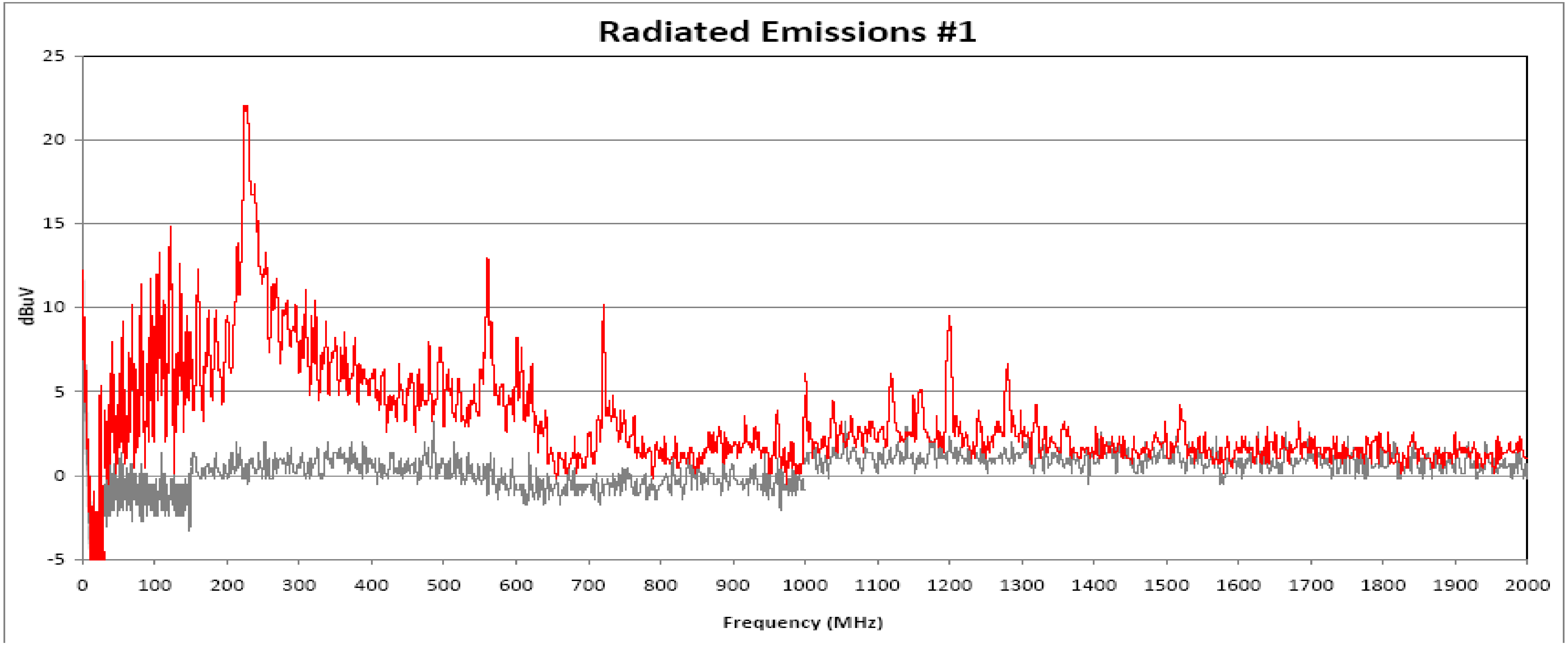
EMC Test Board Schematic



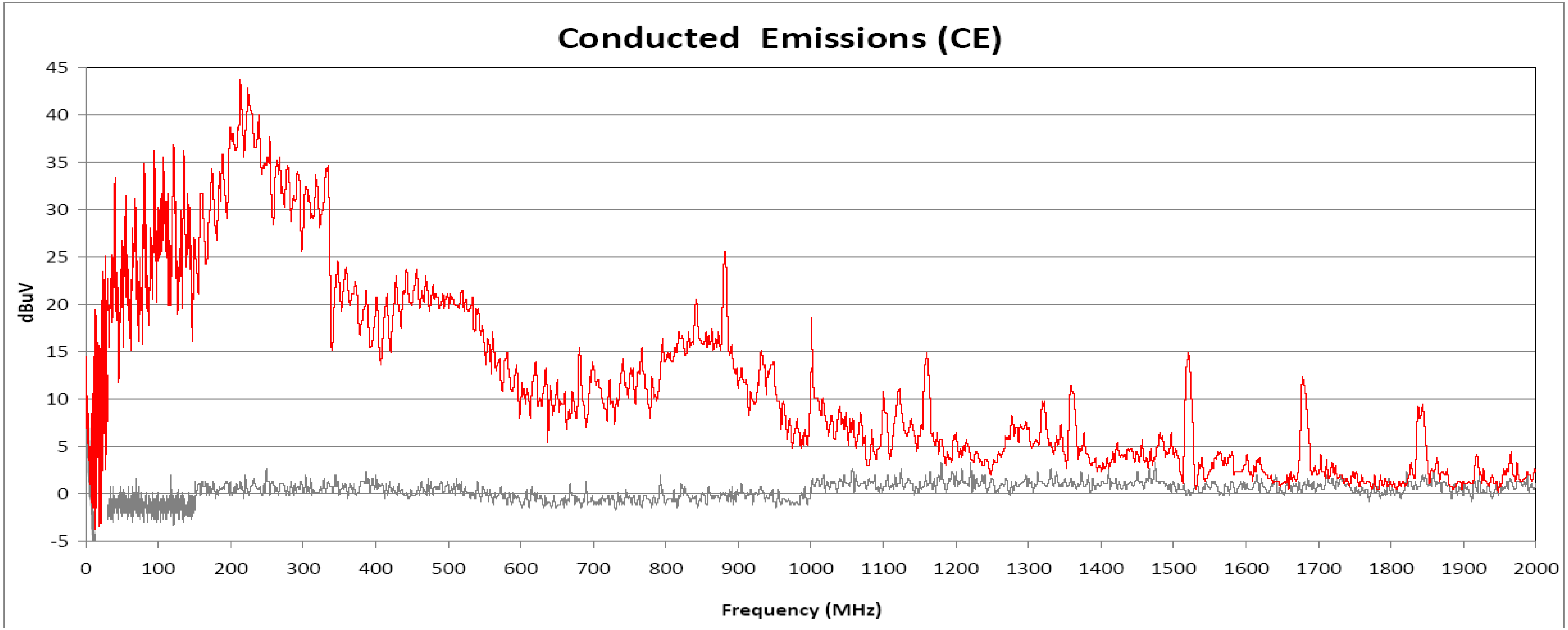
EMC Test Board Layout



Two-layer EMC Test Board Radiated Emissions



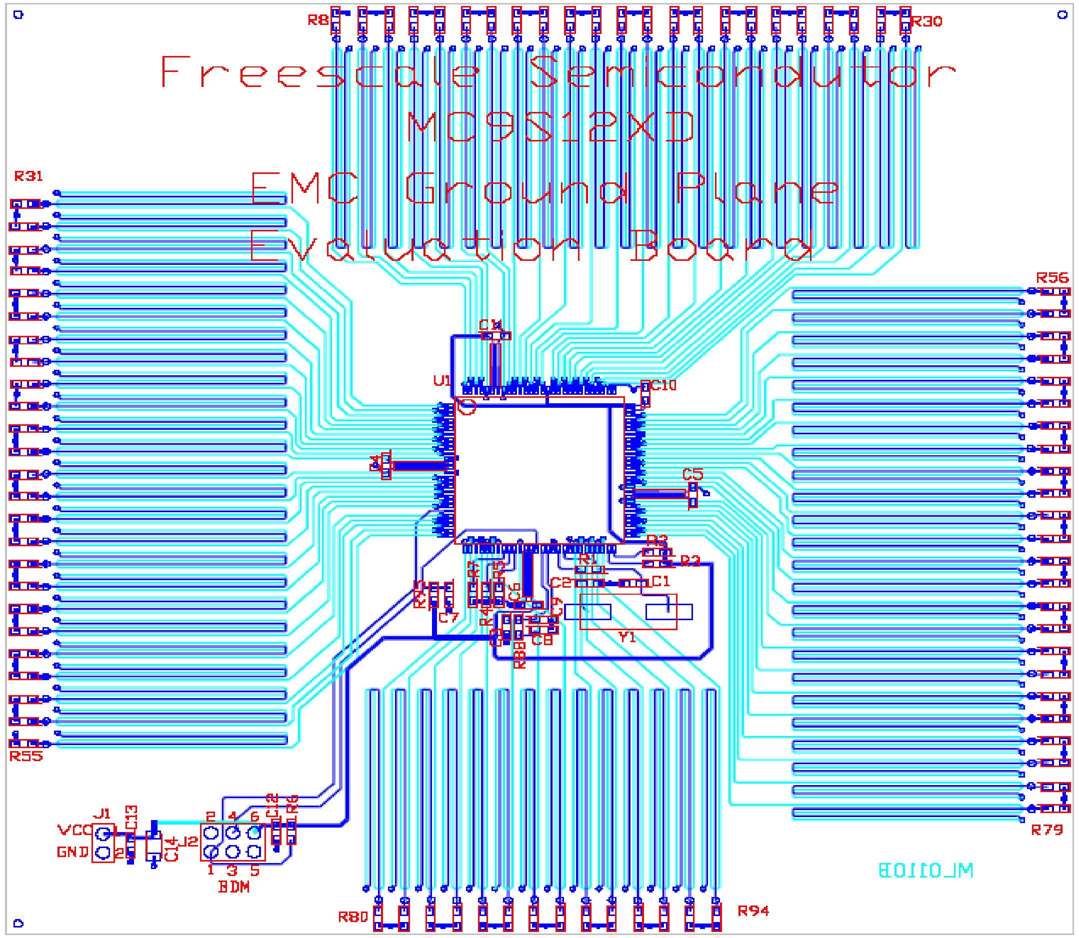
Two-layer EMC Test Board Conducted Emissions



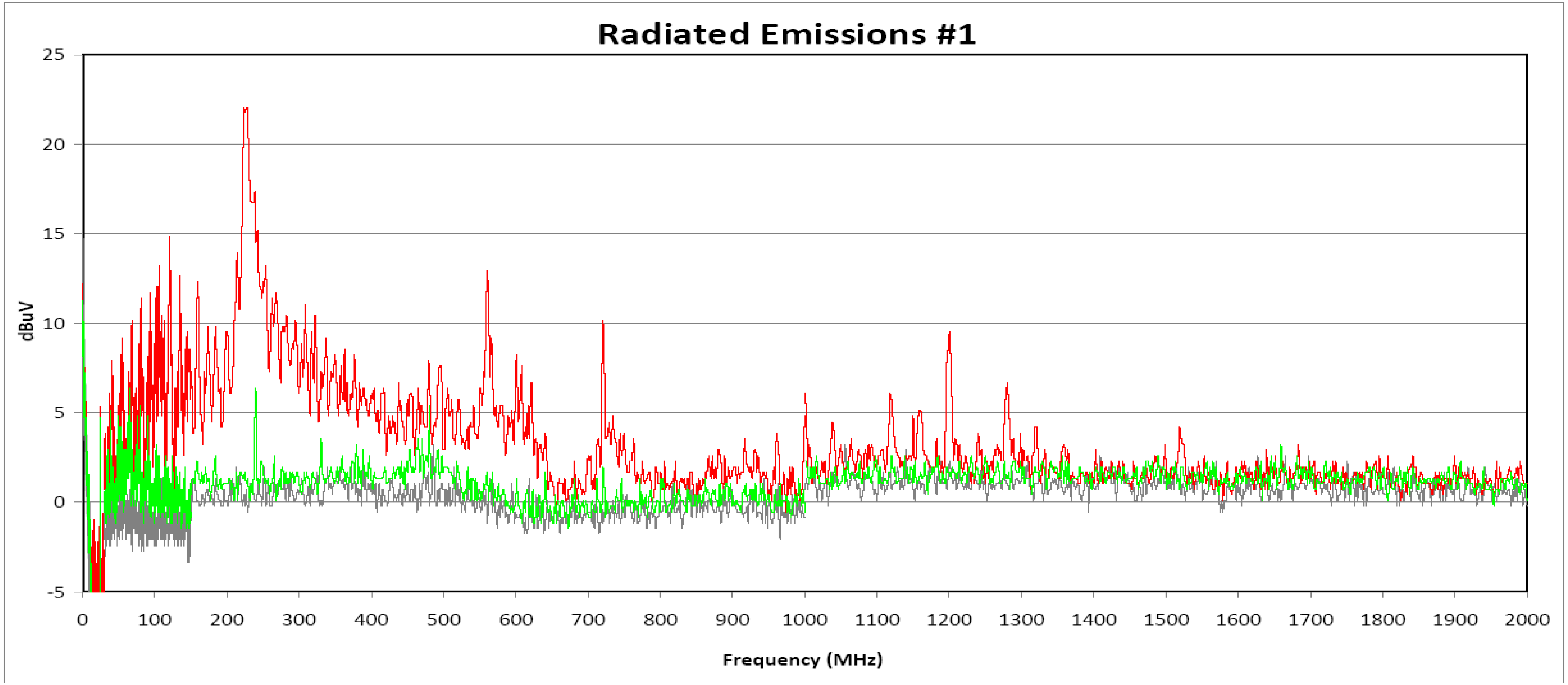
EMC Test Board, Rev 2

- EMC test board with tight field control considered
- Same schematic
- Four layers
- Core inserted with dedicated ground planes
- Outer layers exactly the same as 2 layer
- All ground connections made with via to ground planes
- Line widths and spacing aimed for low-cost FAB
- Same software

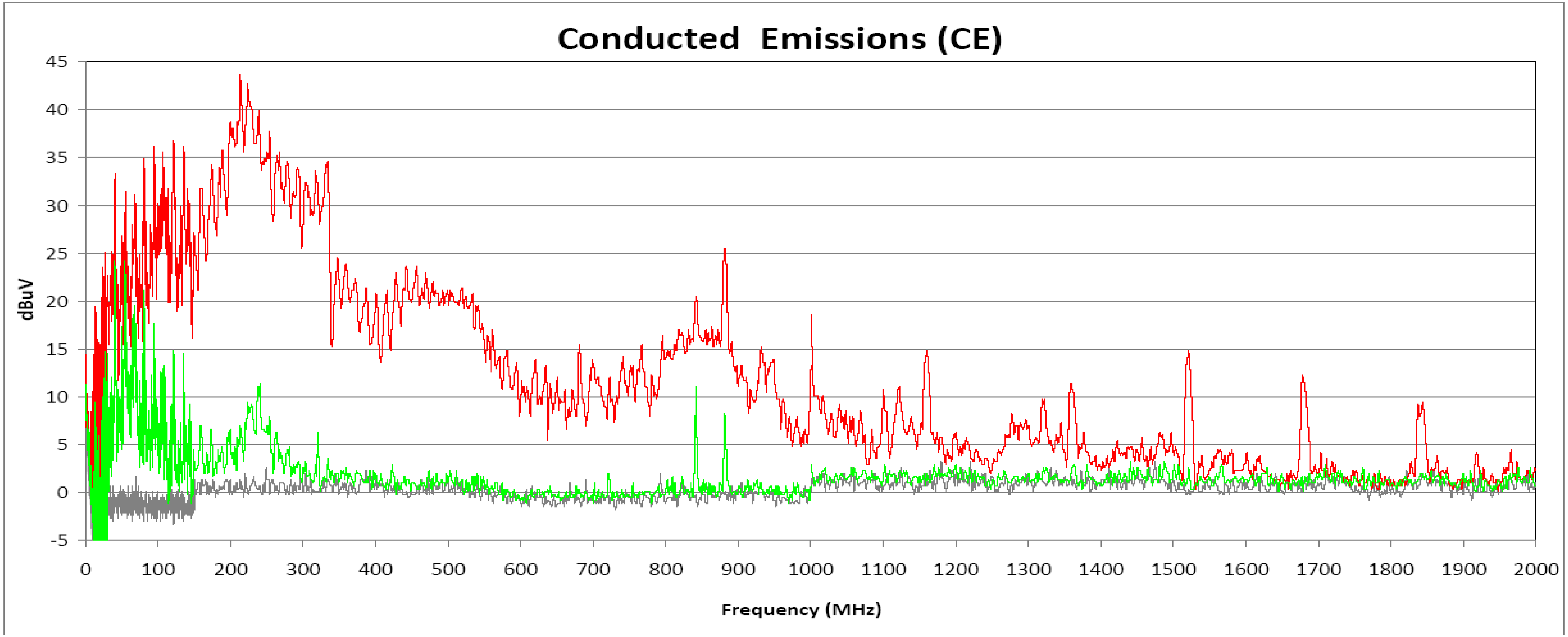
EMC Test Board Layout, Rev 2



2 vs. 4-layer EMC Test Board Radiated Emissions



2 vs. 4-layer EMC Test Board Conducted Emissions



2 vs. 4-layer EMC Test Board Results

WOW! What would you do for 30 db?

Using EMC Test Results

- EMC test results can be used to identify area of concern
- LFBDMPGMR FCC/CE test result first pass:
  - Radiated immunity
  - "The EUT failed with all LEDs turning off. Manual restart worked. The frequencies that caused this fault were 110 MHz, 112 MHz, 134 MHz and 136 MHz up to 149 MHz. After 149 MHz, the EUT worked properly."

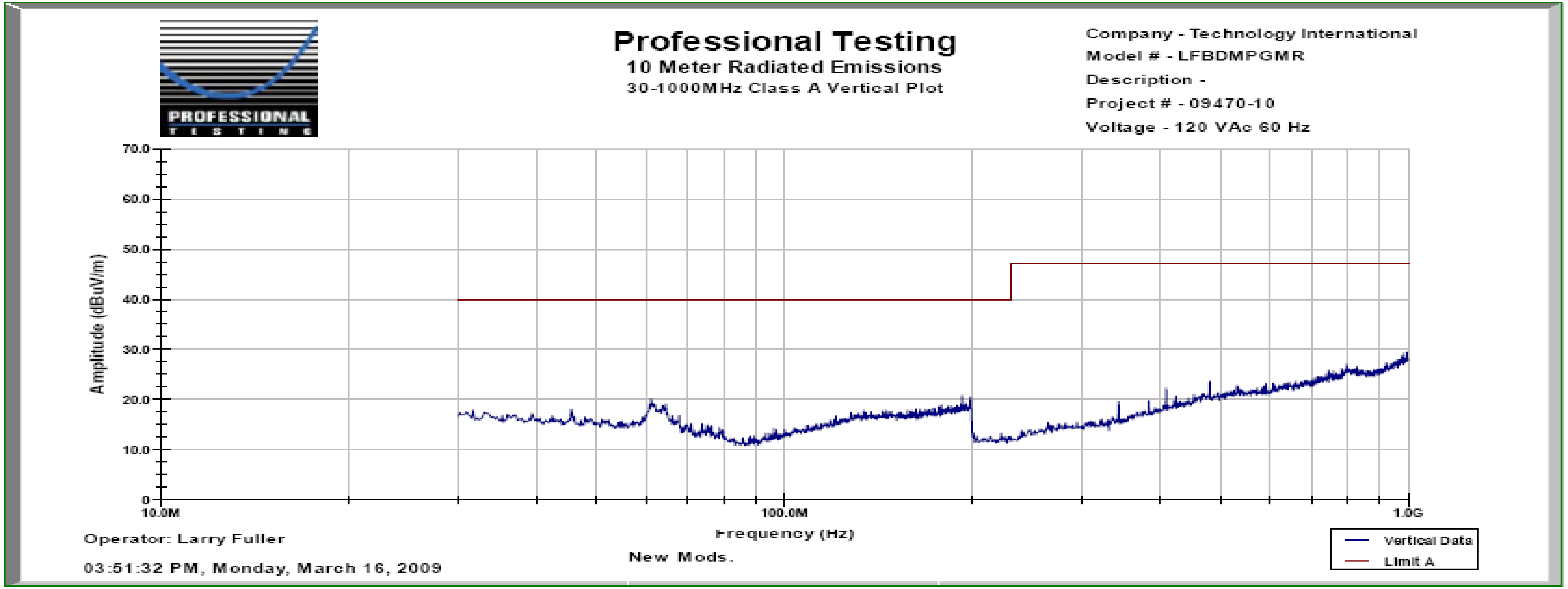
- Not what you want to see in your e-mail.
- This is a four-layer board, the best I know how to design.
- I know, check the chart to see what the ¼ wave length would be.
- About 1 meter, what? My board is only 4 inches square.
- Aha, the USB cable! I forgot to put a filter on the USB power supply. Add a cap quick.
- Send new board for retest.

Using EMC Test Results

Antenna Size vs. Frequency

Frequency	¼ wave length
1 Hertz Rise time equivalent, who cares	246,000,000 feet (46,591 miles) Almost 6 times around the earth
10 Hertz Rise time equivalent, still who cares	24,600,000 feet (4,659 miles) Almost from New York to Honolulu
100 Hertz Rise time equivalent, .01 seconds	2,460,000 feet (466 miles) Almost from New York to Detroit
1 KHz Rise time equivalent, 1 millisecond	246,000 feet (46.6 miles) Almost from Orlando to Cocoa Beach
10 KHz Rise time equivalent, 100 microseconds	24,600 feet (4.659 miles) Almost from the J. W. Marriott to Disney's Magic Kingdom
100 KHz Rise time equivalent, 10 microseconds	2,460 feet (0.466 miles) Almost from the J. W. Marriott to the Central Florida Parkway
1 MHz Rise time equivalent, 1 microsecond	246 feet (0.0466 miles) Less than a football field
10 MHz Rise time equivalent, 100 nanoseconds rise time distance, 100 feet	24.6 feet Across the room
100 MHz (TTL Logic) Rise time equivalent, 10 nanoseconds rise time distance, 10 feet	**2.46 feet Less than a yard**
1 GHz (BiCMOS Logic) Rise time equivalent, 1 nanosecond rise time distance, 1 foot	0.246 feet (2.952 inches) Less than your finger
10 GHz (GaAs Logic) Rise time equivalent, 100 picoseconds rise time distance, 1.2 inches	0.0246 feet (0.2952 inches) Less than the diameter of a pencil
100 GHz (nanometer geometry HCMOS) Rise time equivalent, 10 picoseconds rise time distance, 0.12 inches	0.00246 feet (0.0295 inches) Half the thickness of a standard FR4 PCB

Using EMC Test Results



EMC Test Results, Yeah!

EN 61000-4-3
Radiated Immunity
Technology International
LFBDMPGMR

Test Date: March 13, 2009	**Client: Technology International**
Project #: 09470-10	**Supervisor: Jason Anderson**
EUT: LFBDMPGMR	**Technician: Dan Keenan**

EUT Power Source: 120VAC
Ambient Temperature: 22.6 ° C
Barometric Pressure: 29.97 inches
Relative Humidity: 55 %

EUT Face Illuminated	Frequency Range							
	80-200 MHz 3 V/m		200-1000 MHz 3 V/m		1.4-2.0 GHz V/m		2.0-2.7 GHz V/m	
	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
Front	X	X	X	X				
Right	X	X	X	X				
Rear	X	X	X	X				
Left	X	X	X	X				

Test Results: **Pass** [X] **Fail** [ ]

The EUT met performance criteria:

Criteria A	X
Criteria B	
Criteria C	
Manufacturers Specification	

Notes: The RF signal was modulated with 80% 1000 Hz modulation. The frequency step size was 1% of the preceding frequency. The dwell time at each frequency was 2 seconds.

New Rules of Thumb

PC Board Considerations

Flooding unused spaces on the PCB:

- Properly implemented, will improve EMC performance
- Reduce cost by increasing PCB manufacturing yield
  - Less etch required
  - Balanced copper improves plating
  - Balanced copper improves final assembly
    - Reduced board warping
- Remember to stitch the ground islands and planes together
- Try to make a pseudo-Faraday cage!

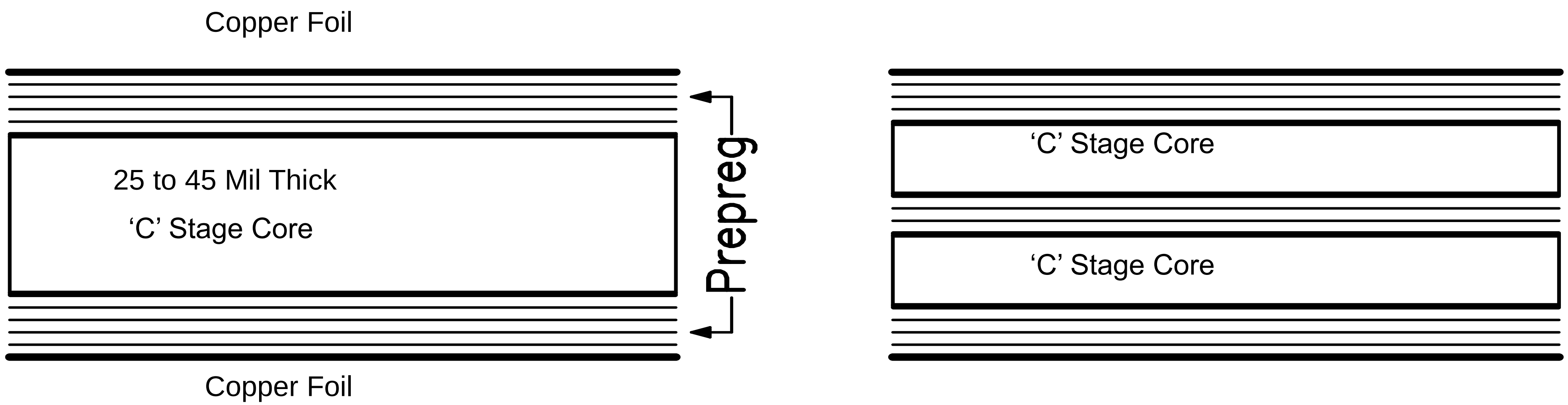
More PC Board Considerations

Use minimum trace widths and spacing for signal transmission lines

- Refer to PCB fabricator’s capabilities without a cost adder
- Same thing goes for drill sizes and pad rings
- May be defined by either customer or internal requirements
- Wider traces for power supply transmission line pairs
- Provides maximum trace density

- Make room for all of those ground traces!

More PC Board Considerations



Most PC boards are "foil laminated"

(Slide compliments of Rick Hartley, Consultant)

More PC Board Considerations

- Made from a two-layer core, L2 and L3
- L1 and L4 made by adding pre-preg layers and copper foil
- Use the “fattest” core and “thinnest” pre-preg possible without a cost adder from fabricator
  - You will have to find this out
  - Your company or customer may have some min-max specs for these materials
- Maximum coupling is from L1 to L2 and from L3 to L4

Four-Layer Boards

- Most effective stackup has one ground layer
- L2 ground means that L1 and L3 are one dielectric from ground
- L4 must be routed as a single layer board, with following ground traces (triplets?)
- Ground transition vias are required when signals go from layer 4 to any other layer to insure the transmission line is continuous

Six-Layer Boards

- Most effective stackup has two ground layers
- L2 as ground means that L1 and L3 are one dielectric from ground
- L5 as ground means that L4 and L6 are one dielectric from ground
- Ground transition vias are required when signals go from one ground reference group (L1-L2-L3 or L4-L5-L6) to any other layer in the other group) to insure the transmission line is continuous

Layer Count Determinations

- Technology of the devices used
- Trace density
- EMC certification level
  - Consumer/commercial
  - Automotive
  - Aviation
  - Military
- All must be considered, not just trace density!

Layer Count Determinations

- Must be a conscious decision based on proper electromagnetic field control
- Not just because you ran out of routing paths
- Smaller IC geometries will require more layers and most likely power and ground planes
- It will not be possible to provide a good power distribution network or good signal integrity without adding planes

- System cost is *not* reduced by reducing IC geometries!

Effective PCB Design: Techniques to Improve Performance

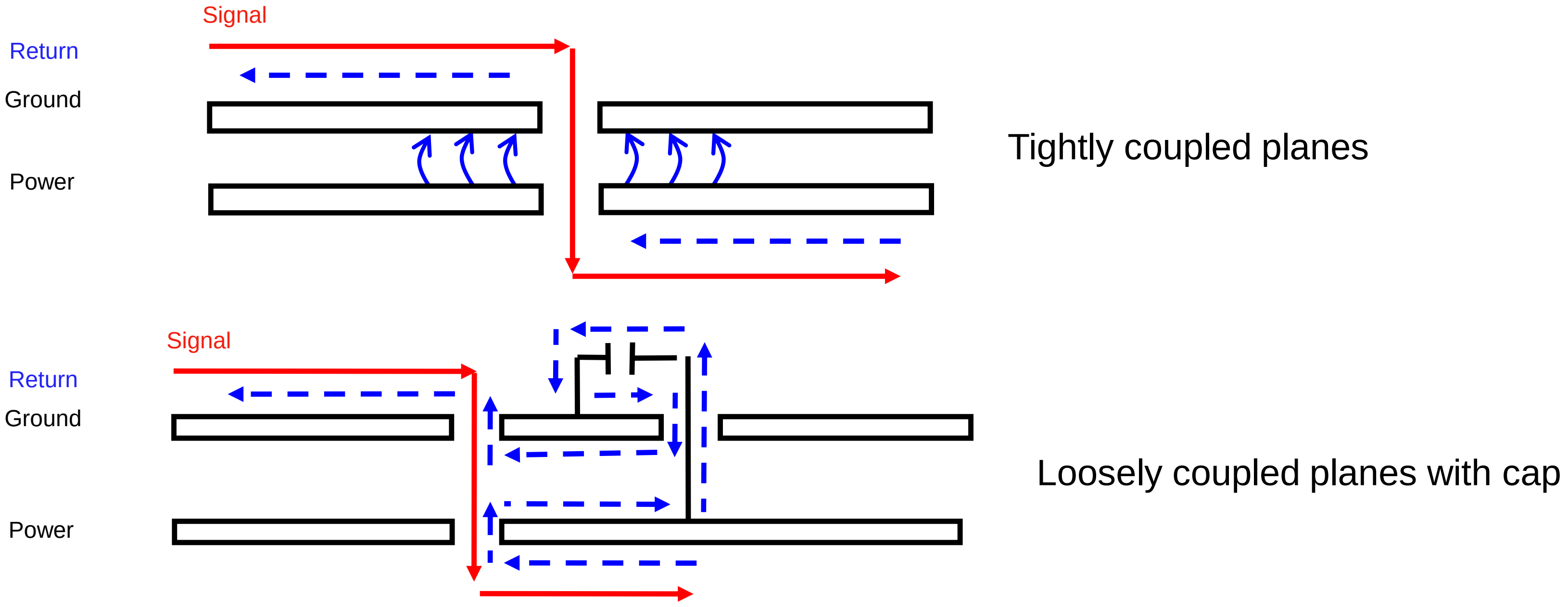
I repeat: **System cost is not reduced by reducing IC geometries!**

Using Planes

- Both power and ground can be used as signal references
- Transition from one reference plane to another requires close proximity to a bypass capacitor
- That is the only way the field can move!
- Only if they are well coupled to each other
- Using Capacitors
  - Impedance is less than 0.1 ohm
- Planes adjacent to each other
  - Dielectric thickness less than 10 mils
- No matter what, each transition from ground reference to power reference and back represents a discontinuity that causes distortion to the signal.
- If you don’t have to, don’t!!
- Never mind, just don’t do it!!

Using Planes

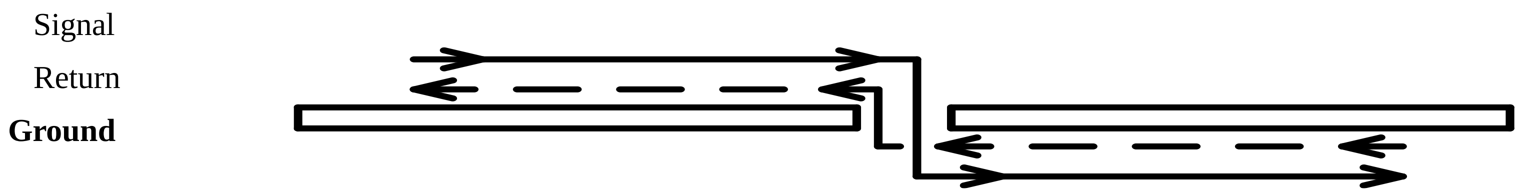
When routing signals with returns between power and ground planes, return energy will transfer as follows:



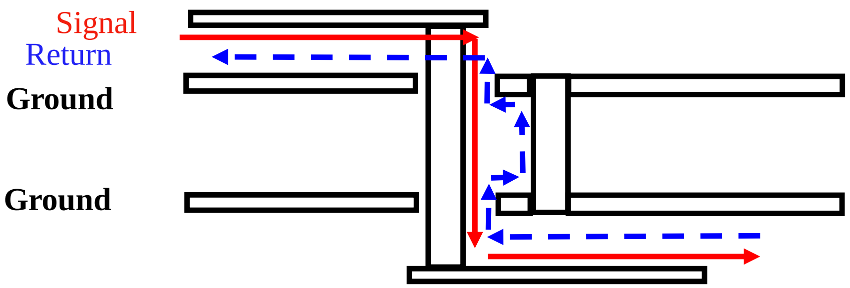
(Slide compliments of Rick Hartley, Consultant)

Using Planes

When moving signals *between layers*, route on either side of the same plane, as much as possible!



When moving signals *between two different planes*, use a transfer or "ground transition" via very near the signal via.



(Slide compliments of Rick Hartley, Consultant)

Using Planes

- Remember, field energy moves in the space between or around the conductors and cannot go through them[1]
  - That means through the holes in the planes – not inside or on the vias, around them!

- You must provide the path you want, or the field will find its own path
  - It will most likely be the one that causes the most problems!

[1] Statement compliments of Ralph Morrison, Consultant

Splitting Ground Planes

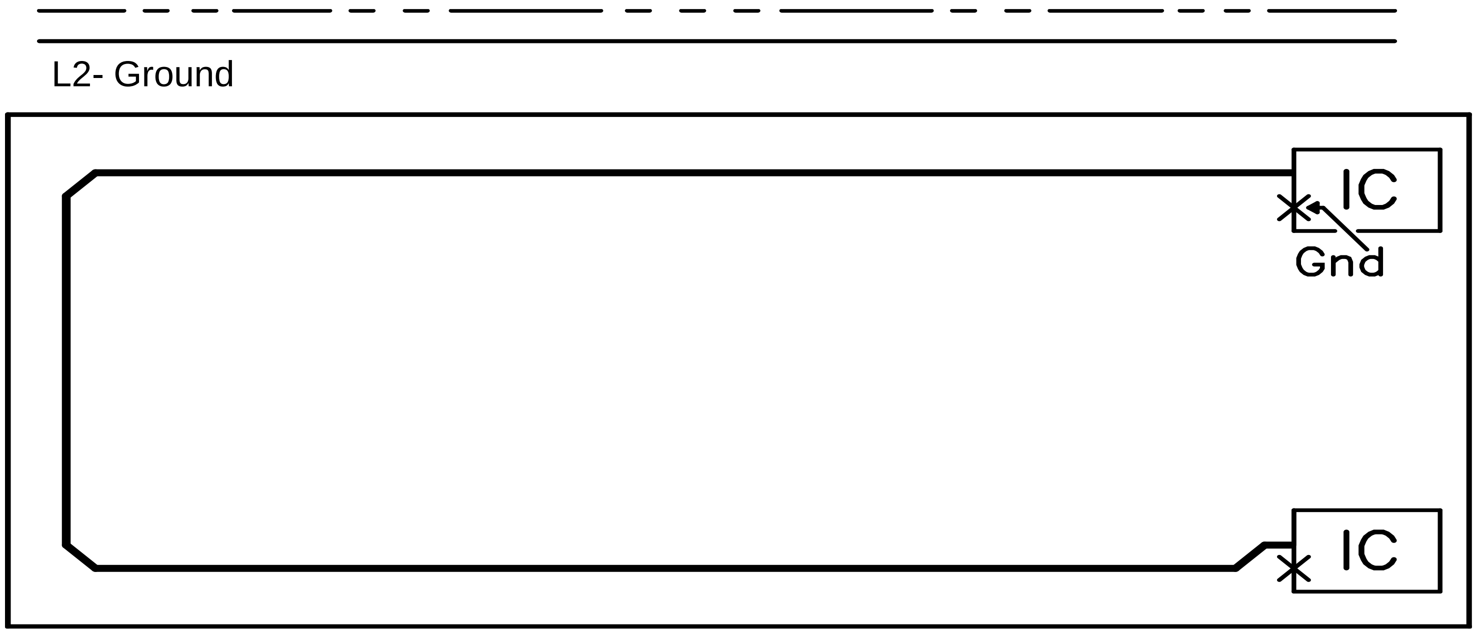
- Splitting ground planes is almost never a good idea
- Only when required by customer or internal specifications
- Question those requirements!

- If you have to split a plane, do not route traces across the split!
- If you must, then you absolutely have to route a following ground trace across the split next to the signal trace

- Splits in planes are very efficient slot antennas!

Splitting Ground Planes

Two-layer Microwave Style PC Board



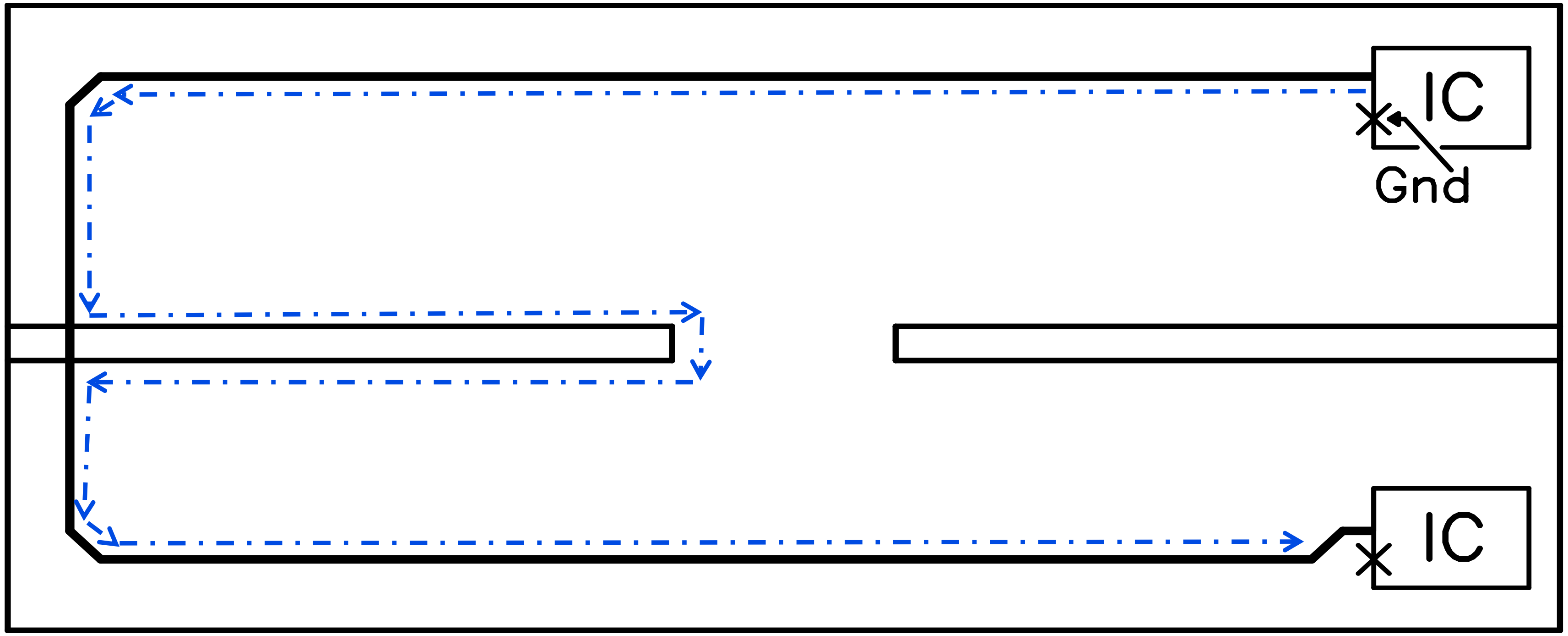
Where does signal's return current flow?

(Slide compliments of Rick Hartley, Consultant)

Splitting Ground Planes

What happens if return plane is split?

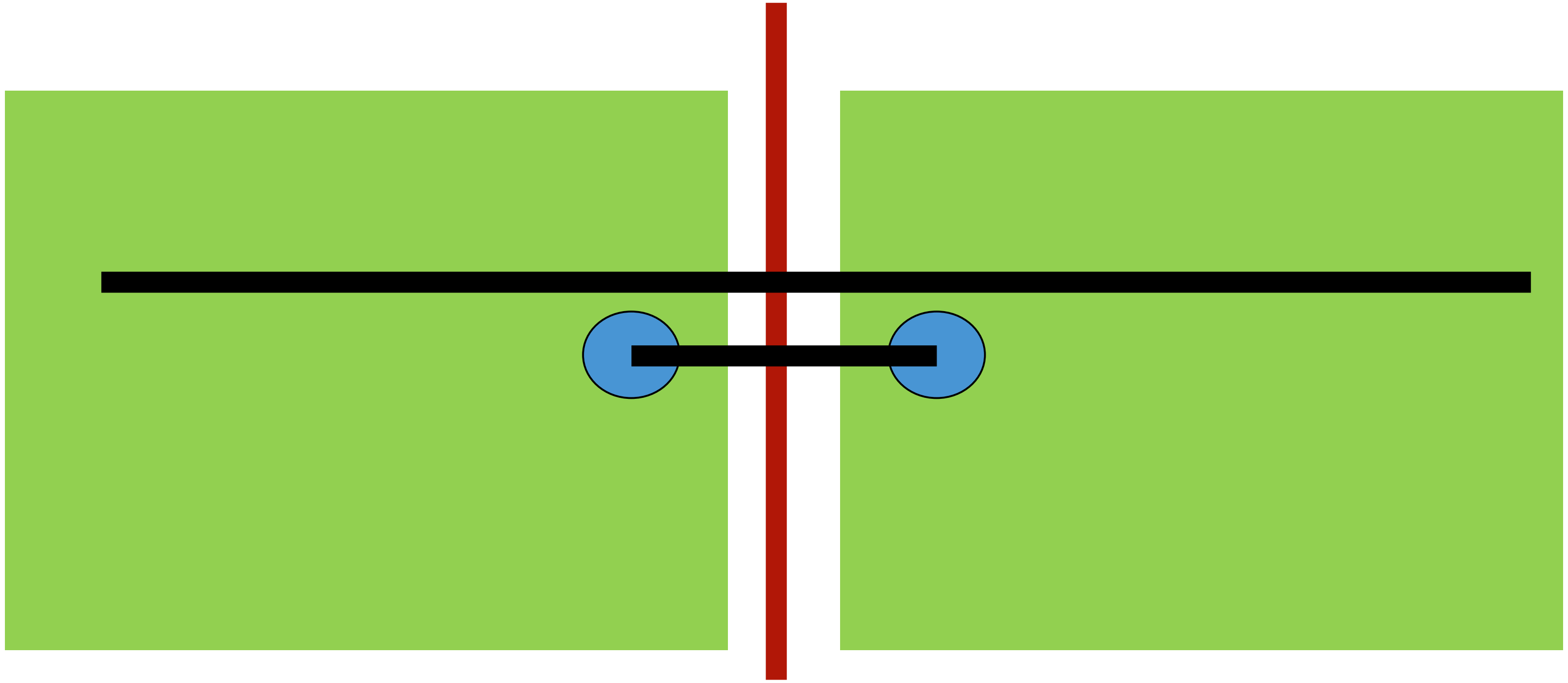
Now where does return current flow?



(Slide compliments of Rick Hartley, Consultant)

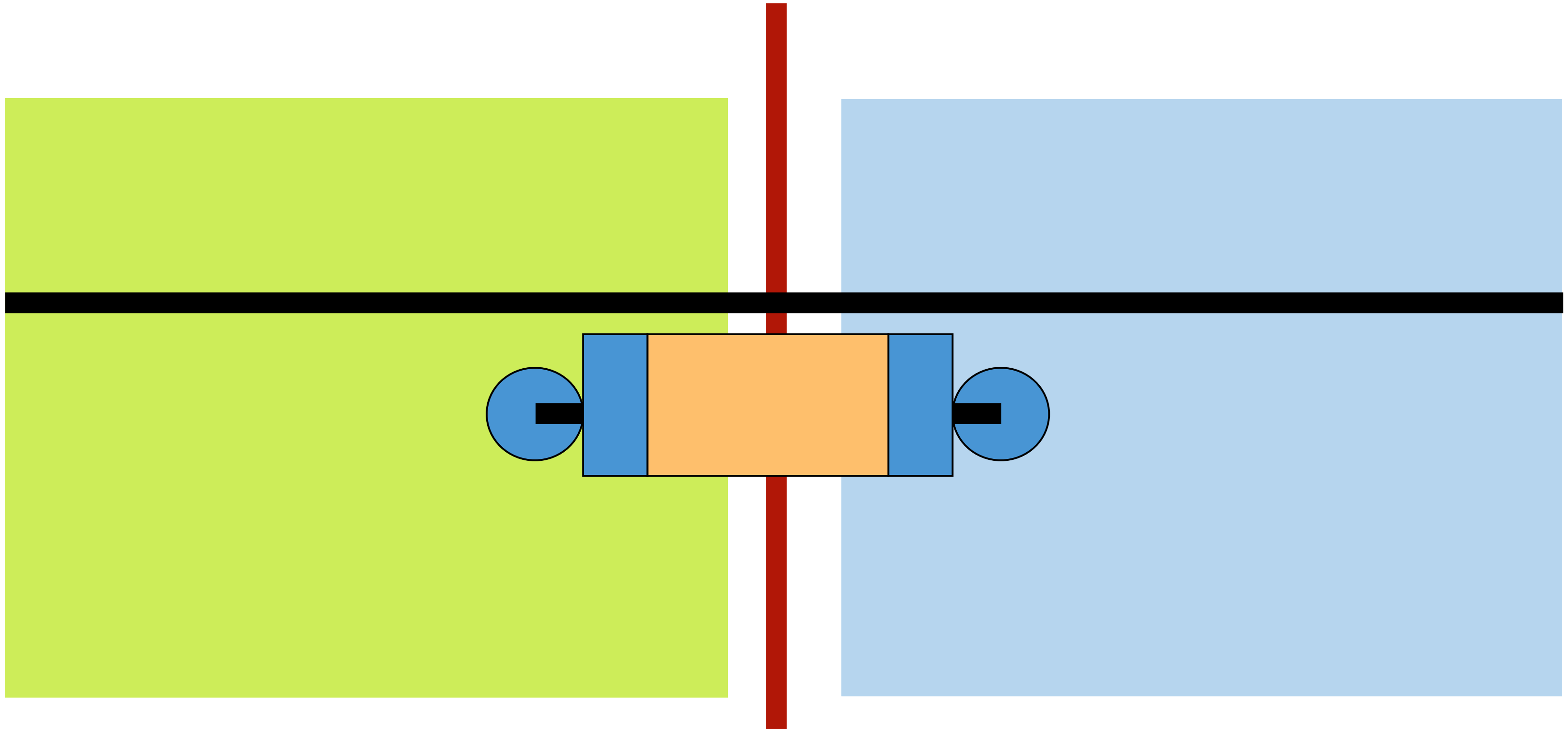
Splitting Ground Planes

- Routing over split planes, same potential
- Just use a bridge tied to each plane
- Better to just not split it, but sometimes you have to route a trace in the split



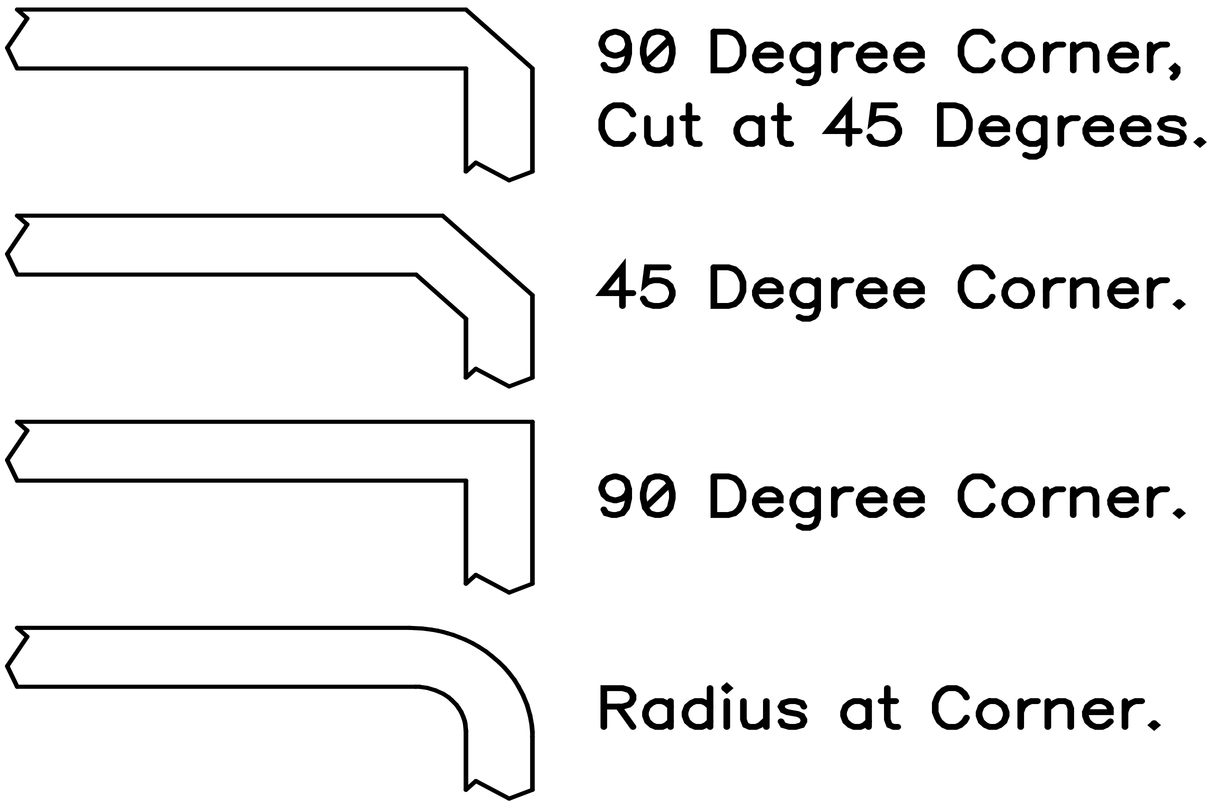
Splitting Ground Planes

Routing over split planes, different potential
You have to bridge with a capacitor



PCB Trace Corners

Which of these
is best?



(Slide compliments of Rick Hartley, Consultant)

PCB Trace Corners

- These small discontinuities are virtually invisible for all applications in the foreseeable future
- The best one is the 45 degree because it is easier to manufacture and easier to draw
- The 90-degree choices tend to be victims of under or over etching, and can form failure points in the future, as well as impacting PCB yields
- The radius is good, but most CAD packages do not support this option

Routing Differential Signals

- Myth: They are coupled to each other
- Differential signals are referenced to each other only when twisted pair wiring is used, NOT on PCBs
- Fact: They are coupled to ground
- Each driver power source is coupled to ground, hence the outputs must be coupled to ground
- They do not have to be routed together
- They do need to be about the same length
- They do need to be treated as transmission lines
  - (You knew I was going to say that, didn't you?)
- They would benefit from being routed as a "triplet"
- Designed to reject common mode noise
- Not possible on PCBs, since there is no way to subject both signals to the same interference by twisting)

Routing Timing-Critical Bus Signals

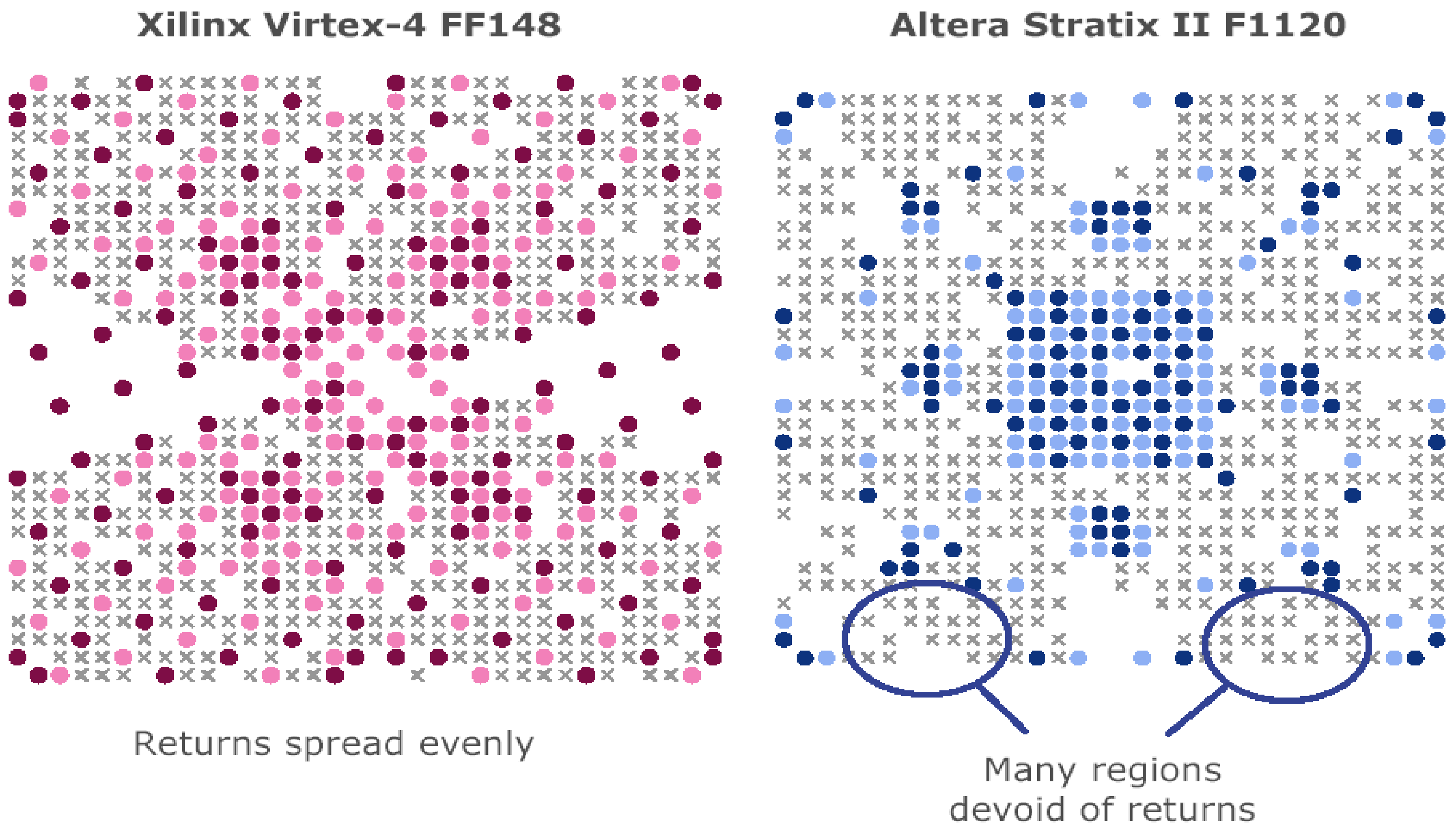
- Myth: They have to be exactly the same length
- Manufacturers often spec allowable trace length differential
- PCB designers spend a lot of time and energy to do this using serpentines and other extreme routing methods
- At high frequency, the serpentines are invisible anyway, and actually result in shorter travel times
- Fact: What matters is the set up and hold time required by the devices
  - This is usually specified in time (ps)
- Remember this? v = 150 mm / ns or 6” / ns
- For a typical 500 MHz DDR memory interface, the data lines only need to be within 500 mils of each other in length

- Way easier than we have been led to believe

Signal Return Path BGA Design

Return Path equally important in IC Package.

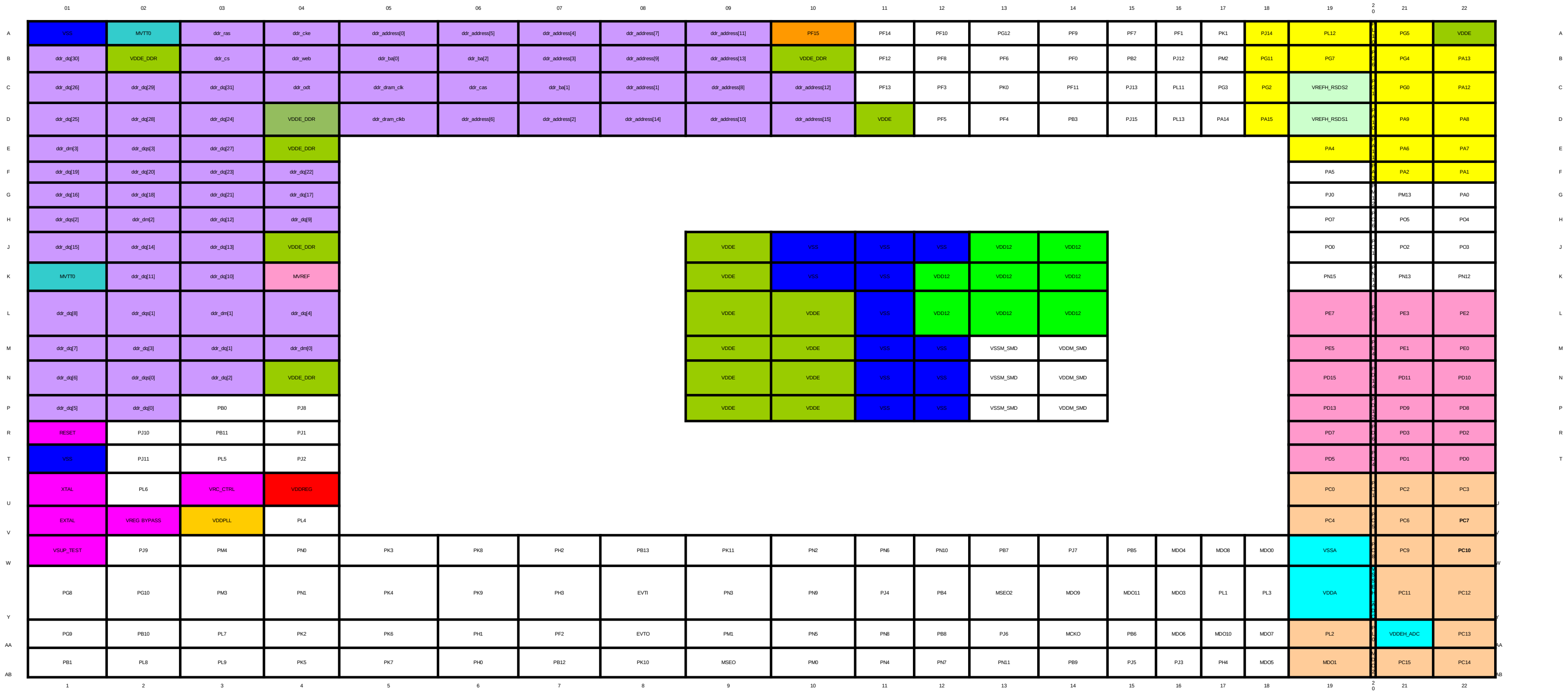
F1120 had 5X greater noise level than FF148



Source: BGA Crosstalk - Dr. Howard Johnson

Signal Return Path BGA Design

Rainbow 324 BGA

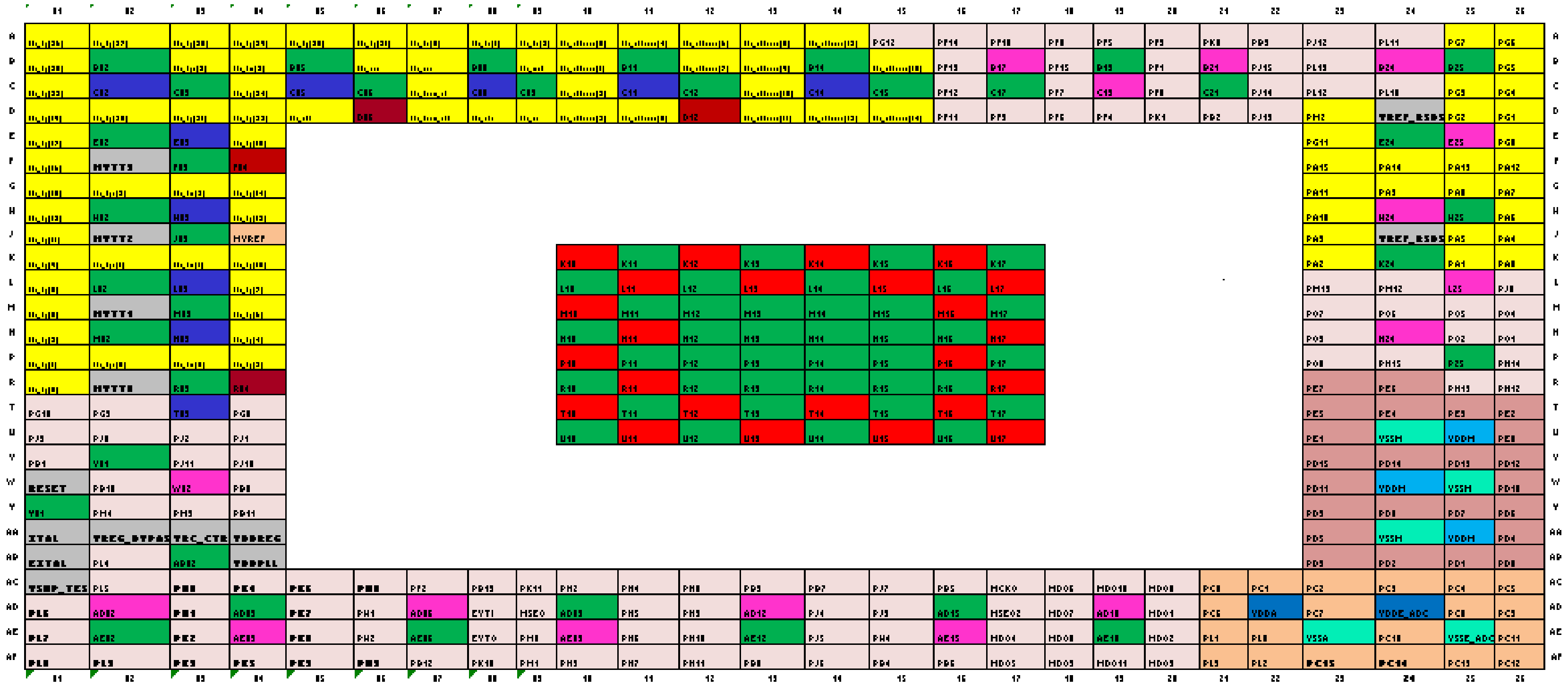


Only 14 **VSS (blue) pins**, but package met original marketing price target.

Significant issues with signal integrity and EMC. Notice, only one VSS for then entire DDR interface.

Signal Return Path BGA Design

Rainbow 416 BGA



Began as 324 pins …is now 416 pins!
Worked with customer to discuss need for larger package with more pins.
Used a mixture of 3x3 grids with center pin **VSS (green)** for outer balls and checkerboard approach to center power balls

Closing Remarks and Reference Materials

PCB Design is Not a Black Art!

Fundamentals to Remember

- Electromagnetic fields travel in the space between the conductors, not in the conductors
- The switching speed of the transistors determines the frequency of operation, not the clock rate
- Signal and power connections need to be one dielectric from ground for their entire length (including layer transitions)
  - Adjacent plane
  - Co-planar trace
- In a 4-layer design, if one layer is a ground plane, the two adjacent layers are one dielectric from ground.
- The 4th layer must be routed as if it were a single layer board.
- There is no such thing as a noisy ground, just poor transmission line design
- To quote Dr. Todd Hubing, “Thou shalt not split ground.”
- Any compromises to these rules will increase system noise and must be done as carefully considered engineering decisions.

Special Thanks to My Mentors

- Rick Hartley (PCB designer extraordinaire) started me down this trail in 2004 at PCB West
- Ralph Morrison (author, inventor and musician) has patiently and steadily moved me from the fuzzy realm of “circuit theory” and “black magic” into the solid world of physics.
- Dr. Todd Hubing (researcher and professor) whose research at UMR and Clemson has provided solid evidence that Maxwell and Ralph have got it right.

High Speed Design Reading List

- Right the First Time: A Practical Handbook on High Speed PCB and System Design Volumes I & II, Lee W. Ritchey. Speeding Edge, ISBN 0-9741936-0-7
- High Speed Digital System Design: A Handbook of Interconnect Theory and Practice, Hall, Hall and McCall. Wiley Interscience 2000, ISBN 0-36090-2
- High Speed Digital Design: A Handbook of Black Magic, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-395724-1
- High Speed Signal Propagation: Advanced Black Magic, Howard W. Johnson & Martin Graham. Prentice Hall, ISBN 0-13-084408-X
- Signal Integrity Simplified, Eric Bogatin. Prentice Hall, ISBN 0-13-066946-6
- Signal Integrity Issues and Printed Circuit Design, Doug Brooks. Prentice Hall, ISBN 0-13-141884-X

(Slide compliments of Rick Hartley, Consultant)

EMI Reading List

- PCB Design for Real-World EMI Control, Bruce R. Archambeault. Kluwer Academic Publishers Group, ISBN 1-4020-7130-2
- Digital Design for Interference Specifications: A Practical Handbook for EMI Suppression, David L. Terrell & R. Kenneth Keenan. Newnes Publishing, ISBN 0-7506-7282-X
- Noise Reduction Techniques in Electronic Systems, 2nd Edition, Henry Ott. John Wiley and Sons, ISBN 0-471-85068-3
- Introduction to Electromagnetic Compatibility, Clayton R. Paul. John Wiley and Sons, ISBN 0-471-54927-4
- EMC for Product Engineers, Tim Williams. Newnes Publishing. ISBN 0-7506-2466-3
- Grounding & Shielding Techniques, 5th Edition, Ralph Morrison. John Wiley & Sons, ISBN 0-471-24518-6

(Slide compliments of Rick Hartley, Consultant)

Additional References

- Ralph Morrison’s Books, Available from Wiley and Amazon:
  - Digital Circuit Boards: Mach 1 GHz.
  - Fast Circuit Boards: Energy Management.
- The Best PCB design conference website: http://pcbwest.com/
- Doug Smith’s website: http://www.emcesd.com/ (He is the best at finding what is wrong! Lots of useful app notes.)
- IEEE EMC Society website: http://www.emcs.org/
- Clemson’s Automotive Electronics website: http://www.cvel.clemson.edu/auto
- Clemson’s EMC website: http://www.cvel.clemson.edu/emc
- Missouri University of Science and Technology website: http://www.mst.edu/about/
- IPC — Association Connecting Electronics Industries website: http://www.ipc.org/default.aspx

It’s All About the **Space**!

“Buildings have walls and halls.

People travel in the halls not the walls.

Circuits have traces and **spaces**.

Energy and signals travel in the **spaces** not the traces.”

- Ralph Morrison

Summary and Q&A

- Well-defined transmission lines result in significantly improved EMC performance
- Careful routing of transmission lines can result in behavior similar to that gained by adding extra PCB ground layers
- Evaluating test results can lead you to solutions
- The *black magic* is tamed!
- Q&A

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