Applications for High-Performance Layerscape Processors

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Strategic Marketing

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SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- About the LX2160A Processor
- LX2160A Applications
- Getting Started
- Conclusion

The LX2160A Value Proposition

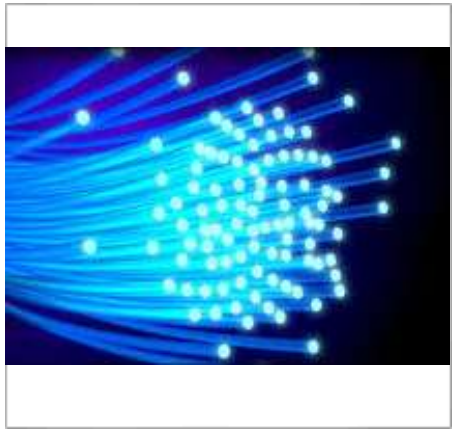
High Performance Processing

- 16x A72 Arm v8 64 cores
- 224k CoreMark
- 143 SpecInt-2006 Rate, similar to an Intel Xeon D-1548
- 100Mpps DPDK forwarding

Advanced Networking accelerators

- Security engine
  - 50Gbps IPSEC
  - 30Gbps elephant flow
- Data compression engine
  - 50G compress
  - 50Gbps decompress

High Bandwidth IO

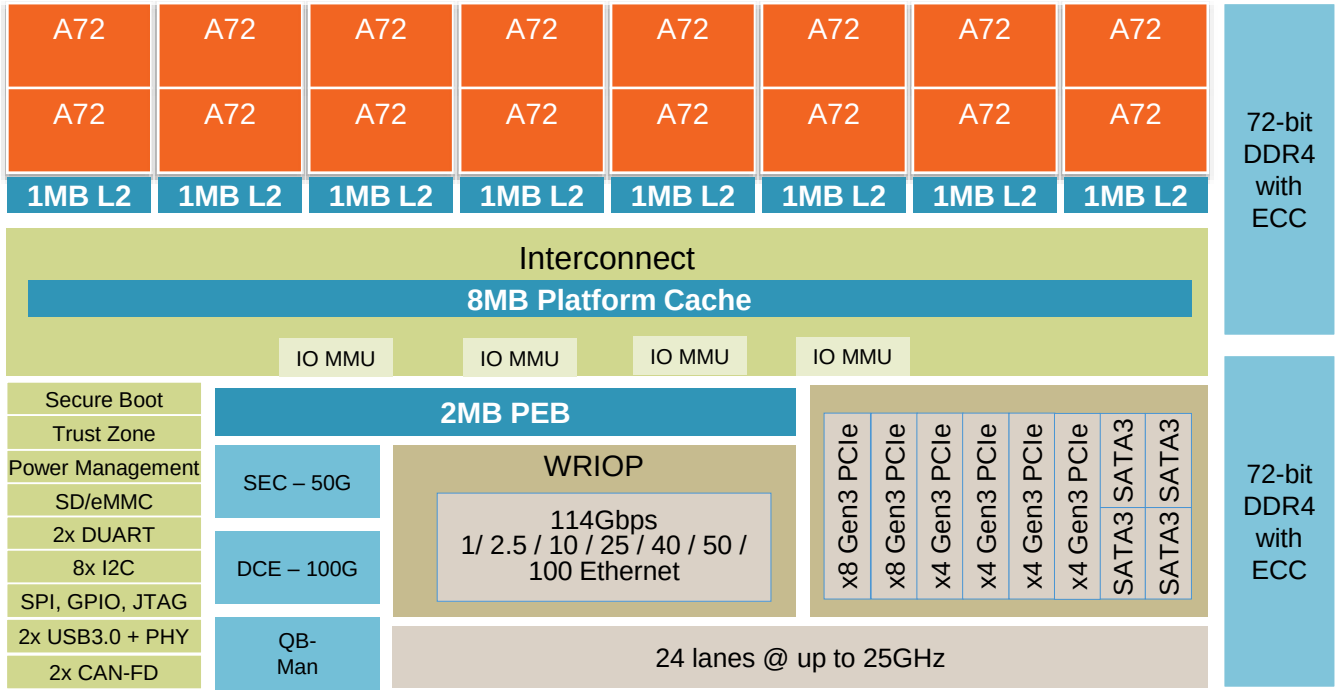


- 24 SerDes lanes to 25GHz
- Dual 100GE ports
- Supports 50GE, 40GE, 25GE, 10GE, 2.5GE and 1GE

Low FinFET Power

- FinFET process technology greatly reduces leakage current
- 25W TPD at 105C, 2.0GHz, 16-core
- 11W TDP at 65C, 1.8GHz, 8-core

LX2160A Block Diagram and Key Features



General Purpose Processing Layer

- 16 ARMv8.0 A72 CPUs, 64b, 2.2GHz
  - 1MB L2 cache / cluster
  - 8 Clusters
- Neon SIMD in all CPUs
- 700MHz Interconnect

Memory

- 2x72b (including ECC) DDR4 up to 3.2GT/s, up to 256GB total capacity
- 8MB Platform Cache
- 2MB packet buffer (PEB)

Accelerated Packet Processing

- QMan for QoS
- 50Gb/s SEC
- 100Gb/s Data Compression Engine (50 Compress + 50 Decompress)

Device

- 16nm FinFET Compact
- 40 x 40 mm, 1mm pitch, 1517 pins
- 25W VDD (thermal) at 105C at 2.0GHz
- AEC-Q100 Grade 3 reliability stresses

Network IO

Wire Rate IO Processor:

- L2 switch with 1G, 2.5G, 10G, 25G, 40G, 50G, 100G
- MACSec on 4x 10GE
- Priority Flow Control (802.1Qbb)
- 1588 timestamping, SyncE
- 2x RGMII

High Speed Serial IO

- 6x PCIe Gen3 controllers
  - x8, x8, x4, x4, x4, x4 Gen3
  - 2 with SR-IOV
- 2x USB 3.0 with PHY
- 24 SerDes lanes: 8 up to 25GHz and 16 up to 16GHz
- 4x SATA3

Performance Projections

Benchmark	T4240-1800	LS2084-2000	LX2160-2200	Comment
Dhrystone / core[1] / MHz	3.64	6.19	6.19[4]	Measured on silicon
Composite CoreMark (gcc 5.1.1 with flag mining)	187,873[2]	101,760	224,000[4]	Measured on silicon
SPECint2006 (gcc 4.9.3 with loop unrolling)	6.9[3]	13.8	13.8[4]	For gcc compilation[5]
SPECint2006-Rate (gcc 4.9.3 with loop unrolling)	109[3]	82.4	143[4]	For gcc compilation[5]
DPDK Forwarding		40Mpps	104Mpps	64B packets
IPSEC	27Gbps	20Gbps[6]	50Gbps	1440B packets (iMIX for LS2)
QDMA transfer rate			36Mpps	

[1] For T4, “core” means one thread of the dual-threaded e6500
[2] Green Hills Multi 6.1.4 Compiler v2013.5.0
[3] gcc-4.7.3, 1667MHz
[4] Estimated
[5] more real-world than Intel’s ICC compiler that optimizes code for SpecInt
[6] IMIX, using AIOP

Target Market Segments: LX2160A Family of SoCs

5G base stations

- 50Gbps IPSEC for transport
- LTE air crypto for PDCP
- 30Gbps elephant flow
- Commercial grade transport and PDCP software available

Industrial

- 15 year product longevity
- 10 year operating life
- -40 to 105C junction temp range
- Neon vector engine
- COM Express Type7 board available

Datacenter: storage and NIC

- 24 SerDes lanes of PCIe Gen3
- Two x8 PCIe Gen3
- Common 25G, 100GE network connections
- 100Gbps data compression engine
- Two NIC board avail

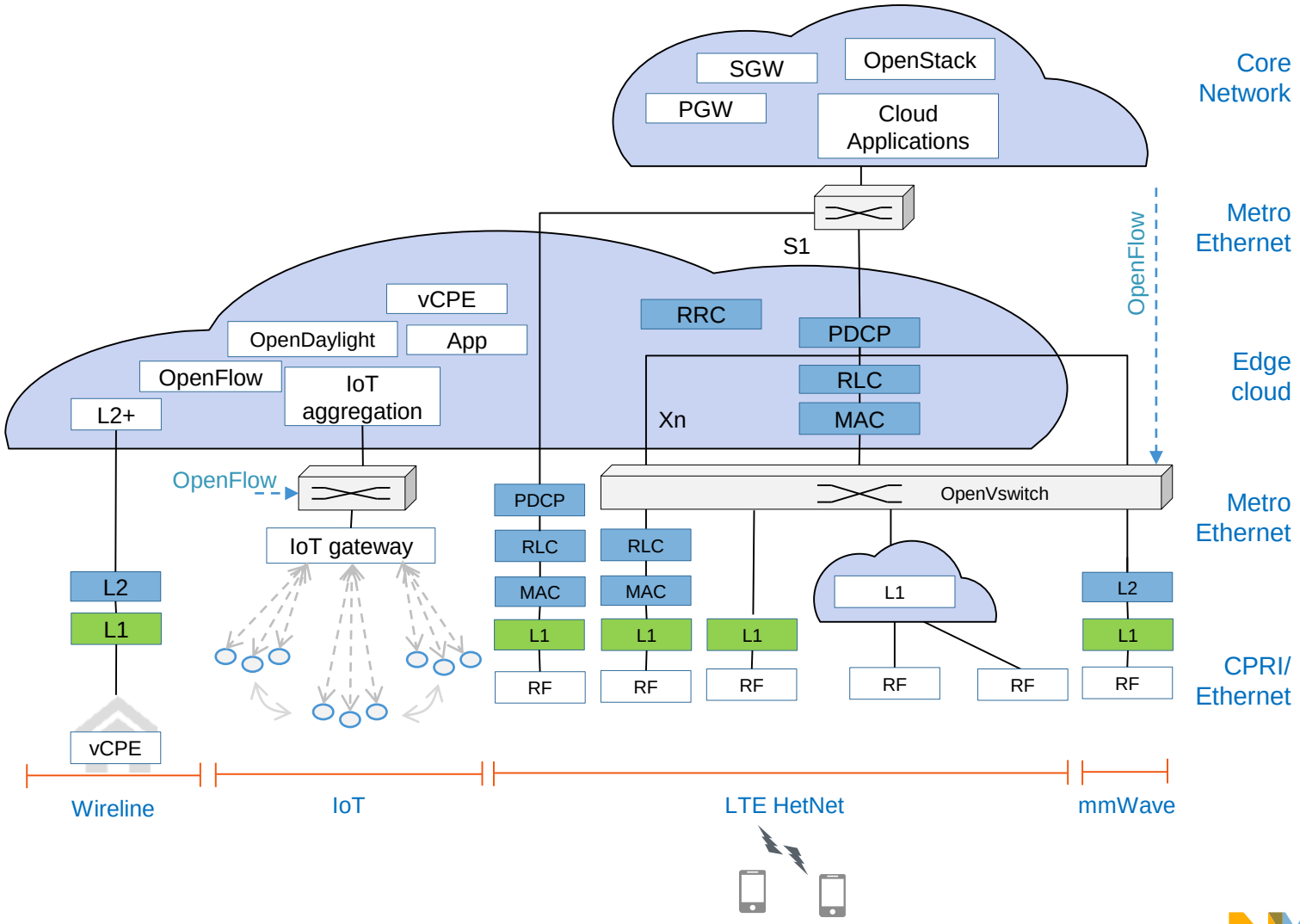
Edge Computing

- Hosts virtual machines on 16 high perf cores
- KVM, QEMU, libvert, Docker
- Accelerated direct access to IO from VMs
- Accelerated VM-VM communications

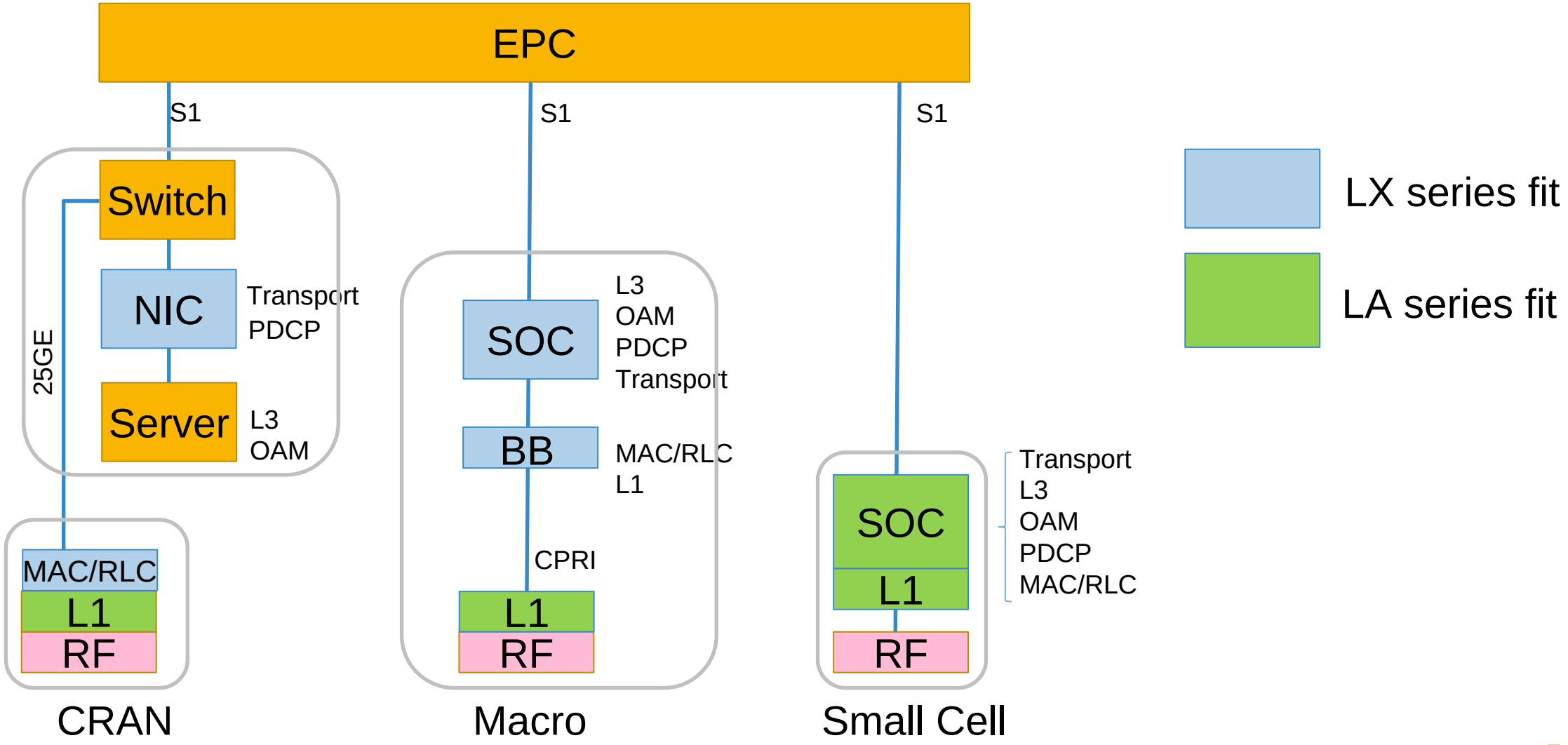
5G Packet Processing

Next Generation / 5G Network Architecture

- Split architecture network
  - Centralization of higher layers
  - Multi-standard access drives virtualization
- Standards based orchestration
  - SDN based network automation
  - NFV for machine management
- Implications to SoC and SW
  - Common ISA (ARM64)
  - Open software (Linux, KVM)
  - SDN API adaptation
  - Scalability and SW stack disaggregation



5G Configurations



LX2160A 5G Performance

- Transport (IPSec + GTP): 50Gbps
- PDCP: 50Gbps

Industrial

Why LX2160A in Industrial and Mil/Aero?

- Advantageous cost/performance and power/performance
- 10GbE/25GbE for backplane interconnect
- Copious PCIe to connect to FPGAs, ASICs, etc.
- NXP has a proven track record in mission-critical and industrial applications
- Good fit for industrial PCs and embedded boards (e.g., ComExpress Type 7)
- Real-time Linux support

NXP Processors in Mission Critical Applications

Aerospace

Fuel Management, Main Flight Control, Secondary Flight Control, Aircraft Engine Management, Cockpit Display

Military and Defense

Rocket navigation, Artillery Control Computer, IFF

IFF, UAV Flight Computer, Defense Airborne Computer, Weapon Navigation System, Ground Control System

Factory Automation

Robotics Controllers, Motion Controllers, Multi-Axis Motor Controllers, Safety PLCs, HMI, Scanners, Gateways

Railway

Traction Control, Railway Signaling Controller, Railway Communications, Brake Controller, Control Panels, Passenger Panels

Power Grid

Power Distribution Relays, Smart Grid Communications, Smart Meters

Extreme Operating Conditions

10 Year

Continuous operation at high temperature

- Product Life Application Notes
- Extreme temperature conditions
  - -40º C cold start option
  - 70-85º C ambient operating conditions
  - Up to 125º C junction temperature*
- Low power consumption for fanless designs*
- Small footprint for space-constrained designs*

*not supported by LX2160A

Supply Longevity

Industrial applications require product longevity

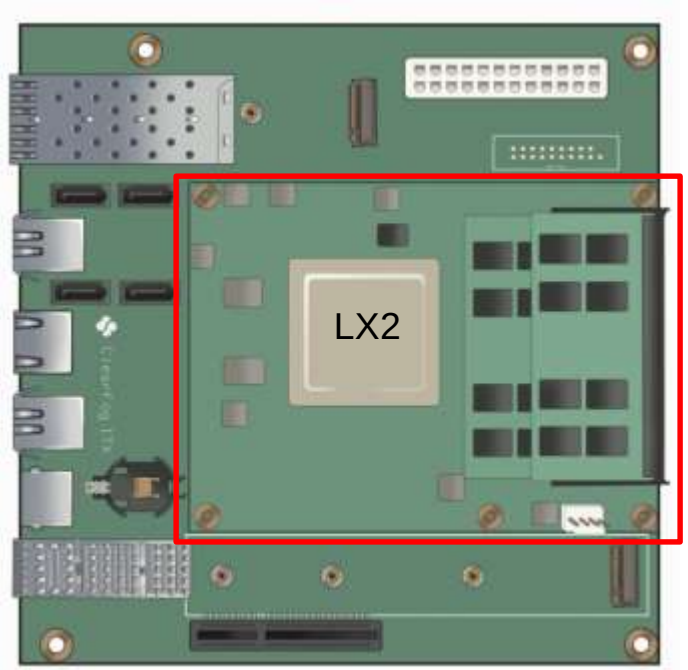
- Long product lifecycles
- Special product certification required

NXP Industrial Application Processors

- 10 and 15 year supply longevity options
- Formal program with products listed at www.nxp.com/productlongevity

SolidRun

- Com Express Type 7
- $550 - $750



phoronix

ARTICLES & REVIEWS NEWS ARCHIVE FORUMS PREMIUM CATEGORIES

The ClearFog ARM ITX Workstation Performance Is Looking Very Good

Written by Michael Larabel in Arm on 1 June 2019 at 11:04 AM EDT. 48 Comments

If there's one Arm hardware launch I am looking forward to this year of known products in the pipeline, it would certainly be SolidRun's ClearFog mini-ITX workstation product.

The SolidRun ClearFog was announced back in April and is the 16-core ITX-based workstation board that is trying to get in at the $500~750 USD price-point. This board is expected to have multiple 10GbE SFP+ connections, Gigabit Ethernet, mPCIe, SATA ports, and socketed DDR4 memory support. The 16 Arm cores are Cortex-A72s.

The ClearFog workstation board is expected to be released later this year but the price doesn't appear to be settled yet. While not yet the workstation board, there are some other ClearFog boards currently available.

I noticed this week some ClearFog benchmark results have begun hitting OpenBenchmarking.org with benchmarks by the Phoronix Test Suite. Search for the SolidRun LX2160A COM type 7 module to see the few results so far.

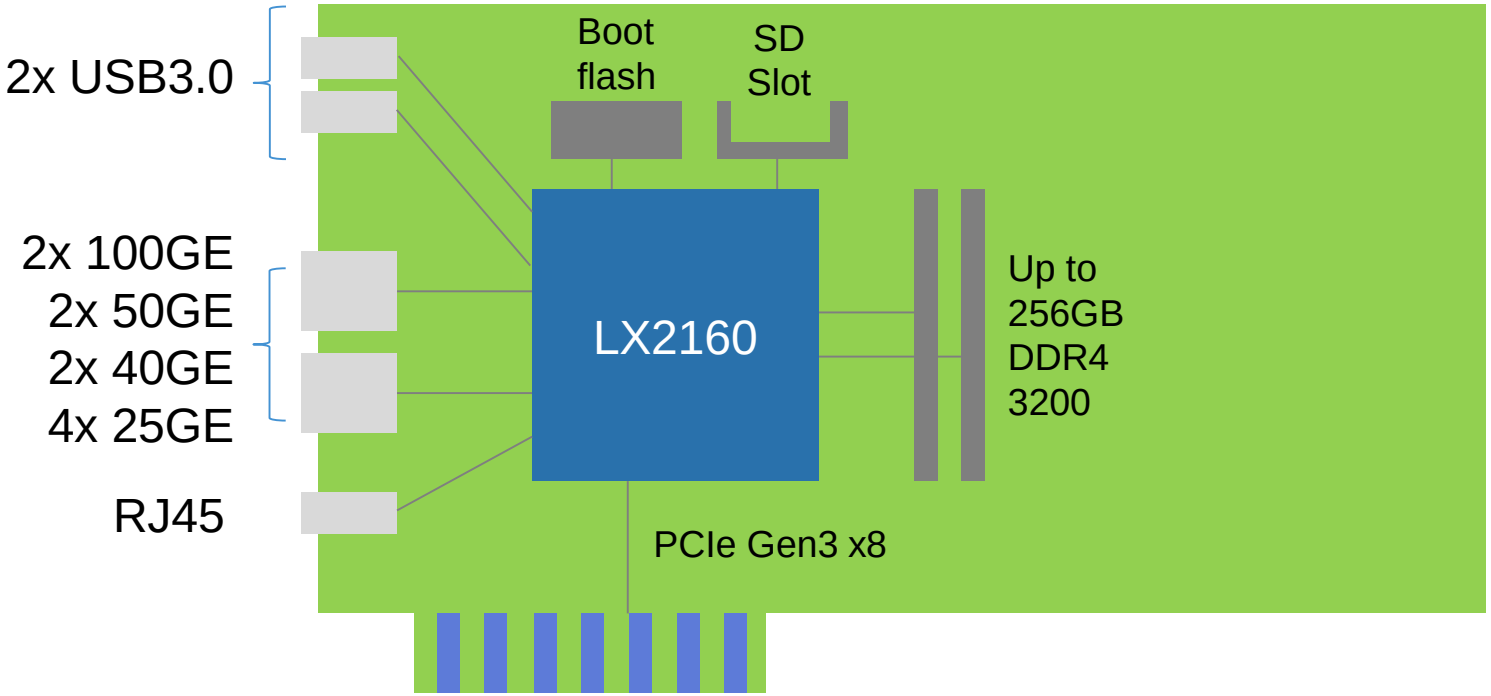
If the price is right for their mini-ITX workstation board, this could be batting a home run and one of the most compelling Arm workstation offerings we have seen to date. We will hopefully see a review sample of the board when the time comes and will put it under plenty of independent tests.

Real-Time Linux

- NXP has regression-tested the RT kernel for Layerscape SDK 19.09 release
- 5G customers are already using the RT kernel on LX2160A
- NXP has supported RT patches for multiple processor generations

NIC

LX2160A as a High Function NIC



- 16x A72 cores at 2.2GHz
- PCIe capabilities
  - RC or EP
  - Up to x8 Gen3
  - SR-IOV, 2 PF each with 64 VF
  - 1024 MSIX, 32 MSI
  - Advanced Error Reporting
- 36Mpps-capable, 96Gbps DMA engine for simultaneous read and write
- Large platform cache minimizes DDR accesses
- 50Gbps IPSEC
- 100Gpbs data de/compression
- 16FFC for low power: 20 – 30W at 105C

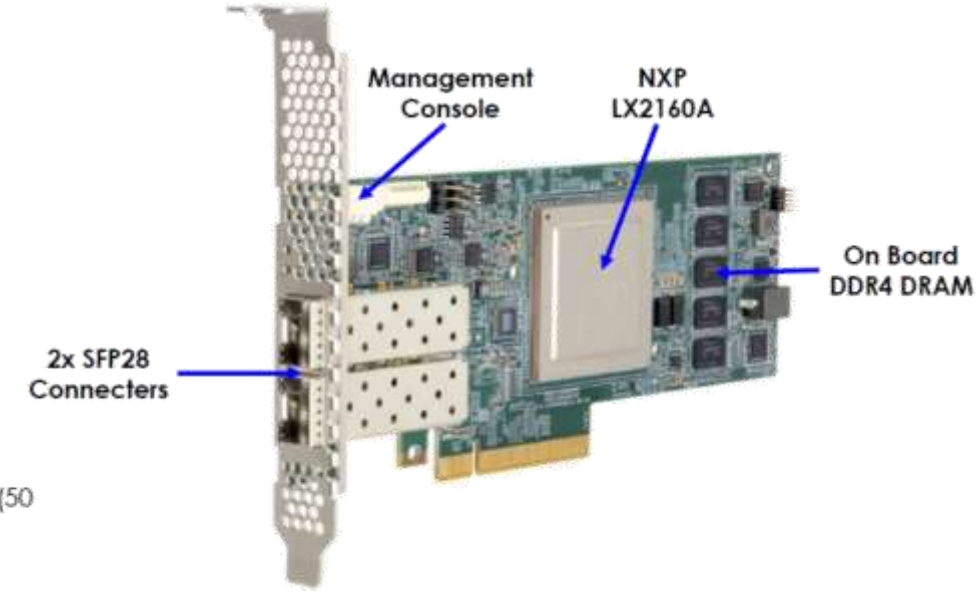
Accton iNIC

NIA-1320 High Level Specs

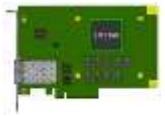
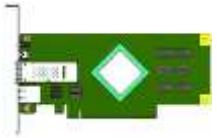
- PCIe Card Size
  - Half-High, Half-Length (HHHL)
- Network Interface
  - Two SFP28 Ethernet ports, 25/10 Gb/s
- Management Serial I/O
  - 3 pin console
- PCIe Interface
  - Eight Lanes PCIe Gen 3.0
  - Support SR-IOV
- Memory Size
  - On board 8GB DDR4 DRAM with ECC
  - One channel
- Flash Size
  - 16GB eMMC

- LX2160A Processor
  - 16nm FinFET Compact
  - 16 ARMv8.0 A72 CPUs, 64b
  - 1MB L2 cache / cluster
  - 8 Clusters
  - 8MB Platform Cache
  - 2MB packet buffer (PEB)
- Acceleration Features
  - QBMan for QoS
  - 50Gb/s SEC
  - 100Gb/s Data Compression Engine (50 Compress + 50 Decompress)
  - L2 Switching (130 Gbps)

NIA-1320 Design

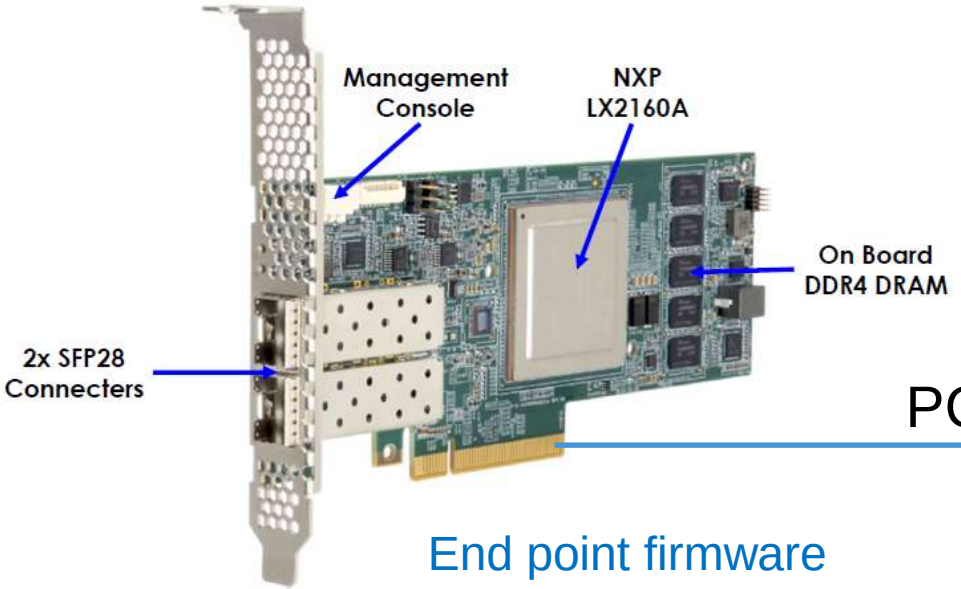


Advantech iNIC

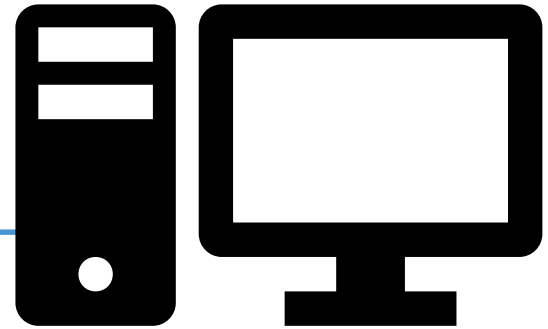
P/N	ESP-2120-25AA00	ESP-2120-25AA10	ESP-2120-25AA20	ESP-2120-25AA30	ESP-2120-100AA00	ESP-2120-100AA10
						
I/O	2x10/25 GbE 1x Mgmt port 1x console	4x10/25 GbE 1x console	2x10/25 GbE 1x console	2x10/25 GbE 1x console	1x40/100GbE 1x Mgmt port 1x console	2x40/100GbE 1x console
CPU	NXP LX series Cortex®-A72 Up to 16 cores	NXP LX series Cortex®-A72 Up to 16 cores	NXP LX series Cortex®-A72 Up to 16 cores	NXP LX series Cortex®-A72 Up to 16 cores	NXP LX series Cortex®-A72 Up to 16 cores	NXP LX series Cortex®-A72 Up to 16 cores
Memory	Up to 32G ECC DDR4 SO-DIMM max, 16G per DIMM	Up to 32G ECC DDR4 SO-DIMM max, 16G per DIMM	8G ECC DDR4 on board	16G ECC DDR4 on board	8G ECC DDR4 on board	8G ECC DDR4 on board
Interface	PCIe Gen4 x8	PCIe Gen4 x8	PCIe Gen4 x8	PCIe Gen 4x8	PCIe Gen4 x16	PCIE Gen4 x16
Dimension	9.5" x 4.2"	9.5" x 4.2"	6.6" x 2.7" (Low profile)	6.6" x 4. (FHHL)	7" x 3.1"	7" x 3.1"
Note	ES available in 2018 Q4	ES available in 2019 Q1			ODM base. Project kick off with binding 800pcs/yr, or 5000pcs forecast in total	ODM base. Project kick off with binding 800pcs/yr, or 5000pcs forecast in total

Available Today

iNIC Software Overview



PCIe



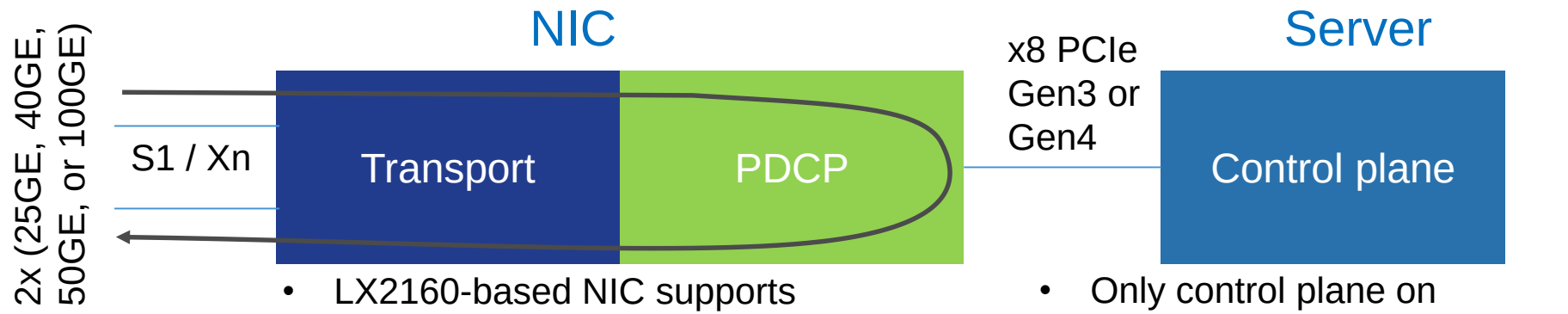
End point firmware

- PCIe x8
- Two physical functions (PF)
- SR-IOV supports with up to 64 Virtual functions
- 32 MSIs for each PF
- 8 MSI-X for each function
- 8K bar0 for register
- 8M bar1 for MSIx
- 2M bar2 for packed ring
- Max 32 receive ring queues
- Max 32 transmit ring queues
- QDMA with Long format/short format

Host driver

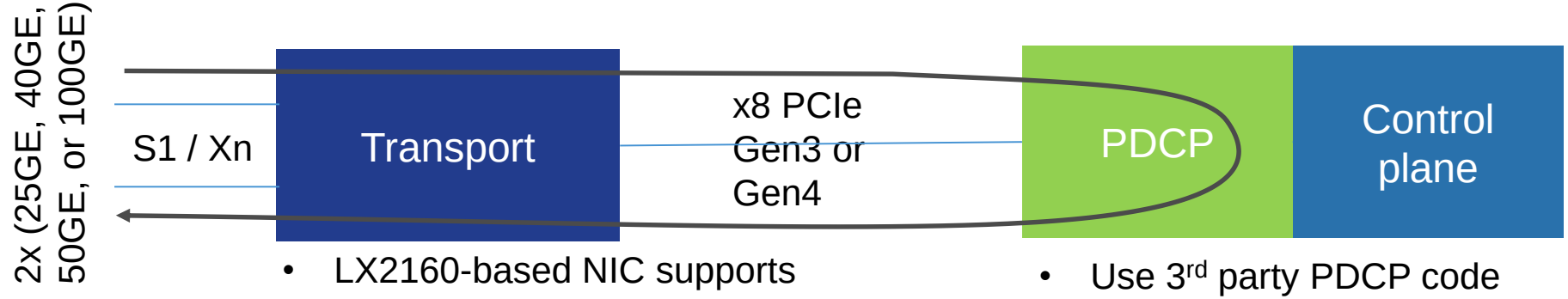
- SR-IOV support
- Max 32 transmit ring queues
- Max 32 receive ring queues
- 8 MSI-X interrupts for each function
- 32 MSIs supports
- Interrupt mode: MSI-X interrupt is used to notify arriving of receive packets and buffer release of transmit packets
- Poll mode: One thread is used for one or more pairs of transmit and receive, and each thread is bound to one CPU core
- Loopback mode: directly transmit the received packets

5G NIC Configurations



- LX2160-based NIC supports ~aggregate 20Gbps Transport and PDCP functionality with 512B packets
- Entire user plane resides on NIC
- Only control plane on server

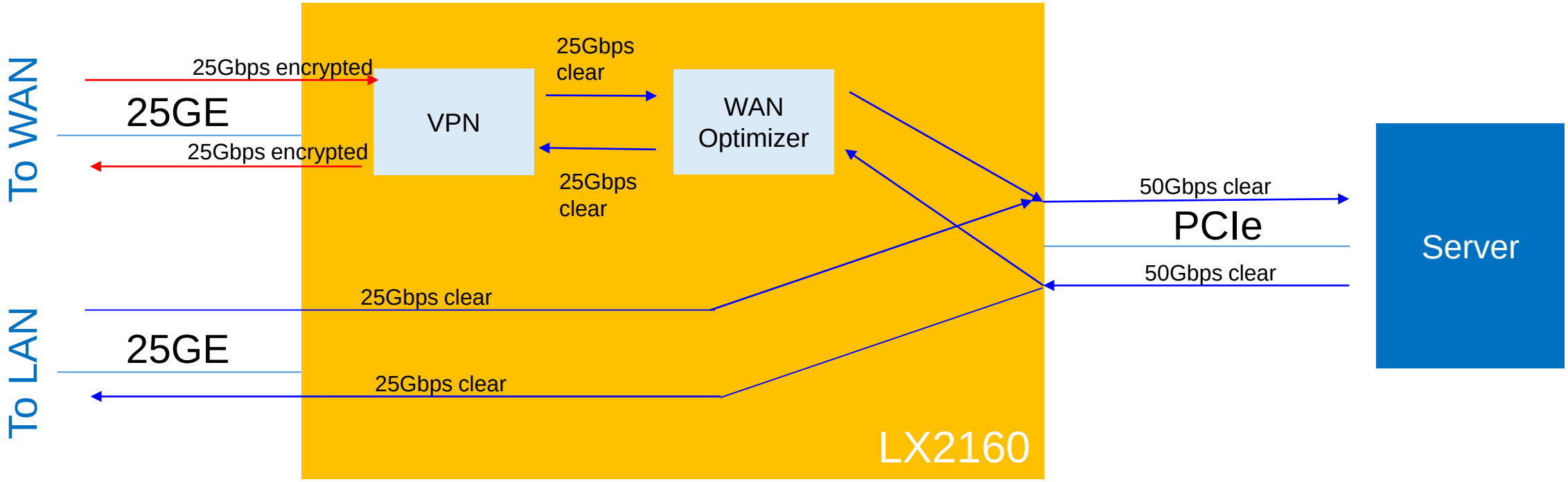
- Only control plane on server
- Minimal bandwidth on PCIe
- Server conserved for value-add apps



- LX2160-based NIC supports ~aggregate 35Gbps Transport functionality with 512B packets

- Use 3rd party PDCP code on server

WAN Optimization and Security



Getting Started with LX2

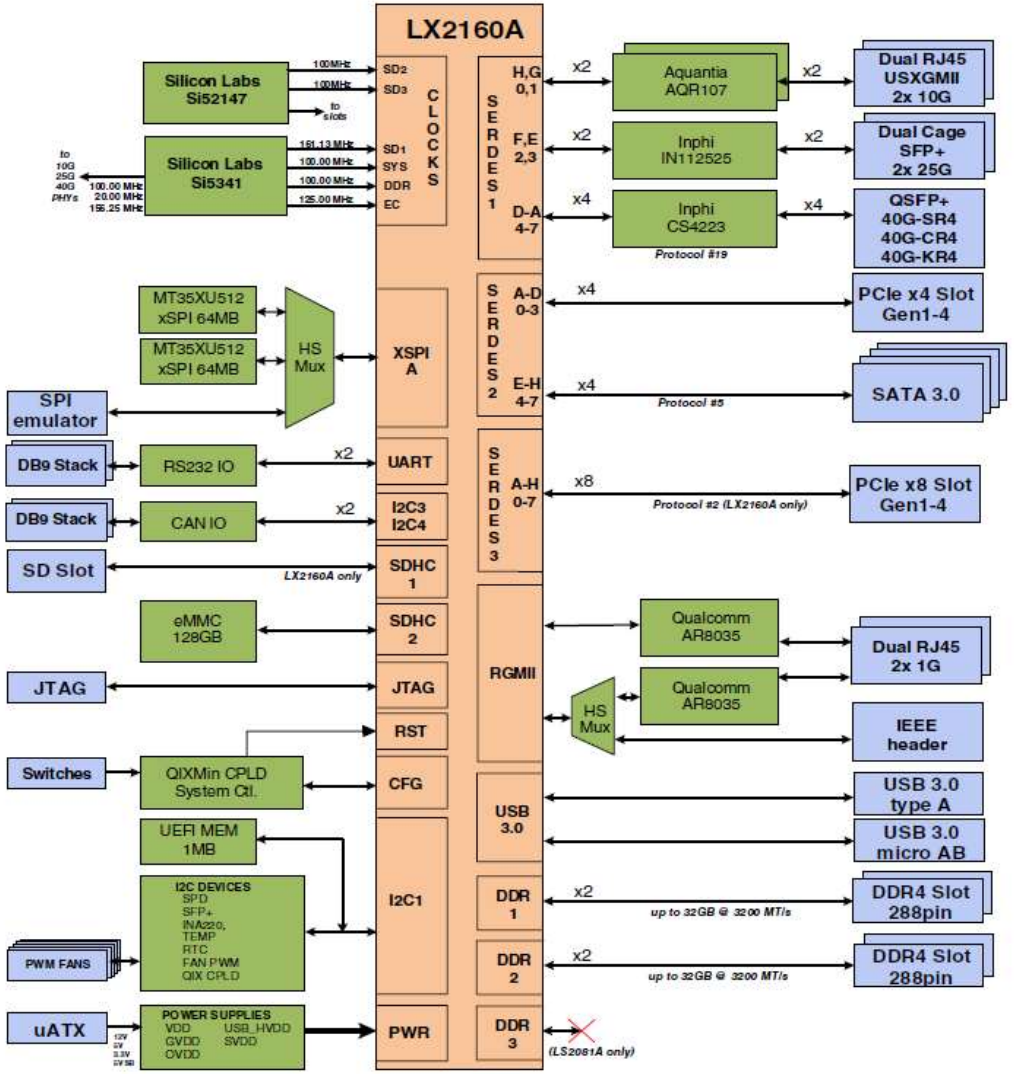
LX2160 Status

- Applications: 5G base station, ORAN, NIC, ADAS, data center, storage controller, Com Express Type 7, factory inspection, machine control, military single board computer, security router
- Customers developing NICs, Com Express Type 7
- Reference Design board in production, LX2160A-RDB, $3995
- Shipped thousands of samples to customers:
- LX2 incorporated into the Layerscape LSDK19.06 release with LTS 4.14 and 4.19
- Benchmarks: CoreMark, Dhrystone, LmBench, DPDK L3 and OVS, SpecInt
- Mature collateral: docs, ref boards, schematics, layouts, IBIS, Flowtherm, BSDL, SDK

Collateral: https://nxp1.sharepoint.com/teams/ext204
Public web: nxp.com/lx2160; nxp.com/lx2160a-rdb

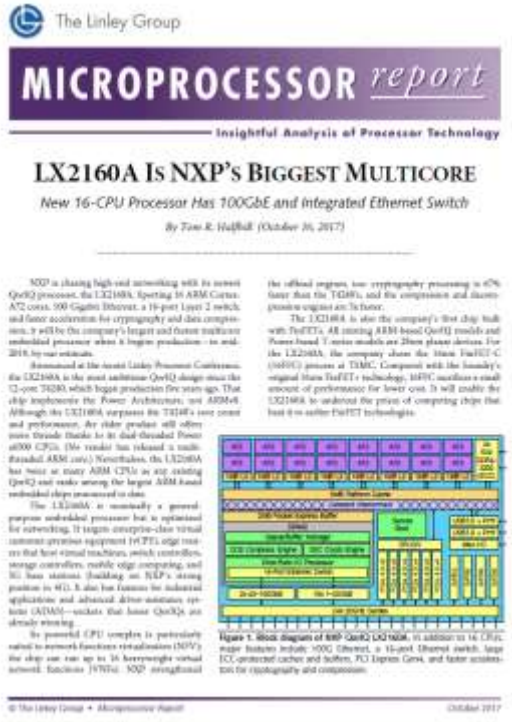
LX2 RDB

- Device: PLX2160PC720ZA, Rev 1.0, 2GHz
- Memory: two 288-pin DIMM slots, each populated with a 16GB 3200MT/s DDR4 UDIMM (for a total of 32GB). LX2 Rev 1.0 will support max DDR data rate of 2900MT/s despite faster DIMM.
- Flash: 128MB NOR flash, 128GB eMMC, and an SD Slot
- SerDes1 (config 19): QSFP+ (40GE), two SFP+ (25GE), and two RJ45 USXGMII (10GE)
- SerDes2 (config 5): x4 PCIe Gen3 slot and four SATA3.0
- SerDes3 (config 2): x8 PCIe Gen3 slot
- One USB Host Type A, one USB3.0 Type AB, two RS232, JTAG, two RGMII
- Part number: LX2160A-RDB, $3995



Documentation

- On External Sharepoint (nxp1.sharepoint.com/teams/ext204), request to be enrolled
  - Datasheet, Rev G, July 2019
  - Design Checklist AN5407, Rev D, April 2019
  - A72 Reference Manual, r0p3 (from ARM)
  - SOC Reference Manual, Rev D, April 2019
  - DPAA Ref Man, April 2019
  - Security Reference Manual Rev B, Sept 2018
  - Enabling Debug Access Port, AN12141, Rev B, May 2018
  - TX Equalization Apps Note AN12521
  - Backplane driver support AN12572
  - IBIS
    - LVCMOS, Dec 12, 2017
    - AMI: Oct 2018
  - Flowtherm: February 28, 2017
  - BSDL: January 18, 2018
- Public web: nxp.com/LX2160
  - Fact Sheet
  - Microprocessor Report
- Ref Design Board: nxp.com/lx2160a-rdb
  - Getting Started Guide, Rev 0, Sept 2018
  - Reference Manual, Rev 0, Sept 2018
  - Board errata Rev 0
  - Schematics (Rev B5, Nov 2018), layout (Rev B2), BOM (Rev B5, Nov 2018), Assembly (X8), Fab (B2)
  - Fact sheet


The Linley Group

MICROPROCESSOR report

Insightful Analysis of Processor Technology

LX2160A Is NXP's Biggest Multicore

New 16-CPU Processor Has 100GbE and Integrated Ethernet Switch

Software: LX2 is Supported in Layerscape SDK

LSDK 19.06

- Supports: LX2160A-RDB
- Toolchain: gcc: Ubuntu/Linaro 7.3.0-16 ubuntu3~18.04, glibc-2.27, binutils-2.30-0, gdb-8.1
- Mgmt Complex: 10.16.2
- DPDK v18.11: L2fwd, L3fwd, L2fwd_crypto, ipsecgateway
- Trusted Firm – A: pwr mgmt. and OP-TEE OS binary
- Virtualization: OVS-DPDK 2.11, Libvirt 4.0, LXC, QEMU 2.9 and 2.11, KVM and Containers, DPDK in VM or on Docker, direct assignment guest kernel
- Edgescale: secure manufacturing, provisioning, keys; user dashboard; apps mgmt
- OP-TEE 3.4.0
- Debugger: CodeWarrior, Lauterbach

Boot

- **Uboot 2019.04**
- non-secure boot and secure boot, boot from flexspi NOR and SD, Clock, UART, DDR4, eSDHC, eMMC, GIC, I2C, OCRAM, PCIe, USB, SATA, Flexspi access to NOR flash, TF-A, networking, Voltage ID
- **UEFI**
- Base platform boot with ACPI
- TianoCore EDK2
- DDR4, DUART, GPIO, I2C, IFC, PCIe, RTC, SATA, SD, Networking support, Watchdog, USB 3.0
- KASLR
- SMP Linux boot via EFI_STUB on SD card, MC High Memory
- PXE boot via PCIe and DPAA interfaces

Kernel

- Kernel: LTS 4.14.122 and LTS 4.19.46 with KASLR
- 32b and 64b addressing
- Kexec
- Kernel drivers: CEETM, CAAM (security), UART, EVB, eSDHC, eMMC, GIC, PCIe (EP, RC, MSI), USB, SATA, Flexspi, power management, Networking interfaces (RGMII, SGMII, UXGMII, XFI, XLAUI4, 25G-AUI), MDIO, QBMAN, MDIO, QDMA, MPIC, OP-TEE, VFIO, watchdog timer, 1588, Huge page, LXD, LXD-Bridge, IMA-EVM (4.14),

Conclusion

- Applications where the Layerscape LX2160A processor excels
  - Communications
  - Industrial
  - Data center
  - Military and aerospace
- Key differentiators
  - Price/performance
  - Power/performance
  - Supply availability
  - Safety and robustness
- Available for new designs now
- Contact your local NXP sales office, distributor, or nxp.com

SECURE CONNECTIONS
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