FTF 2016
TECHNOLOGY FORUM

NEW KE1X SERIES

FTF-HMB-N1945

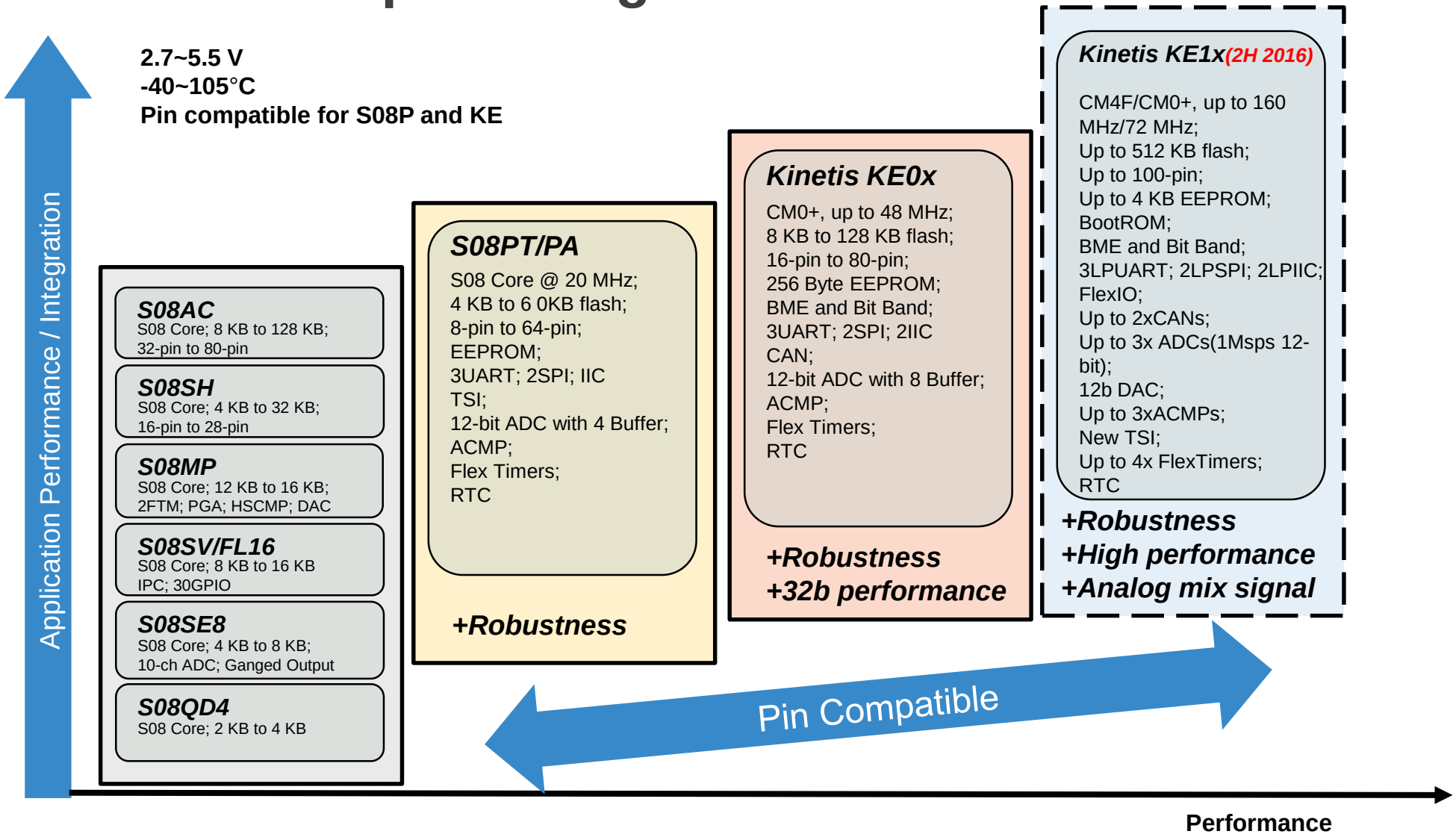
CONST YU/喻宁宁
MCU FAE
JUN 29, 2016

AGENDA

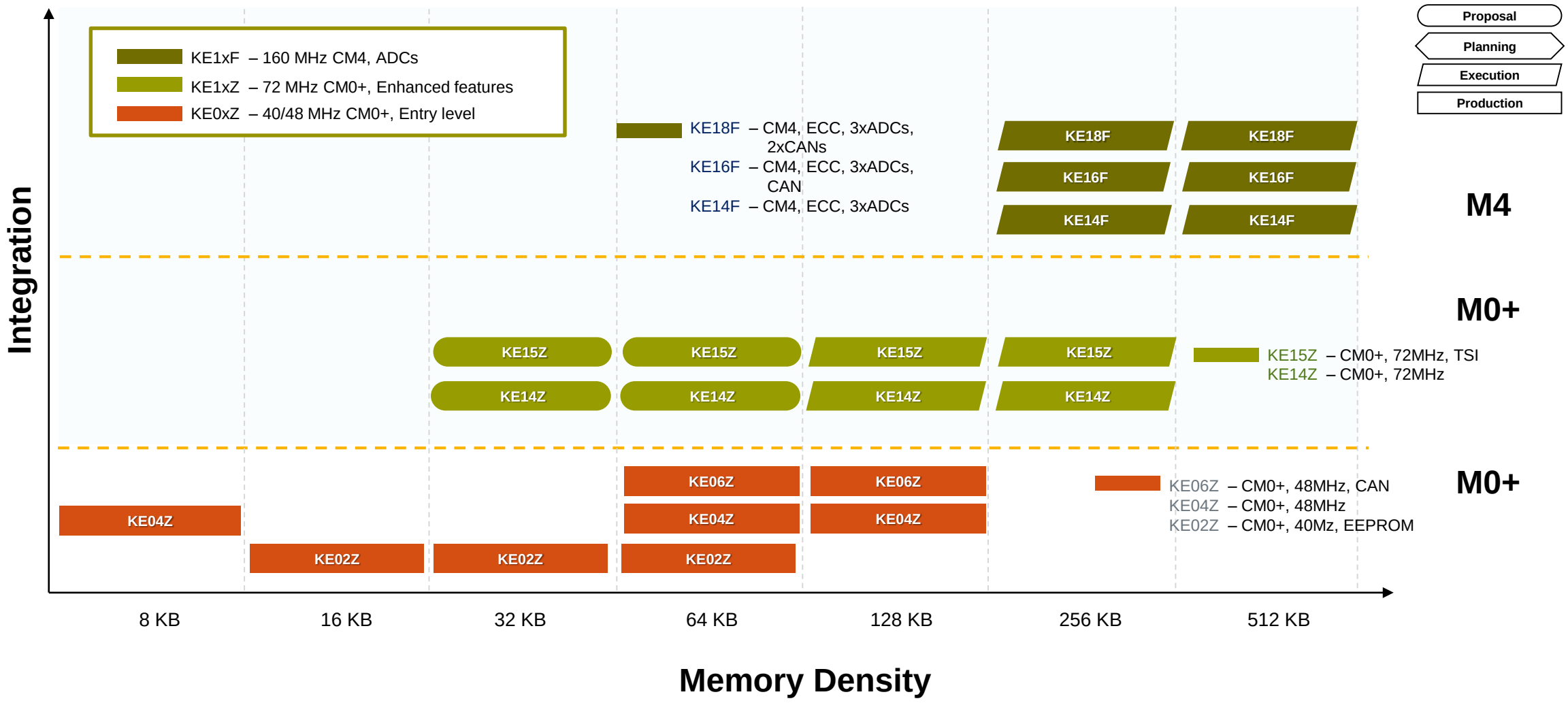
- Kinetis E Roadmap
- Typical Applications
- KE1x Key Features
  - Robust and Safety
  - Performance and Efficiency
  - HMI
  - Power Efficiency
  - Analog & Peripherals
- Enablement

KINETIS E ROADMAP

5V Products Roadmap and Migration

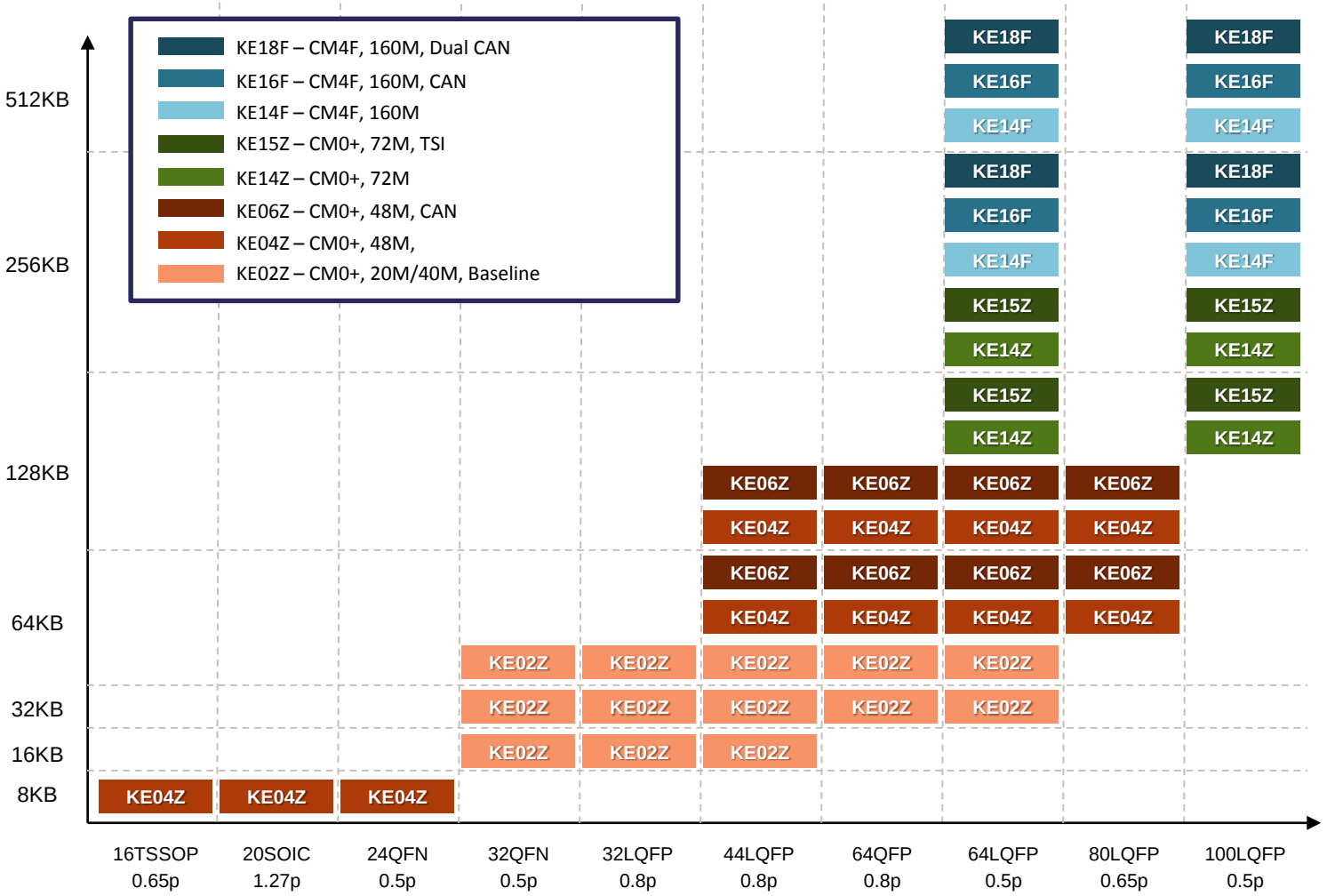


Kinetis E Series Product Roadmap



Packages and Memory Size

- 2.7~5.5 V, -40 to +105°C
- High EMC/ESD robustness
- Pin compatible within Kinetis E series MCUs



KE0xZ Master Block Diagram

Key Features:

Core/System
• ARM® Cortex®-M0+ up to 48 MHz

Memory
• up to 128 KB Flash
• up to 16 KB SRAM
• up to 256B EEPROM

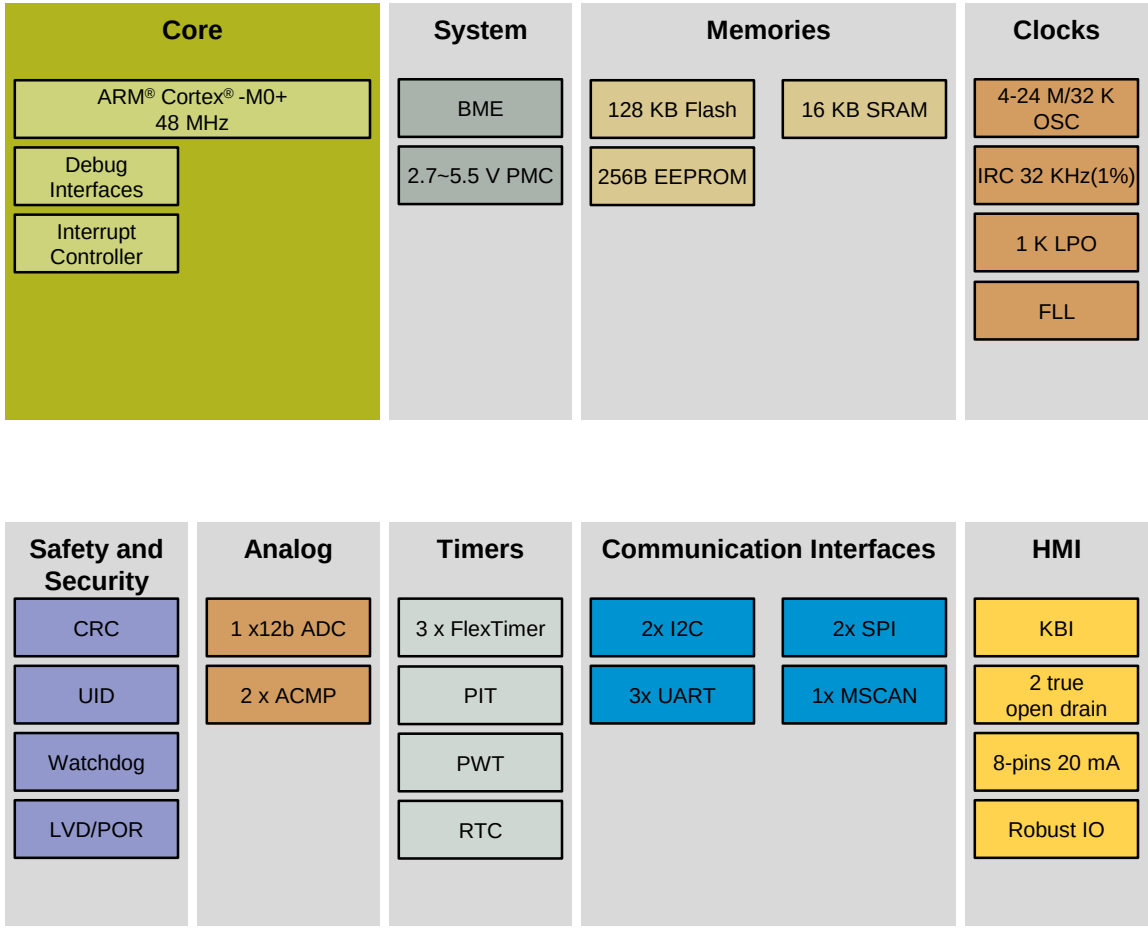
Communications
• 1 x MSCAN
• 3 x UART / 2 x SPI / 2 x I2C

Analog
• 1 x 12b ADC
• 2 x ACMP

Timers
• 1 x 6-ch FTM (PWM)
• 2 x 2-ch FTM (PWM)
• 1 x PIT / 1 x PWT
• RTC

Others
• Up to 71 I/Os
• 2.7-5.5 V, -40 to 105ºC

Packages: 80LQFP(0.65 mm pitch)
64LQFP(0.5 mm pitch)
64QFP(0.8 mm pitch)
44LQFP(0.8 mm pitch)
32LQFP(0.8 mm pitch)
32QFN(0.5 mm pitch)
24QFN(0.5 mm pitch)
20SOIC(1.27 mm pitch)
16TSSOP(0.65 mm pitch)
Pin compatible within KE



KE1xZ Master Block Diagram

Key Features:

Core/System
- ARM® Cortex®-M0+ up to 72 MHz
- 8-ch eDMA
- TRGMUX
- MMDVSQ

Memory
- up to 256 KB Flash
- up to 32 KB SRAM
- up to 32 KB FlexMemory / 2 KB EEPROM
- Boot ROM

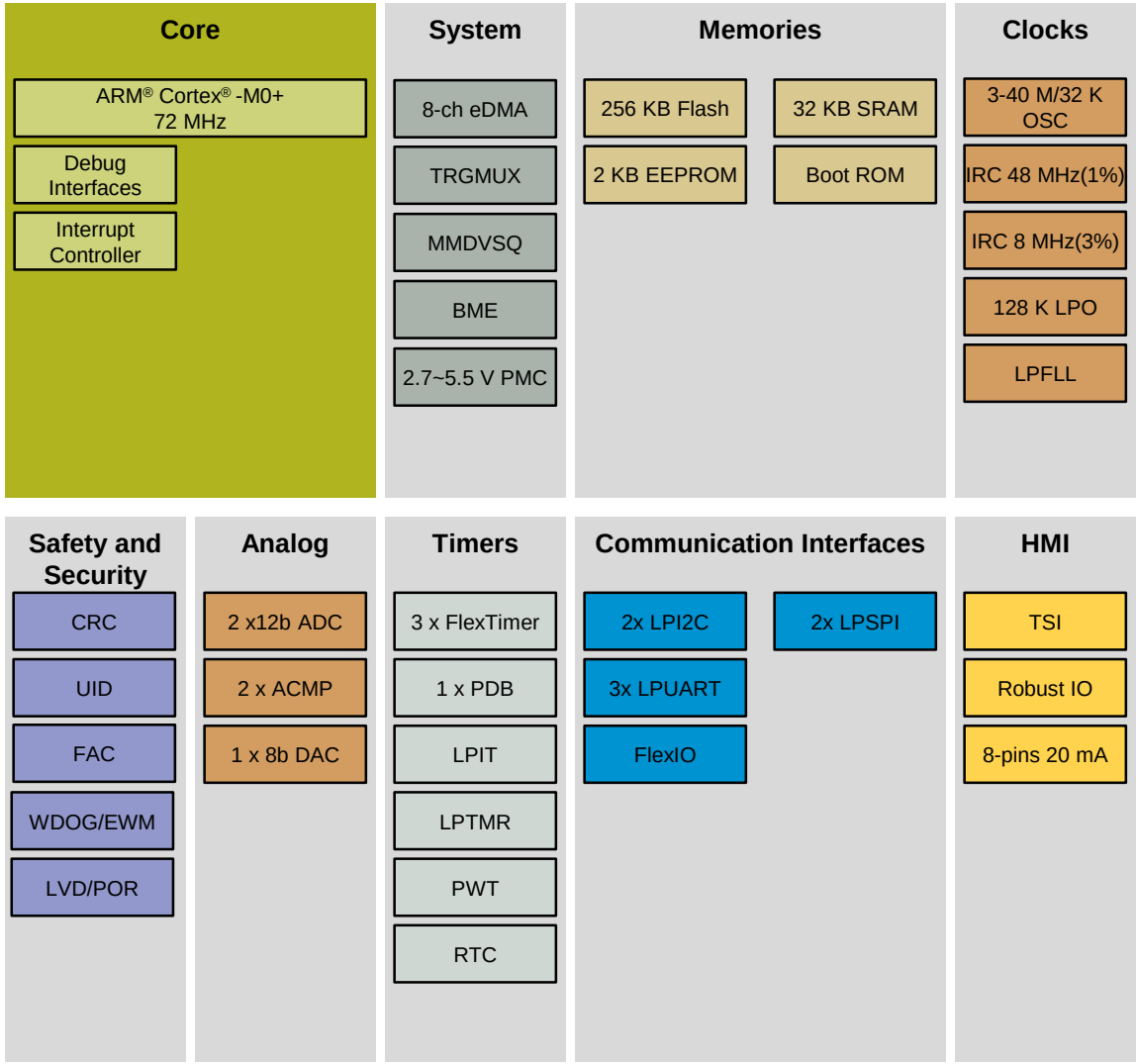
Communications
- 3 x LPUART / 2 x LPSPI / 2 x LPI2C / FlexIO

Analog
- 2 x 12b ADC, 1MSPS
- 2 x ACMP
- 1 x 8b DAC

Timers
- 1 x 8-ch FTM (PWM)
- 2 x 4-ch FTM (PWM/Quad Dec.)
- 1 x PDB
- 1 x 4-ch LPIT / 1 x LPTMR / 1 x PWT
- 1 x RTC

Others
- Up to 36 keys TSI
- Up to 89 GPIO with glitch filter
- 2.7-5.5 V, -40 to 105ºC

Packages: 100LQFP(0.5 mm pitch)
64LQFP(0.5 mm pitch)
Pin compatible within KE



KE1xF Master Block Diagram

Key Features:

Core/System
- ARM® Cortex®-M4F up to 160 MHz
- 16-ch eDMA
- TRGMUX
- MPU

Memory
- up to 512 KB Flash with ECC
- up to 64 KB SRAM with ECC
- up to 64 K FlexMemory / 4 KB EEPROM
- 8 KB I/D Cache
- Boot ROM

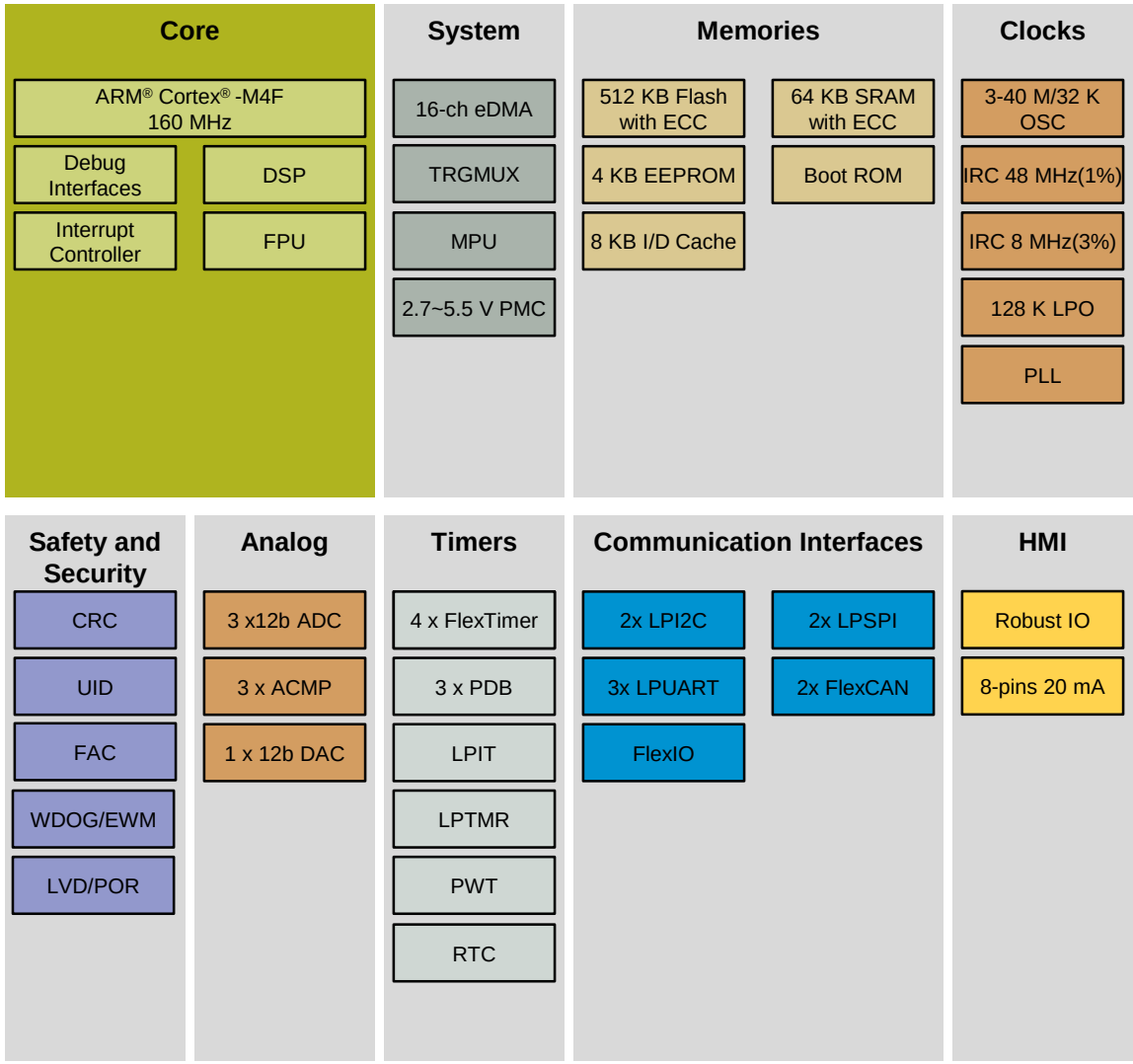
Communications
- 2 x FlexCAN
- 3 x LPUART / 2 x LPSPI / 2 x LPI2C / FlexIO

Analog
- 3 x 12b ADC, 1MSPS
- 3 x ACMP
- 1 x 12b DAC

Timers
- 2 x 8-ch FTM (PWM)
- 2 x 8-ch FTM (PWM/Quad Dec.)
- 3 x PDB
- 1 x 4-ch LPIT / 1 x LPTMR / 1 x PWT
- 1 x RTC

Others
- Up to 89 GPIO with glitch filter
- 2.7-5.5 V, -40 to 105ºC

Packages: 100LQFP(0.5 mm pitch)
64LQFP(0.5 mm pitch)
Pin compatible within KE



KE0xZ Parts List – All Available Now

Sub-Family	Part Number	CM0+ (MHz)	Memory			Features									16TSSOP	20SOIC	24QFN	32QFN	32LQFP	44LQFP	64LQFP	64QFP	80LQFP
			Flash (KB)	SRAM (KB)	EEPROM (KB)	DMA(ch)	BME	UART	SPI	I2C	CAN	FlexTimer	ACMP	12b ADC									
KE02Z	MKE02Z16Vxx4	40	16	2	0.256	-	-	2/3	2	1	-	3	2	1				√	√	√			
	MKE02Z32Vxx4	40	32	4	0.256	-	-	2/3	2	1	-	3	2	1				√	√	√	√	√	
	MKE02Z64Vxx4	40	64	4	0.256	-	-	2/3	2	1	-	3	2	1				√	√	√	√	√	
KE04Z	MKE04Z8Vxx4	48	8	1	-	-	Y	1	1	1	-	2	2	1	√	√	√						
	MKE04Z64VLx4	48	64	8	-	-	Y	3	2	2	-	3	2	1						√	√	√	√
	MKE04Z128Vxx4	48	128	16	-	-	Y	3	2	2	-	3	2	1						√	√	√	√
KE06Z	MKE06Z64Vxx4	48	64	8	-	-	Y	3	2	2	1	3	2	1						√	√	√	√
	MKE06Z128Vxx4	48	128	16	-	-	Y	3	2	2	1	3	2	1						√	√	√	√

KE1xZ Parts List – Coming in 2H'16

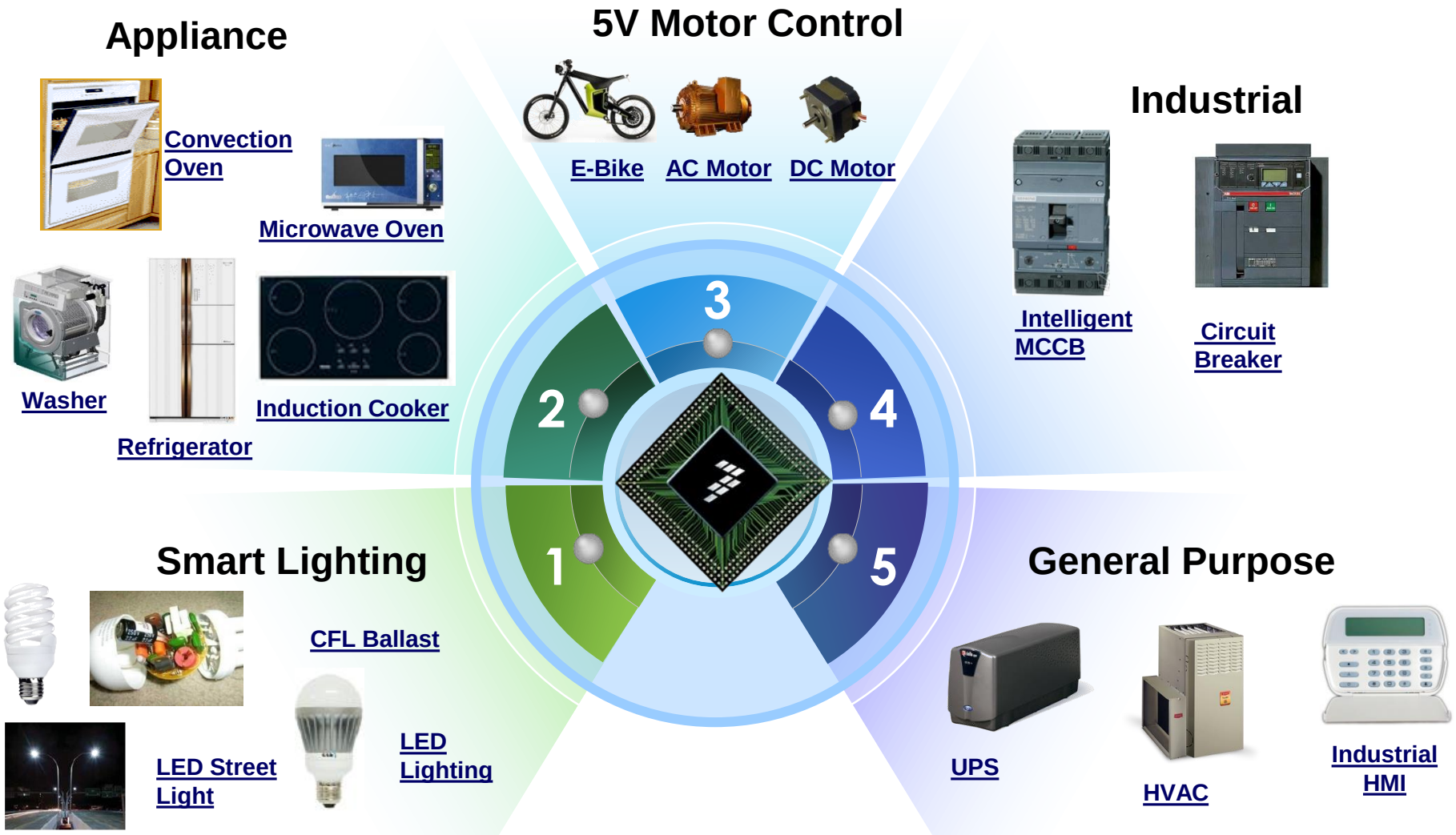
Sub-Family	Part Number	CM0+ (MHz)	Memory				Features											64LQFP	100LQFP
			Flash (KB)	SRAM (KB)	EEPROM (KB)	Boot ROM	DMA(ch)	BME	UART	SPI	I2C	TSI	FlexIO	ACMP	FlexTiimer	12b ADC	8b DAC	Total # of IOs	
KE14Z	MKE14Z128VLH7	72	128	16	2	Y	8	Y	3	2	2	-	1	2	3	2	1	58	√	
	MKE14Z128VLL7	72	128	16	2	Y	8	Y	3	2	2	-	1	2	3	2	1	89		√
	MKE14Z256VLH7	72	256	32	2	Y	8	Y	3	2	2	-	1	2	3	2	1	58	√	
	MKE14Z256VLL7	72	256	32	2	Y	8	Y	3	2	2	-	1	2	3	2	1	89		√
KE15Z	MKE15Z128VLH7	72	128	16	2	Y	8	Y	3	2	2	1	1	2	3	2	1	58	√	
	MKE15Z128VLL7	72	128	16	2	Y	8	Y	3	2	2	1	1	2	3	2	1	89		√
	MKE15Z256VLH7	72	256	32	2	Y	8	Y	3	2	2	1	1	2	3	2	1	58	√	
	MKE15Z256VLL7	72	256	32	2	Y	8	Y	3	2	2	1	1	2	3	2	1	89		√

KE1xF Parts List – Coming in 2H'16

Sub-Family	Part Number	CM4F (MHz)	Memory				Features											64LQFP	100LQFP
			Flash (KB)	SRAM (KB)	EEPROM (KB)	Boot ROM	DMA(ch)	UART	SPI	I2C	CAN	FlexIO	ACMP	FlexTimer	12bit ADC	12b DAC	Total IOs		
KE14F	MKE14F256VLH15	160	256	32	2	Y	16	3	2	2	-	1	3	4	3	1	58	√	
	MKE14F256VLL15	160	256	32	2	Y	16	3	2	2	-	1	3	4	3	1	89		√
	MKE14F512VLH15	160	512	64	4	Y	16	3	2	2	-	1	3	4	3	1	58	√	
	MKE14F512VLL15	160	512	64	4	Y	16	3	2	2	-	1	3	4	3	1	89		√
KE16F	MKE16F256VLH15	160	256	32	2	Y	16	3	2	2	1	1	3	4	3	1	58	√	
	MKE16F256VLL15	160	256	32	2	Y	16	3	2	2	1	1	3	4	3	1	89		√
	MKE16F512VLH15	160	512	64	4	Y	16	3	2	2	1	1	3	4	3	1	58	√	
	MKE16F512VLL15	160	512	64	4	Y	16	3	2	2	1	1	3	4	3	1	89		√
KE18F	MKE18F256VLH15	160	256	32	2	Y	16	3	2	2	2	1	3	4	3	1	58	√	
	MKE18F256VLL15	160	256	32	2	Y	16	3	2	2	2	1	3	4	3	1	89		√
	MKE18F512VLH15	160	512	64	4	Y	16	3	2	2	2	1	3	4	3	1	58	√	
	MKE18F512VLL15	160	512	64	4	Y	16	3	2	2	2	1	3	4	3	1	89		√

KE1X TYPICAL APPLICATIONS

Kinetis E Series Target Market and Applications



KE1X KEY FEATURES

Robust & Safety

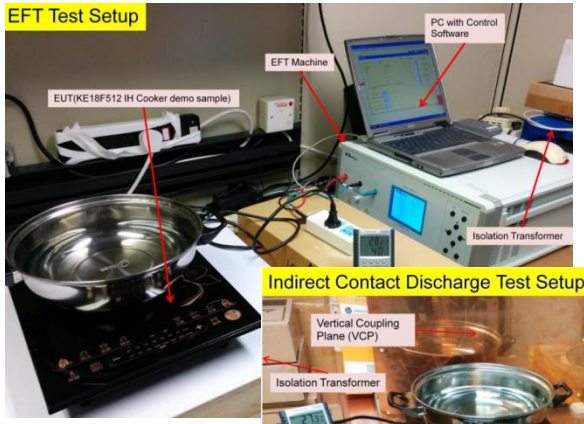
Feature Category	Description
Robust	Improved 5 V I/O pad with digital filter
Safety Library	NXP proprietary safety library for IEC60730 class B
RAM with ECC Check [1]	SRAM with error-correcting code and SECDED capability
Flash with ECC Check [1]	Flash with error-correcting code (ECC) and SECDED capability
CRC Checking	Programmable polynomial with 16-bit and 32-bit CRC standard
On-chip WDOG	Internal WDOG with independent clock source for system safety
Clock Loss Monitor	On-chip clock loss monitors with interrupt or reset capability
Memory Protection Unit	NXP proprietary MPU engine for memory access protection
Flash Access Control	Flash access control unit (FAC) for customer code protection
Flash security	Flash security options to provide extra flash accessing & programing control

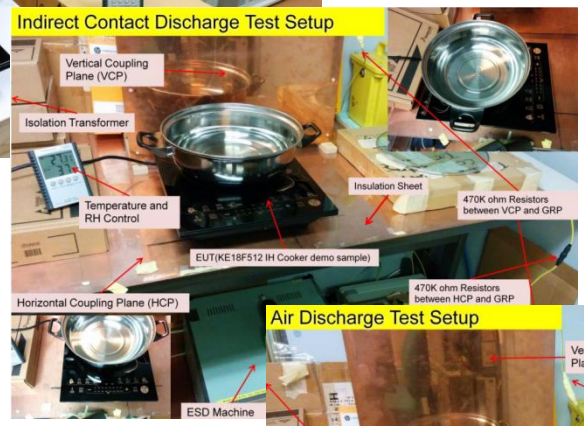
1: KE1xF only

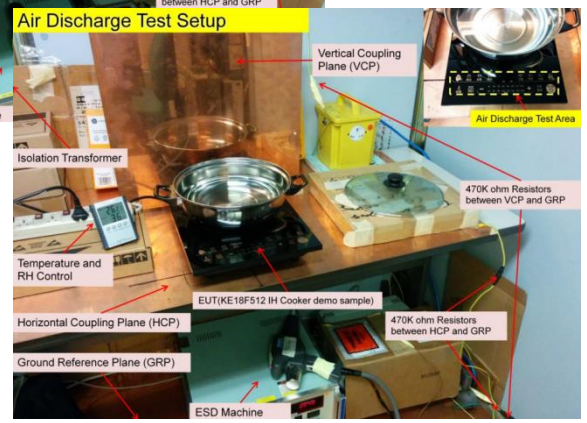
Robust & Safety – EMC Performance

Test Conditions

- PKE18F512VLL15
- IH Cooker as the test platform
- System level tests based on
  - IEC 61000-4-4(EFT)
  - IEC 61000-4-2(ESD)







Test Results

- System level
  - IEC 61000-4-4(EFT):+/- 4.5k V*
  - IEC 61000-4-2(ESD): Contact Discharge(at the case) +/- 20 kV
  - IEC 61000-4-2(ESD): Air Discharge (at the control panel) +/- 15 kV

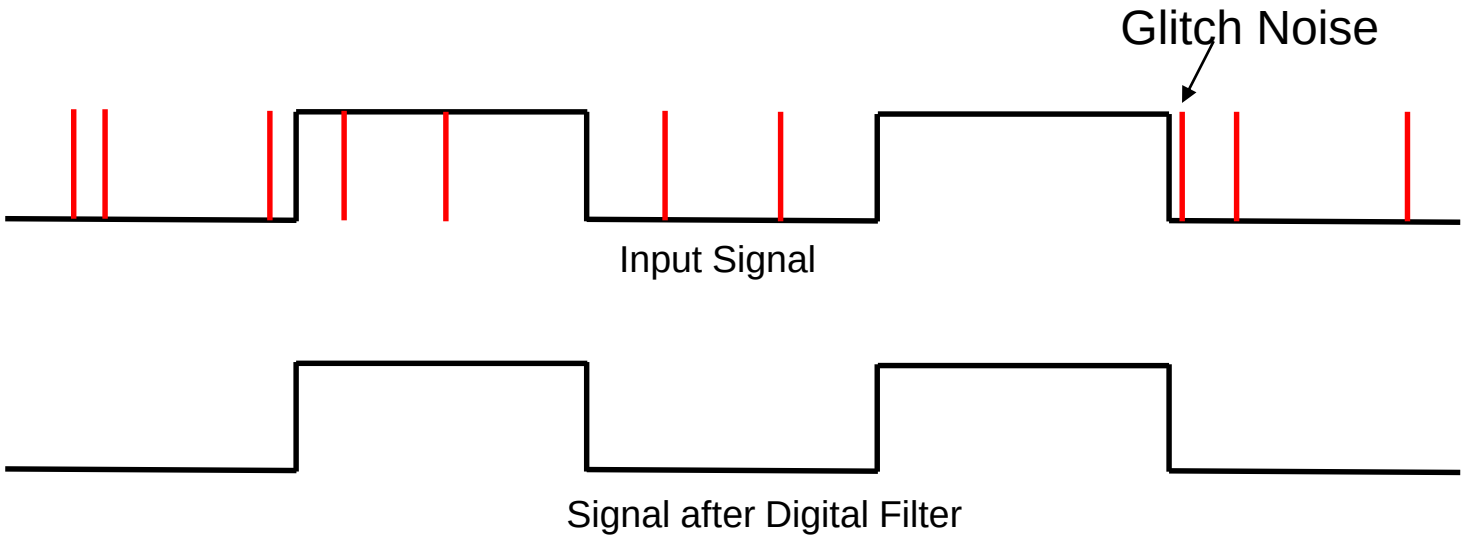
*Limited by the test equipment max output voltage

Robust & Safety – IEC60730

- IEC60730 safety standard
  - Defines the test and diagnostic methods
  - Ensure safe operation HW and SW
  - For household appliances
- Kinetis E IEC60730 Class B Compliance
  - KE0x got certification from VDE and UL
  - KE1x target to get certification in Q3'16
  - NXP developed IEC60730 Safety Library

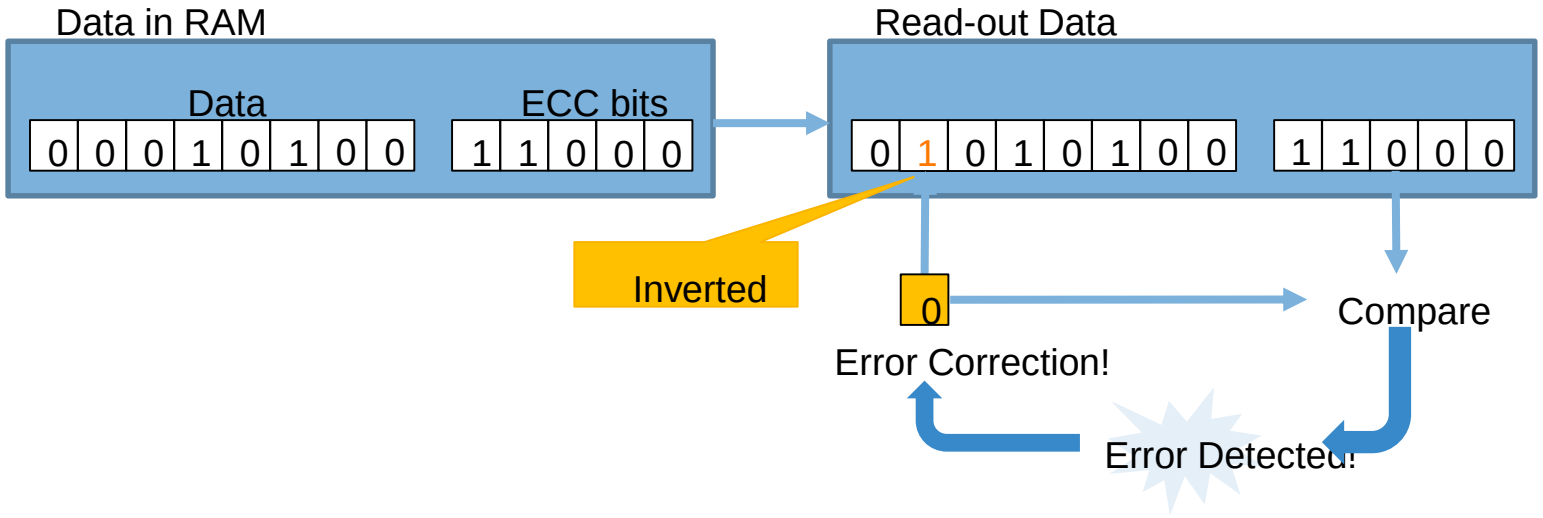
Robust & Safety – Digital Glitch Filter

- Configurable filter width:
  - BUS Clock Source: 1-32 x Bus clock period
  - LPO Clock Source: 5 x LPO clock period
- Independent filter width control on each pin



Robust & Safety – Error Correction Code1

- RAM ECC:
  - 8-bit data with 5-bits ECC
  - detect & correct up to 1-bit error
  - detect out up to 2-bits error
  - support ECC bits self error check
- Flash ECC:
  - 64-bit data with 8-bits ECC
  - detect & correct up to 1-bit error
  - support ECC bits self error check

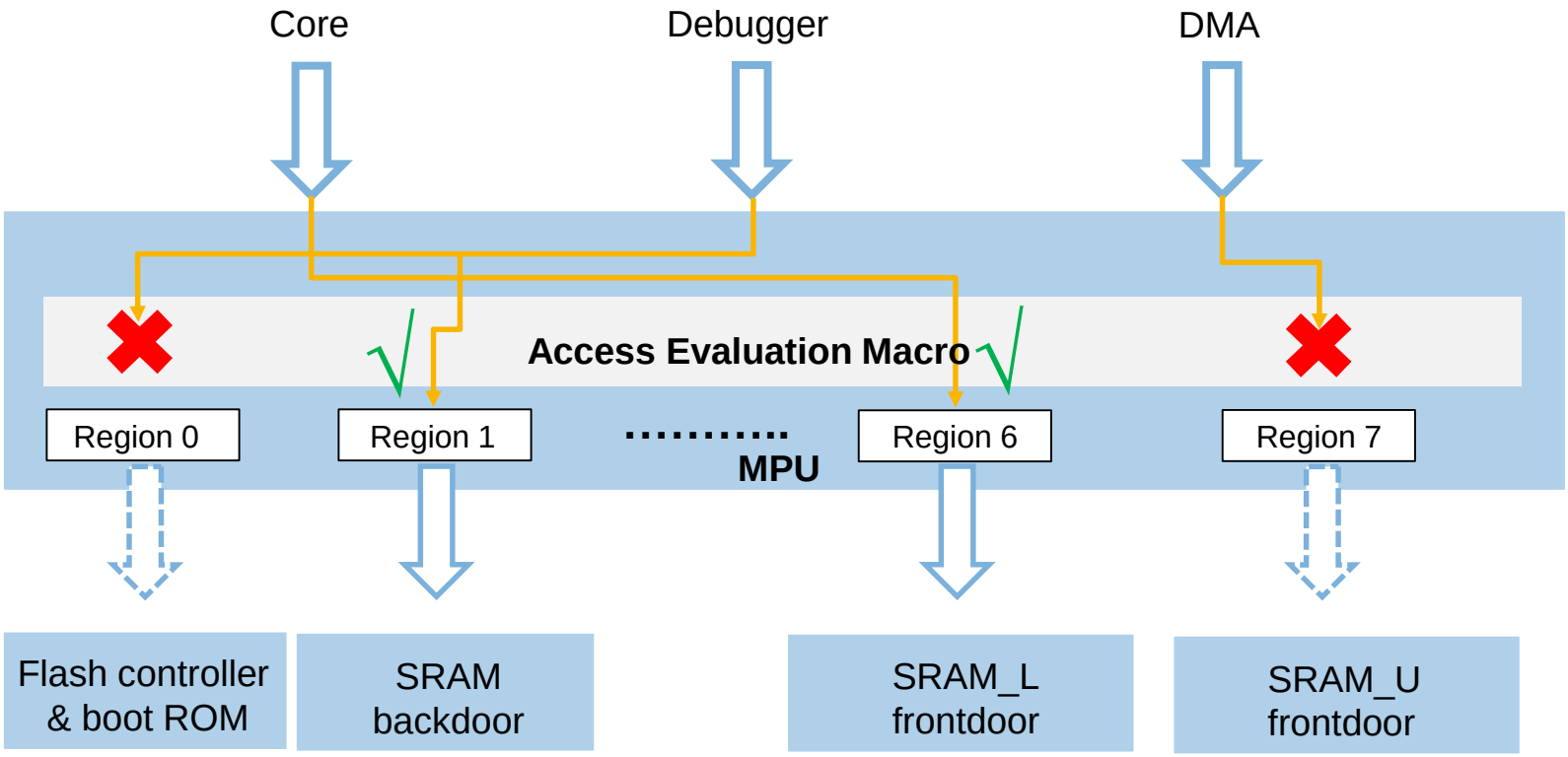


1: KE1xF only

Robust & Safety – MPU[1]

- Support up to 8 memory regions
- Read/write/ execution permission arbitration
- Region sizes can vary from 32 bytes to 4 GB

Example:



3.5.3.3 SRAM accesses

The SRAM is split into two logical arrays that are 32-bits wide.

- SRAM_L — Accessible by the code bus of the Cortex-M4 core and by the backdoor port.
- SRAM_U — Accessible by the system bus of the Cortex-M4 core and by the backdoor port.

The backdoor port makes the SRAM accessible to the non-core bus masters (such as DMA).

The following figure illustrates the SRAM accesses within the device.

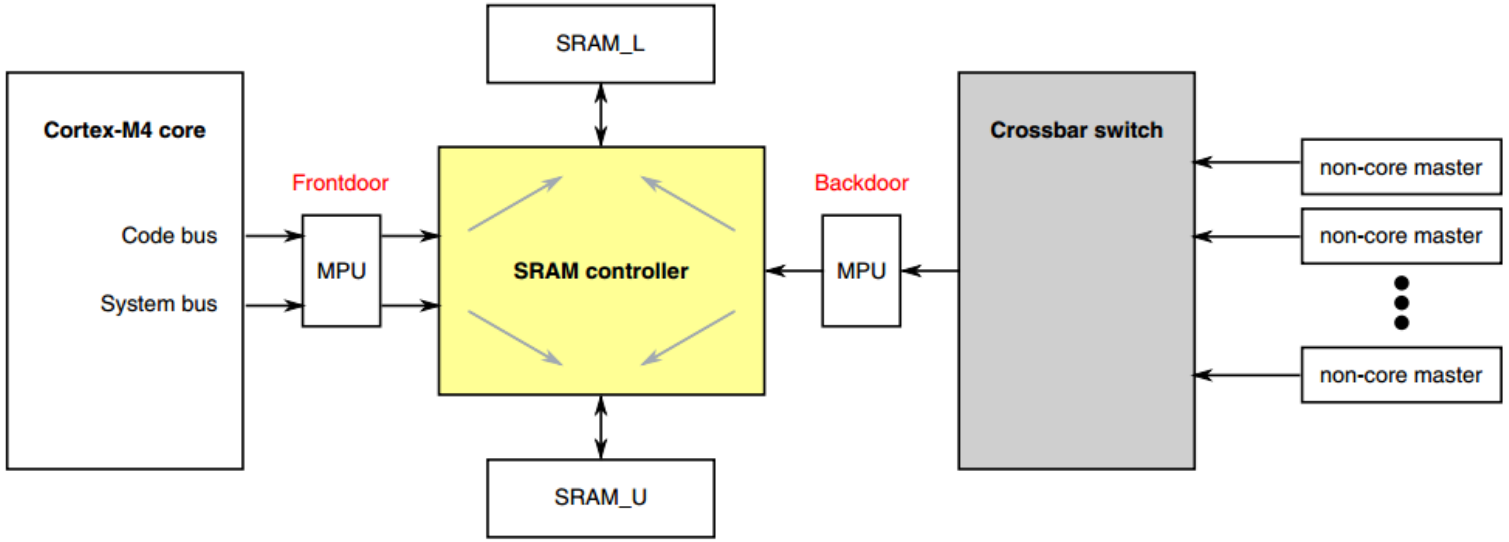
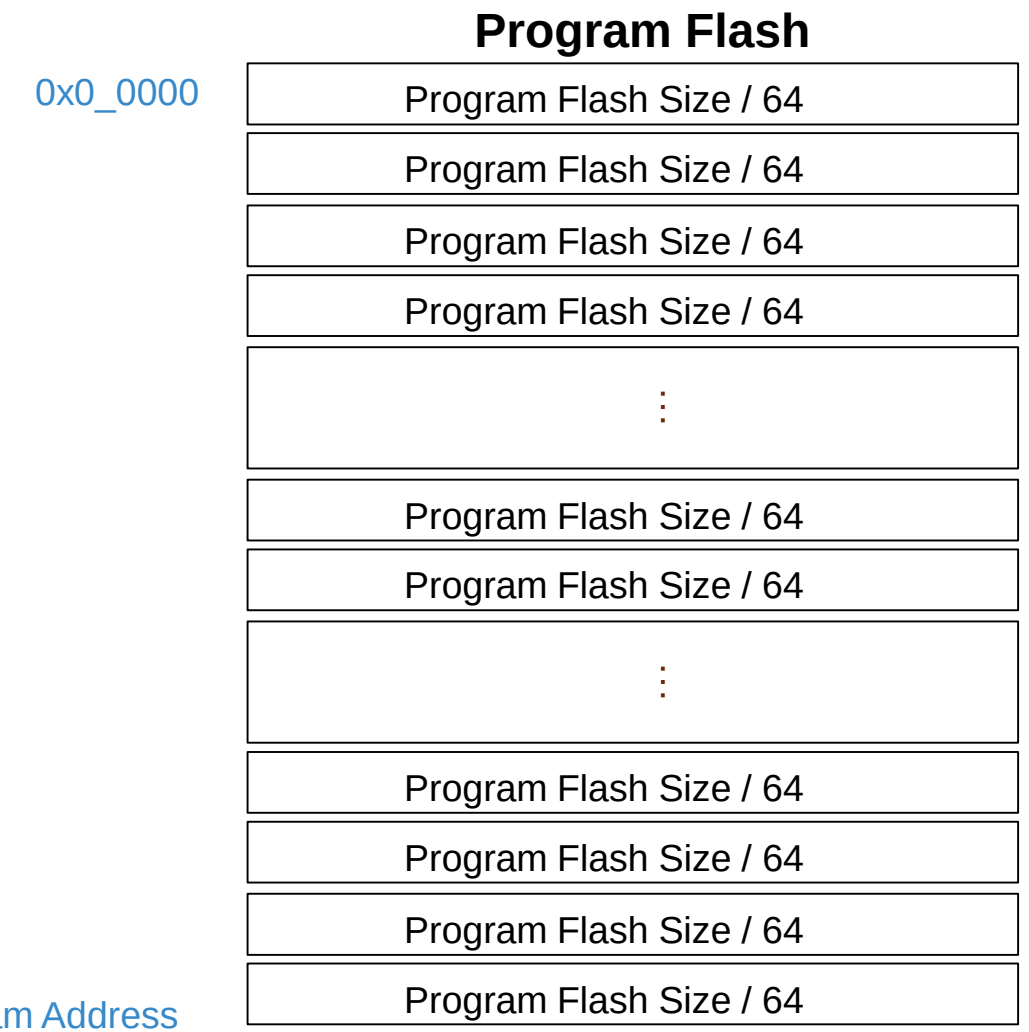


Figure 3-26. SRAM access diagram

Robust & Safety – FAC

- Programmable flash memory divided into equal size, up to 64 segments
- Provides a cycle-by-cycle evaluation of access
- Different secure state:
  - Supervisor/privileged secure state – Execute & Modify
  - Mid-level state – Execute Only
  - Unsecure state – No Access Right
- Access control logic can be implemented in Program Once Area by user

Prevents unauthorized access to selected code segments!



Performance and Efficiency

Feature	Benefit to Customer
High frequency CPU core	KE1xF, CM4 core runs up to 160 MHz KE1xZ, CM0+ core runs up to 72 MHz Improve system performance
8 KB I/D Cache[1]	Improving the code and data access efficiency Improve system performance
MMDVSQ [2]	Hardware engine for math operation, reducing CPU workload
TRGMUX	Improve system performance, more flexible for internal connection
eDMA	Improve system performance, reducing power consumption and CPU workload

1: KE1xF only
2: KE1xZ only

Performance and Efficiency – Core

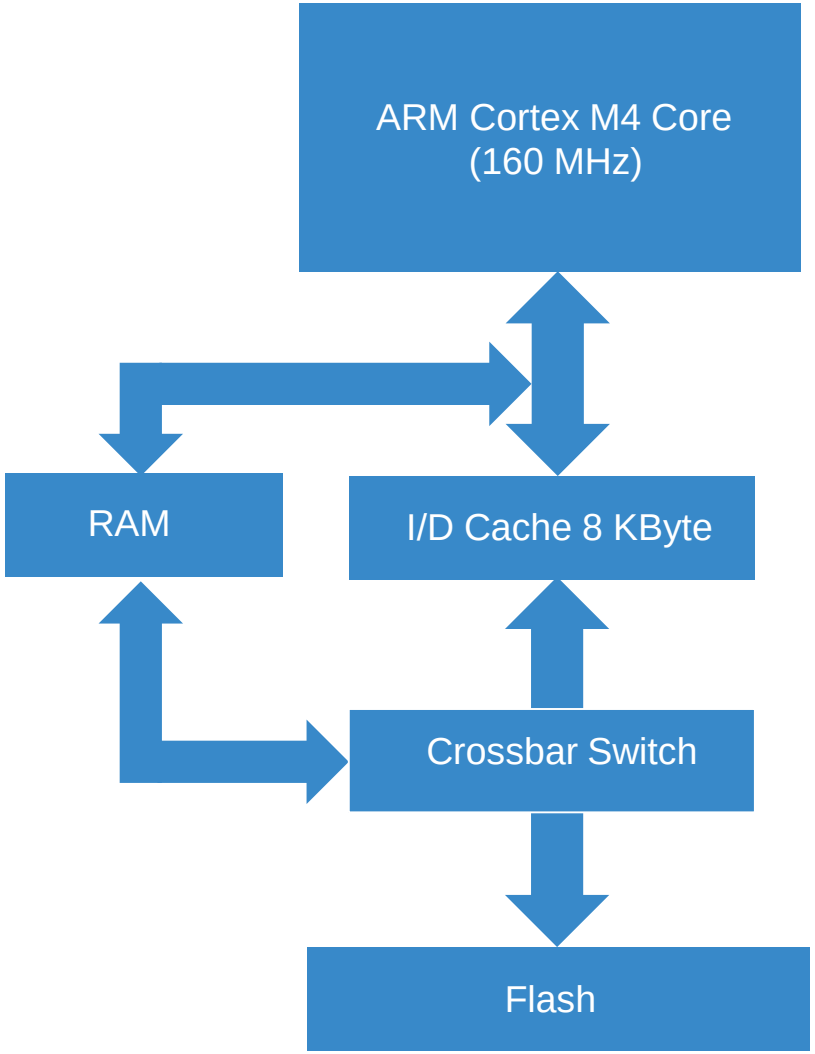
- KE1xF:
  - ARM Cortex M4F, **up to 160 MHz**
  - DSP & FPU embedded
  - **8 KB I/D Code Cache**
  - Bit-banding
  - FPB / DWT / ITM / TPIU tracing units
  - JTAG/SWD support

- KE1xZ:
  - ARM Cortex M0+, **up to 72 MHz**
  - Single cycle 32-bit multiplier
  - Single cycle fast IO port
  - **MMDVSQ** hardware arithmetic engine
  - **128 byte** Flash Cache
  - Watchpoint / Breakpoint / MTB tracing units
  - SWD support

Performance and Efficiency – Cache

- Pre-fetch Instructions and Data for CPU
- Accelerate P-Flash data transfers
- Increase CPU processing efficiency

- KE1xF Cache features:
  - 8 KB I/D Code Cache
  - 2-way set associative
  - 4 word lines
  - Lines can be individually flushed
  - Entire cache can be flushed at once
  - Cache memory with parity check



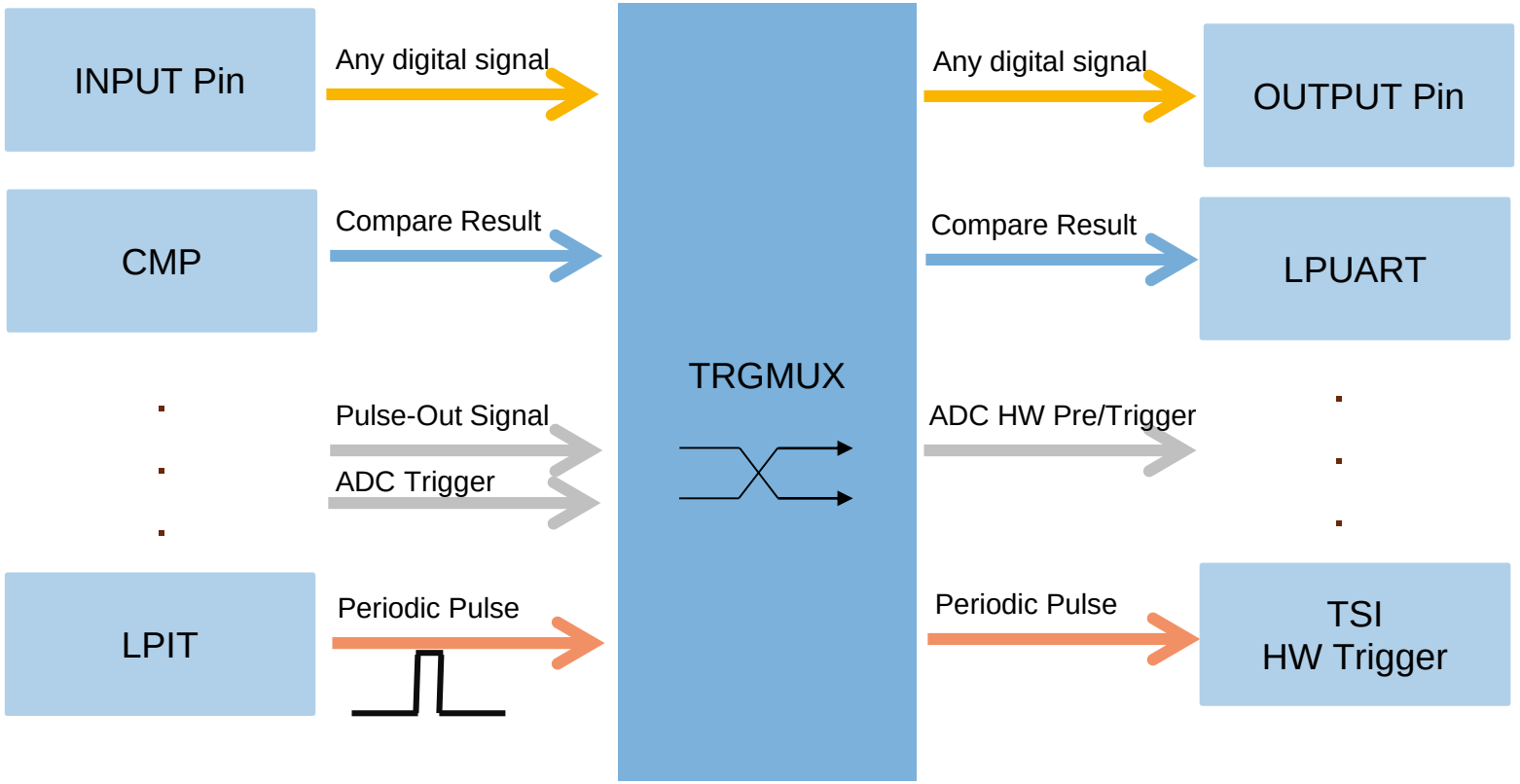
8 KB code cache to minimize Flash access latencies!

Performance and Efficiency - DVSQ Hardware Engine

- Co-processor and hardware support for arithmetic operation: division and square root
  - Supports 32/32 signed and unsigned division calculations
  - Supports 32-bit unsigned square root calculations
  - More than 25% performance improvement running math intensive applications such as Sensorless PMSM FOC algorithms
  - Simple programming model includes input data and result registers plus a control/ status register

Performance and Efficiency – TRGMUX

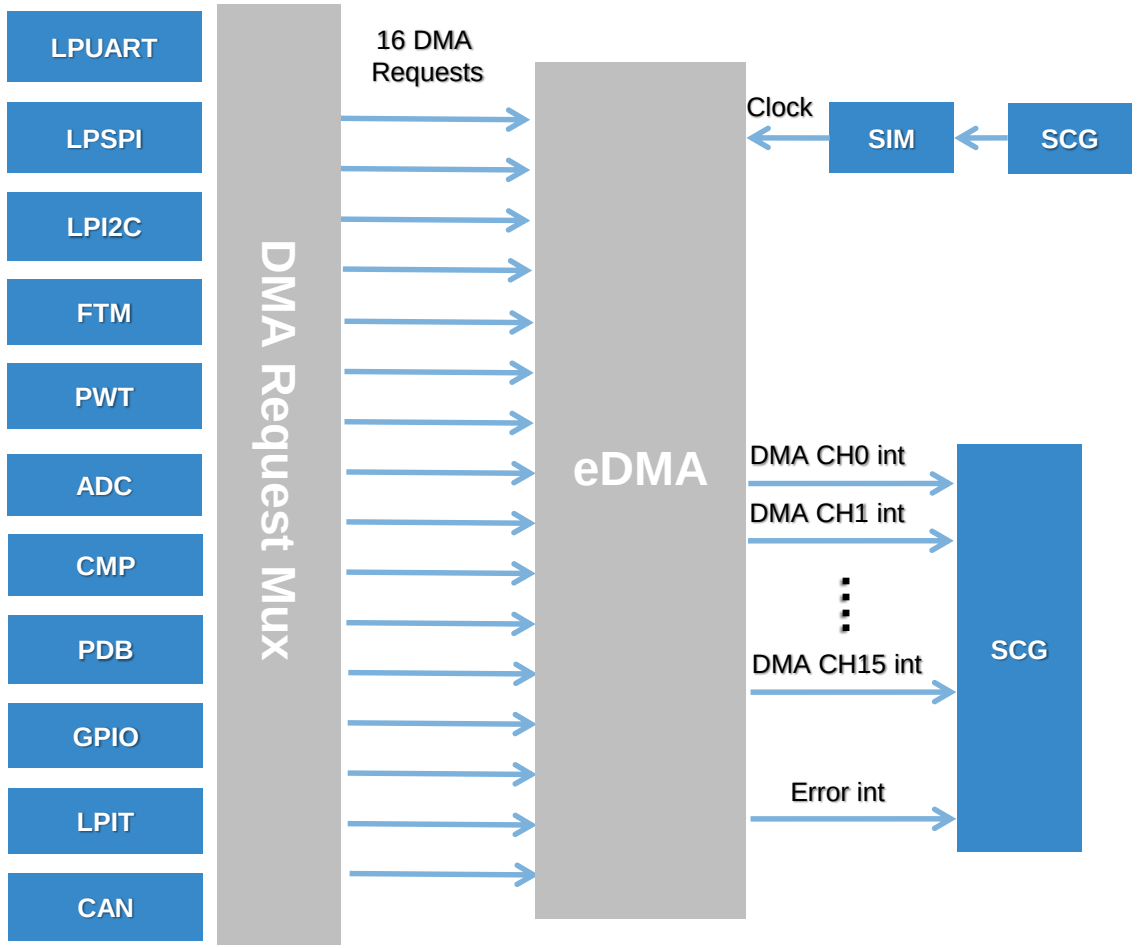
Flexible Trigger Scheme for Module Interconnectivity



Flexible trigger scheme for Module Interconnectivity

Performance and Efficiency – eDMA

- Data movement via dual-address (source & destination) transfers, support enhanced addressing modes
- 16-channel implementation performs complex data transfers with minimal intervention from host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Fixed-priority and round-robin channel arbitration
- Optional interrupt after channel completion
- Support complex data structures



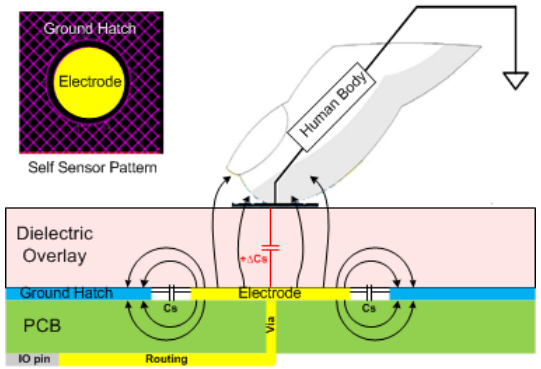
HMI

Feature	Benefit to customer
TSI[1]	Up to 36 touch keys Pass IEC61000-4-6 test, enhanced EMC/waterproof performance Supports both self-cap and mutual-cap sensing mode
High Drive IO	8 high drive pins offer maximum 20 mA driver current each
More GPIOs	More control signal Input/Output More flexible hardware design Up to 89 GPIOs on 100LQFP, 58 GPIOs on 64LQFP

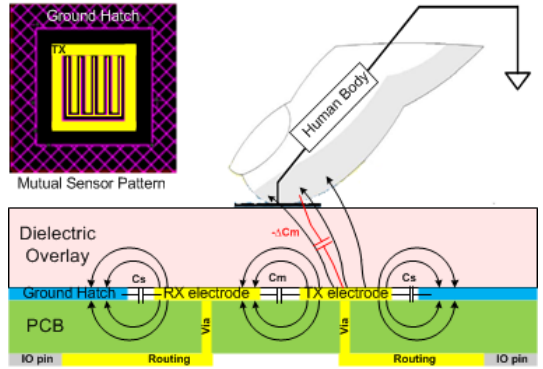
1: KE15Z only

HMI – Touch Sensing Interface

- Self-cap Mode
  - Simple and mature electrode pattern design
  - Least crosstalk among sensing channels
  - Single point sensing: buttons, sliders, wheels
- Mutual-cap Mode
  - Intrinsic good sensitivity and moisture immunity
  - Good pin utilization by matrix floor-plan
  - Easier pin routing
  - Single point sensing and Multipoint sensing
- High Performance in EMC
  - IEC61000-4-6 Certification by GRGTest
  - IEC61000-4-6 Certification by AUDIX



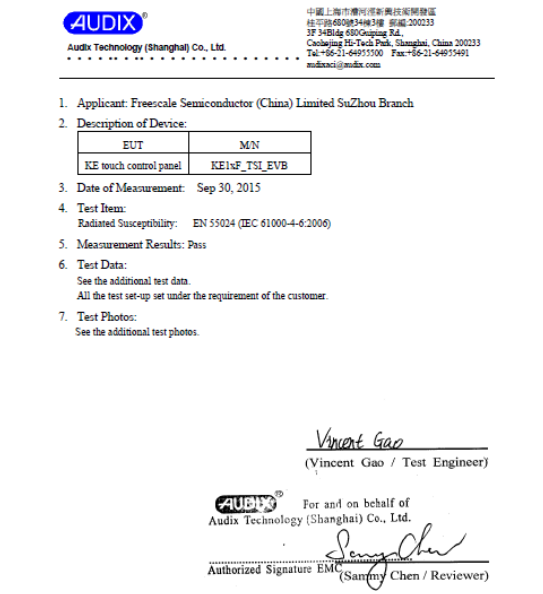
Self-cap Touch Sensor structure and Electric field



Mutual-cap Touch Sensor structure and Electric field

TSI Value Features

- ❑ Two operation modes
  - Self-cap: up to 25 keys
  - Mutual: up to 36 key
- ❑ Advanced robust in EMC
  - Pass IEC61000-4-6 standard test
- ❑ Advanced robust in waterproof
- ❑ High sensitivity and resolution
- ❑ No need for CPU interference
- ❑ Ease of use
  - NXP Touch Library support
  - SDK touch APIs support
- ❑ No need for external components


AUDIX
Audix Technology (Shanghai) Co., Ltd.

1. Applicant: Freescale Semiconductor (China) Limited SuZhou Branch
2. Description of Device:

EUT	M/N
KE touch control panel	KE1xF_TSI_EVB

3. Date of Measurement: Sep 30, 2015
4. Test Item: Radiated Susceptibility: EN 55024 (IEC 61000-4-6:2006)
5. Measurement Results: Pass
6. Test Data: See the additional test data. All the test set-up set under the requirement of the customer.
7. Test Photos: See the additional test photos.

Vincent Gao
(Vincent Gao / Test Engineer)

For and on behalf of Audix Technology (Shanghai) Co., Ltd.
Authorized Signature EMC
(Sammy Chen / Reviewer)

Power Efficiency

Feature	Benefit to Customer
Multiple power modes	Include HSRUN[1], RUN, WAIT, STOP, VLPR, VLPW, VLPS to save power Improve system power efficiency
Smart peripherals	Support working in low power modes Avoid frequently waking CPU and reduce power (TSI[2], LPUART, LPSPI, LPI2C, FlexIO, ADC, eDMA)

1: KE1xF only
2. KE15Z only

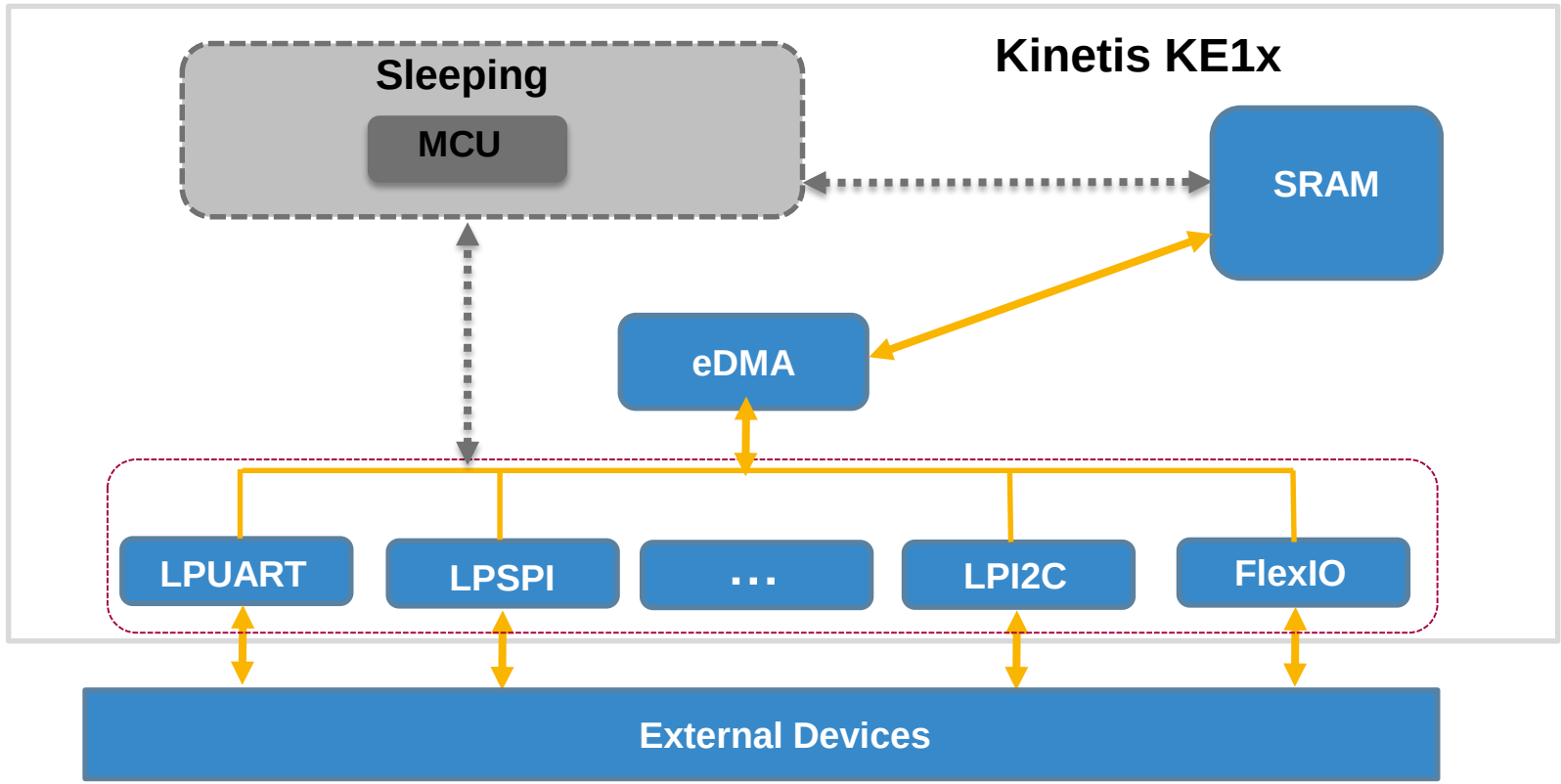
Power Efficiency – Multiple Power Modes

Expands beyond typical run, sleep, and deep sleep modes with power options to provide different power requirement based application

	Mode	Definition
RUN	**HSRUN(High speed Run)**	Allows maximum performance of chip. On-chip voltage regulator is on but with a slightly elevated voltage output. In this state, the MCU is able to operate at a faster frequency compared to normal run mode.
RUN	**Run**	Default mode out of reset; on-chip voltage regulator is on.
RUN	**VLPR (Very Low Power Run)**	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; internal oscillator provides a low power 4 MHz source for the core, the bus and the peripheral clocks.
SLEEP	**Wait**	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.
SLEEP	**VLPW (Very Low Power Wait)**	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.
DEEP SLEEP	**Stop**	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.
DEEP SLEEP	**VLPS (Very Low Power Stop)**	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but LPTMR, RTC, CMP, DAC can be used. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).

Power Efficiency – Smart Peripherals

LPUART, LPSPI, LPI2C, FlexIO also can work in WAIT/STOP modes, avoid frequently waking CPU and further reduce power consumption.



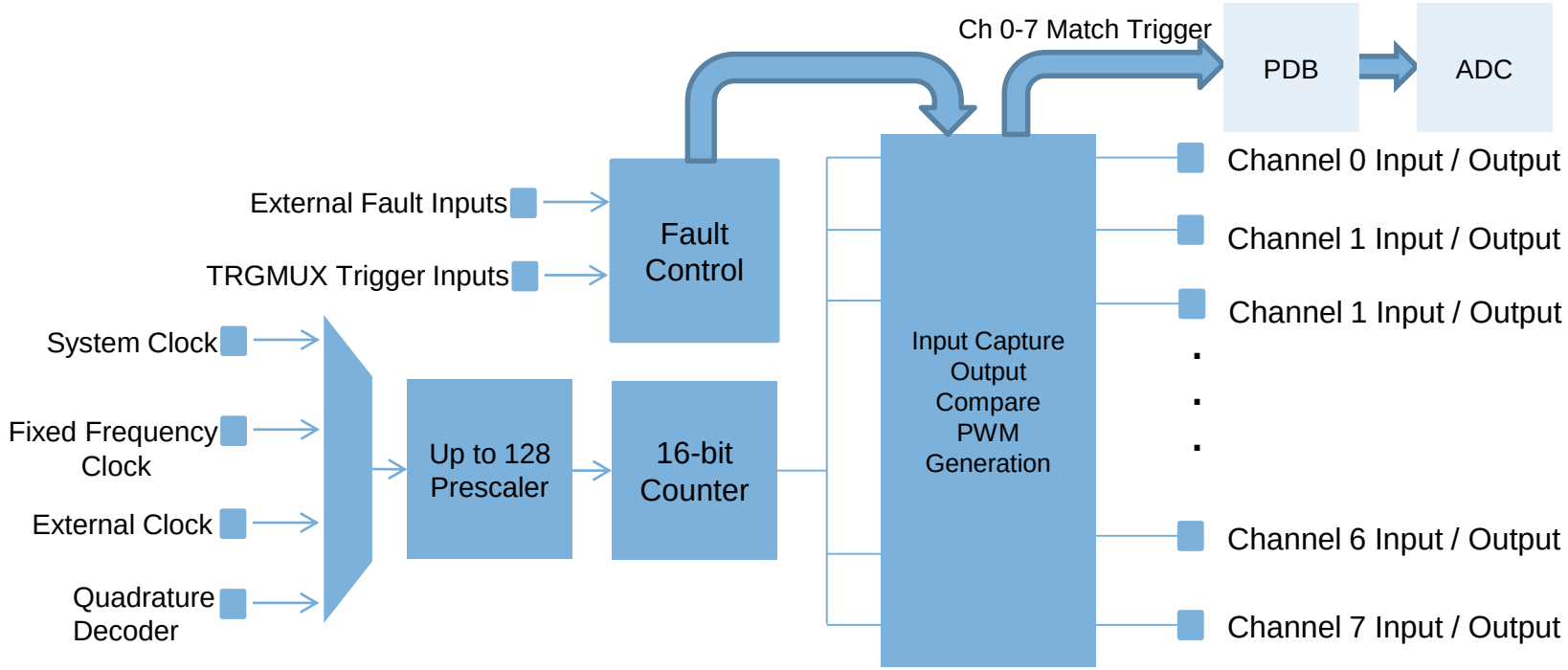
Analog and Peripherals

Feature	Benefit to Customer
1 Msps 12-bit ADC	More ADCs: KE1xF 3x, KE1xZ 2x Higher resolution and speed, improve the system performance
High performance FlexTimer	Support PWM & Motor control, Quadrature Decoder
PDB	More flexible internal trigger with ADC and Timers
FlexIO	More flexible for customized serial communication interface
FlexCAN[1]	Full implementation of CAN 2.0 version B protocol
FIFO	LPUART, LPSPI, LPI2C all with 4 word TX and RX FIFOs Higher speed in communication
BootROM	Support UART/SPI/I2C/CAN[1] interface, easier to upgrade the SW

1: KE16F and KE18F only

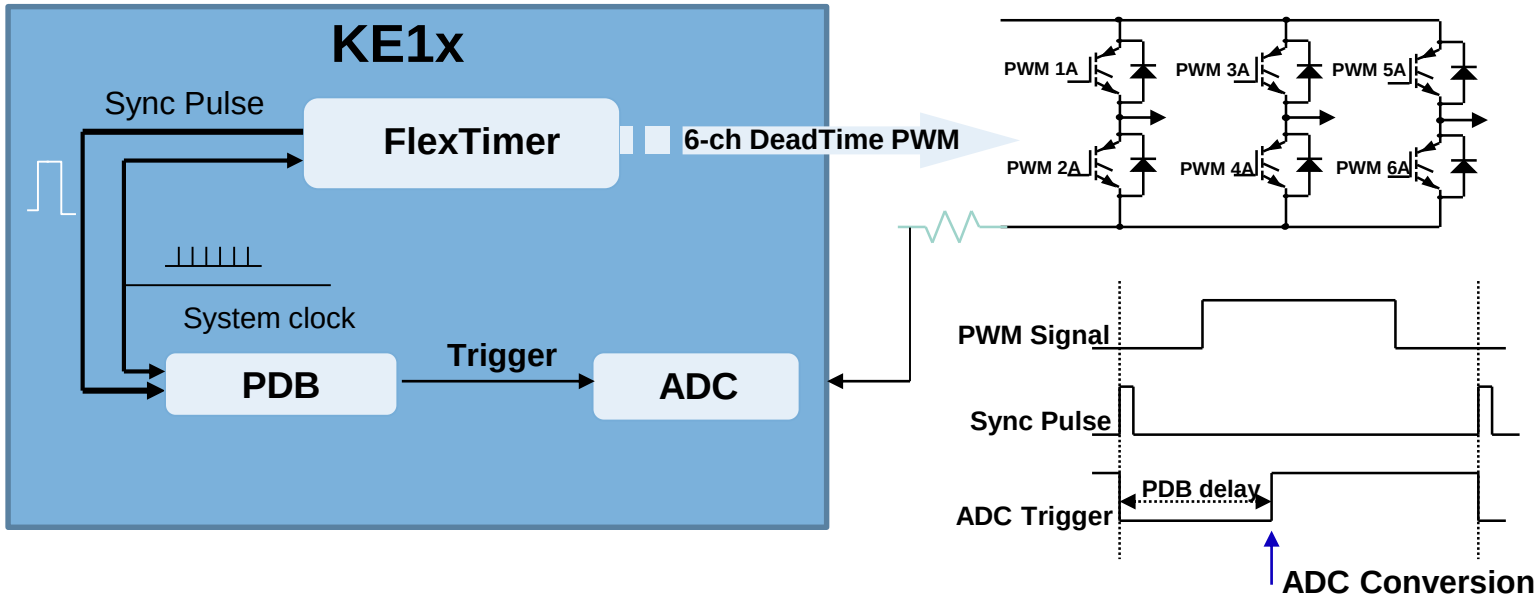
Analog and Peripherals – FlexTimer

- Clock source: system clock, fixed frequency clock, external clock
- 16-bit counter
  - Free-running or with initial and final value
  - Up or up-down
- Each channel can be configured for input capture, output compare, PWM generation mode
- Deadtime insertion
- Up to 4 fault inputs for global fault control
- Interrupt and trigger generation
- Quadrature Decoder (FTM1 and FTM2)



Analog and Peripherals - PDB

- Provides controllable delays from either an internal or an external trigger, or a programmable interval tick.
- Provide pulse outputs used as the sample window in CMP block.
- PDB triggering scheme is the default and suggested trigger method for ADC. One ADC and one PDB work as one pair.3×PDB generate triggers and pre-triggers for 3×ADC, each PDB channel will have up to 8 pre-triggers for ADC channel control, which provides an automatically trigger scheme so that the CPU involvement is not necessary.



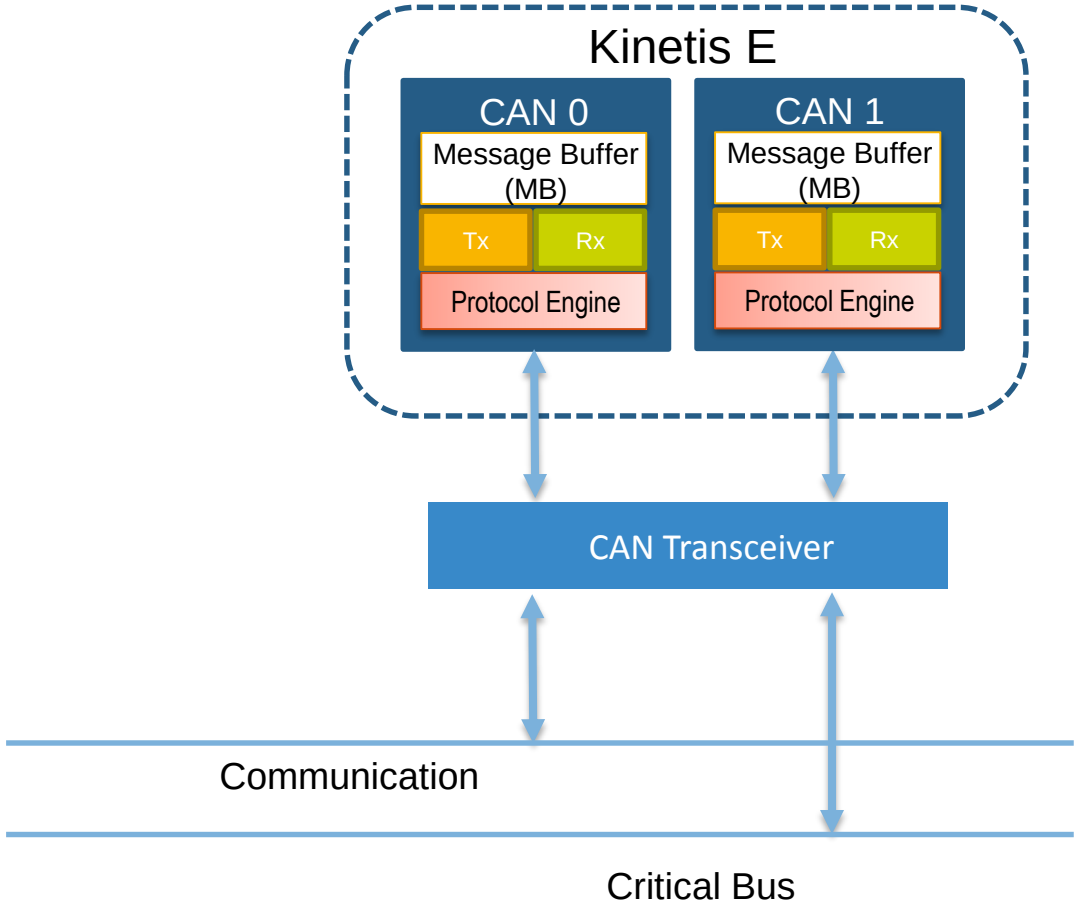
Analog and Peripherals – FlexIO

- A Highly configurable module that can emulate variety of serial communication protocols
  - UART
  - I2C
  - SPI
  - I2S
  - PWM / Waveform generation
  - Customized non-standard UART/I2C/SPI, etc
- Flexible 16-bit timers with support for a variety of trigger, reset, enable and disable conditions
- Programmable logic blocks allowing the implementation of digital logic functions on-chip
- Configurable interaction of internal and external modules Shifter concatenation to support large transfer sizes
- Programmable state machine for offloading basic system control functions from CPU

Analog and Peripherals – FlexCAN[1]

- Support up to **2x** CANs
- Full implementation of CAN 2.0 version B protocol
- Compliant with the ISO 11898-1 standard
- Support up to 16 message box (MBs)
- Each mailbox configurable as receive or transmit
- Configurable numbers of Tx/Rx buffers
- Support operational in VLPR and VLPW modes
- Very good programming models
- Time stamp support
- Bit time counting
- Listen-Only mode capability

1: KE16F and KE18F only



Analog and Peripherals – Boot ROM

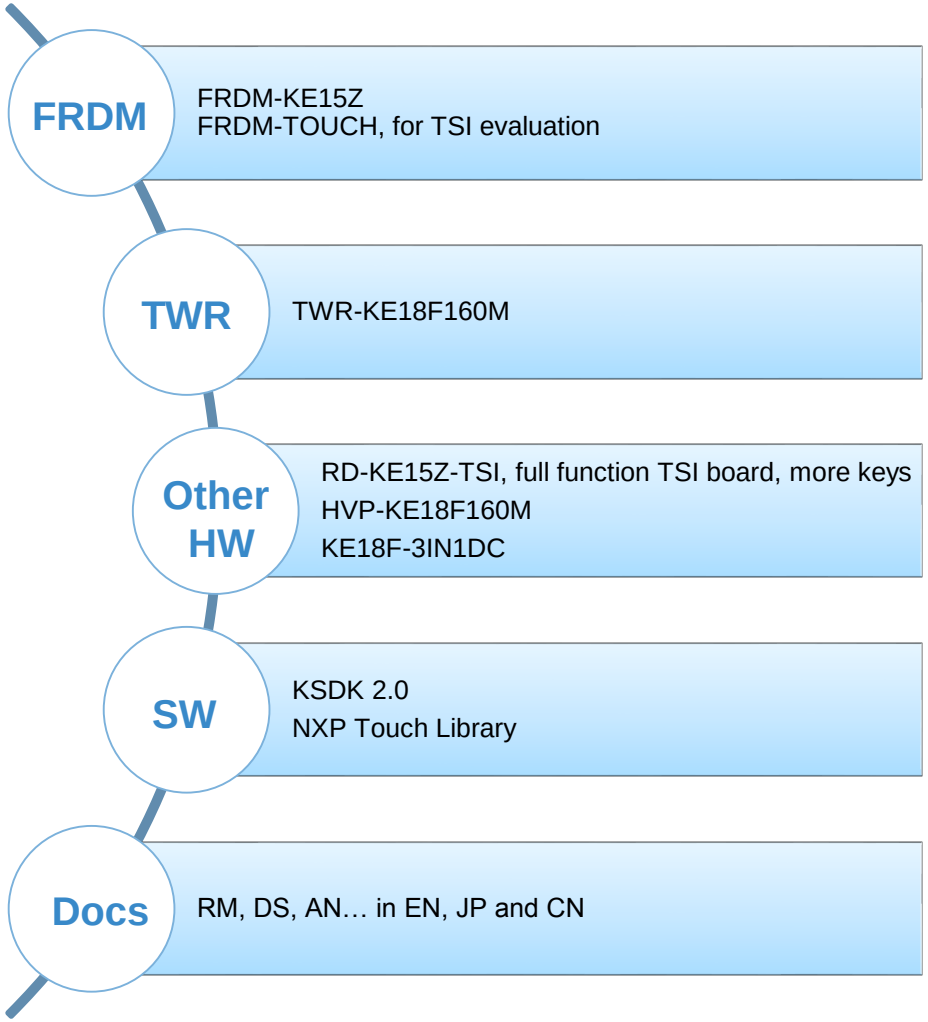
- The host can be a firmware-download application running on a PC or an embedded host
- Peripheral interface supported
  - CAN1
  - I2C
  - SPI
  - UART
  - Packet error detection and retransmission
  - Fully supports flash security (ex: mass erase or unlock security via the backdoor key)
  - Provides command to read properties of the device, such as flash and RAM size
  - Executing the boot loader either at system start-up or under application control at runtime

1: KE16F and KE18F only

ENABLEMENT

KE1x Enablement

- Software Tools
  - KDS, IAR, KEIL
  - KSDK Kinetis Software Development Kit
  - IEC60730 compliant library (Class B Safety S/W routines certified by VDE)
- Hardware Platform
  - Freedom development boards
  - Tower System development boards
- Reference Design / Evaluation
  - 3-in-1 motor control, dual motor control and PFC
  - High voltage motor control daughter board
  - Touch sensing in pad, slider and wheel



KE1x Enablement – Hardware Development Platforms

Freedom Platform

FRDM-KE15Z

- Ultra low-cost/power development platform
- Form factor compatible with Arduino platform
- Compatible with Freedom shield

Freedom Shield

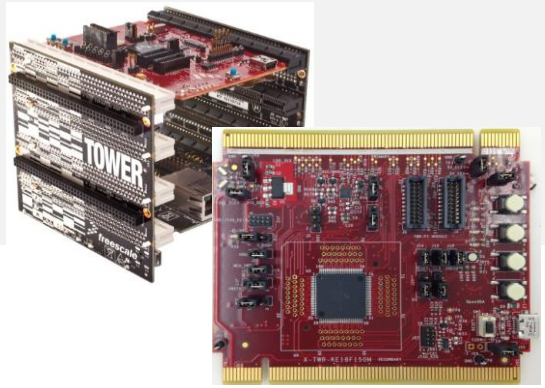
FRDM-TOUCH

- This evaluation board, in a shield form factor, effectively turns an NXP Freedom development board platform into a complete motor control reference design

Tower System

TWR-KE18F160M

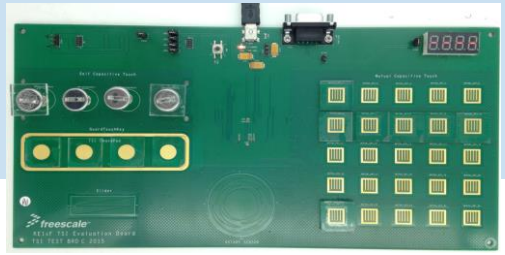
- Richer feature set
- Standard Tower Controller Module
- Compatible with existing Tower System peripherals



TSI Evaluation Board

RD-KE15Z-TSI

- Evaluation board for new TSI hardware and software design



Software, Professional Support & Services

- **Professional Services**
  - Managing Skills Gaps & Engineering Capacity
  - Global Staffing Capability
  - Vested Interest in Mutual Success
  - Graphic, Security, Linux/Android, Cloud, Connectivity
- **Complimentary Support**
  - NXP Boards
  - Communities
  - Technical Information Center
  - Customer Application & Technical Support
  - Distributor technical support
- **Hardware Services**
  - 1st Time Boot
  - Schematics & Layout Review
- **Professional Support**
  - Risk Reduction
  - Fast Answers
  - Hot Fixes
- **Complimentary Software & Tools**
  - Kinetis Design Studio, Software Development Kit, Pin Config, Power Estimator/Analyzer
  - THREAD, BLE, ZigBee, Bootloader, RTOS
  - Linux & Android BSP…
- **Software Products / Technology**
  - AVB, Miracast, HDCP2.x, TRLE, TEE, Home Kit, CarPlay, Android Auto, MICROEJ, Sensor Fusion, AUTOSAR, Connected Audio Solution, Graphic Tools, VisionECG, GPU Driver, AGL, Genivi, XBMC, HAB

SECURE CONNECTIONS
FOR A SMARTER WORLD

ATTRIBUTION STATEMENT