

# ULTRA SCALABLE: I.MX APPLICATION PROCESSORS

**SINGAPORE**

WOON SOCK KENG  
JULY 2016

PUBLIC USE



# i.MX Driving Explosive Growth in Automotive and Smart Devices



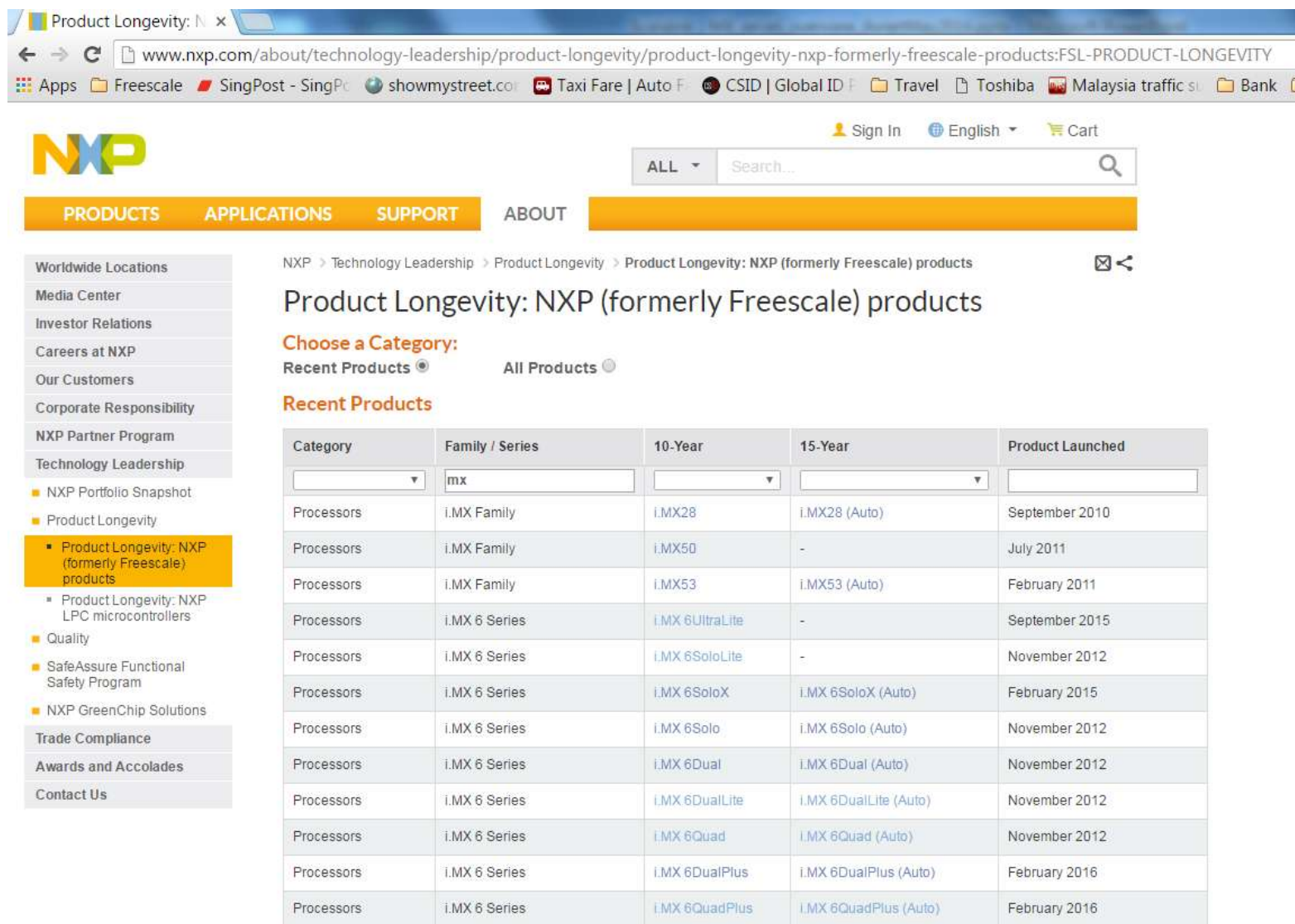
# i.MX Applications Processors Core Values

- **Scalability**
  - CPU (single/dual/quad, asymmetric), GPU, IO
  - Software: Linux, Android, QNX, Windows-embedded, RTOS
  - Industry leading ecosystem and partnerships
  - Pin compatibility and software portability
- **Integration**
  - Automotive/Industrial/Consumer peripheral sets
  - Qualifications: AEC-Q100, JEDEC Industrial and Consumer
- **Trust**
  - Market knowledge/expertise in industrial, consumer and automotive
  - Longevity: minimum of 10-15 years in all markets
  - Consistency of supply, product availability
  - Quality, robustness, zero-defect methodology
  - Security and Safety
- **Ease of Adoption**
  - Communities, innovation, support
  - Design collateral, distribution
  - System solutions: SoC, sensors, PMIC, IoT comms, SBC



# i.MX Product Longevity and Energy Efficiency Programs

For terms and conditions and to obtain a list of available products, visit [www.nxp.com/productlongevity](http://www.nxp.com/productlongevity)

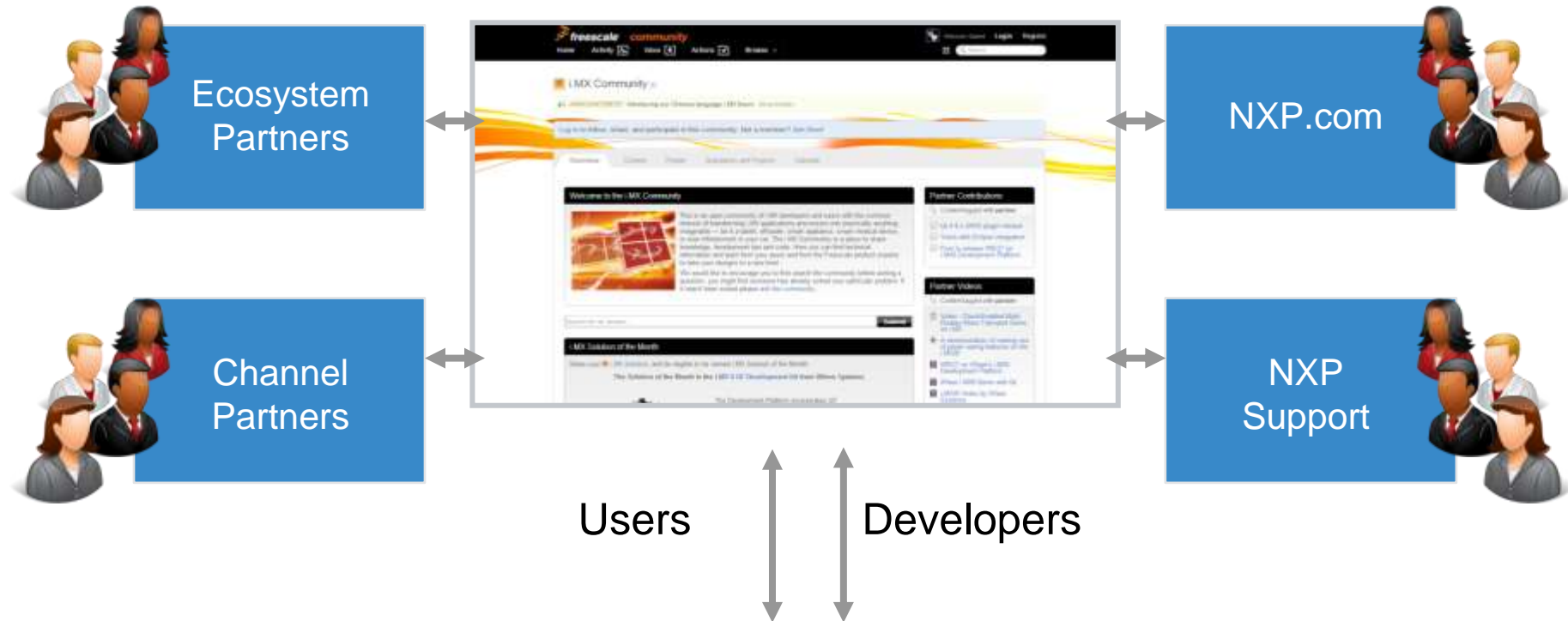


The screenshot shows the NXP website's 'Product Longevity' section. The page title is 'Product Longevity: NXP (formerly Freescale) products'. Below the title, there is a 'Choose a Category' section with 'Recent Products' selected. A table titled 'Recent Products' lists various i.MX processors and their longevity programs. The table has five columns: Category, Family / Series, 10-Year, 15-Year, and Product Launched. The table lists 13 rows of processors, including i.MX Family, i.MX 6 Series, and i.MX 6QuadPlus. The '10-Year' and '15-Year' columns show specific product names or series, and the 'Product Launched' column shows the date of launch.

Category	Family / Series	10-Year	15-Year	Product Launched
Processors	i.MX Family	i.MX28	i.MX28 (Auto)	September 2010
Processors	i.MX Family	i.MX50	-	July 2011
Processors	i.MX Family	i.MX53	i.MX53 (Auto)	February 2011
Processors	i.MX 6 Series	i.MX 6UltraLite	-	September 2015
Processors	i.MX 6 Series	i.MX 6SoloLite	-	November 2012
Processors	i.MX 6 Series	i.MX 6SoloX	i.MX 6SoloX (Auto)	February 2015
Processors	i.MX 6 Series	i.MX 6Solo	i.MX 6Solo (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6Dual	i.MX 6Dual (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6DualLite	i.MX 6DualLite (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6Quad	i.MX 6Quad (Auto)	November 2012
Processors	i.MX 6 Series	i.MX 6DualPlus	i.MX 6DualPlus (Auto)	February 2016
Processors	i.MX 6 Series	i.MX 6QuadPlus	i.MX 6QuadPlus (Auto)	February 2016



# iMXCommunity.org – Connect, Collaborate, Share



Greater than **4,000 members**

3500 **new content** added **every year**

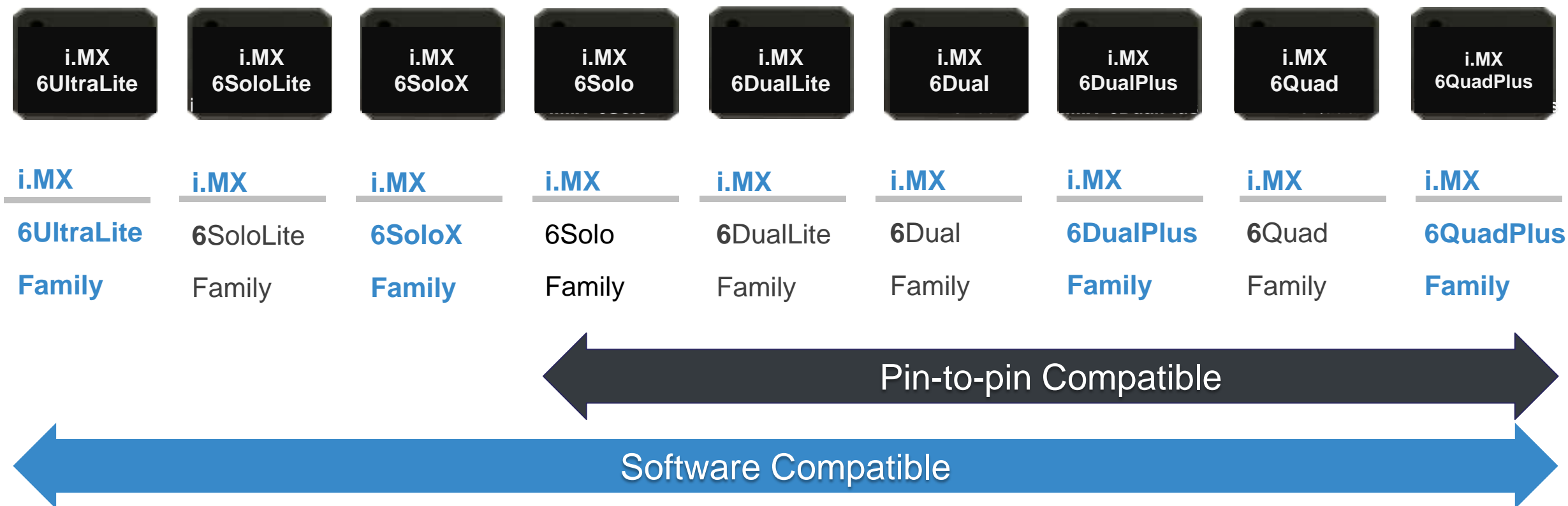
**Support and enablement** for i.MX processors and software – **share** tips, **ask** questions, **spark ideas**

Federated **search capability** integrated with our website

**Forums – Discussions – Groups – Blogs Posts – News – Multimedia Gallery – Training**

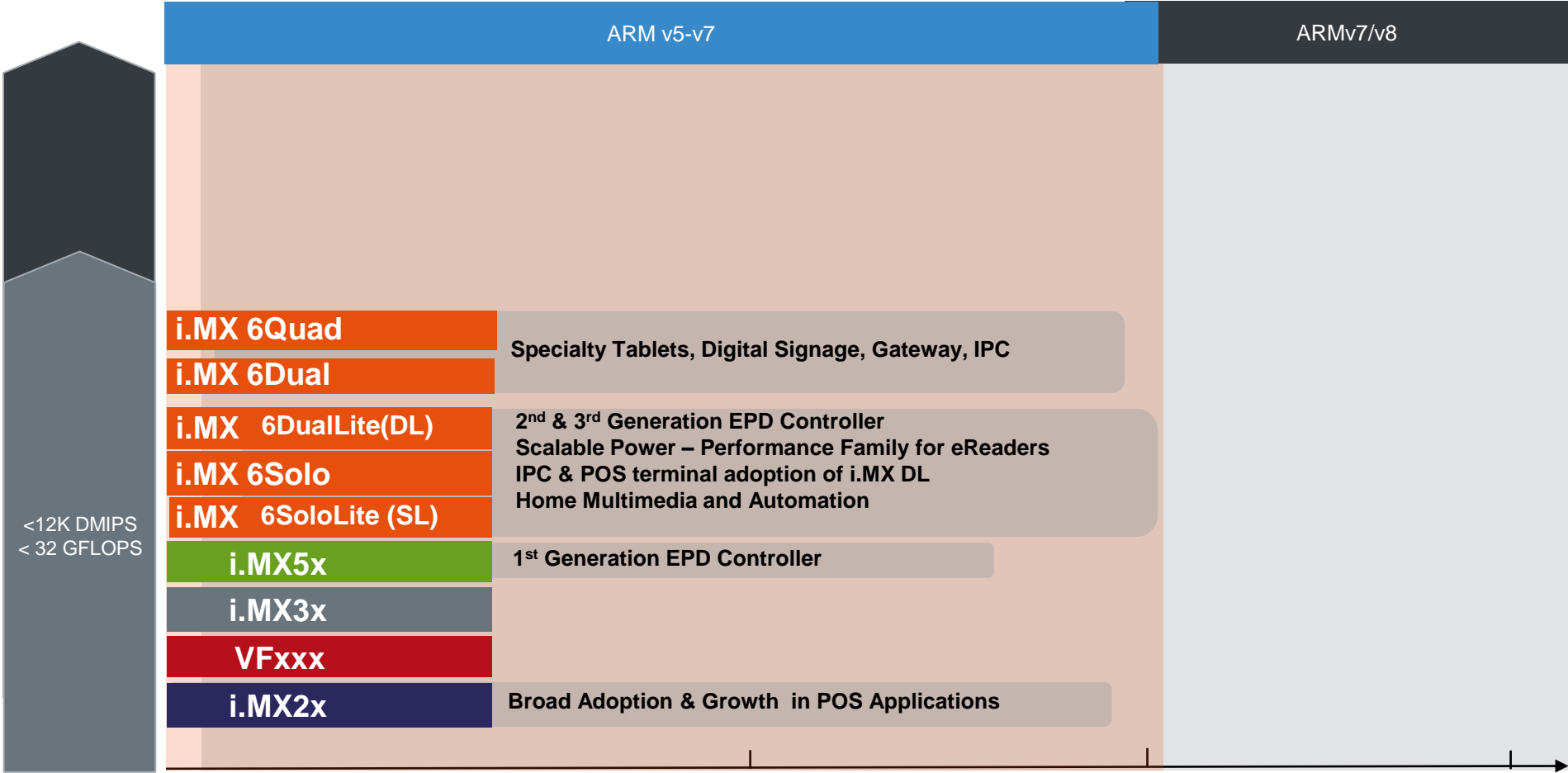
# i.MX 6 Series: Supreme Scalability and Flexibility

Scalable series of **NINE** ARM-based SoC Families



Expanded series for performance, power efficiency and lower BOM

# Applications Processor Family: Consumer and Industrial



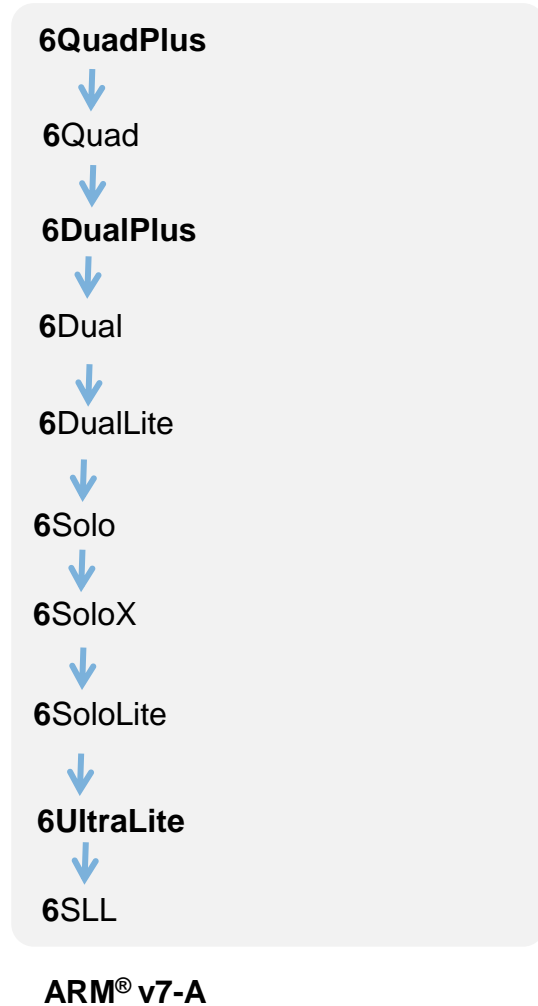
i.MX and VF-Series Products Available Prior to 2015

ARM9 Cortex-A8 A5+M4  
ARM11 Cortex-A9



# i.MX Processor Roadmap:

## Two New i.MX Platforms Based on 28nm Technology



### i.MX 8

Advanced Graphics  
& Performance

ARM® v8-A

### i.MX 7

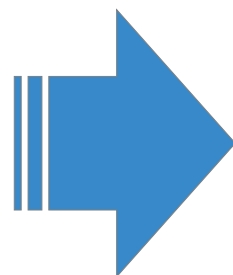
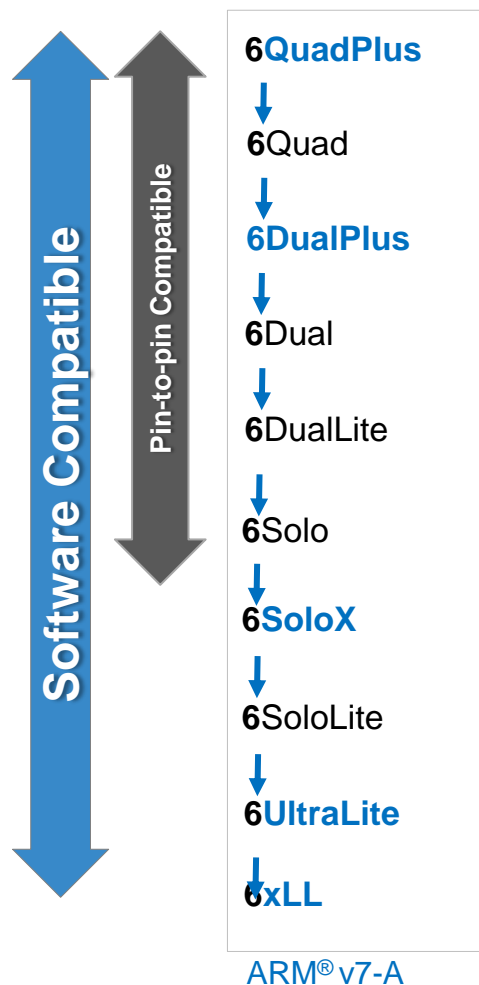
Power Efficiency

ARM® v7-A



72 °

# i.MX 8 Platform: 3 Series of Parts With Targeted Features



## i.MX 8 series

Advanced Graphics and Performance

ARM® v8-A  
(32-Bit / 64-Bit)

## i.MX 8M series

Advanced Audio and Video

ARM® v8-A  
(32-Bit / 64-Bit)

## i.MX 8X series

BOM and Energy Efficiency

ARM® v8-A  
(32-Bit / 64-Bit)



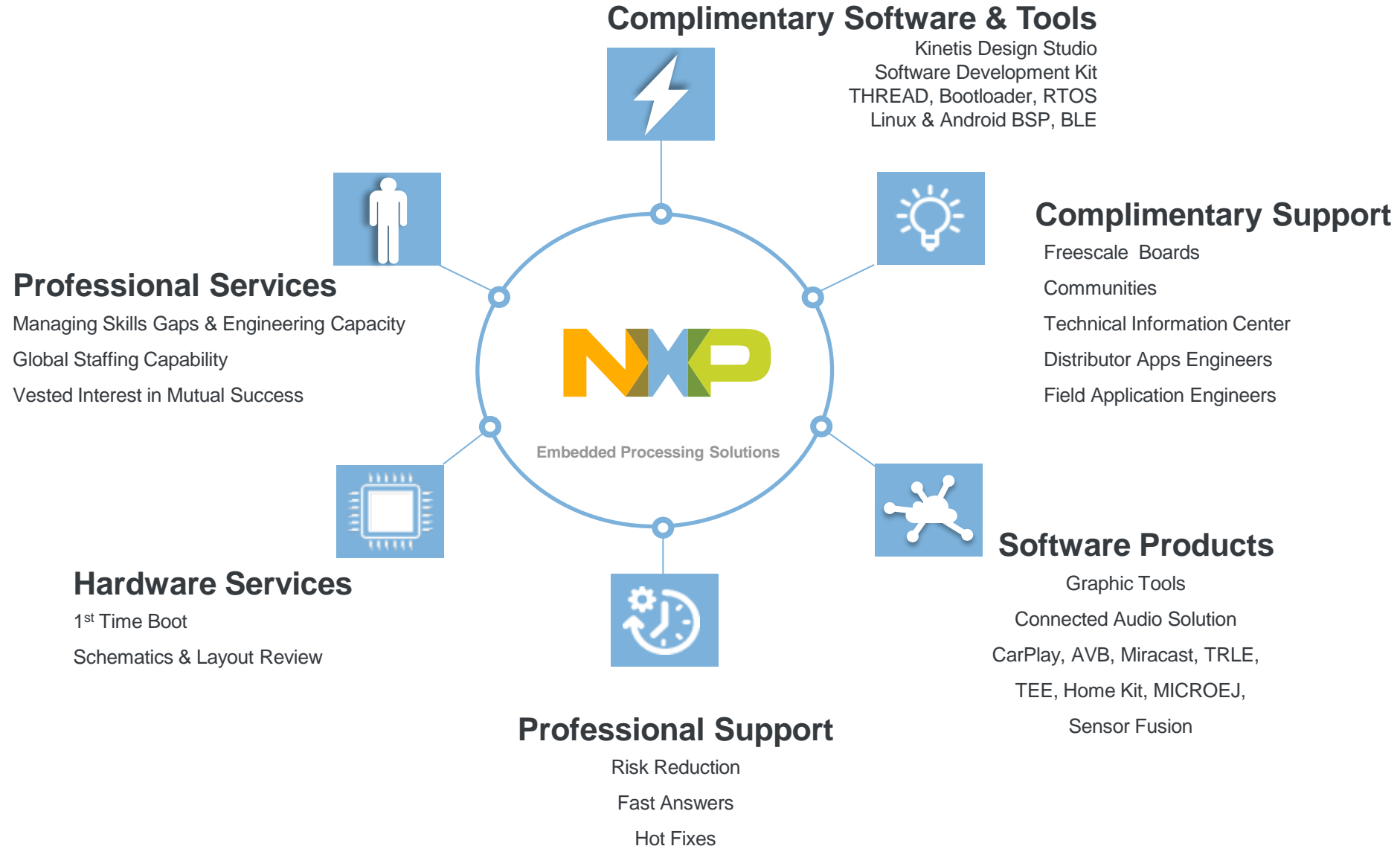
## i.MX 7

Power Efficiency & BOM Cost Optimizations

ARM® v7-A  
(32-Bit)



# Software, Professional Support & Services



# Enablement Through Reference Designs

## SABRE Platform for Smart Devices



- Builds on SABRE Board design with additional features including 10.1" capacitive multi-touch display, 2x MIPI camera sensors, SPI Nor Flash, GPS, ambient light sensor and digital microphones

Supported	Description
i.MX 6Quad i.MX 6Dual (emulated)	Quad-core 1-1.2 GHz ARM Cortex-A9 Dual-core 1-1.2 GHz ARM Cortex-A9
i.MX 6DualLite i.MX 6Solo (emulated)	Dual-core 1GHz ARM Cortex-A9 Single-core 1GHz ARM Cortex-A9

## SABRE for Auto Infotainment



- Support for terrestrial and satellite radio tuners, Wi-Fi, Bluetooth, GPS, cellular modem, iAP authentication modules, MOST vehicle networking, cameras and displays

Supported	Description
i.MX 6Quad i.MX 6Dual (emulated)	Quad-core 800MHz-1GHz ARM Cortex-A9 Dual-core 800MHz-1GHz ARM Cortex-A9
i.MX 6DualLite i.MX 6Solo (emulated)	Dual-core 800MHz ARM Cortex-A9 Single-core 800MHz ARM Cortex-A9
i.MX 6SoloX (Q3'15)	800MHz ARM Cortex-A9 200MHz ARM Cortex-M4

## SABRE Board for Smart Devices



- Multiple connectivity options: Wi-Fi®, Bluetooth®, GPS, Ethernet, SD, parallel/serial interfaces, SATA (i.MX 6Quad only), and PCIe

Supported	Description
i.MX 6Quad i.MX 6Dual (emulated)	Quad-core 1-1.2 GHz ARM Cortex-A9 Dual-core 1-1.2 GHz ARM Cortex-A9
i.MX 6SoloX	1GHz ARM Cortex-A9 200MHz ARM Cortex-M4

## i.MX 6SoloLite Evaluation Kit



- Enables EPD and/or LCD or HDMI display, touch control and audio playback, and the ability to add WLAN, a 3G modem or Bluetooth technology
- E-Ink display available separately

Supported	Description
i.MX 6SoloLite	Single-core 1GHz ARM Cortex-A9

# IMX 6DUALPLUS & 6QUADPLUS



# i.MX 6QuadPlus / i.MX 6DualPlus Applications Processor

- NXP identified multiple fabric and IP changes to improve the overall memory and graphics performance of the existing i.MX 6Dual/6Quad processors while minimizing software changes, resulting in the i.MX 6DualPlus/6QuadPlus family of processors
- **i.MX 6DualPlus/6QuadPlus key features:**
  - Updated 3D, 2D and OpenVG GPUs
  - New pre-fetch and resolve modules to improve efficiency (effective for improving performance and memory bandwidth utilization and decreasing bus load)
  - Fabric modifications to improve memory bandwidth
  - Pin compatible with existing i.MX 6Dual/6Quad processors
  - Multiple i.MX 6Dual/6Quad errata fixes

# i.MX 6DualPlus/i.MX 6QuadPlus Target Applications



## Automotive

- Infotainment
- Instrument Clusters



## Smart Devices

- Aerospace / Defense
- Digital Signage
- Health Care – patient monitoring, fitness equipment
- Factory, process and building automation (gateways, surveillance, HMI)
- Home entertainment, appliances
- Media Streaming
- Transportation - industrial vehicle with control & HMI, e.g. tractor, train, ship, heavy equipment

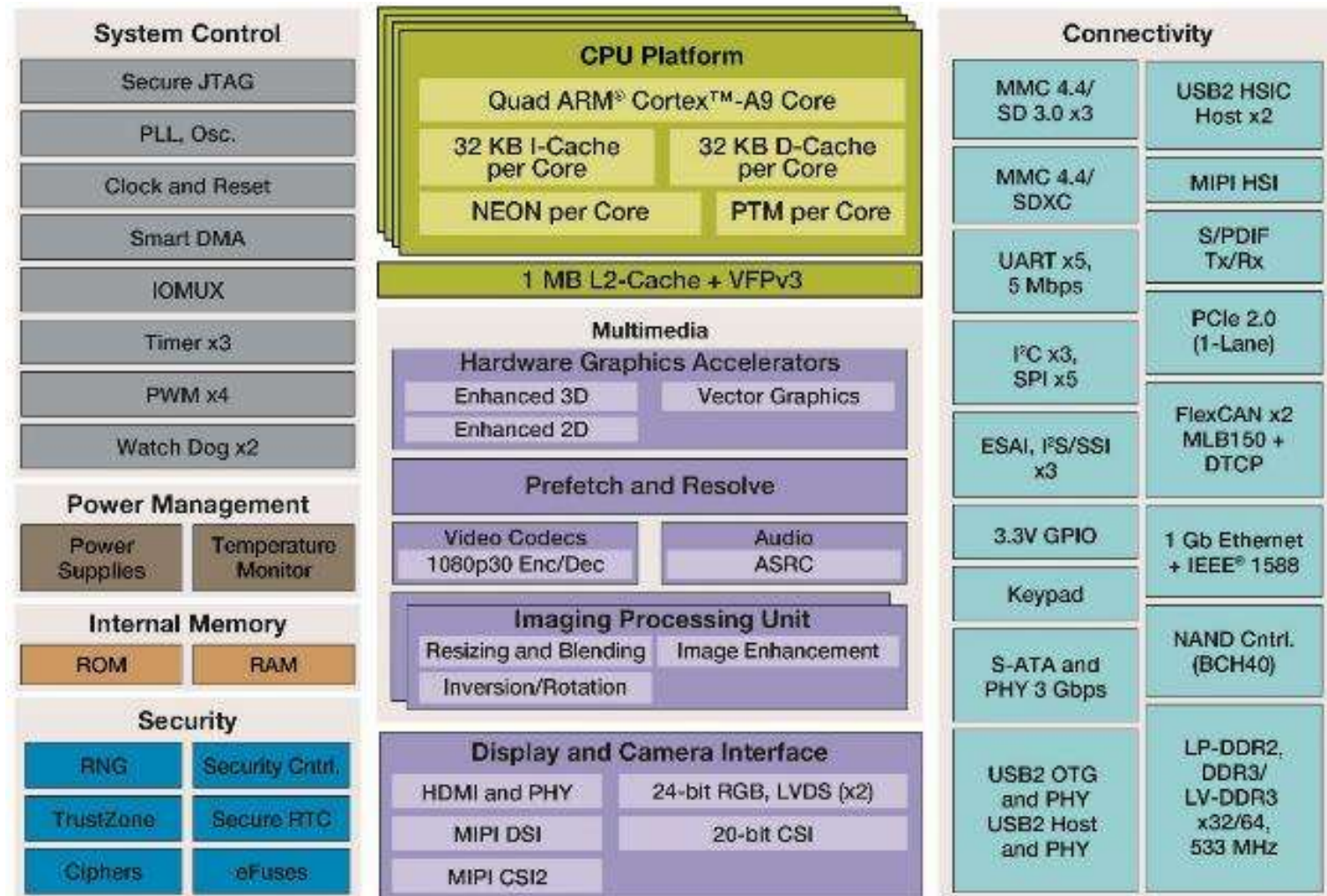


# i.MX 6QuadPlus/DualPlus Block Diagram

## Specifications

- **CPU:**
  - i.MX 6Quad**Plus**: **4x** Cortex-A9 @ 800MHz/852MHz/1GHz/1.2 GHz\*
  - i.MX 6Dual**Plus**: **2x** Cortex-A9 @ 800MHz/852MHz/1GHz/1.2 GHz\*
- **GPU:** GC2000+, 21.78 GFLOPS
- **Process:** 40nm
- **Package:** 21x21 0.8mm Flip-chip BGA
- **Temp Range (Tj):**
  - Auto -40 to 125C
  - Industrial -40 to 105C
  - Extended Commercial -20 to 105C
- **Pin compatible with i.MX 6Quad/6Dual**
- Up to 11,520 DMIPS

\* 1.0 GHz available now. For 1.2 GHz, contact NXP for availability



# SABRE Board for Smart Devices (SDB) – i.MX 6QuadPlus

Website: [www.nxp.com/sabresdb](http://www.nxp.com/sabresdb)

Part Numbers: MCIMX6QP-SDB (Feb 23, 2016)

Display (10.1"): MCIMX-LVDS1

Display (4.3"): MCIMX28LCD

## Overview

- NXP i.MX 6QuadPlus
  - i.MX 6DualPlus emulation on 6QuadPlus
- NXP MMPF0100 vF9 PMIC
- 1 GB DDR3 memory (non terminated)
- 3" x 7" 8-layer PCB

## Display Connectors

- 2x LVDS connectors
- Connector for 24 bit 4.3" 800x480 WVGA with 4-wire touch screen
- HDMI Connector

## Audio

- Audio Codec
- Microphone and headphone jacks

## Connectivity

- 2x full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector



## Debug

- JTAG connector
- Serial to USB connector

## Expansion Connector

- Enables parallel LCD or HDMI output
- Camera CSI port signals
- I2C, SSI, SPI signals

## Additional Features

- 3-axis NXP accelerometer
- eCompass
- Power supply
- No battery charger

## OS Support

- Linux and Android BSPs from NXP
- Others: 3<sup>rd</sup> parties

## Tools Support

- Lauterbach
- ARM (DS-5)
- Macraigor

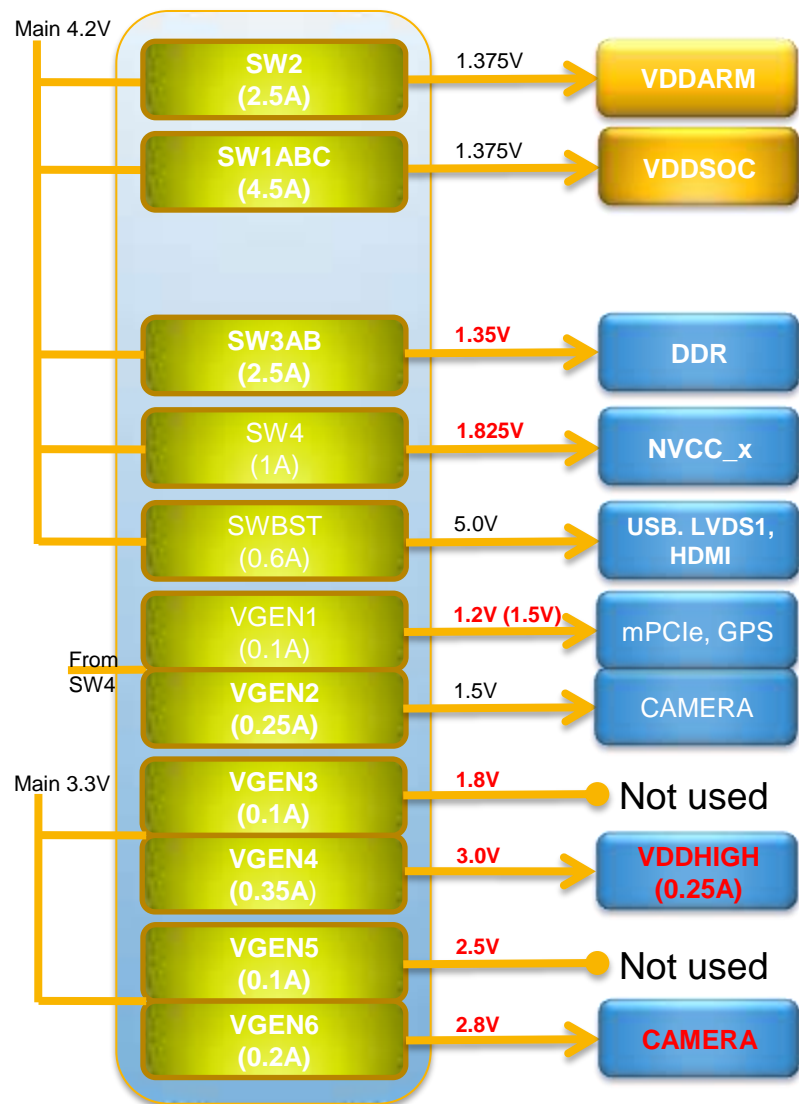
## WiFi: (not included with kit)

- Sillex WiFi module
- Murata WiFi module

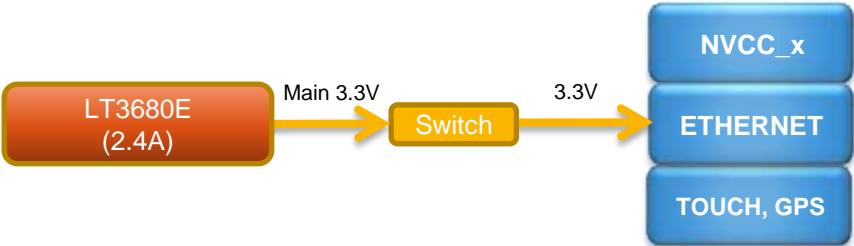
# Power

- Because of the changes to GPU, bus fabric and other modules in the VDD\_SOC domain, the maximum power consumption will increase compared to i.MX 6Dual/6Quad
- Customer applications that are DDR intensive may consume more power, including NVCC\_DRAM supply rail due to the increased throughput in the Plus' DRAM sub-system
- Datasheet provides max power numbers to help board/system designers budget for the power supply. Typical power numbers are lower.
- Power consumption is use case dependent and also varies with temperature of operation
- Various SW power management techniques are available in the BSP to help with power management in the customer application

# i.MX 6DualPlus/6QuadPlus SABRE SDB PF0100 Configuration



Power Sequence	
0	SNVS (not shown)
1	VGEN4
2	SW1ABC, SW2
3	SW3AB, VREFDDR
4	SW4, VGEN6
5	VGEN2, 3 & 5



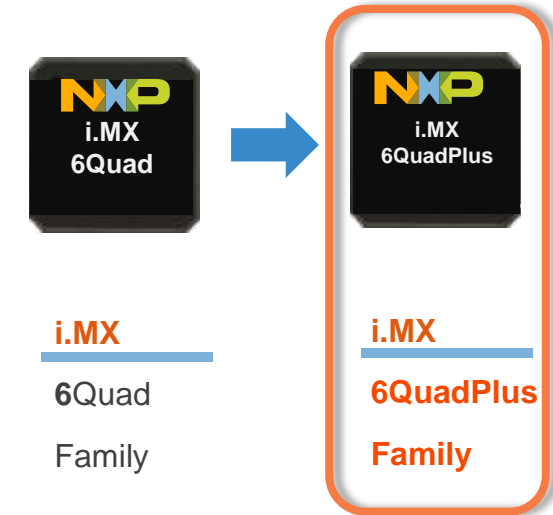
PF0100 Part Number: **MMPF0100F9ANES**  
(Recommended for Consumer and Industrial Applications)



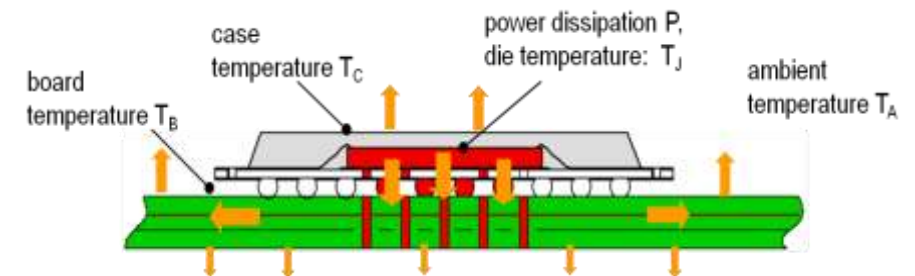
# Package & Thermals

- Plus uses the same package and ball map as i.MX 6Dual/6Quad
- VDD\_HIGH and VDD\_SNVS are specified to a maximum 3.3V in i.MX 6Dual/6Quad, in Plus the specified maximum is increased to 3.6V
- Improved thermal management may be required, compared to i.MX 6Dual/6Quad, due to the increased power consumption
- Software should take advantage of i.MX6 hardware features that allow power optimization
- Factor thermals in early in the Board Design process
- Run thermal simulations to get a holistic system thermal design & identify possible thermal bottlenecks
- NXP can provide Flotherm thermal models on request

## Same package and ball map



## Heat flow through the board



# Conclusion

- Major changes between the i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus processors
  - Updated 3D, 2D and OpenVG GPUs
  - New pre-fetch and resolve modules to improve efficiency
  - Fabric modifications to improve memory bandwidth
  - Increased On Chip RAM (OCRAM)
  - Multiple i.MX 6Dual/6Quad errata fixes
  - Pin compatible with existing i.MX 6Dual/6Quad processors
- Design changes required to migrate to the Plus processors
  - Increased power supply requirements for VDD\_SOC domain and DRAM sub-system
  - SW changes minimized to new IP modules and issue fixes
- PF0100 PMIC for use with Plus designs
- F9 PF0100 derivative, as used on the SABRE AI CPU3 and SABRE SDB Plus platforms
- Performance benchmarks between the i.MX 6Dual/6Quad and i.MX 6DualPlus/6QuadPlus processors
- Improved ARM performance
- Improved graphics and DRAM performance

# Q & A

- i.MX 6QuadPlus Product Summary Page:

- <http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-6-processors/i.mx6qp/i.mx-6quadplus-processor-quad-core-high-performance-advanced-3d-graphics-hd-video-advanced-multimedia-arm-cortex-a9-core:i.MX6QP>

- i.MX 6DualPlus Product Summary Page:

- <http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-6-processors/i.mx6qp/i.mx-6dualplus-processor-dual-core-high-performance-advanced-3d-graphics-hd-video-advanced-multimedia-arm-cortex-a9-core:i.MX6DP>

- i.MX 6 Sabre Tool Summary Page:

- [www.nxp.com/imx6tools](http://www.nxp.com/imx6tools)

Contact your local NXP representative

# FAQ

Q: Was the VPU enhanced and did the VPU performance change on Plus?

A: Same IP for the VPU on Plus, however users can expect improved performance in multi-master use cases using the VPU due to fabric enhancements discussed.

Q: Is the PMIC configuration proposed for Plus backward compatible to 6Dual/6Quad ?

A: Yes, we recommend all new 6Dual/6Quad to use this new configuration to allow for future upgrades to the Plus

Q: What guidelines should I follow if I am starting a new design with the i.MX 6Dual/6Quad and i.MX 6DualPlus/QuadPlus?

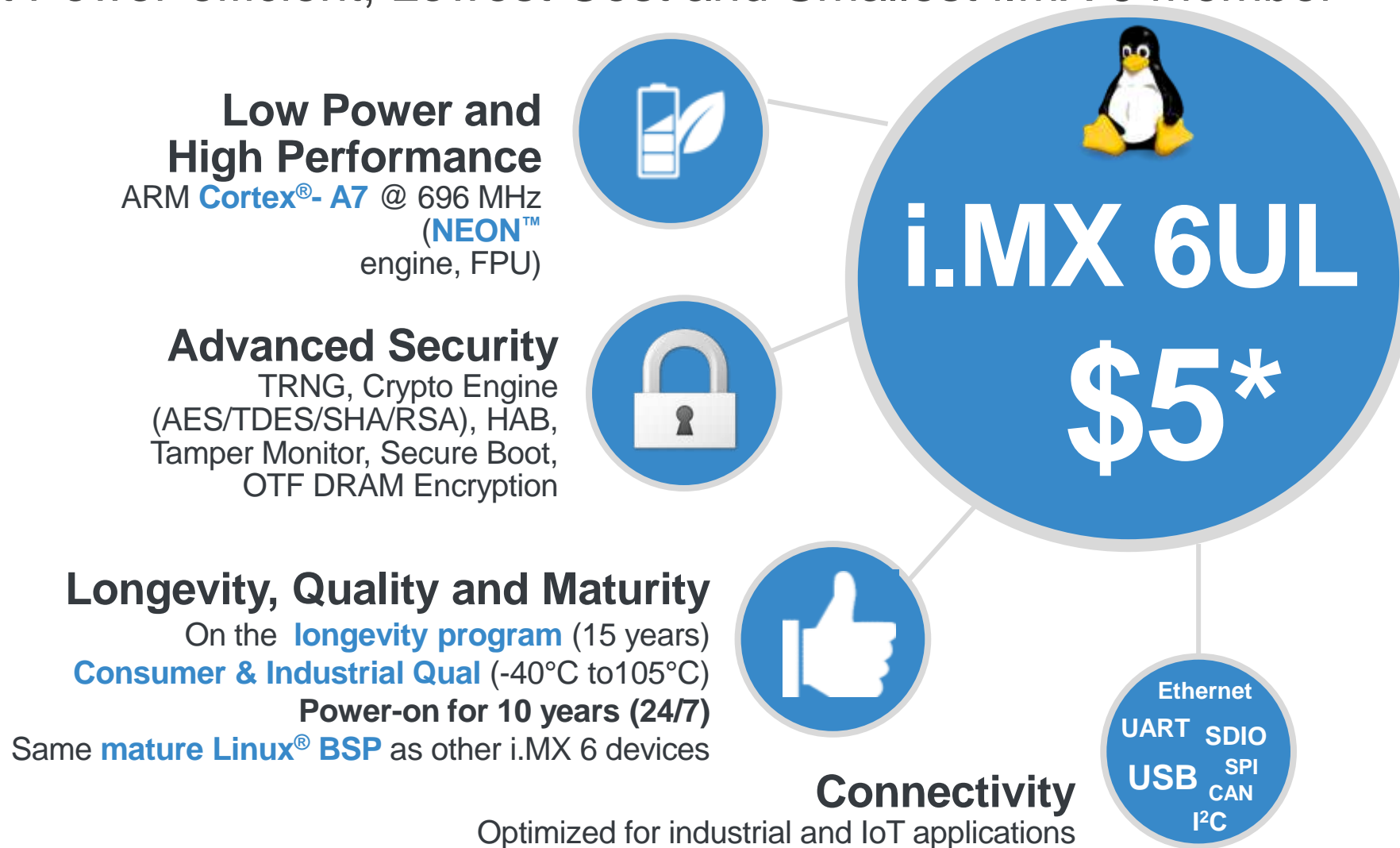
A: For new designs it is recommended to use F9, FA or similar custom OTP flavor of the PF0100 for powering the system. This provides a single power solution for i.MX 6Dual/6Quad and i.MX 6DualPlus/QuadPlus while also providing sufficient margin for the worst case load currents.

# IMX 6ULTRALITE



# i.MX 6UltraLite

The Most Power-efficient, Lowest Cost and Smallest i.MX 6 Member



# i.MX 6UltraLite Target Applications



## Industrial HMI

- XGA industrial HMI with basic UI
- Large or high-quality small appliance
- Industrial scanner or printer
- Vending machine with display and basic UI



## Building Control

- Access control (security) panel
- Surveillance monitoring
- Building control, e.g. elevator or automated door



## Medical

- Mobile patient care, e.g. infusion pump or respirator
- Blood pressure monitor
- Activity and wellness monitor
- Exercise equipment with display



## Integrated Connectivity

- Wired and wireless audio streaming
- Energy management hub
- Industrial gateway
- VoIP



## Financial Payment

- Point of Sale
- Financial payment system

# i.MX 6UltraLite Evaluation Kit Key Features

**Part Numbers:** MCIMX6UL-EVKB (\$149)

**Display (4.3"):** LCD8000-43T (\$100)

## Processor

- NXP Semiconductors i.MX 6UltraLite 528MHz ARM® Cortex™-A7 CPU

## Memory

- 4Gb DDR3L DRAM memory
- 256Mb Quad SPI Flash
- Footprint for NAND
- Footprint for eMMC
- TF socket for boot

## Display

- Parallel WVGA LCD add-on card via expansion connector
- Camera Connector

## Audio

- Audio Codec
- 4-pole Audio Headphone Jack
- External speaker connection
- Microphone

## Connectivity

- USB Host connector
- Micro USB OTG connector
- Two Ethernet (10/100T) connector
- SD/SDIO Connector
- Two CAN Transceivers
- EMV Smart Card connector

## Debug

- JTAG connector
- Serial to USB connector

## Sensors

- Footprint for FXAS21000CQR1 Gyro
- FXLS8471Q three-axis digital accelerometer
- MAG3110 Digital eCompass

## Tools & OS Support

- Linux® BSPs from NXP Semiconductors

## Others

- CPU Module: 1.67x2.66 inch
- Base Board: 4.25x5.12 inch
- 4 layer through hole PCB



# BOARD BRING-UP: WHERE DDR BRING- UP FITS IN

# i.MX 6UL MMDC Overview

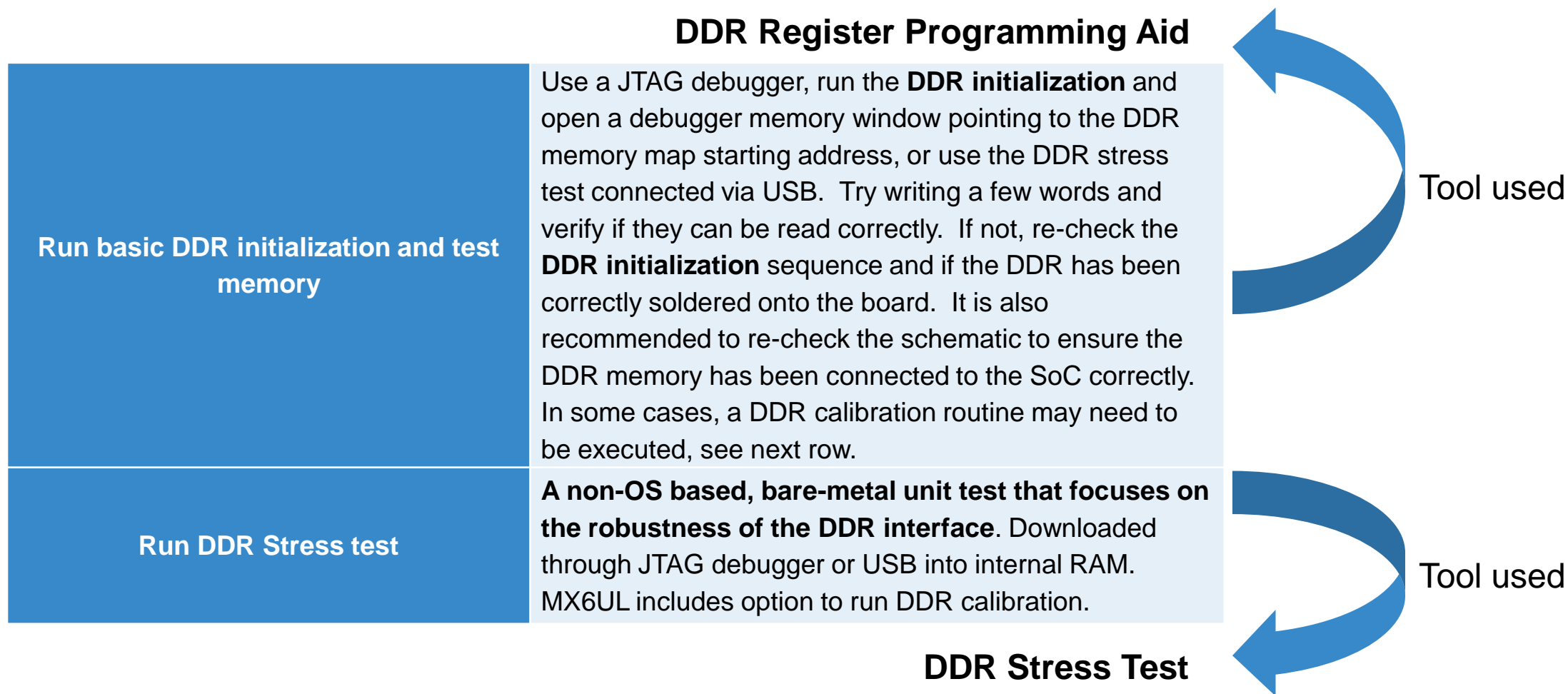
## DDR Initialization

- i.MX 6UL MMDC is used to program DDR device for proper operation
  - Achieved by initialization sequence of specific register writes prior to accessing external DDR device
- DDR initialization is dependent on various factors such as:
  - DDR type (DDR3 or LPDDR2)
  - DDR memory timing and speed grade
  - Bus width (x16 only)
  - Drive Strength and Board/Memory layout (Fly-by, T topology)
- Common programming recommendations cannot be provided as they will be unique for each customer design based on the above factors
- NXP provides a DDR Register Programming Aid to help in configuring these specific parameters as well as DDR stress test that optimizes and tests the DDR interface

# Board Bring-Up and Debug Checklist

Checklist Item
The following items need to be completed serially
Visual Inspection
Verify all SoC voltage rails
Verify power up sequence
Measure/probe input clocks (32kHz, 24MHz, others)
JTAG connectivity (DS-5, RV-ICE, Lauterbach, Macraigor, etc)
Access internal RAM
<b>Run basic DDR initialization and test memory</b>
<b>Run DDR Stress test</b>
The following items may be worked on in parallel with other bring up tasks
Verify CLK0 outputs (measure and verify default clock frequencies for desired clock output options); this assumes that the board design supports probing of the CLK0 pin.
Measure boot mode frequencies (set the boot mode switch for each boot mode and measure the following, depending on what is available in the system): <ul style="list-style-type: none"><li>- NAND (probe CE to verify boot, measure RE frequency)</li><li>- SPI-NOR (probe slave select and measure clock freq)</li><li>- MMC/SD (measure clock freq)</li></ul>
Run other unit tests

# Tools for DDR Bring-up and debug



# Recommended Flow and Tools for Optimal DDR Initialization

**Create initial DDR initialization script**

- Use the **DDR Register Programming Aid**
- Input values from Memory vendor datasheet

**Perform calibration to optimize script**

- Use the **DDR Stress Test : Calibration Routine**
- Generates optimal calibration values

**Validate DDR interface with optimized script**

- Use **DDR Stress Test : Memory Sub routines**
- Using updated calibration values

# DDR REGISTER PROGRAMMING AID



# i.MX 6UL DDR Register Programming Aid

## Intro

- DDR Register Programming Aid creates JEDEC compliant sequence to initialize DDR memory and interface
  - IOMUX register writes to set i.MX 6UL DDR IO drive strength
  - MMDC register writes and DDR mode register writes
- Mainly used to program JEDEC timing and DDR parameters
  - Timings: tRCD, tRC, tRFC, etc; Parameters: rows, cols, bank address, and chip selects
  - Memory timing information obtained from DDR vendor datasheet for respective speed grade and density
- Automatically generates DDR initialization scripts
  - For specific memory types (DDR3 or LPDDR2)
  - For ARM RVD (.inc file) and ARM DS5 (.ds file) debugger formats
  - Scripts can be converted by user to DCD format for inclusion in SW OS Bootloader
- Developed based on NXP development boards; can be customized by user for their board design

# i.MX 6UL DDR Register Programming Aid

## Intro

- Each Programming Aid tool based on DDR technology: DDR3 or LPDDR2
- Useful for quickly changing parameters:
  - Drive strength, user selects via pull down menu
  - DDR Mode register settings – configures mode register “word” to send to the DDR
- Calibration fields highlighted for user update
- Applies correct order of programming MMDC registers
- Detailed instructions on how to generate custom scripts

How to use the DRAM register programming aid outline

Step 1. Obtain the desired DRAM data sheet from the DRAM vendor

The following are to be completed in the Register Configuration Worksheet tab.

How To Use **Register Configuration** DStream .ds file

Step 2. Update the Device Information table to include the DRAM information and system usage

Device Information	
Memory type	DDR3
Manufacturer	Micron
Memory part number	MT41J128M16HA-1GE
Density of each DDR3 device (Gb)	2
Number of DRAM devices per chip select	4
Density per chip select (Gb)	8
Number of Chip Selects used	2
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Number of BANKS	8
Bus Width (input 16, 32, or 64 bits)	64
Clock Cycle Freq (MHz)	533
Clock Cycle Time (ns)	1.875

Step 3. Go through the various shaded cells in the spread sheet to update with data from the DRAM sheet (take special note of the “Legend” table to ascertain the meaning of different shaded cells; in many cases, the cells may not need to be updated).

Instructions	Legend
Shaded cells may require updating per the DRAM memory data sheet parameters. Certain registers should not need to be modified by the user. If a register is not provided then it is assumed this parameter is not to be changed per the provided initialization script or that the register is read-only. Certain registers are provided though they may be noted as recommended to not change.	On Register Configuration Tab, this color indicates the bitfields that would commonly require updating.
	On Register Configuration Tab, this color indicates the bitfields that may be updated, but should typically not require it.
	On Register Configuration Tab, this color indicates the bitfields that are updated automatically from setting provided in the “Device Information” table or other cells, and should not be changed manually.
	On Register Configuration Tab, an unshaded cell means that the value should remain as is and should not be modified. In these cases, the settings are provided for completeness.
	On other tabs, this color indicates the cells that are affected by changes on the Register Configuration tab. Note, this cell shading should not be used in this worksheet Register Configuration tab, only in other tabs that are affected by cells in this tab.

The following refers to the “DStream .ds file” Worksheet tab. In this tab, the entire DRAM initialization can be obtained. This initialization can be used as a DStream .ds file (see below) or as reference for the bootloader DRAM initialization.

How To Use **Register Configuration** **DStream .ds file**

Step 4. Go to the “DStream .ds file” file worksheet tab and copy and paste this into a text document (make sure to rename the document with a “.ds” file ending); this is ready to use with the ARM DStream development system.

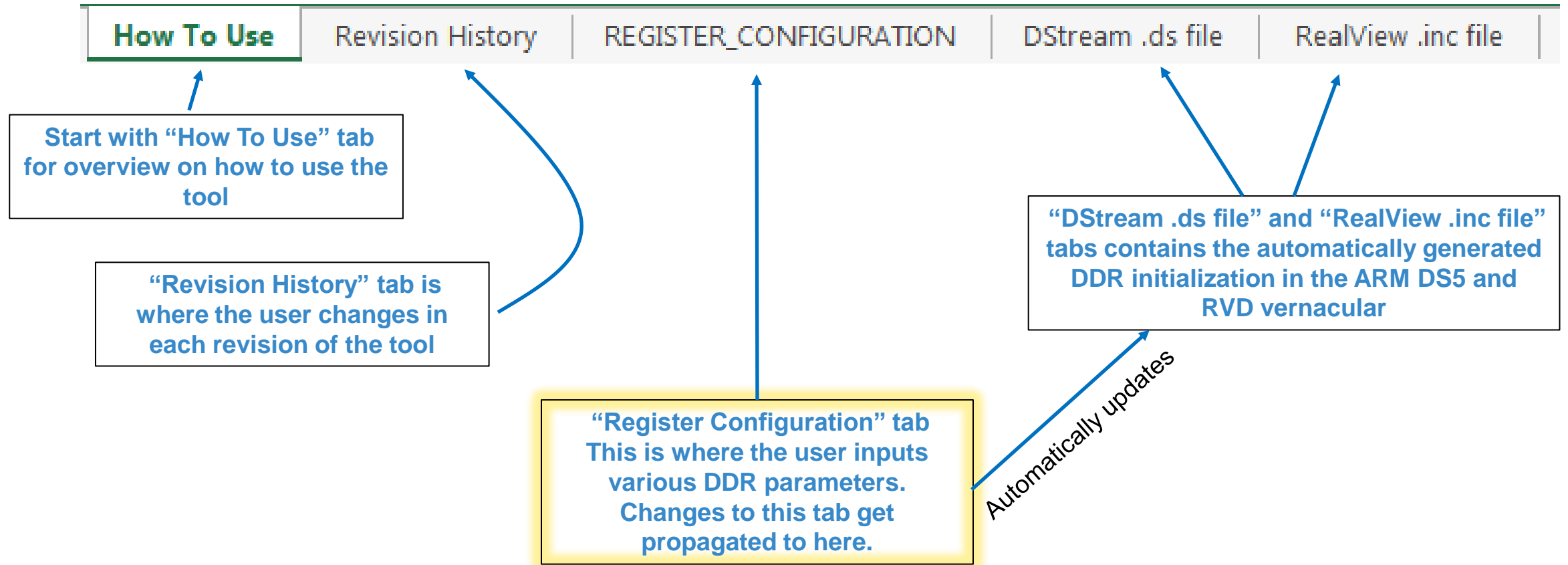
Step 5. This .ds file can also be used as a reference for other debugger tools and bootloaders.

Note, there are some commands that are specific for the DSS debugger and are noted in the “Dstream .ds file” work sheet. These commands should be commented out or removed for use in bootloaders or non-debugger based DDR stress tests (for example, when using a USB loadable DDR stress test)

# i.MX 6UL DDR Register Programming Aid

## Walkthrough

There are several tabs (worksheets), described below



# i.MX 6UL DDR Register Programming Aid

## Walkthrough

Debugger scripts automatically generated

[How To Use](#) [Revision History](#) [REGISTER\\_CONFIGURATION](#) [DStream .ds file](#) [RealView .inc file](#)

DStream .ds file format

```
#=====
#init script for i.MX6UL          DDR3
#=====
# Revision History
# 0.3
#=====

stop                                # needed when using DS5 debugger, remove if not using a debugger

set semihosting enabled true        # needed when using DS5 debugger, remove if not using a debugger

memory 0x00B00000 0x0BFFFFFF neverify # needed when using DS5 debugger, remove if not using a debugger

#=====
# Disable WDOG
#=====
#memory set 0x020BC000 16 0x30

#=====
# Enable all clocks (they are disabled by ROM code)
#=====
memory set 0x020c4068 32 0xffffffff #[CCM_CGCR0]CCM Clock Gating Register 0
memory set 0x020c406c 32 0xffffffff #[CCM_CGCR1]CCM Clock Gating Register 1
memory set 0x020c4070 32 0xffffffff #[CCM_CGCR2]CCM Clock Gating Register 2
memory set 0x020c4074 32 0xffffffff #[CCM_CGCR3]CCM Clock Gating Register 3
memory set 0x020c4078 32 0xffffffff #[CCM_CGCR4]CCM Clock Gating Register 4
memory set 0x020c407c 32 0xffffffff #[CCM_CGCR5]CCM Clock Gating Register 5
memory set 0x020c4080 32 0xffffffff #[CCM_CGCR6]CCM Clock Gating Register 6

#=====
# IOMUX
#=====
#DDR IO TYPE:
memory set 0x020E04B4 32 0x000C0000 # IOMUXC_SW_PAD_CTL_GRP_DDR_TYPE
memory set 0x020E04AC 32 0x00000000 # IOMUXC_SW_PAD_CTL_GRP_DDRPKE

#CLOCK:
memory set 0x020E027C 32 0x00000030 # IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P
```

RealView .inc file format

```
#=====
#init script for i.MX6UL          DDR3
#=====
# Revision History
# 0.3
#=====

stop                                # needed when using DS5 debugger, remove if not using a debugger

set semihosting enabled true        # needed when using DS5 debugger, remove if not using a debugger

memory 0x00B00000 0x0BFFFFFF neverify # needed when using DS5 debugger, remove if not using a debugger

#=====
# Disable WDOG
#=====
#memory set 0x020BC000 16 0x30

#=====
# Enable all clocks (they are disabled by ROM code)
#=====
memory set 0x020c4068 32 0xffffffff #[CCM_CGCR0]CCM Clock Gating Register 0
memory set 0x020c406c 32 0xffffffff #[CCM_CGCR1]CCM Clock Gating Register 1
memory set 0x020c4070 32 0xffffffff #[CCM_CGCR2]CCM Clock Gating Register 2
memory set 0x020c4074 32 0xffffffff #[CCM_CGCR3]CCM Clock Gating Register 3
memory set 0x020c4078 32 0xffffffff #[CCM_CGCR4]CCM Clock Gating Register 4
memory set 0x020c407c 32 0xffffffff #[CCM_CGCR5]CCM Clock Gating Register 5
memory set 0x020c4080 32 0xffffffff #[CCM_CGCR6]CCM Clock Gating Register 6

#=====
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#CLOCK:
memory set 0x020E027C 32 0x00000030 # IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P
```

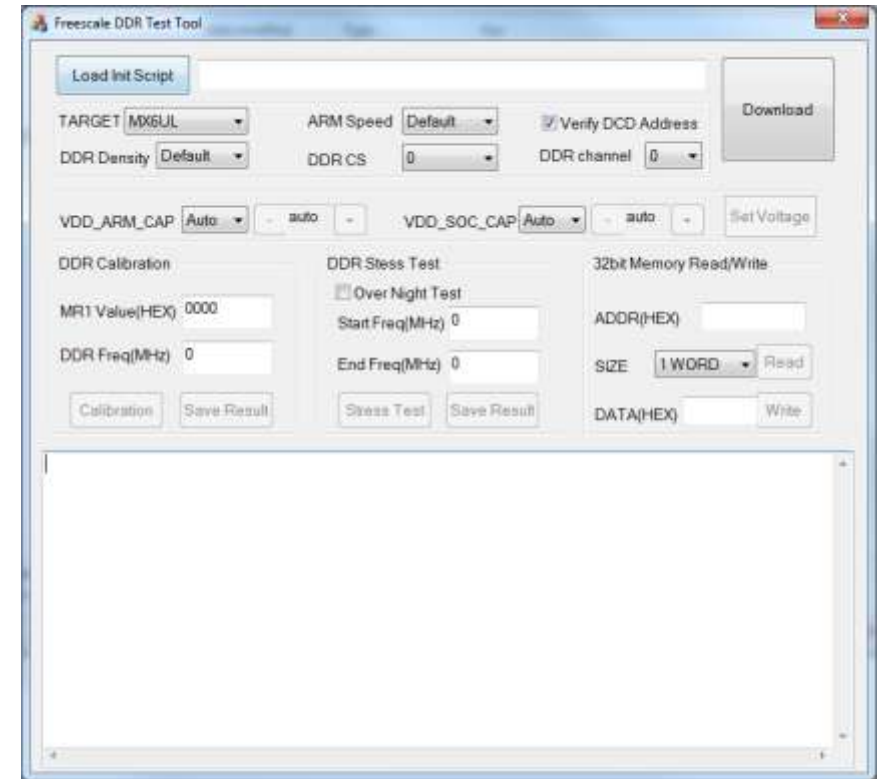
 Copy and paste these commands into a text file and re-name file as <file\_name>.ds or <file\_name>.inc

# DDR STRESS TEST

# DDR Stress Test

## Overview

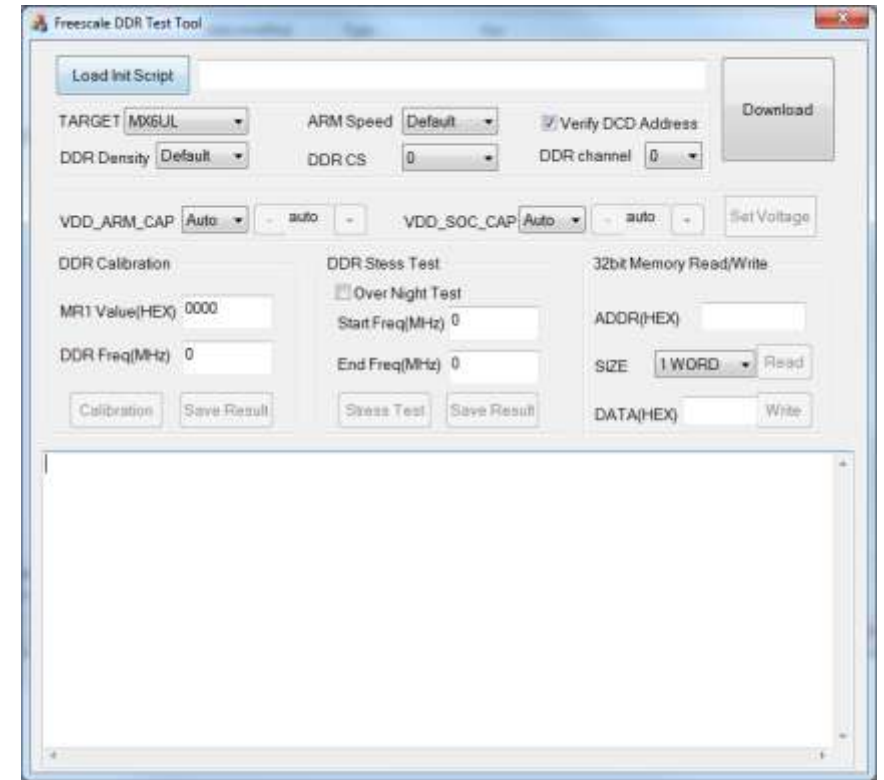
- Non-OS test to exercise DDR interface
  - Non-OS (bare-metal): easier than OS to catch/debug DDR failures
  - Helps diagnose but doesn't fix DDR problems
  - Primarily uses sequential bursts of back-to-back data looking for simultaneous switching noise (SSN)
  - Validation vehicle that reports how robust DDR interface is given current set of parameters (i.e. drive strength settings, timing parameters, board layout, etc)
- Runs from internal RAM
  - Device under test is DDR itself, doesn't execute from same memory being tested
  - DDR region tagged as cacheable to take advantage of cache line flush/fill resulting in long burst accesses
- Increment DDR frequency
  - Method to stress interface accounting for variations in PVT



# DDR Stress Test

## Overview

- Supports Calibration
  - MMDC has built-in support for various calibrations
  - All controllers support run-time ZQ calibration: ZQ calibration is something simply enabled, no user interaction
- New GUI version developed to make it easier to run
  - GUI-based tool uses USB connected from Host PC to i.MX 6 board USB OTG port
- JTAG version (elf) allows use with debugger and serial terminal
- Binary version (bin) allows user to run under u-boot
- Available on i.MX Community:  
<https://community.freescale.com/docs/DOC-105652>



# DDR Stress Test

## Overview

Once DDR stress test passes with ample margin, are we guaranteed the OS will never fail due to DDR issues?

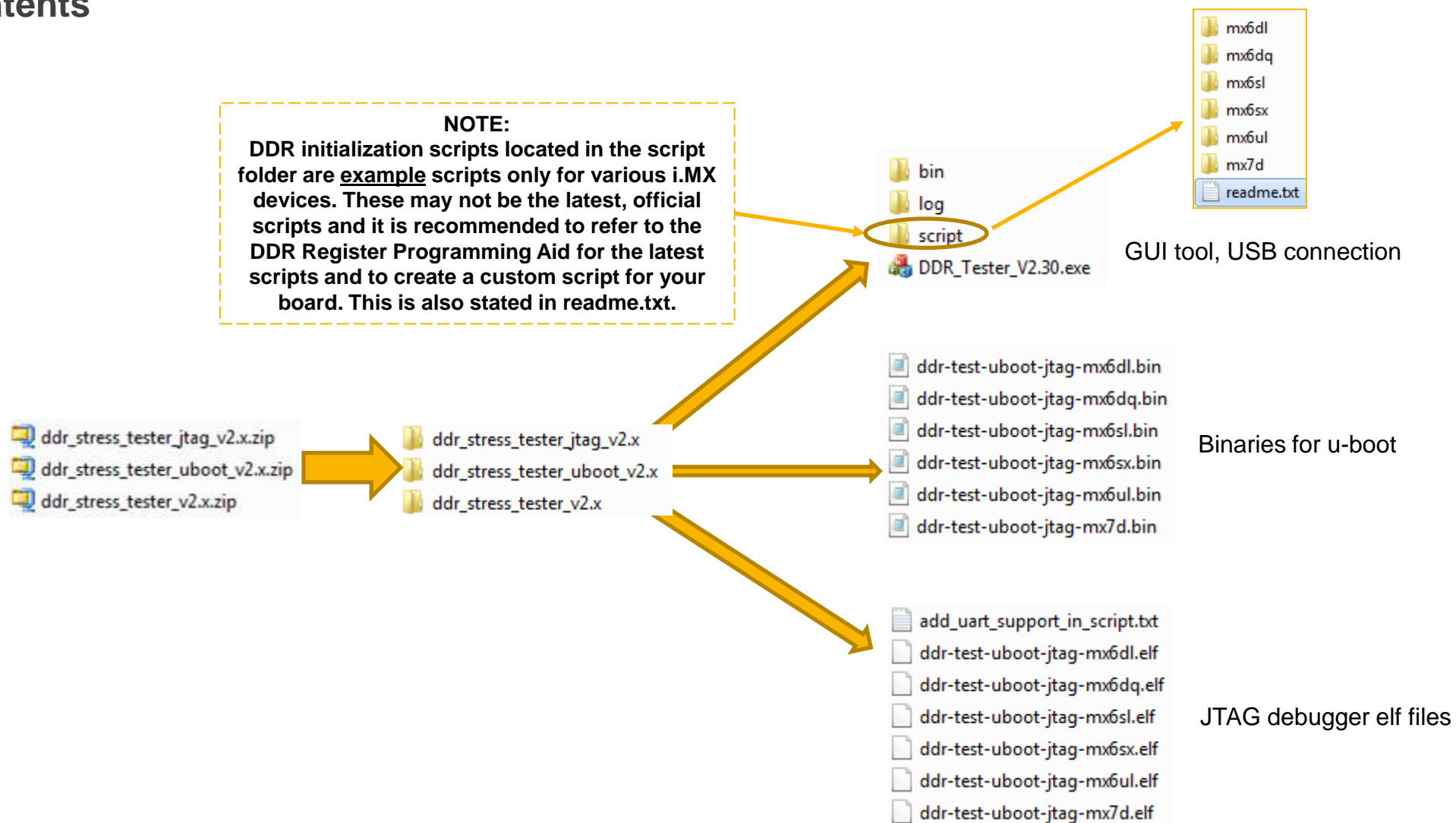
- High degree of confidence DDR robust enough, but...
- OS is still the most stressful, particularly an OS stress test like memtester or u-boot decompressing the Linux kernel
- Recommend to run any OS stress tests to double check

Differences between non-OS DDR stress test and OS based stress

DDR Stress Test	OS stress test (like memtester)
increments DDR frequency above max	runs at fixed frequency
single-task, lightweight (nothing else runs)	runs under OS, lots of stuff running, more system stress
runs from OCRAM, easier to catch DDR failures (data failures)	harder since it runs from DDR (could see data failure or code lockup)

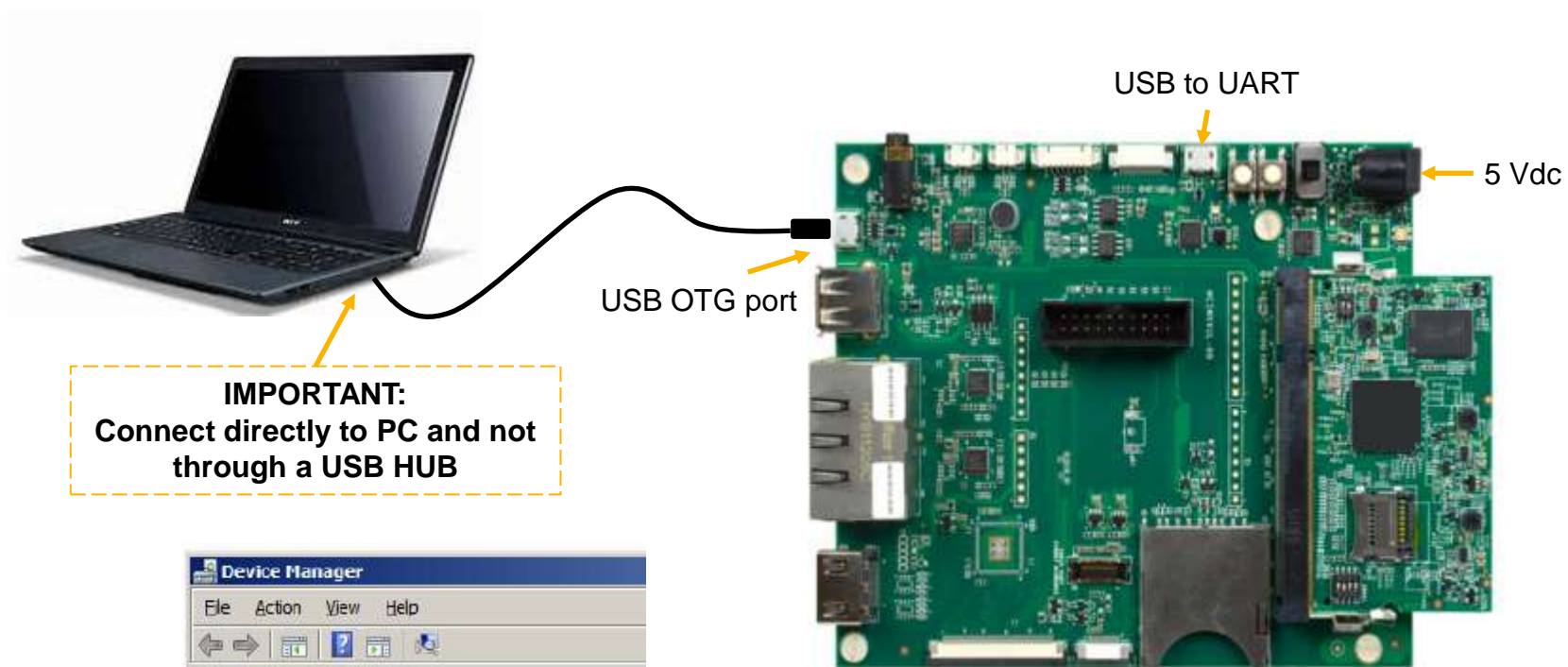
# DDR Stress Test

## Zip contents



# DDR Stress Test

## Connecting to the EVK



**IMPORTANT:**  
Connect directly to PC and not  
through a USB HUB



“HID-compliant device” or “USB Input Device” in the Device Manager

# DDR Stress Test

## GUI walk through: downloading to EVK

The screenshot shows the Freescale DDR Test Tool interface. The 'Load Init Script' field contains the path `is_tester_v2.30\script\mx6ul\EVK_IMX6UL_DDR3L_400MHz_16bit_V1.2.ind`. The 'TARGET' dropdown is set to 'MX6UL'. The 'ARM Speed' dropdown is set to 'Default'. The 'Verify DCD Address' checkbox is checked. The 'Download' button is highlighted. The 'DDR Density' dropdown is set to 'Default'. The 'DDR CS' dropdown is set to '0'. The 'DDR channel' dropdown is set to '0'. The 'VDD\_ARM\_CAP' dropdown is set to 'Auto'. The 'VDD\_SOC\_CAP' dropdown is set to 'Auto'. The 'Set Voltage' button is visible. The 'DDR Calibration' section has 'MR1 Value(HEX)' set to '0000' and 'DDR Freq(MHz)' set to '0'. The 'DDR Stress Test' section has 'Over Night Test' checked, 'Start Freq(MHz)' set to '0', and 'End Freq(MHz)' set to '0'. The '32bit Memory Read/Write' section has 'ADDR(HEX)' set to an empty field, 'SIZE' set to '1 WORD', and 'Read' and 'Write' buttons. The bottom section shows the SRC\_SPMR2(0x020d801c) = 0x01000001 and ARM Clock set to 528MHz. The DDR configuration section shows: DDR type is DDR3, Data width: 16, bank num: 8, Row size: 15, col size: 10, Chip select CSD0 is used, Density per chip select 512MB.

1 Select the desired DDR init script

2 Select MX6UL as target

3 It is recommended to leave the DDR density option as Default. The Density information is obtained from the init script. Future improvements will allow user to select a lower density allowing them to run a quicker test.

4 EVK uses CSD0 only, so this should be 0.

5 For MX6UL, it is recommended to leave the ARM Speed as default as the current max speed is 528MHz. The other ARM speed options are not applicable to i.MX 6UL.

6 For use with LPDDR2 memories, MX6UL only supports single channel, leave as default

7 When the MX6UL option is selected for TARGET and the desired DDR init script is selected, hit Download

# DDR Stress Test

## GUI walk through: voltage select option

Pull down option selects between Auto and Manual. “Manual” allows user to adjust voltages, but user must abide by data sheet (see below).

When manually setting the voltage, hit Set Voltage to engage.

VDD_ARM_CAP	A7 core at 528 MHz	1.15	—	1.3	V	Output voltage must be set to the following rules: <ul style="list-style-type: none"><li>• VDD_ARM_CAP &lt;= VDD_SOC_CAP</li><li>• VDD_SOC_CAP - VDD_ARM_CAP &lt; 330 mV</li></ul>
	A7 core at 396 MHz	1.00	—	1.3		
	A7 core at 198 MHz	0.925	—	1.3		
VDD_SOC_CAP	—	1.15	—	1.3	V	—

Freescal

DDR Test Tool

Load Init Script

is\_tester\_v2.30\script\mx6ul\EVK\_IMX6UL\_DDR3L\_400MHz\_16bit\_V1.2.ind

Download

TARGET

MX6UL

ARM Speed

Default

Verify DCD Address

☒

DDR Density

Default

DDR CS

0

DDR channel

0

VDD\_ARM\_CAP

Auto

-

auto

+

VDD\_SOC\_CAP

Auto

-

auto

+

Set Voltage

DDR Calibration

MR1 Value(HEX)

0000

DDR Freq(MHz)

0

Calibration

Save Result

DDR Stress Test

Over Night Test

☐

Start Freq(MHz)

0

End Freq(MHz)

0

Stress Test

Save Result

32bit Memory Read/Write

ADDR(HEX)

SIZE

1 WORD

Read

DATA(HEX)

Write

d801c) = 0x01000001

=====

8MHz

=====

on

num: 8

Row size: 15, col size: 10

Chip select CSD0 is used

Density per chip select 512MB

=====



# DDR Stress Test

## GUI walk through: calibration

1

If using DDR3 and if you plan to run calibration, then it is important to fill out the MR1 value, like "0004".

2

Input "400" for DDR Freq (MHz).  
Note that the tool will actually set to nearest freq of 396MHz

3

Hit Calibration to start

4

This saves the results to a log file

The screenshot shows the Freescale DDR Test Tool interface. At the top, there's a 'Load Init Script' button and a text field containing a file path. Below this are dropdown menus for 'TARGET' (set to MX6UL), 'ARM Speed' (Default), 'DDR Density' (Default), 'DDR CS' (0), and 'DDR channel' (0). There are also checkboxes for 'Verify DCD Address' and a 'Download' button. Further down, there are voltage control sections for 'VDD\_ARM\_CAP' and 'VDD\_SOC\_CAP', each with 'Auto' and 'Set Voltage' options. The 'DDR Calibration' section includes an 'MR1 Value(HEX)' field (0004) and a 'DDR Freq(MHz)' field (400), with 'Calibration' and 'Save Result' buttons. The 'DDR Stress Test' section has an 'Over Night Test' checkbox, 'Start Freq(MHz)' and 'End Freq(MHz)' fields, and 'Stress Test' and 'Save Result' buttons. The '32bit Memory Read/Write' section has fields for 'ADDR(HEX)', 'SIZE' (1 WORD), and 'DATA(HEX)', with 'Read' and 'Write' buttons. The bottom section displays a log of calibration steps and their results, ending with 'Success: DDR calibration completed!!!'. Arrows from numbered callouts point to specific fields and buttons in the GUI.

Load Init Script: s\_tester\_v2.30\script\mx6ul\EVK\_IMX6UL\_DDR3L\_400MHz\_16bit\_V1.2.ind

TARGET: MX6UL ARM Speed: Default Verify DCD Address: ☒ Download

DDR Density: Default DDR CS: 0 DDR channel: 0

VDD\_ARM\_CAP: Auto - auto + VDD\_SOC\_CAP: Auto - auto + Set Voltage

DDR Calibration: MR1 Value(HEX): 0004 DDR Freq(MHz): 400 Calibration Save Result

DDR Stress Test: ☐ Over Night Test Start Freq(MHz): 0 End Freq(MHz): 0 Stress Test Save Result

32bit Memory Read/Write: ADDR(HEX): SIZE: 1 WORD Read DATA(HEX): Write

MMDC\_MPWLDECTL0 ch0 (0x021b080c) = 0x00000000

Read DQS Gating calibration

MPDGCTRL0 PHY0 (0x021b083c) = 0x41500148

MPDGCTRL1 PHY0 (0x021b0840) = 0x00000000

Read calibration

MPRDDCTL PHY0 (0x021b0848) = 0x40404644

Write calibration

MPWRDLCTL PHY0 (0x021b0850) = 0x4040524E

Success: DDR calibration completed!!!

Copy Calibration values and  
put into your init script

5

# DDR Stress Test

## GUI walk through: simple memory write/read test

The screenshot shows the Freescale DDR Test Tool interface. Annotations point to various fields and buttons:

- Input Address, in HEX format, as shown here**: Points to the ADDR(HEX) field, which contains 80000000.
- Input the data you wish to write, in HEX format, as shown here. Hit "Write" to write the word into the address location above. Note, only one word is written regardless of the "SIZE" field.**: Points to the DATA(HEX) field, which contains a5a5a5a5, and the Write button.
- Select how many (32-bit) words you want to read out, from 1 word to 32 words. Hit "Read" to read out the selected number of words.**: Points to the SIZE dropdown menu, which is set to 32 WORD, and the Read button.
- Outputs when "Write" is hit**: Points to the output window showing the success message and the memory read results.
- Outputs when "Read" is hit**: Points to the memory read results table.

The output window displays the following data:

```
addr=0x80000000,data=0xA5A5A5A5
Success to write address 0x80000000
```

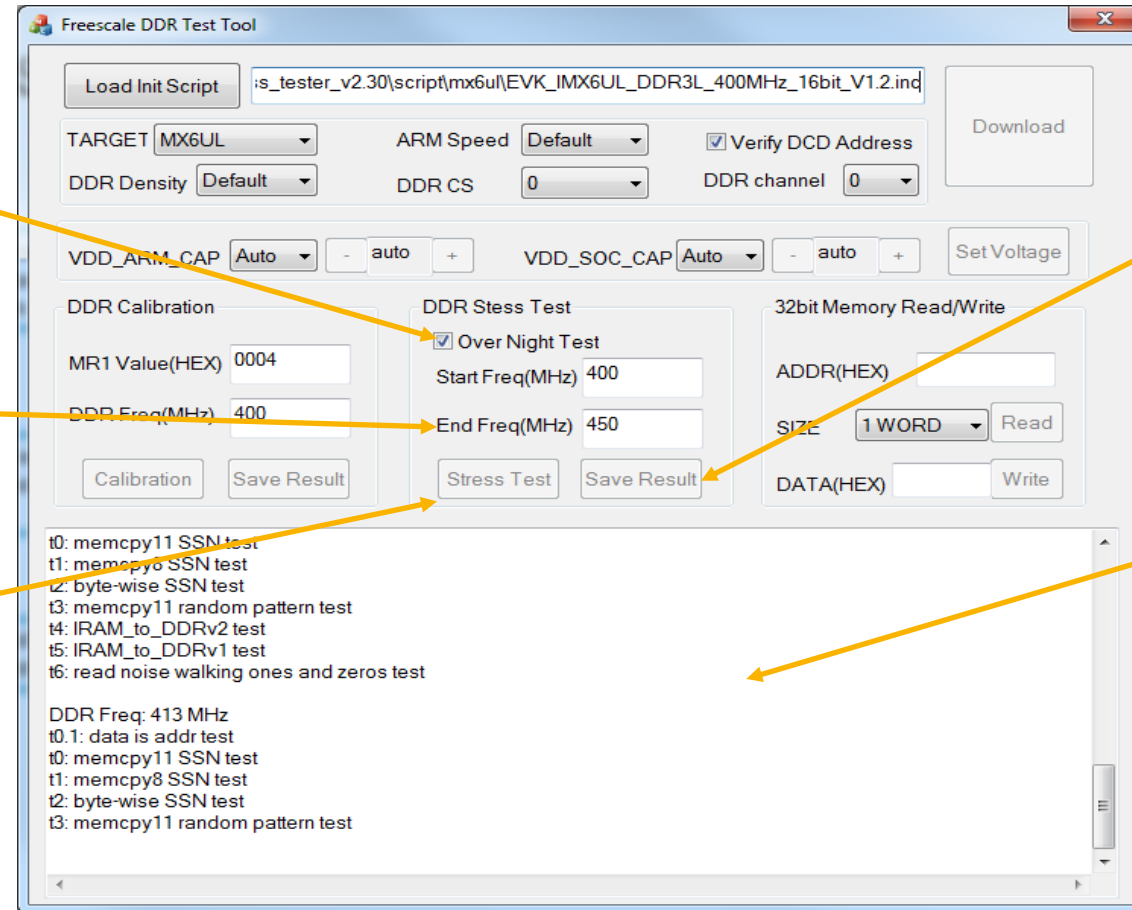
	0x0	0x4	0x8	0xC
0x80000000:	0xA5A5A5A5	0x75EBACF4	0x779D53F8	0x59D15BF8
0x80000010:	0xDFA5F25A	0xFF7A0FF8	0x7FEE5DCD	0x91E2B3D4
0x80000020:	0xE7F76E3C	0xFF9B60B0	0xC93FFFE9	0xDB745DF1
0x80000030:	0xEDB87598	0xFFDCFAD0	0x1391738E	0x2BCFE781
0x80000040:	0x357FBDF8	0x5FBE1471	0x59E27AFA	0x7DDFCF62
0x80000050:	0x7E4B17D8	0x977F6F54	0xB2B3C4C8	0xB4EA9BC1
0x80000060:	0xC75CF5B8	0xD950E932	0xEBDDEE9	0xFDB9F529
0x80000070:	0x0FEFFFB9	0x23AB2E97	0x75FE7AEA	0x6FFAEF88

memory read is done

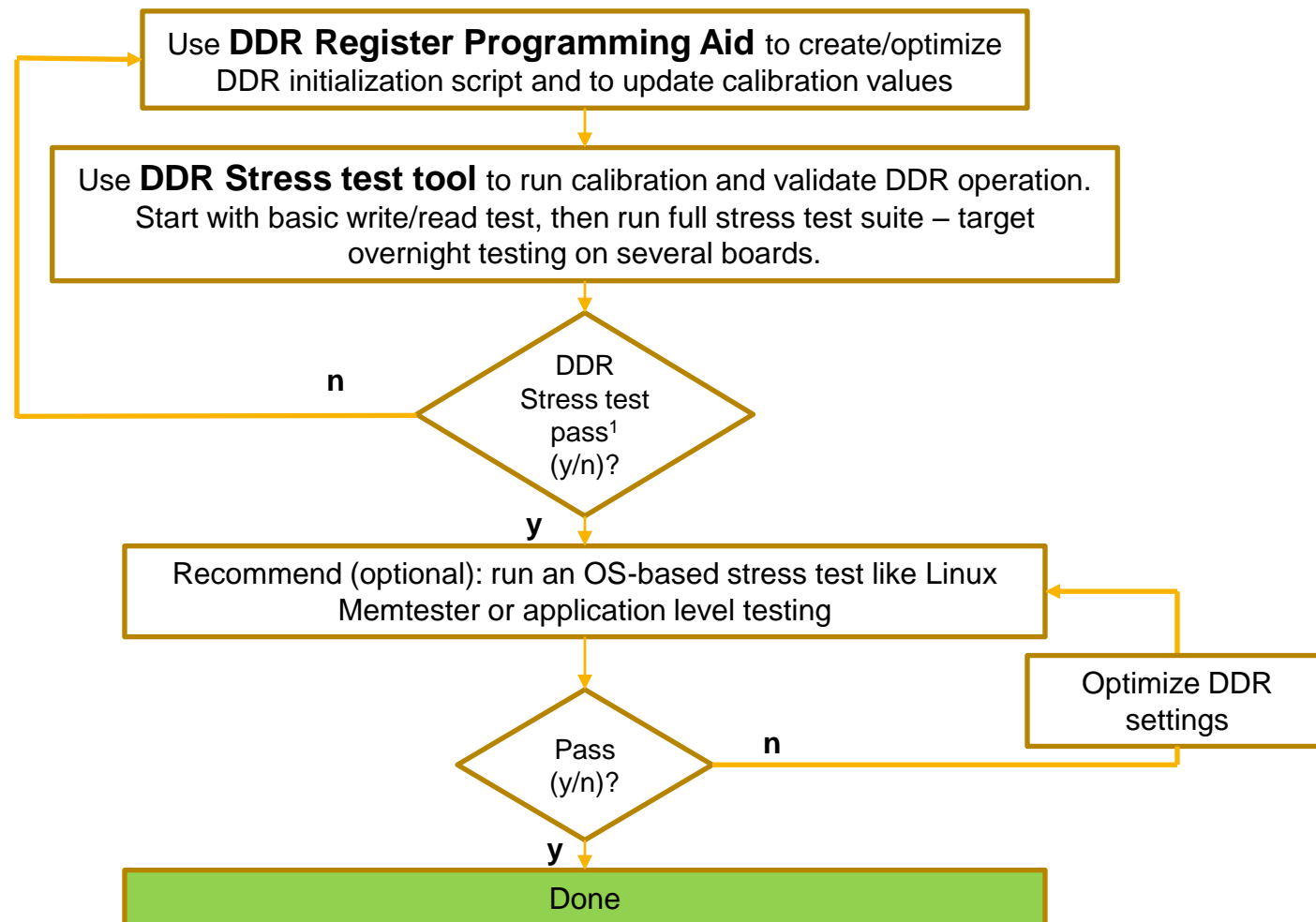
Note: when writing or reading, care should be taken to ensure you are writing-to/reading-from a valid DDR address, else you could hang the tool (at which point you'll have to re-start the tool).

# DDR Stress Test

## GUI walk through: running the stress test



# i.MX 6UL MMDC Tool Usage Flow Chart



1. When running stress test with incrementing frequency, usually target ~%10 above maximum freq. For 400MHz, target at least 440MHz

# I.MX 7SOLO & I.MX 7DUAL

# Growing Number of Embedded Use Cases Require Concurrent Execution of Isolated and Secure Software Environments



**OFFLOAD TASKS**



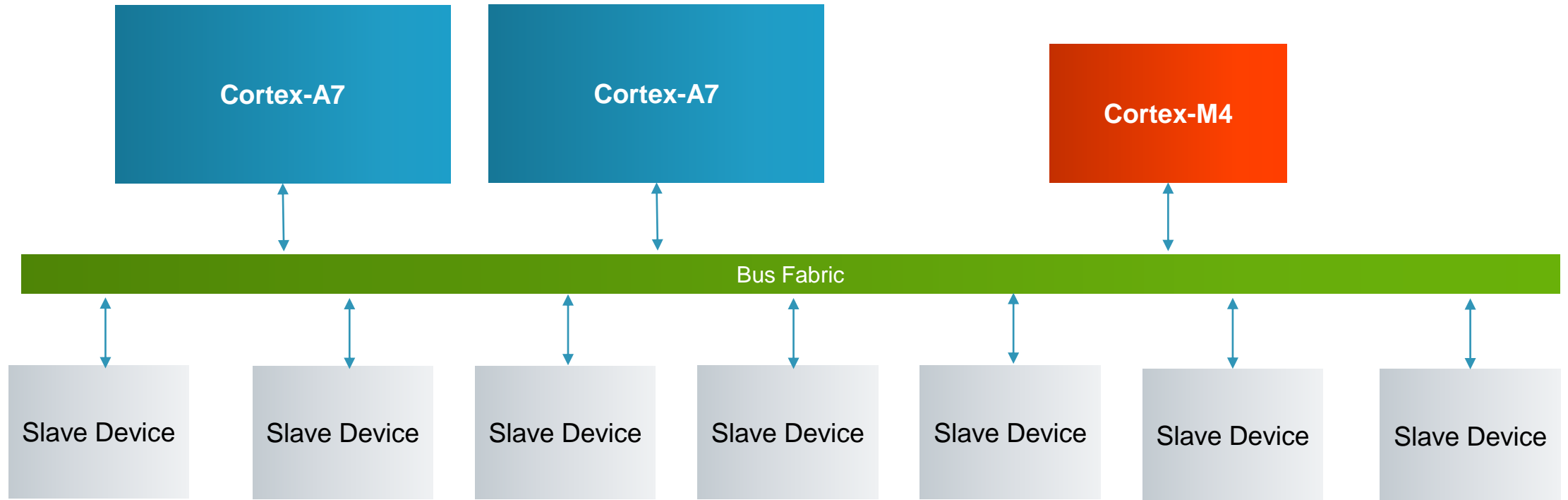
**OPTIMIZE POWER**



**INCREASE SECURITY**

# Heterogeneous Multicore Processing (HMP)

## Shared Topology



# i.MX 7Dual/Solo Family Target Applications

## MOBILE DEVICES

LPDDR2/3  
Small Package



- Healthcare / Patient Monitoring
- HMI Control / Security
- Point of Sale
- Printing
- Home Control
- Wearables
- eReaders
- General Embedded Control
- Embedded Board Solutions
- IoT

## CONNECTED DEVICES

Low Cost DDR3  
Larger Pitch Package



# i.MX 7Solo and i.MX 7Dual



## i.MX 7Solo

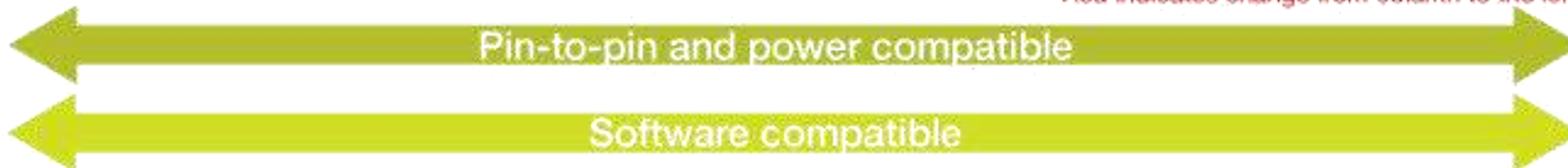
- Single ARM® Cortex®-A7 up to 800 MHz
- Cortex-M4 up to 200 MHz
- 512KB L2 cache
- 16/32-bit DDR3/DDR3L and LPDDR2/3 at 533 MHz
- Single Gigabit Ethernet (AVB)
- Full security with tamper resist



## i.MX 7Dual

- **Dual** ARM® Cortex®-A7 up to **1.0** GHz
- Cortex-M4 up to 200 MHz
- 512 KB L2 cache
- 16/32-bit DDR3/DDR3L and LPDDR2/3 at 533 MHz
- **Dual** Gigabit Ethernet (AVB)
- Full security with tamper resist
- **EPD controller**
- **PCIe (x1 lane)**

Red indicates change from column to the left



Consumer



Extended  
Consumer

# Q & A

- **i.MX Product Summary Page:**

- [http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors:IMX\\_HOME](http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors:IMX_HOME)

- **i.MX 6 Series Software and Development Tool Resources**

- [http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors/i.mx-6-processors/i.mx6qp/i.mx-6-series-software-and-development-tool-resources:IMX6\\_SW?tid=vanIMX6TOOLS#bsp](http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors/i.mx-6-processors/i.mx6qp/i.mx-6-series-software-and-development-tool-resources:IMX6_SW?tid=vanIMX6TOOLS#bsp)

- **i.MX 6 Sabre Tool Summary Page:**

- [www.nxp.com/imx6tools](http://www.nxp.com/imx6tools)

Targeted i.MX7 Global Full Market Launch (which means mass market launch) date is July 18, 2016 (US time)



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FOR A SMARTER WORLD

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