i.MX 7 HETEROGENEOUS MULTICORE PROCESSING

FTF-DES-N1932

AUG 4, 2016

PUBLIC

SECURE CONNECTIONS FOR A SMARTER WORLD

AGENDA

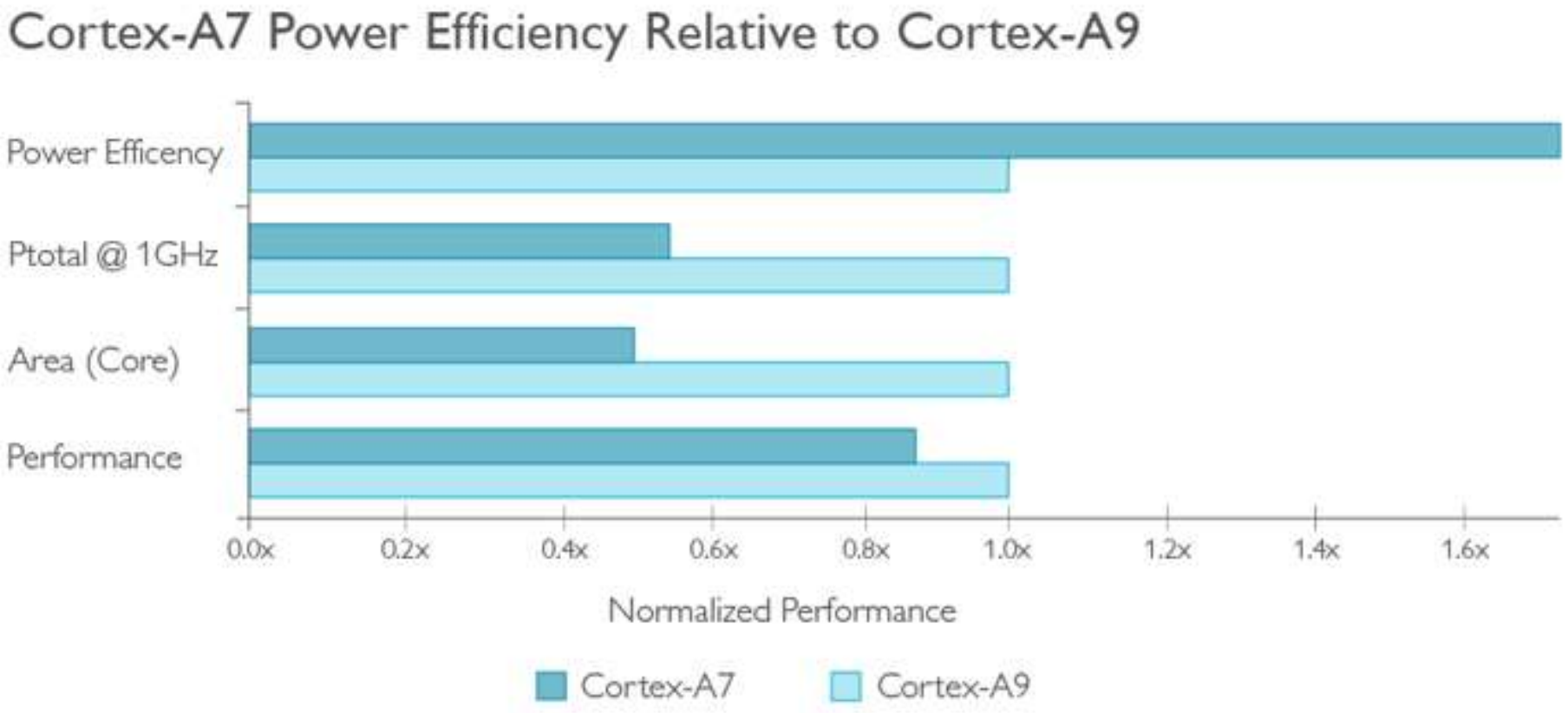
- Introduction/Overview
- Heterogeneous Multicore Processing
- Software

Learning Goals

- Basic knowledge about i.MX 7Dual
  - Summary of the chip and capabilities
- What is HMP and why it’s important
- Review the i.MX 7 SABRE board and its capabilities
- Basic information about FreeRTOS & HMP
- RPMsg and how inter-processor communication works between the Cortex-M4 and Cortex-A7 cores

i.MX 7
INTRODUCTION

Comparison Cortex-A7 vs Cortex-A9



i.MX 7Dual/Solo Family Target Applications

MOBILE DEVICES

LPDDR2/3
Small Package




- Healthcare / Patient Monitoring
- Wearables
- IoT
- Point of Sale
- eReaders

- HMI Control / Security
- Printing
- Home Control
- General Embedded Control

CONNECTED DEVICES

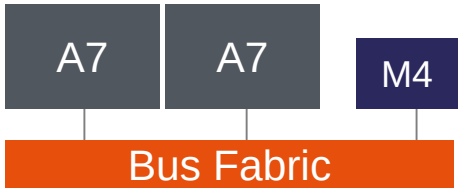
Low Cost DDR3
Larger Pitch Package






Advanced Heterogeneous Architecture

- Up to Dual Cortex-A7 @ 1GHz
- Cortex-M4 @ 200MHz
  - Offload Tasks
  - Optimize Power
  - Increase Security



Unmatched Power Efficiency

- 3x improvement in Power Efficiency vs i.MX 6
- 100 uW/MHz for Cortex-A7
- 70 uW/MHz for Cortex-M4
- One third the power consumed in the Low Power suspend mode (250uW) vs i.MX 6

Enabling Flexible High Speed Connectivity

- PCI-e v2.1
- Dual Gbit Ethernet with AVB
- DDR QuadSPI support
- eMMC 5.0

Complete Security Infrastructure

- Secure Boot
- Crypto H/W Acceleration
- Secure JTAG
- Internal and External Tamper Detection
- DPA attack Resistance
- Secure Storage

i.MX 7Solo

- Single ARM® Cortex®-A7 up to 800 MHz
- Cortex-M4 up to 200 MHz
- 512KB L2 cache
- 16/32-bit DDR3/DDR3L and LPDDR2/3 at 533 MHz
- Single Gigabit Ethernet (AVB)
- **Full security with tamper resist**

i.MX 7Dual

- Dual ARM® Cortex®-A7 up to 1.0 GHz
- Cortex-M4 up to 200 MHz
- 512 KB L2 cache
- 16/32-bit DDR3/DDR3L and LPDDR2/3 at 533 MHz
- Dual Gigabit Ethernet (AVB)
- **Full security with tamper resist**
- EPD controller
- PCIe (x1 lane)

Red indicates change from column to the left

Pin-to-pin and power compatible

Software compatible

Consumer

Extended Consumer

i.MX non-GPU/VPU Product Lineup

Feature	i.MX25x	i.MX28x	i.MX 6UL	i.MX 7Solo	i.MX 7Dual
Core	ARM9	ARM9	**Cortex-A7 @ 528 MHz**	Cortex-A7 **@800 MHz**	**Dual** Cortex-A7 **@1GHz**
L2 Cache	-	-	128KB	**512KB**	512KB
RAM	128KB	128KB	128KB	**256KB**	256KB
2nd Core	-	-	-	**Cortex-M4**	Cortex-M4
Flash Interface	MLC/SLC NAND Flash w/ 8-bit RS, NOR Flash	SLC/MLC/Managed NAND Flash w/ 20-bit BCH	SLC/MLC/Managed NAND Flash w/ 40-bit BCH	SLC/MLC/Managed NAND **Flash 60-bit BCH**, 8-bit RS	SLC/MLC/Managed NAND Flash 60-bit BCH, 8-bit RS
DRAM Interface	150 MHz 16-bit DDR2, mDDR, SDRAM	**200 MHz** 16-bit DDR2, LV-DDR2, mDDR	**400 MHz 16-bit DDR3/L, LPDDR2**	**533 MHz 32-bit** DDR3/L, LPDDR2, **LPDDR3**	**533 MHz 32-bit** DDR3/L, LPDDR2, **LPDDR3**
Display	24-bit Parallel-640x480	24-bit Parallel RGB-640x480	24-bit Parallel RGB-**1366x768**	24-bit Parallel RGB-**1920x1080 MIPI-DSI (2 lane) 1.5Gbps**	24-bit Parallel RGB-1920x1080 MIPI-DSI (2 lane) 1.5Gbps **EPDC**
Imaging	1 overlay, alpha blending, panning	**8 overlays**, alpha blending, scaling, rotation, CSC	PXP – Scaling, Alpha Blending, CSC, Dithering	PXP – Scaling, Alpha Blending, CSC, Dithering.	PXP – Scaling, Alpha Blending, CSC, Dithering
Camera Interface	Parallel Camera I/F	-	Parallel Camera I/F	Parallel Camera I/F, **MIPI-CSI**	Parallel Camera I/F, **MIPI-CSI**
CAN	x2	x2	x2	x2	x2
Ethernet	Single 10/100	Dual 10/100 **and L2 Switch**	Dual 10/100	Single **1Gb (AVB)**	**Dual** 1Gb (AVB)
Audio	I2S	I2S, S/PDIF	I2S, S/PDIF	**MQS**, I2S	MQS, I2S
USB	HS port (Host/Device) HS PHY x1,HS Host with FS PHY x1	HS port (Host/Device) with PHY x1, HS port Host with PHY x1	OTG with PHY x2	OTG with PHY x1 **HOST with HSIC**	OTG with PHY **x2** Host with HSIC
SIM	x2	-	x2	x2	x2
PCIe	-	-	-	-	**Yes**
Security	Tamper Detection, RNG	HAB4, PRNG	**Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins, OTF**	Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins,	Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins,
Power	External	**Integrated PMIC w/ Charger**	Analog LDOs	Analog LDOs	Analog LDOs

BOM Advantage

Performance Advantage

i.MX 7Solo

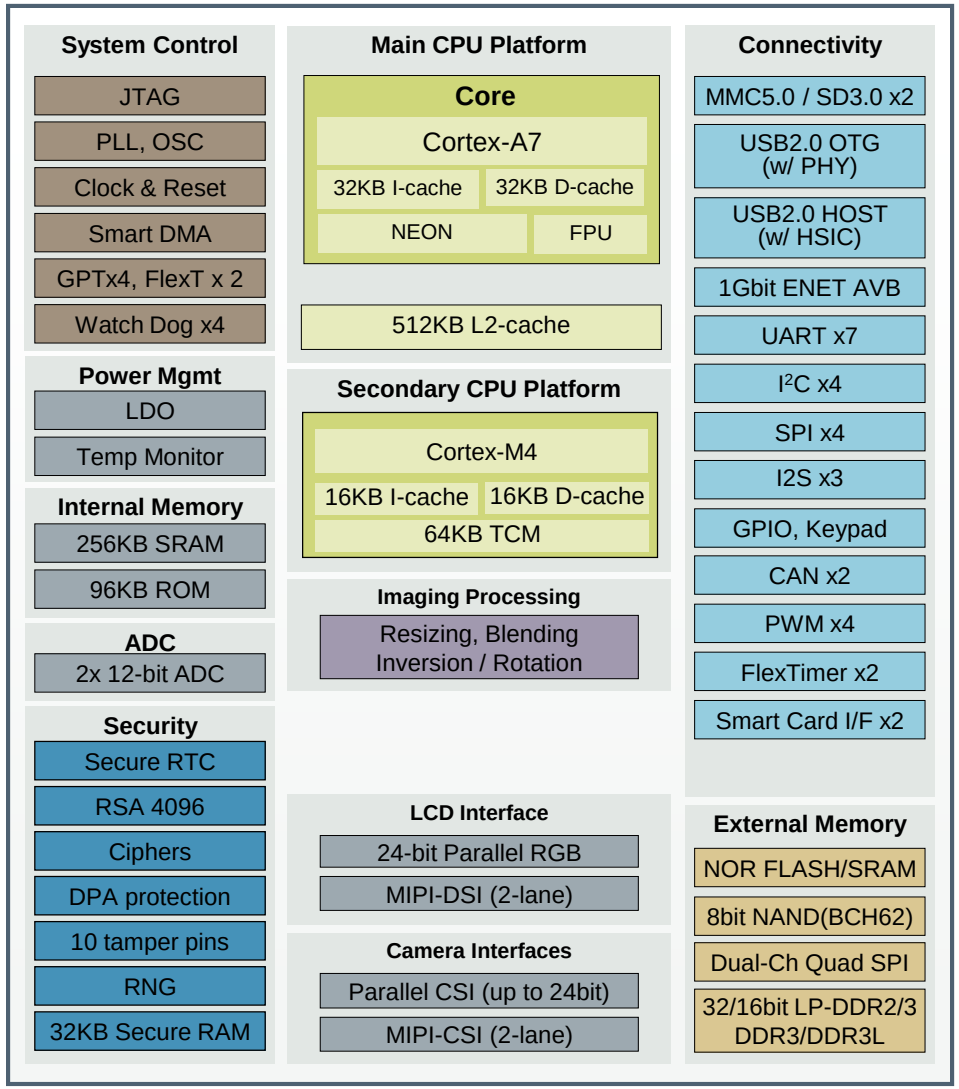
- **Specifications:**
  - Package: 19x19@0.75mm BGA
    12x12@0.4mm BGA*
  - Qualification: Consumer (0C to 95C Tj)
    - Extended Consumer (-20C to 105C Tj)
      - 10yr lifetime at 100% duty cycle

- **Key Features and Advantages**
  - 800MHz, Cortex-A7, 32KB I/D, 512KB L2 Cache
  - 200MHz Cortex M4, 16KB I/D, 64KB TCM
  - Memory Support
  - 16/32bit LP-DDR2/3, DDR3/L @ 533MHz
  - Total of 256KB OCRAM
  - 2x SDIO3.0/eMMC5.0, 8-bit NAND (BCH62)
  - Display / Camera
  - 24-bit Parallel LCD and MIPI DSI (2-lane)
  - Parallel (up to 24-bit) and MIPI CSI (2-lane)

  - I/O
  - 1x USB 2.0 OTG w/ PHY + 1xUSB 2.0 HOST/HSIC
  - 1x GigE Ethernet Ports-AVB;

  - Security module - enabling PCI 4.0 compliance

* Feature limited (1 ADC, 4 tamper pins)



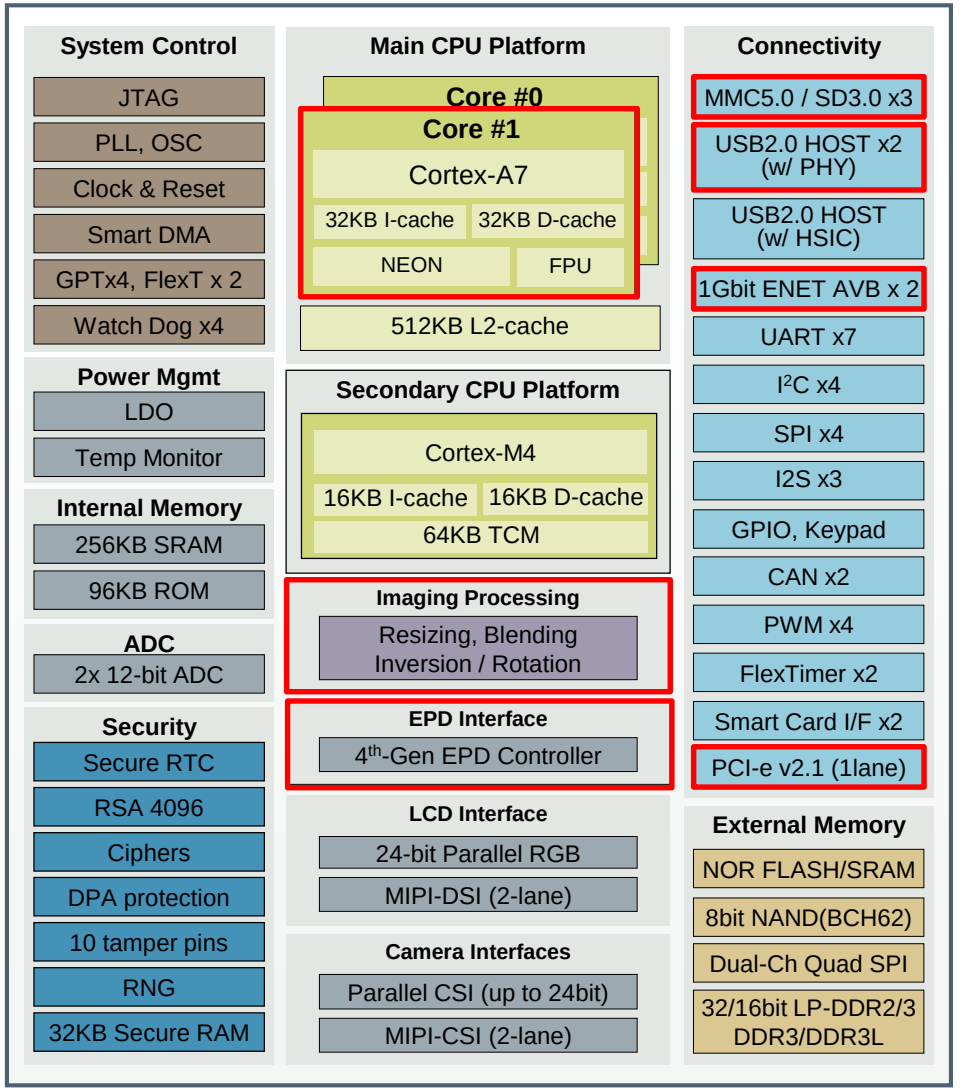
i.MX 7Dual

- **Specifications:**
  - Package: 19x19@0.75mm BGA
    12x12@0.4mm BGA*
  - Qualification: Consumer (0C to 95C Tj)
    - Extended Consumer (-20C to 105C Tj)
      - 10yr lifetime at 100% duty cycle

- **Key Features and Advantages**
  - 1 GHz, Cortex-A7, 32KB I/D, 512KB L2 Cache
  - 200MHz Cortex M4, 16KB I/D, 64KB TCM
  - Memory Support
  - 16/32bit LP-DDR2/3, DDR3/L @ 533MHz
  - Total of 256KB OCRAM
  - 3x SDIO3.0/eMMC5.0, 8-bit NAND (BCH62)
  - Display / Camera
  - 24-bit Parallel LCD and MIPI DSI (2-lane)
  - Parallel (up to 24-bit) and MIPI CSI (2-lane)
  - EPDC
  - I/O
  - 2x USB 2.0 OTG w/ PHY + 1xUSB 2.0 HOST/HSIC
  - 2x GigE Ethernet Ports-AVB;
  - PCIe 2.1

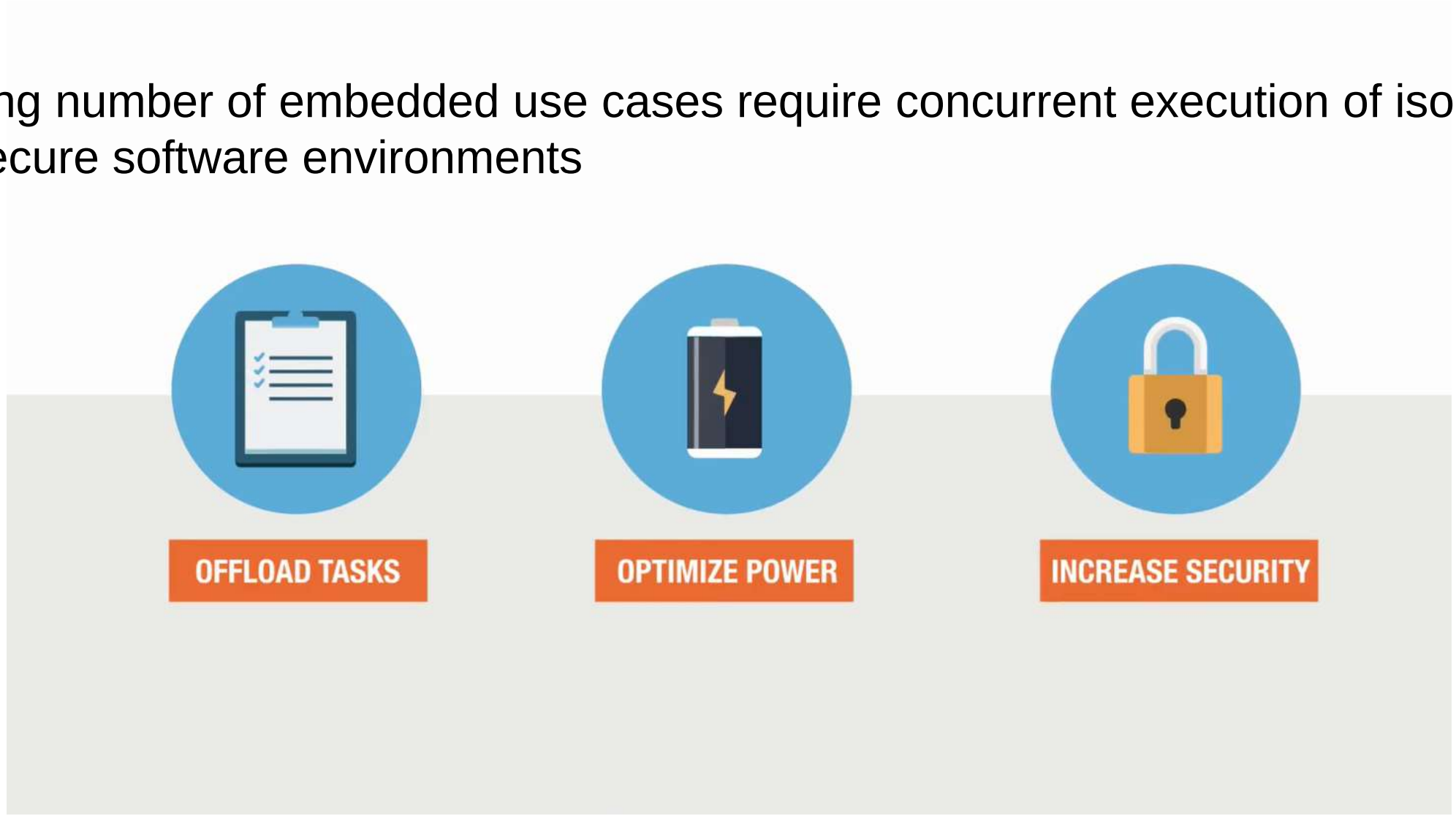
  - Security module - enabling PCI 4.0 compliance

* Feature limited (1 ADC, 4 tamper pins)



Updated from i.MX 7Solo

Growing number of embedded use cases require concurrent execution of isolated and secure software environments



HMP

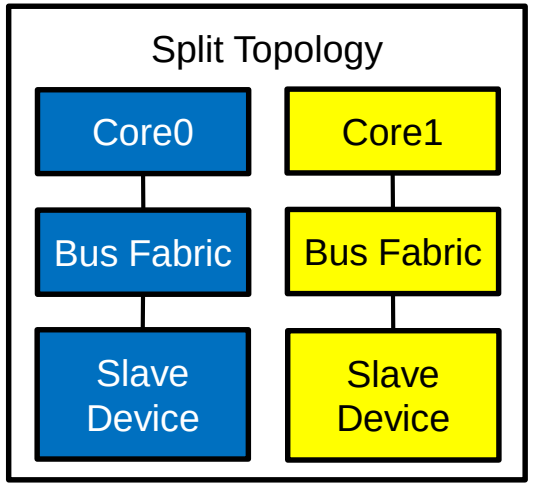
HMP Challenges – Synchronization and Communication

- **Interprocessor Synchronization**
  - Access to shared memory and peripherals must be synchronized
  - Development of cooperative software is more challenging than SMP systems due to separate development environments
  - Hardware support needed to enforce the development of cooperative software

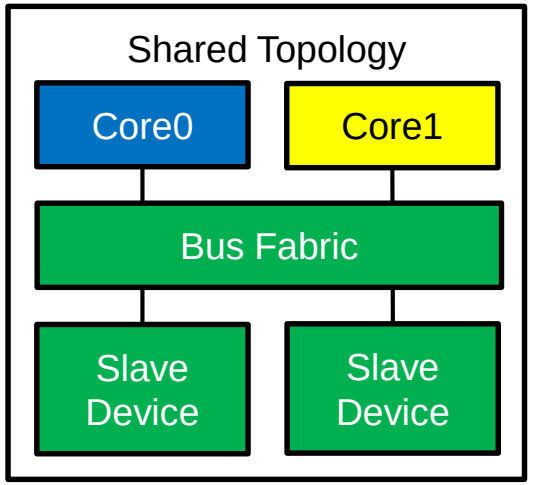
- **Interprocessor Communication**
  - Robust and efficient interprocessor communication is needed

HMP Challenges – Resource Partitioning and Protection

- **Split bus topology**
  - Provides immutable isolation of resources
  - Lacks flexibility to repartition the resources to adapt to new use cases
  - Resources such as memory may need to be duplicated

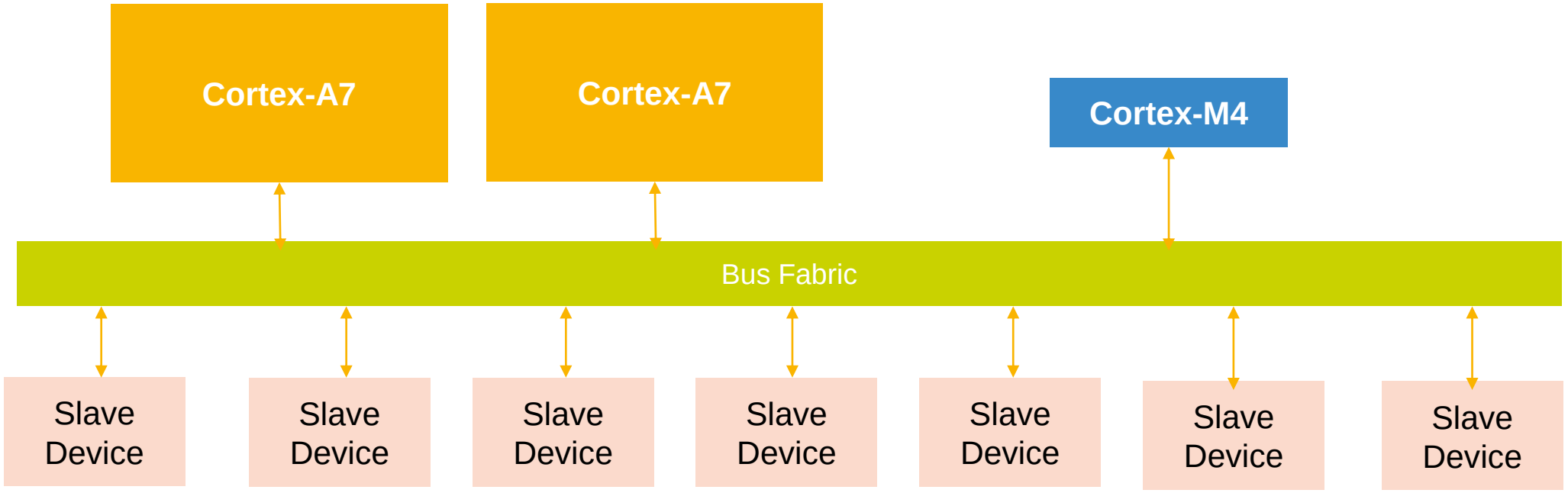


- **Shared bus topology**
  - Provides flexibility to repartition the resources for new use cases
  - Memory partitioning necessary to specify shared and isolated regions
  - Potential issues with isolation and protection of resources



Heterogeneous Multicore Processing (HMP)

Shared Topology

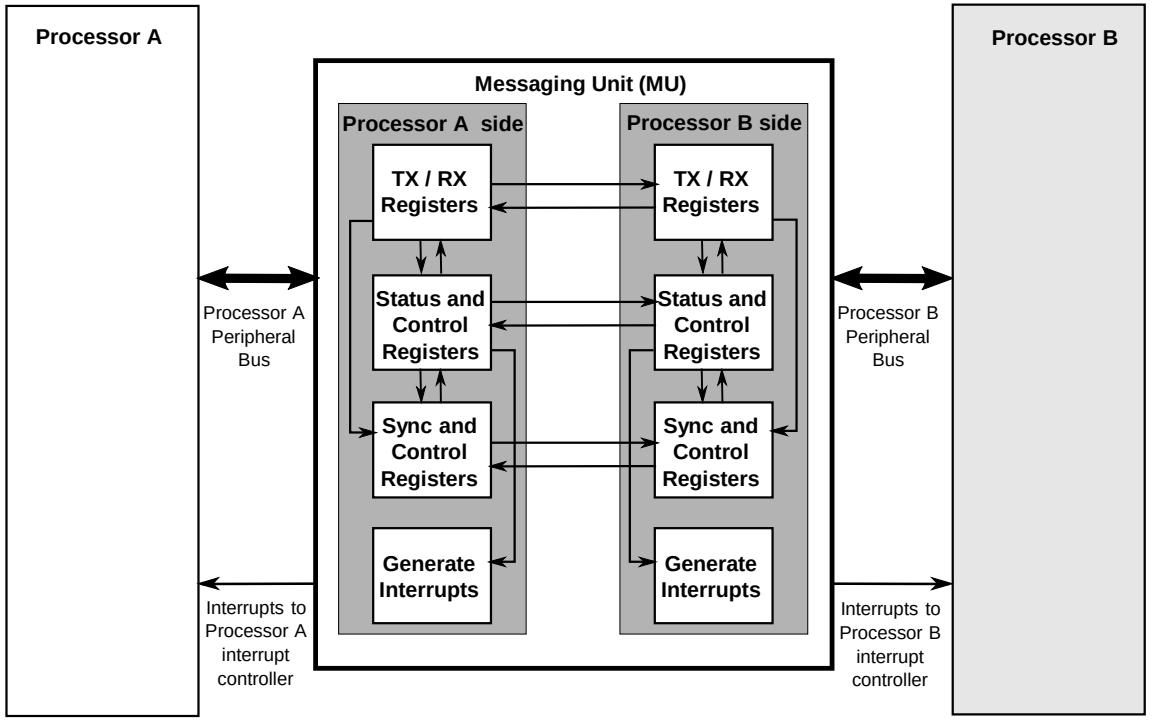


IPC Hardware Summary

Hardware	Features
Messaging Unit (MU)	Mailbox registers to send/receive messages Provided interprocessor interrupts
SEMA4	Hardware-based general-purpose semaphore module
Shared Memory	Bus topology allows shared memory RDC and CSU can provide memory protection/isolation
Exclusive Access	ARMv7-A and ARMv7-M defines exclusive access instructions (LDREX/STREX)

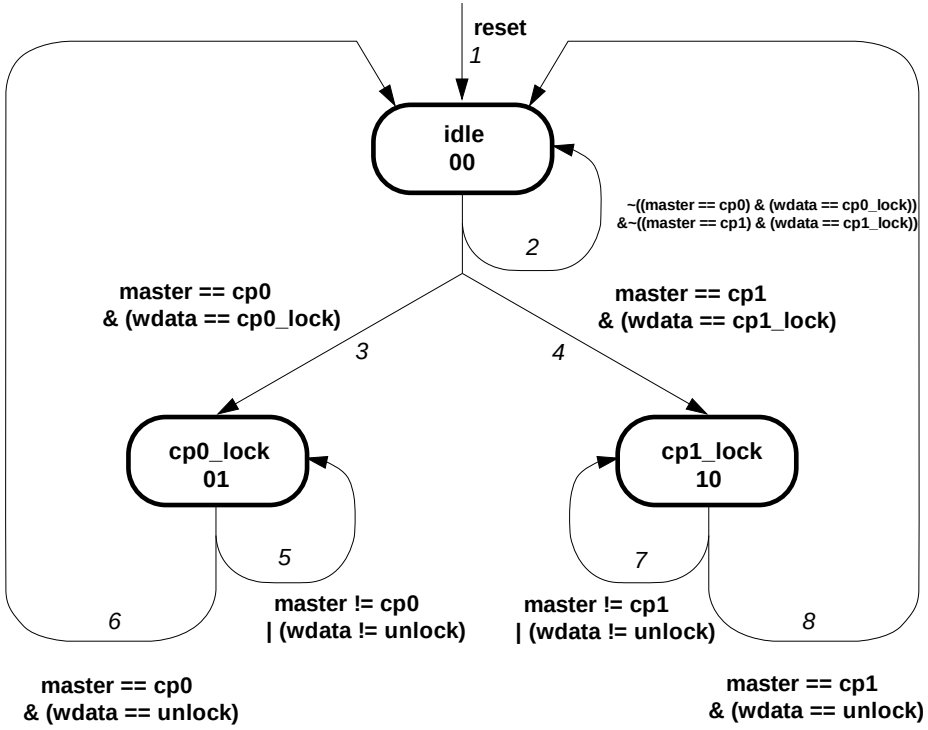
Messaging Unit (MU)

- Proven IP from cellular baseband SoCs
- Messaging control by interrupts or polling
- 4 RX/TX registers on each side
- 12 interrupt requests (IRQs) per side
  - 4 RX register full IRQs
  - 4 TX register empty IRQs
  - 4 general-purpose IRQs
- 3 general-purpose flags per side



Semaphore (SEMA4)

- Provides a hardware mechanism for cooperative software to safely share resources in HMP systems
- Separate module from RDC semaphore
- Supports 16 general-purpose hardware semaphores
- Semaphore can only be unlocked by locking processor
- Optional interrupt notification after failed lock attempt to indicate when semaphore is unlocked
- Software conventions still required to ensure only processor with semaphore lock can access shared resources

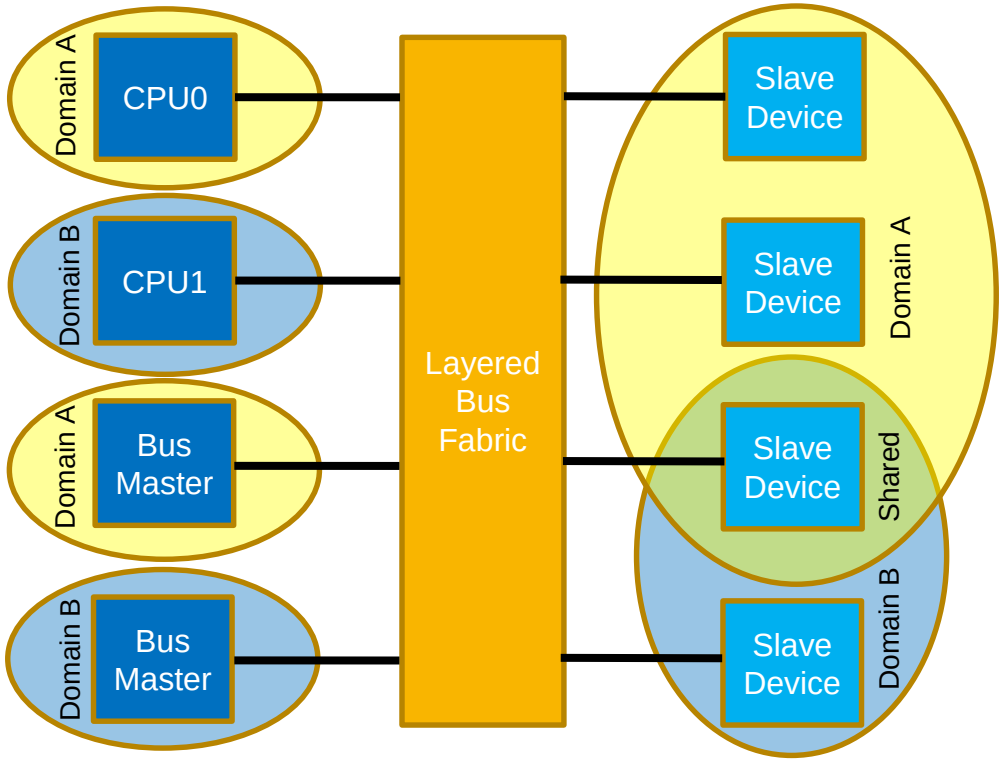


Exclusive Access

- Cortex-A (ARMv7-A) and Cortex-M (ARMv7-M) support exclusive access instructions (LDREX/STREX).
- Exclusive access bus signals generated by the CPUs are connected to monitors in the memory gaskets to support load/store exclusive instructions.
- Exclusive access is widely used for synchronization in SMP systems, but is applicable to HMP systems that have architectural support.
- For HMP systems, the memory referenced during exclusive accesses must be configured such that the access will occur at the point of coherency for the CPUs.

Resource Domains

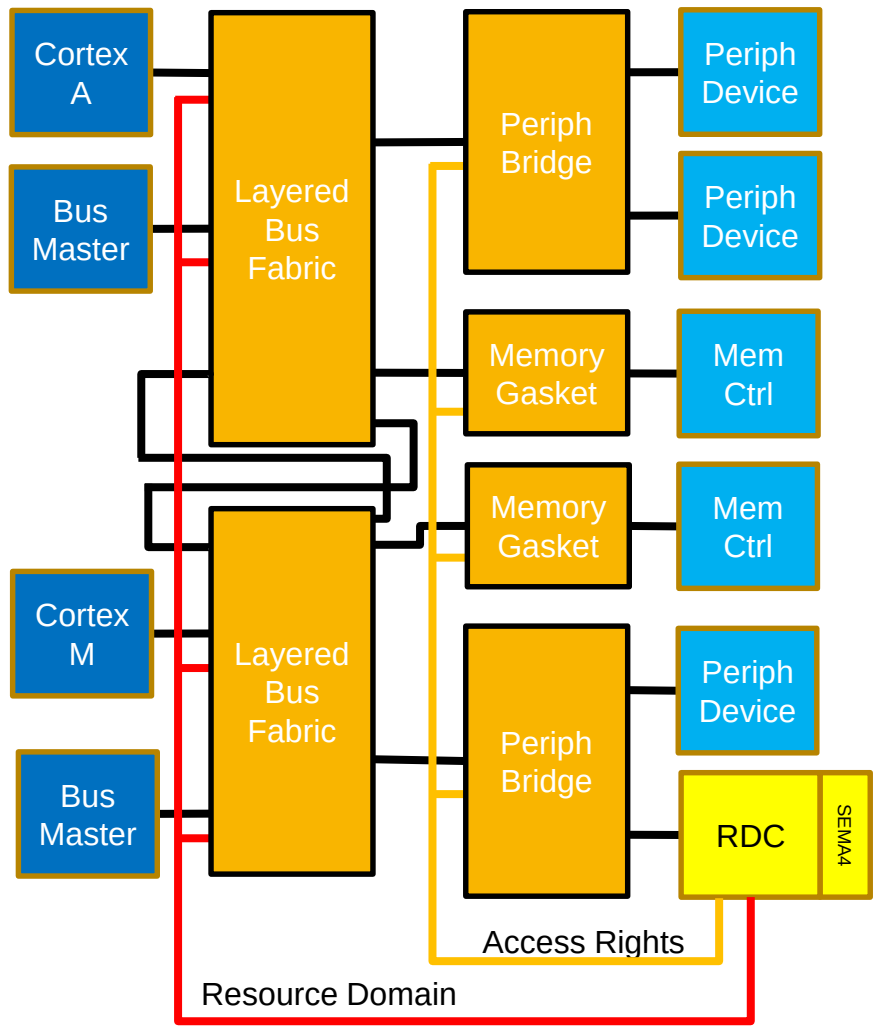
- Use resource domains to partition the system
  - Masters are assigned to a resource domain
  - Slave access permissions are defined per resource domain
  - Memory region access permissions are defined per resource domain
- Sideband signals of bus fabrics carry resource domain ID



Resource Domain Controller (RDC)

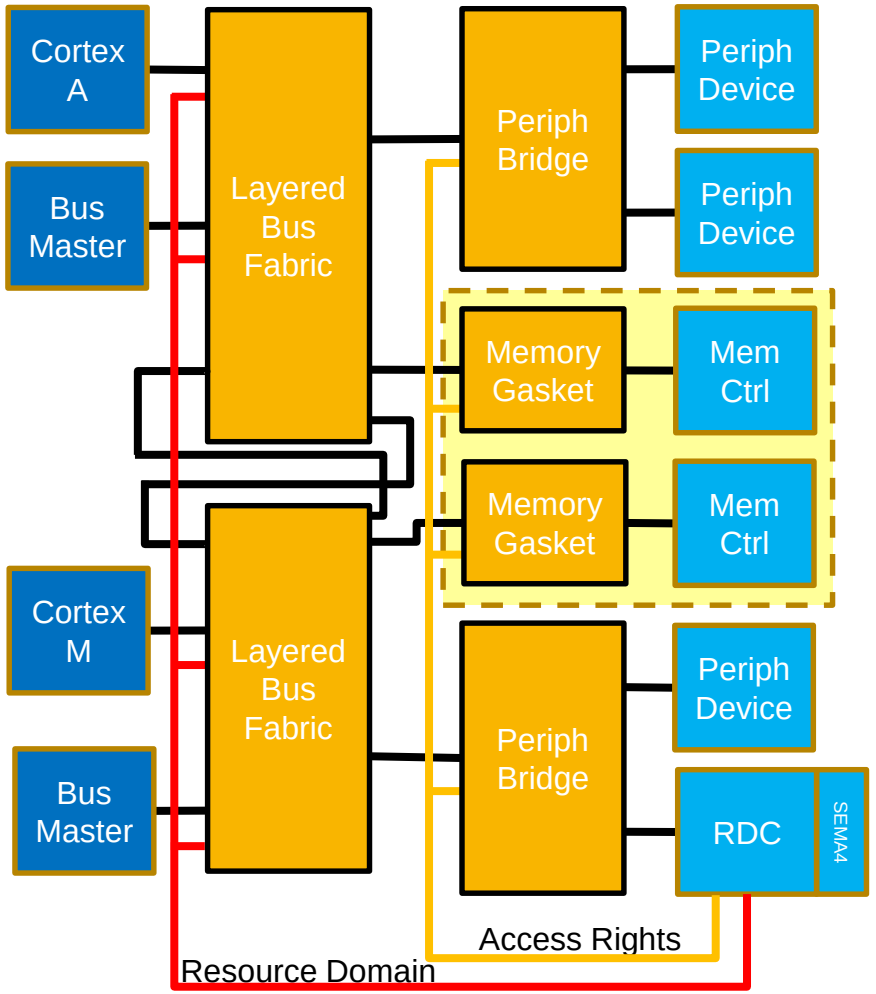
- Resource Domain Controller (RDC) is a new module integrated into next-gen i.MX devices
- RDC provides a centralized programming model to configure isolation and sharing of system resources

- **Key RDC features:**
  - Assignment of master resources (CPUs and bus mastering peripherals) to a **resource domain**
  - Configuration of read/write access for slave peripherals based on **resource domain**
  - Partitioning of memory into regions that can have separate domain access controls
  - Configuration of read/write access for memory regions based on **resource domain**
  - Integral semaphore hardware enables cooperative software to safely access peripherals with access by multiple domains
  - Optional enforcement of semaphore usage to reject accesses by master resources that have not obtained the semaphore lock



Shared Memory

- Shared bus topology allows sharing of internal/external memories
- RDC hardware can be used to partition each memory individually and restrict access based on resource domain

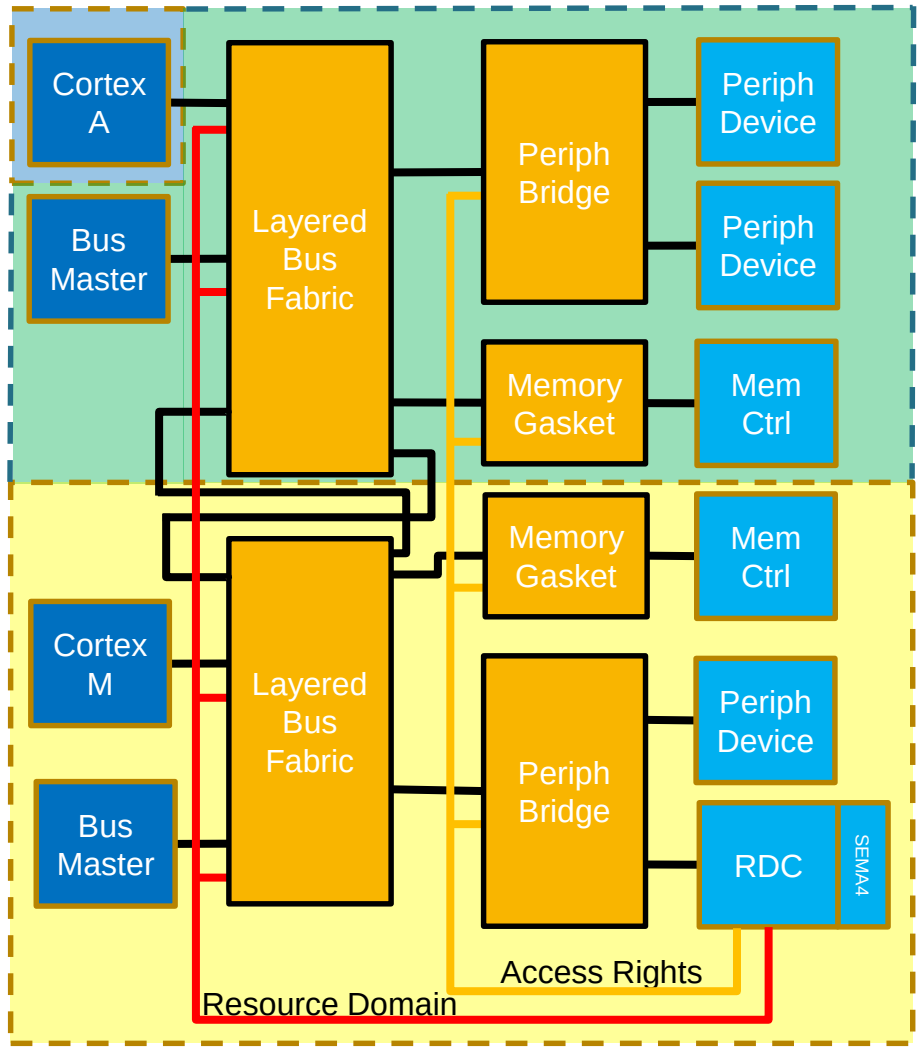


RDC Initialization

- RDC should be isolated to ensure that only a trustworthy master resource can configure the registers
- Recommended options for initialization of RDC:
  - Configure RDC during secure boot and lock configuration registers from further modification
  - Configure the RDC to accessible only from CA9 and use CSU to further restrict access to secure supervisor software (TrustZone)
  - Configure the RDC to be accessible only from trustworthy domain and use CSU to further restrict access to supervisor software

Power Domain Partitioning

- System resources are partitioned into multiple power domains
- Power domains with unused resources can be powered down under software control to save leakage
- Cortex-M and low-power peripherals are located in a separate low-leakage domain to enable low-power processing



High-Power CPU Domain

High-Power Peripheral Domain

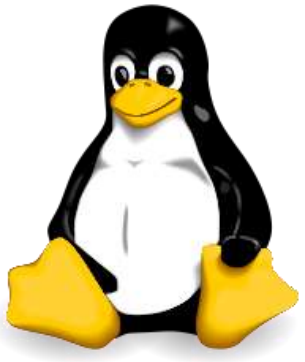
Low-Power CPU and Peripheral Domain

Summary of i.MX HMP Features

Feature	HMP Benefits
Integration of Cortex-A and Cortex-M processors	• Execute rich OS on Cortex-A and real-time software on Cortex-M • Cortex-M enhances low-power capability • Use Cortex-M to increase system integrity and security • Leverage proven Cortex-M software solutions
Shared Bus Topology	• Efficient use of system resources • Flexibility to adapt to new use cases
Resource Domain Controller	• Allows software to partition peripherals and memories into resource domains with assignable access permissions • Integrated hardware semaphore facilitates safe sharing of peripherals
Messaging Unit (MU)	Flexible interprocessor communication
Hardware Semaphore (SEMA4)	HMP synchronization to shared resources
Shared Memory	Efficient interprocessor communication
Power Domain Partitioning	Flexibility to enable low-power processing

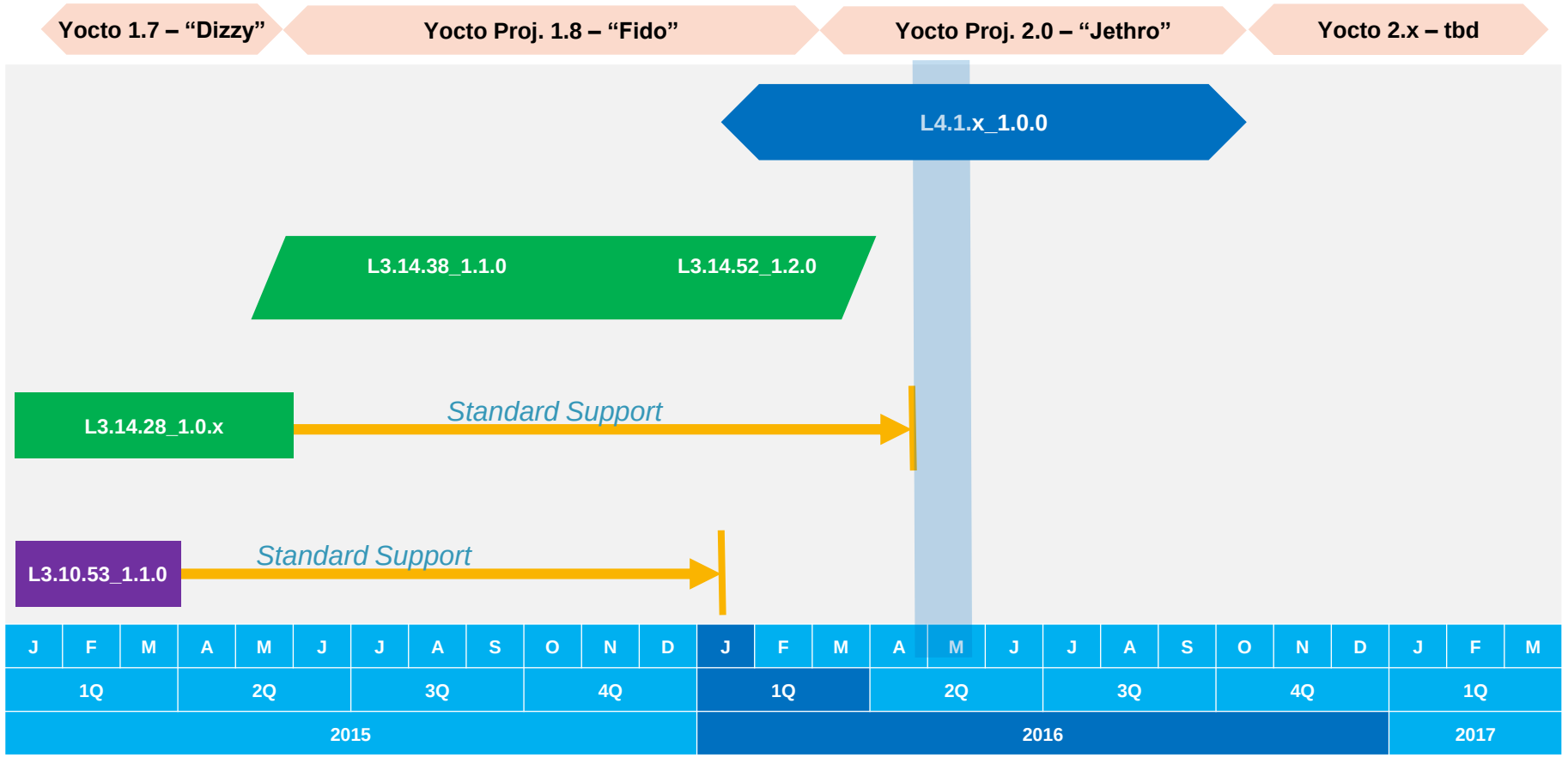
SOFTWARE

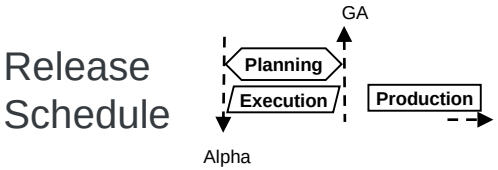
i.MX 7: Software



yocto PROJECT

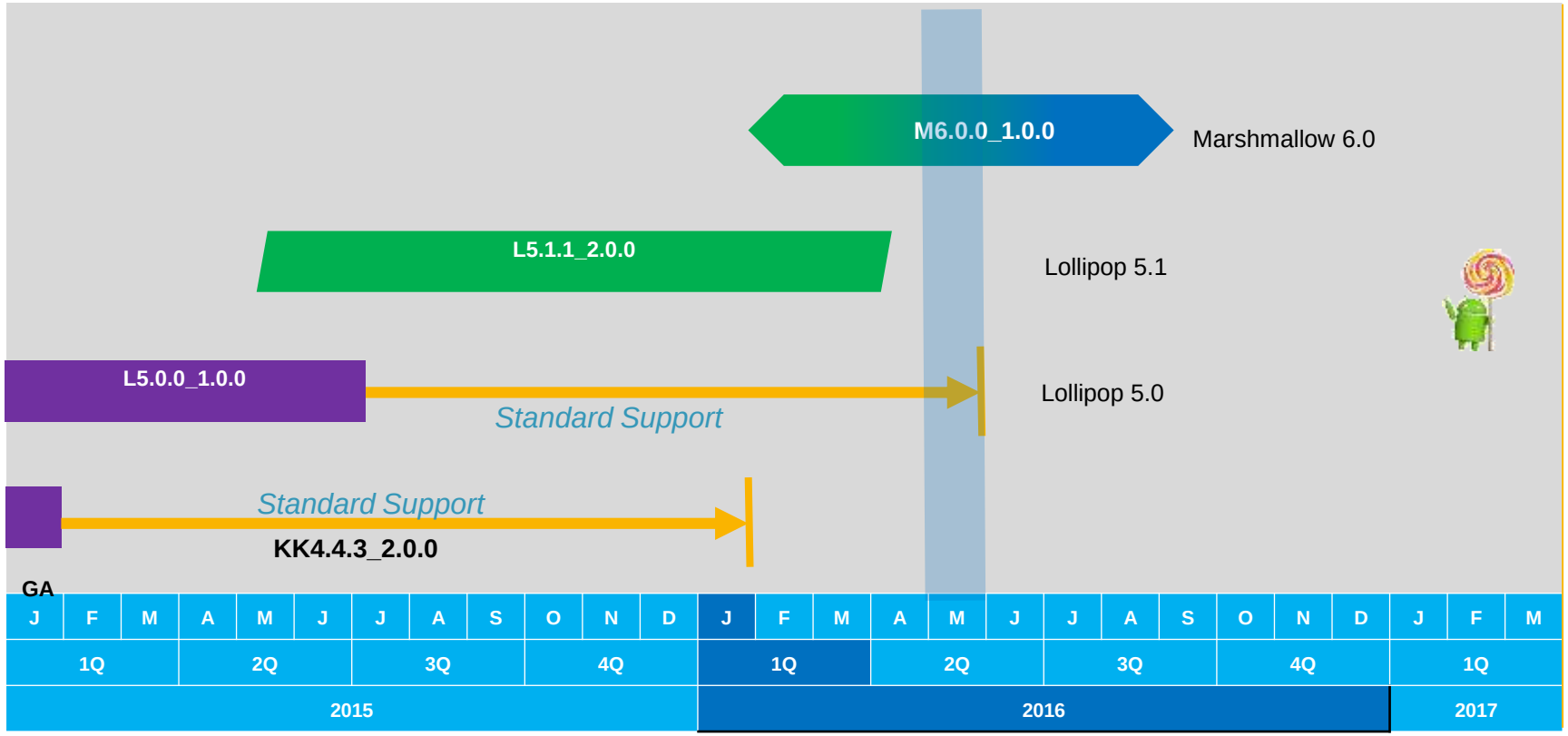
Linux Roadmap

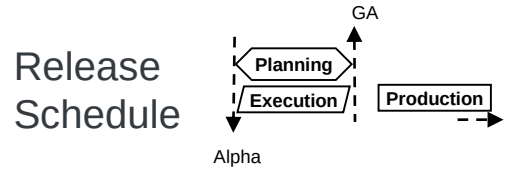




Consolidated GA – Support for 1 year

Android Roadmap





Linux Kernel

- 4.1.x
- 3.14.x
- 3.10.x

Supported Platforms

Consolidated GA – Support for 1 year

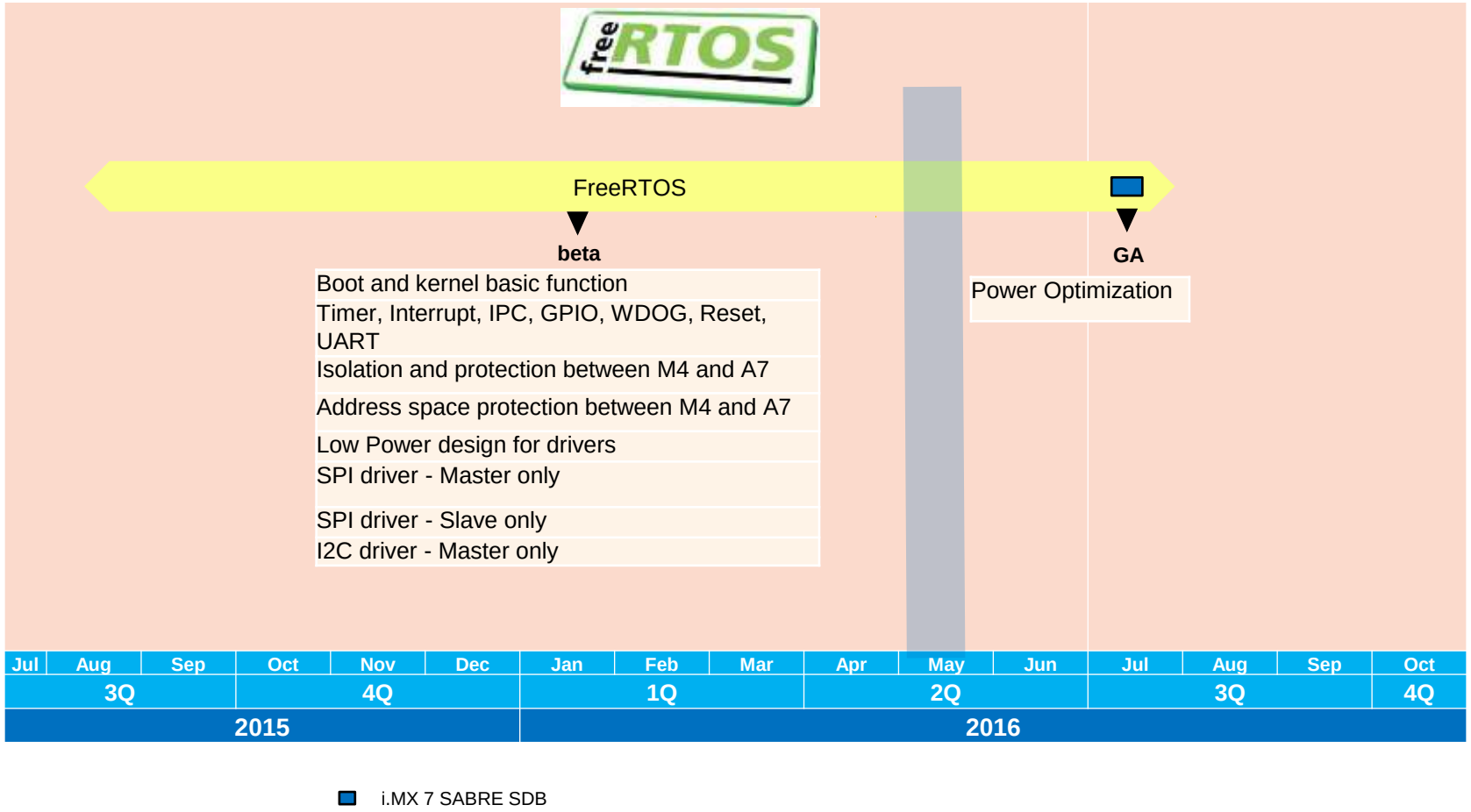
GA – Support for 1 year

Alpha & Beta & SAGA – Availability until next release

i.MX 7 FreeRTOS Roadmap

Supported Peripherals

- ADC
- CCM
- GPIO
- I2C
- MU
- UART
- WDOG
- ECSPI
- FlexCAN
- GPT
- Resource Domain Control (RDC)
- SEMA4



GA – Support for 1 year
Alpha & Beta – Support until next release

FreeRTOS Key Features

- From their website
- ”The Market Leading, De-facto Standard and Cross Platform Real Time Operating System RTOS).”
- Multiple tasks with priority support
- Priority-based pre-emptive scheduler
- Semaphores/Mutexes (w/ priority inheritance)
- Message Queues and Message Passing
- Power Saving in Idle Modes

FreeRTOS – Usability Features

- Full Source Code
- Small (<10KB) code size (configurable based on options)
- Kernel Aware Debugging in IDE
- Example FreeRTOS projects for RTOS features available
- Most configuration occurs via header file (FreeRTOSConfig.h in the FreeRTOS case)

FreeRTOS Unique Features

- Task notifications: An RTOS task notification is an event sent directly
  - to a task that can unblock the receiving task, and optionally update the receiving task's notification value.

- Recursive mutex: A mutex used recursively can be 'taken' repeatedly by the owner

- Stack overflow hook/notification: There are two optional mechanisms that can be used to assist in the detection and correction of stack overflow events.

- Deferred interrupt handling: A mechanism is provided that allows the interrupt to return directly to the task that will subsequently execute the pended function.

- Blocking on multiple objects: Queue sets are a FreeRTOS feature that enables an RTOS task to block (pend) when receiving from multiple queues and/or semaphores at the same time.

FreeRTOS Licensing

- Open Source (LGPL), Free of charge, no royalties
- Uses a modified GPL to allow you to distribute a combined work that includes FreeRTOS without being obliged to provide the source code for proprietary components
- OpenRTOS available if want to modify kernel without releasing changes

- Details at http://www.freertos.org/a00114.html

ENABLEMENT

NXP Full Solutions

i.MX 7

- **1 GHz** ARM® Cortex™-A7
  - **NEON™ coprocessor**
- ARM® Cortex™-M4,
- **Electronic Paper Display (EPD)** in addition to LCD.
- Targeting a broad range of applications including many **low power**, **portable** consumer devices

+

PMIC

- Integration of NXP'sPMIC chip set with i.MX processor for optimization of power efficiency and software/hardware integration
- One-stop customer service and support during development phase to enable the design process

+

Sensors

- MEMS gyroscopes for reliable sensing and measuring
- Magnetometers: measuring the magnitude and direction of magnetic fields
- Pressure Sensing Devices, composed of single silicon, piezoresistive devices

=

i.MX 7 SABRE Board

Development platform:

- Single-board evaluation kit
- Linux® and Android™ Board Support Packages are available out of box and updates through NXP.com

A Single Solution for Streamlined Performance

i.MX Software and Support

Professional Services
- Managing Skills Gaps & Engineering Capacity
- SW&HW Services, GFX, Linux Kernel expertise,

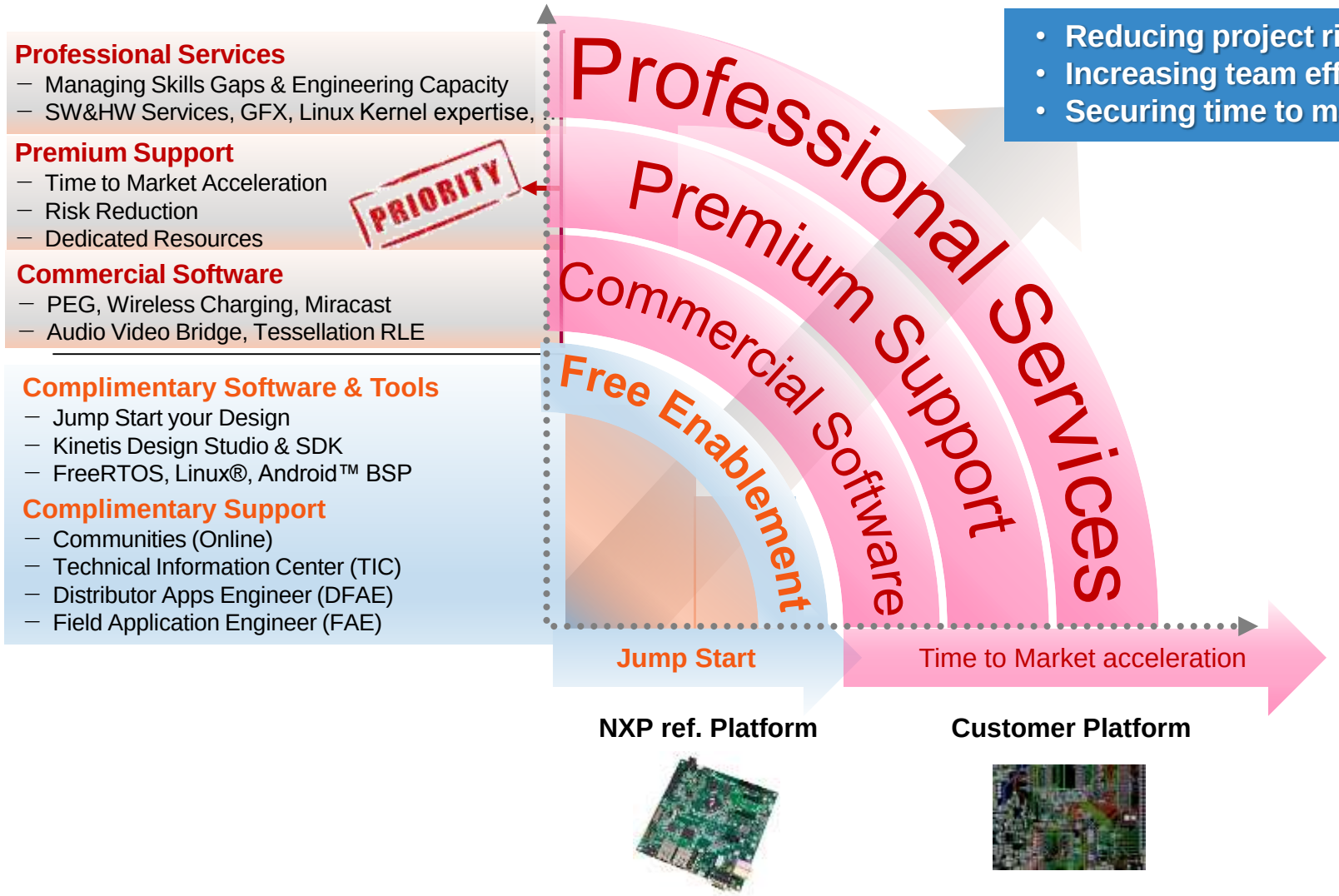
Premium Support
- Time to Market Acceleration
- Risk Reduction
- Dedicated Resources

PRIORITY

Commercial Software
- PEG, Wireless Charging, Miracast
- Audio Video Bridge, Tessellation RLE

Complimentary Software & Tools
- Jump Start your Design
- Kinetis Design Studio & SDK
- FreeRTOS, Linux®, Android™ BSP

Complimentary Support
- Communities (Online)
- Technical Information Center (TIC)
- Distributor Apps Engineer (DFAE)
- Field Application Engineer (FAE)



- Reducing project risk
- Increasing team efficiency
- Securing time to market

i.MX 7D SABRE

i.MX 7: SABRE Platform Key Features

Processor
- NXP i.MX 7Dual
  - Dual Cortex™-A7 @1GHz
  - 512KB L2$
- NXP PF3000 PMIC

Memory
- 1 GB DDR3
- eMMC5.0 footprint
- QuadSPI Flash
- SD/MMC socket
- NAND footprint

Display/Camera Connectors
- HDMI
- Parallel LCD
- MIPI-DSI
- Electronic Paper Display
- MIPI-CSI (camera)

Wireless
- Wifi (802.11ac) onboard
- BT4.0 / BLE onboard

Audio
- Audio HP Jack
- External speaker connection

Connectivity
- USB Host connectors
- microUSB OTG connector
- 2 ETH (1Gbit) Receptacle
- Full Mini PCIe socket
- SIM Card slot
- CAN (DB-9)
- GPIO
- MikroBus expander

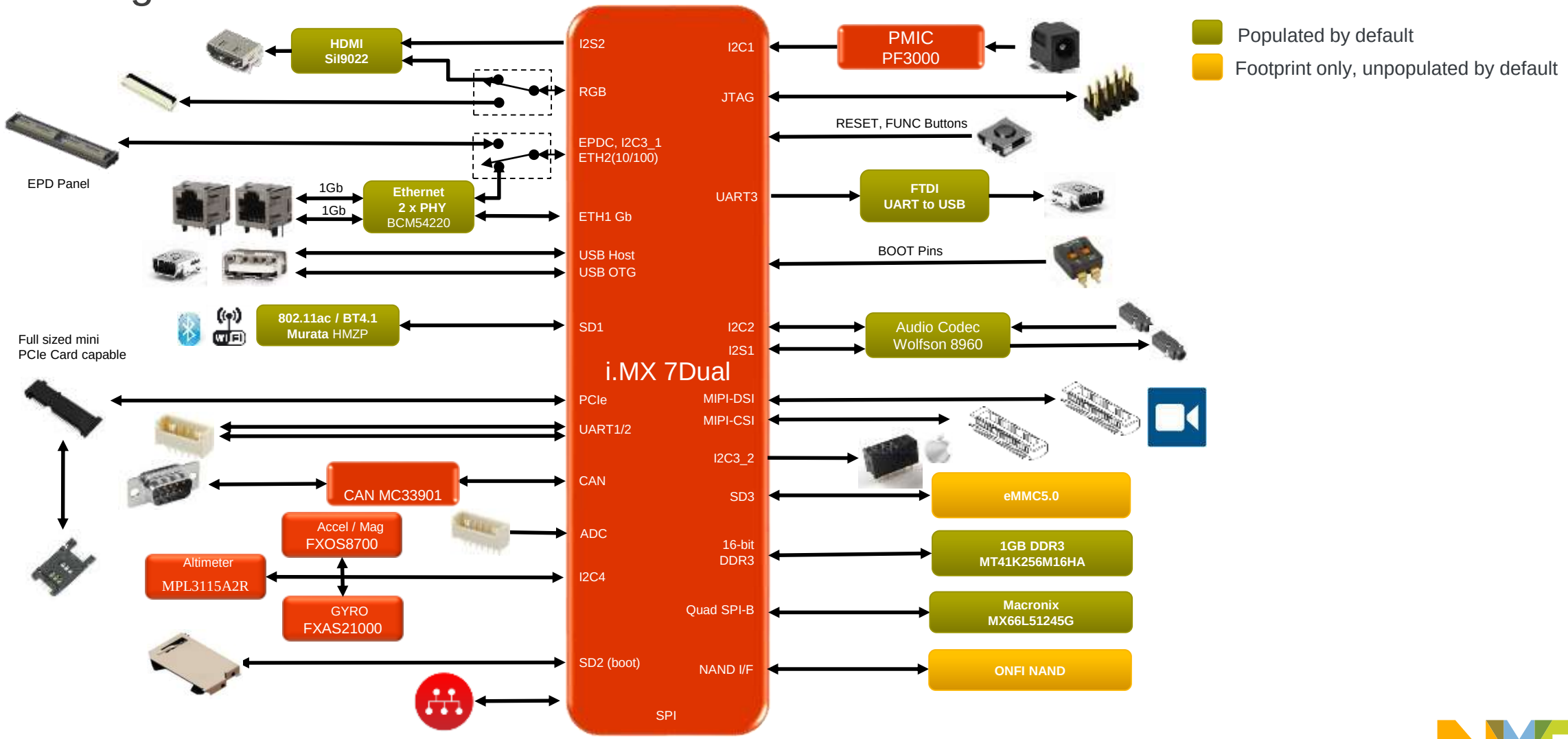
Debug
- JTAG connector
- UART via USB

Sensors
- **FXOS8700** three-axis digital accelerometer/Magnetometer
- **MPL3115A2R** Altimeter/Pressure sensor
- **FXAS21000** three-axis digital Gyroscope

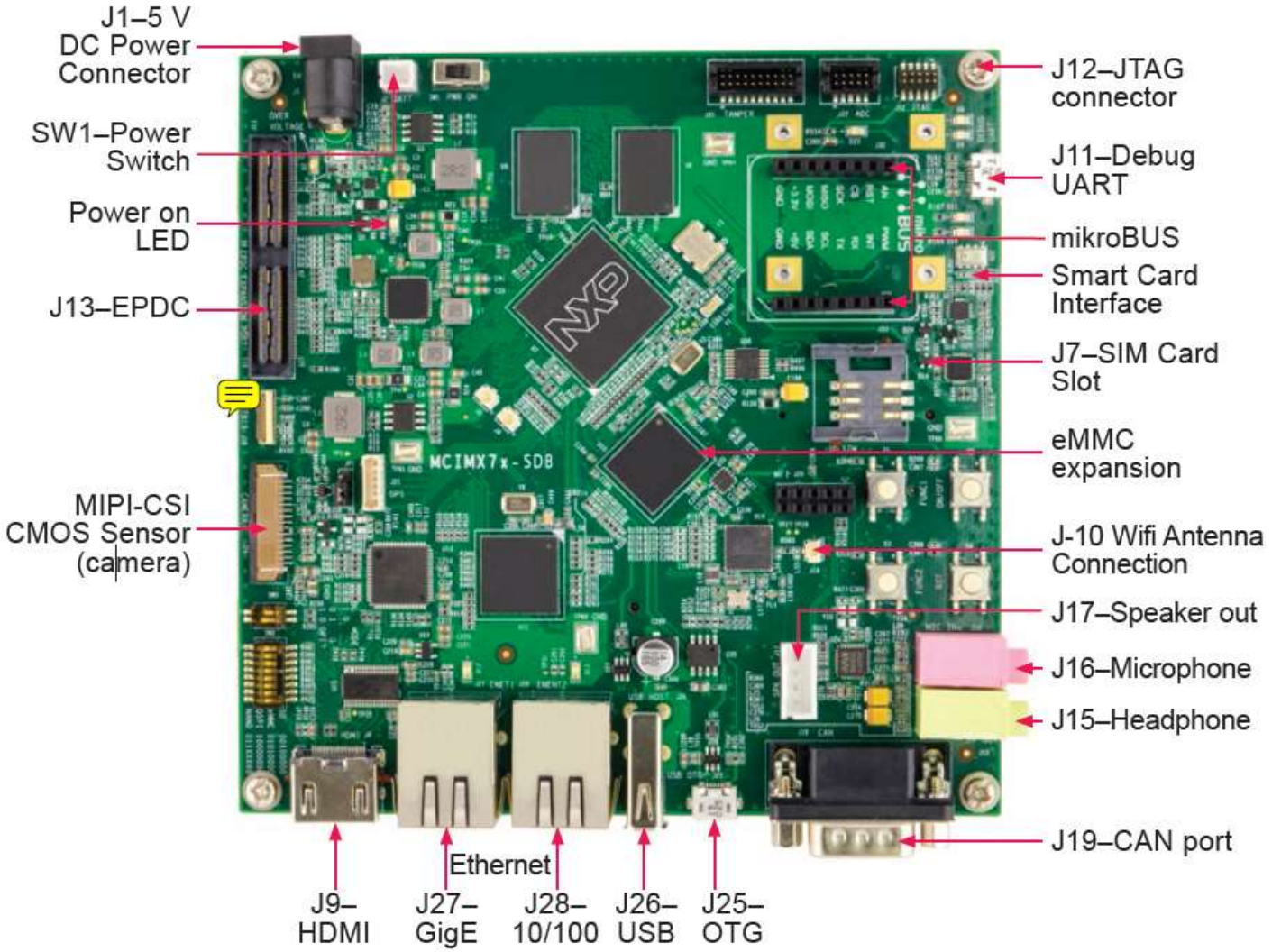
Tools & OS Support
- Linux®
- Android™
- FreeRTOS

i.MX 7 Platform

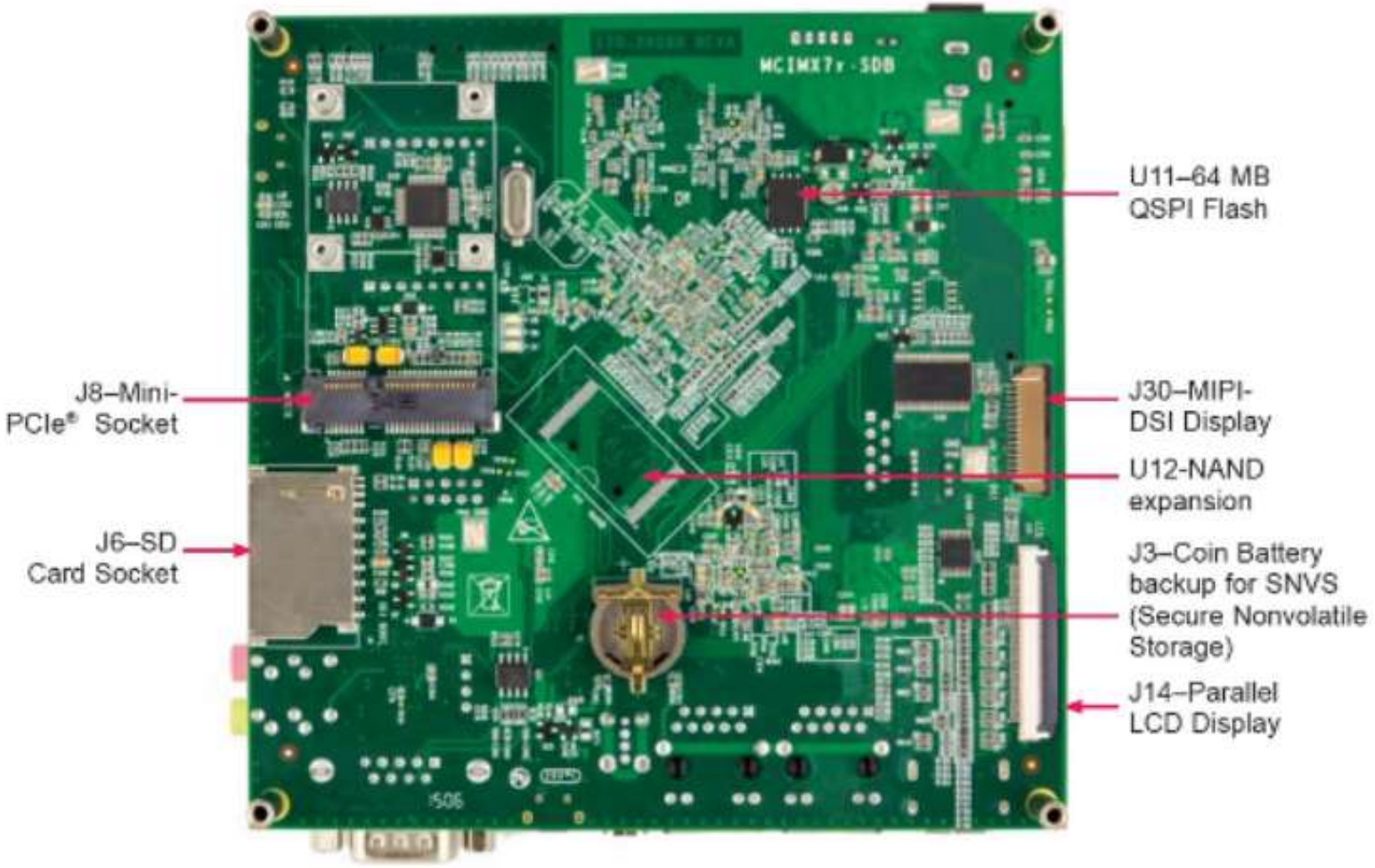
Block Diagram



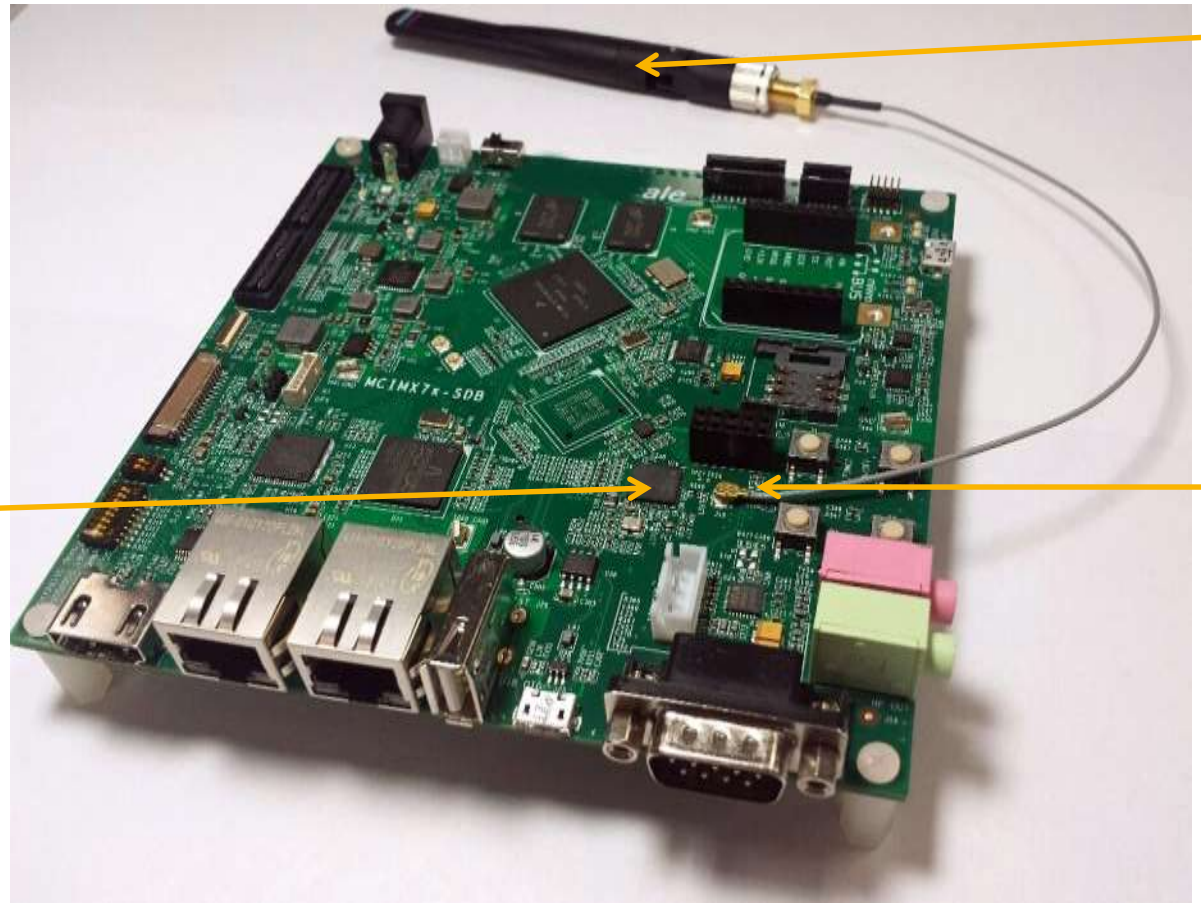
SABRE Top Side



SABRE Bottom Side



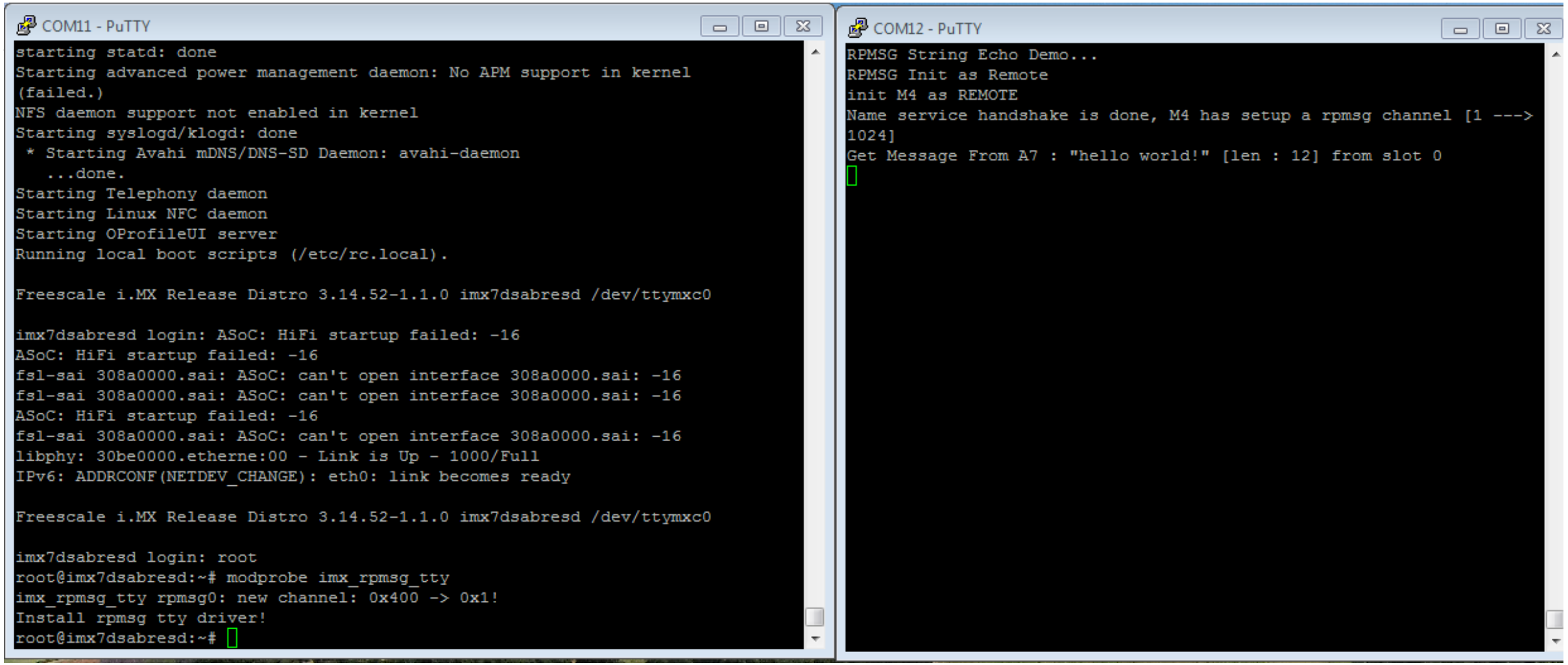
NXP i.MX 7D EVK with Wi-Fi/BT Module



SECURE CONNECTIONS
FOR A SMARTER WORLD

RPMSG DEMO

Virtual TTY Demo



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