

Vehicle Network Processing with the MPC5748G MCU + LS1043A MPU

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FAE - Automotive
Gateway

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SECURE CONNECTIONS
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Agenda

- Automotive Gateway Evolution
- NXP Next-Gen Gateway Solution
- Hardware Enablement
- Software Enablement
- Demo Applications
- Summary

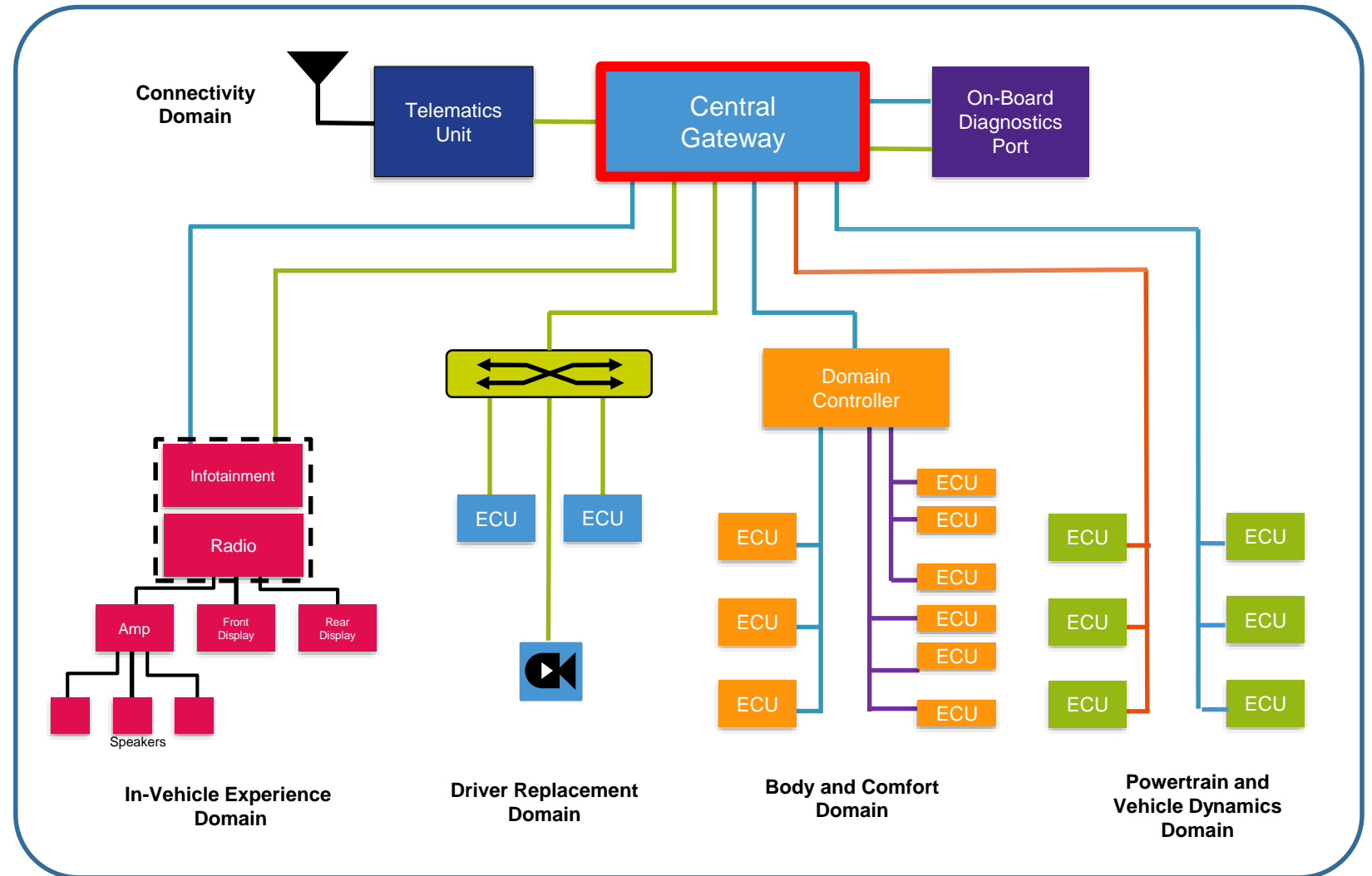
Automotive Gateway Evolution



Next-Gen Gateway in Vehicle Network

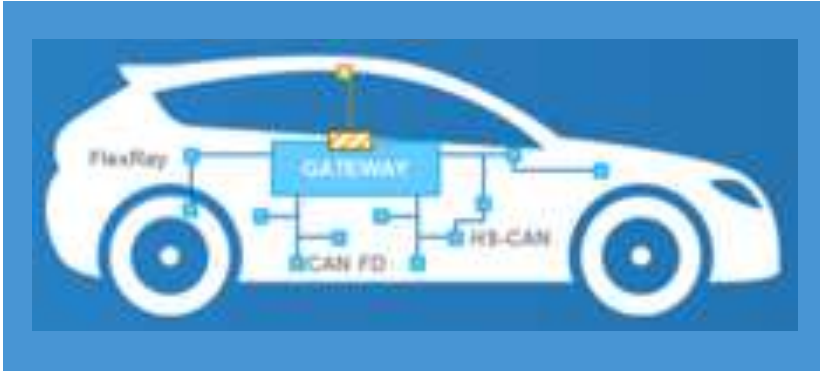
Key Gateway Use Cases

- Protocol Translation
- Network Security
- OTA Updates Management
- Diagnostics / Prognostics
- Applications & Services



Next-Gen Gateways: More Processing and Networking

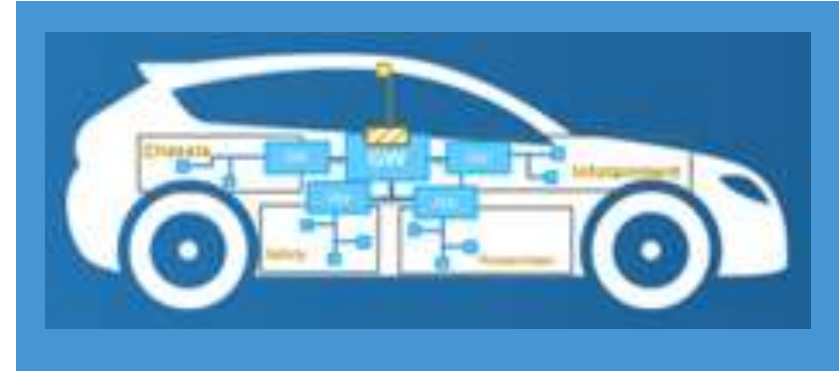
Today's Gateways



- Basic Gateway
- Microcontroller
- < 1000 DMIPS performance
- 1 or 2, 100 Mbps Ethernet
- 5 – 8 CAN interfaces

> 10x

2020+ Gateways



- Advanced Gateway with Services
- Microcontroller + Microprocessor
- 10,000+ DMIPS performance
- 3 – 5, Gigabit Ethernet
- >8 CAN / CAN FD interfaces

Next-gen Gateway: Processing

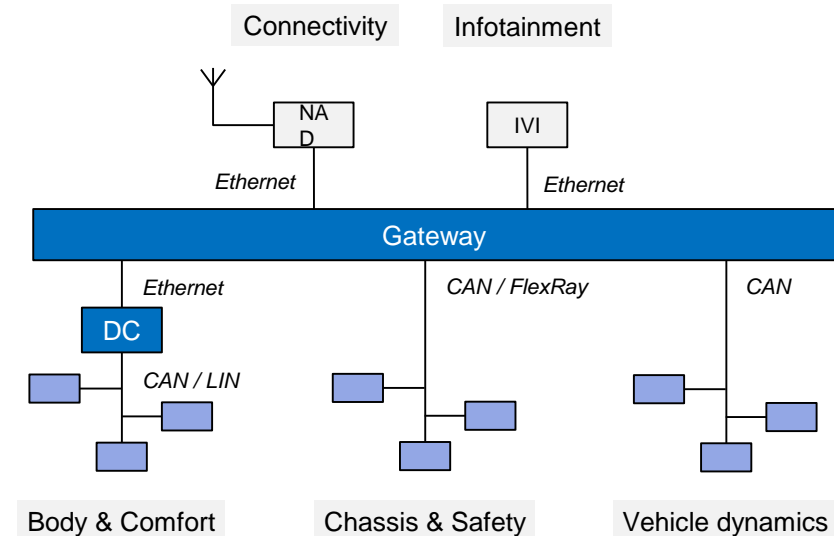
- **1000's of DMIPS performance** required for 2020+ gateway architectures
- **Applications and Services:** Feature deployment through software modules rather than new ECUs
 - **ECU Consolidation**
 - **Advanced OTA updates**
 - **Vehicle Configuration**
 - **Data Logging**
- **Big Data Analytics:** Leverage vehicle data through gateway - Descriptive / Diagnostics / Predictive
 - Security, safety & integrity of the vehicle & network
 - Data analytics

GW Feature	Processor Requirements
Applications and Services	- Application Processing (w/support for high-level OS – Linux, QNX... and hypervisors)
Big Data Analytics	- AUTOSAR Adaptive Platform for service-oriented gateways (services and APIs)
ECU Consolidation	- Compute Performance - Scalability to higher performance (e.g., expansion via PCIe)

Next-gen Gateway: Networking

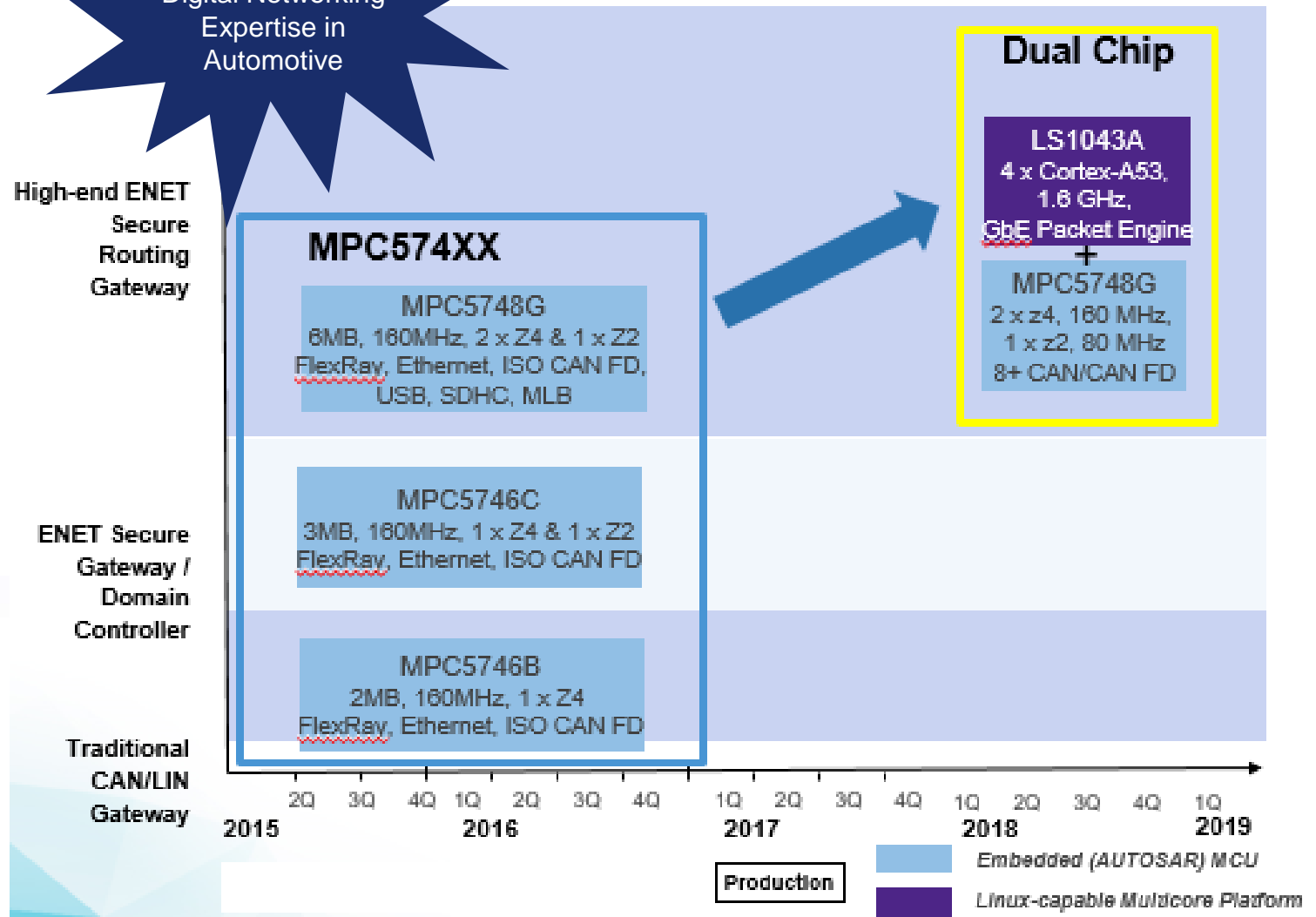
- Move toward an **Ethernet backbone** to connect domains to gateway
 - Bandwidth needs – Autonomous Platforms
 - Domain controller approach – simplifies logistics of deploying vehicle platform
 - **IP Routing, VLAN & >L3 firewalling** to Isolate & Protect Ethernet domains
 - Diagnostics over IP (DoIP) usage widespread
- Hybrid Approach in 2020+
 - Typical: **3-5 Ethernet domains + 8 or more CAN**
- CAN channels increasing with majority of OEMs
 - Driven by domain isolation
 - Higher bandwidth needs move to CAN FD
 - **10 to 12 typical for 2020+**

GW Feature	Processor Requirements
Ethernet Network Processing	<ul style="list-style-type: none"> - Packet Acceleration hardware - Deep Packet Inspection driver need for higher processor performance - Ethernet Intrusion Detection
CAN Network Processing	<ul style="list-style-type: none"> - >8 CAN/CAN FD interfaces - More performance for CAN Intrusion Detection



NXP Gateway Processor Roadmap

Leveraging NXP Digital Networking Expertise in Automotive



NXP Next-Gen Gateway Solution



Dual Chip Gateway Solution

- **Enables Next-gen CAN-Ethernet Gateways**

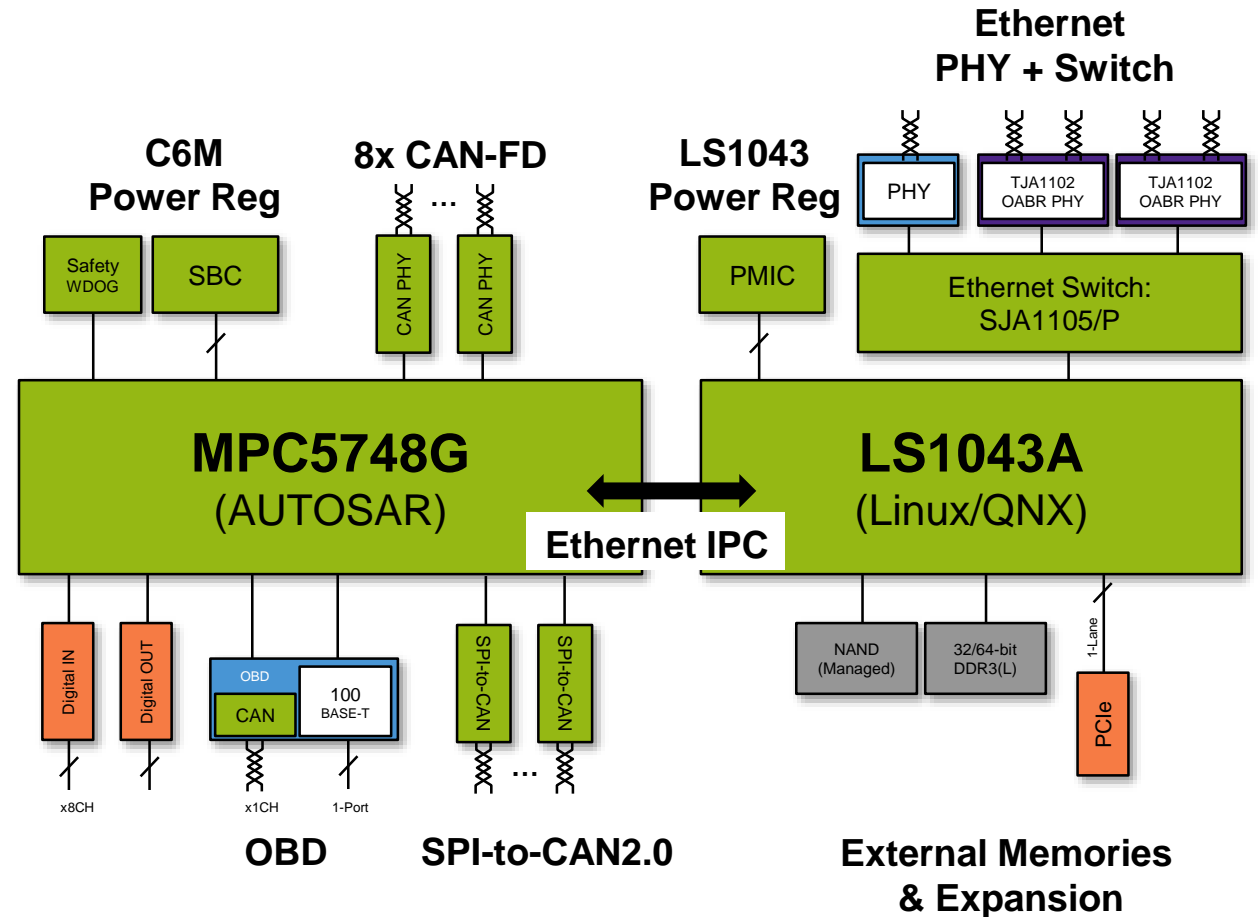
- Automotive Gateway + Network Processing (Gigabit Ethernet Packet Routing) + Applications
- MPC5748G (MCU) + LS1043A (MPU)
- Available today

- **Feature Set**

- CAN Signal Gateway (ASIL B)
- 4x Arm Cortex-A53 (LS1043A) for Applications
- Packet Forwarding Engine

- **OS Support**

- AUTOSAR: Real-time CAN gateway
- Linux / QNX: Ethernet routing, applications processing



MPC5748G Gateway Microcontroller

Multicore architecture

2x e200z4 + 1x z2 Power Architecture cores

Floating Point Unit (FPU)

on z4 cores for additional computational algorithm support

High performance:

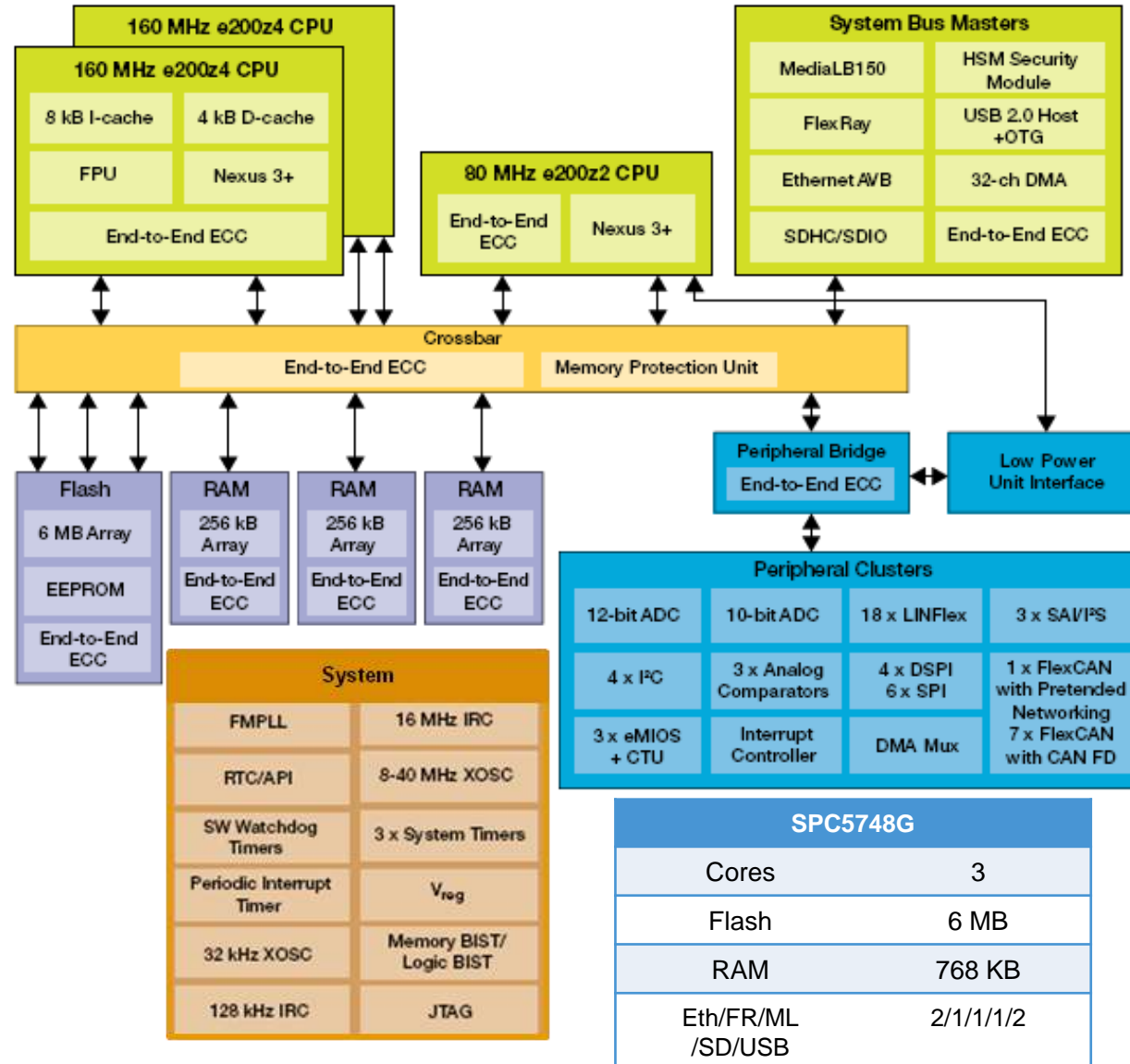
160 MHz max e200z4 cores, 80 MHz e200z2 core

Triple ported flash

and multiple RAM minimize access time to memory

Part of Safe Assure

Functional Safety Program: Designed for ISO 26262 ASIL B systems



Media Local Bus

Supports MOST for infotainment domain networking

Robust security

Hardware Security Module (HSM) option supports both SHE and EVITA low/medium security specifications

USB 2.0 (OTG and host module) supports interfacing to both wireless modems and infotainment domain

2 x Ethernet modules and **Ethernet Switch** support 10/100 Mb/s for diagnostics, backbone and AVB applications

Low-Power Unit (LPU)

provides CAN, LIN, SPI, ADC functionality in a new low power state

Broad Communications

Multiple CAN, LIN, I²C, I²S for integrated BCM & Gateway applications

QorIQ Layerscape LS1043A

Auto quality

- AEC Q100 Grade 3 (105 Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Process & Package

- 28HPM, ~4-8W Thermal Max @ 105C
- 23x23mm, Unlidded FCBGA, .8mm pitch (780 pins)

Performance

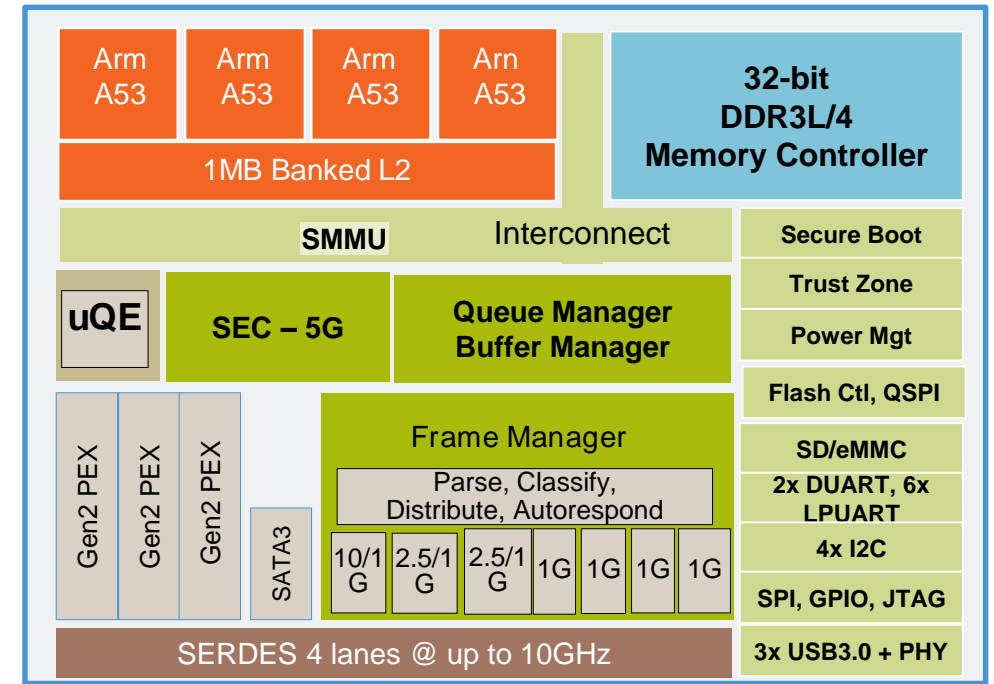
- Arm Cortex-A53 x 4 @ 1.6 GHz
 - 19.5K DMIPS
 - SpecInt2k6 – 5.95, Rate -15
 - NEON SIMD in all CPUs
- 1x36b (including ECC) DDR3L/4 up to 1.6GT/s
 - 6.4GB/s memory BW
- High Speed IO
 - Multiple PCIe Gen2 controllers
 - Multiple Ethernet MACs (up to 10G)

Functional Safety

- Target ASIL B (retroactive)
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security

- 10Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
 - Secure Boot
 - Secure Debug
 - Secure Storage
 - Tamper Detection
 - HW Enforced Partitioning
 - Arm TrustZone



NXP MPC5748G + LS1043A Features

MPC5748G+LS1043A

Microcontroller + Microprocessor

Six processor cores:
(2) PowerPC z4 + (1) PowerPC z2
(4) ARM Cortex-A53 @ 1.6 GHz

Up to 14,720 DMIPS processing

Ethernet Packet Acceleration

768 KB SRAM, 6MB embedded flash, DDR3L/DDR4 support

(2) 10/100 Ethernet (Calypso)
(4) Up to 10G Ethernet (Layerscape)

(8) CAN FD / (18) LIN

(1) USB 2.0, (3) USB 3.0, (3) Gen2 PCIe

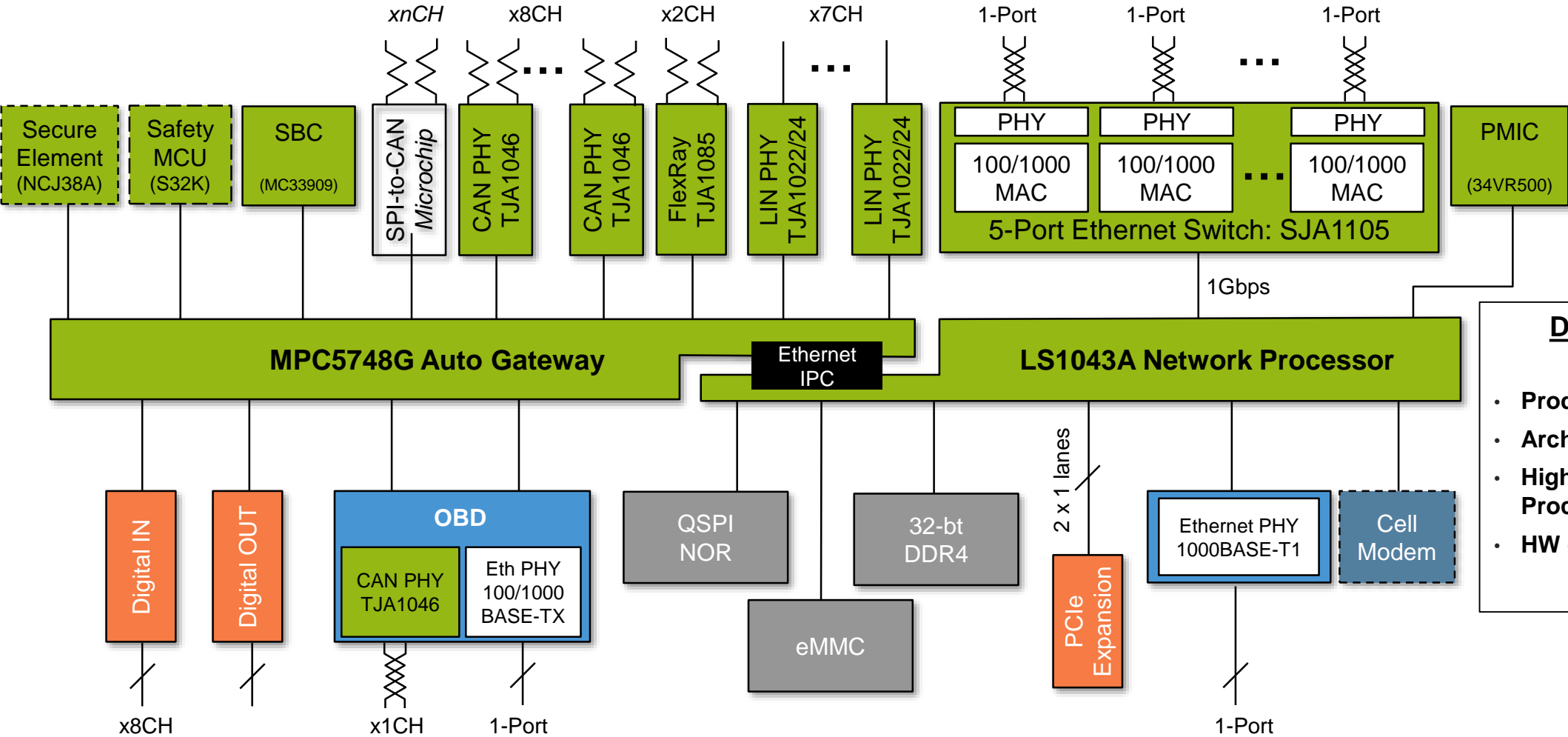
HSM Security + SEC Security

ASIL B functional safety

Production: Now

NXP Dual Chip System Solution

NXP Device



- Dual Chip System Solution**
- Production platform
 - Architecture: MCU + MPU
 - High-performance Apps Processor
 - HW offload for Ethernet

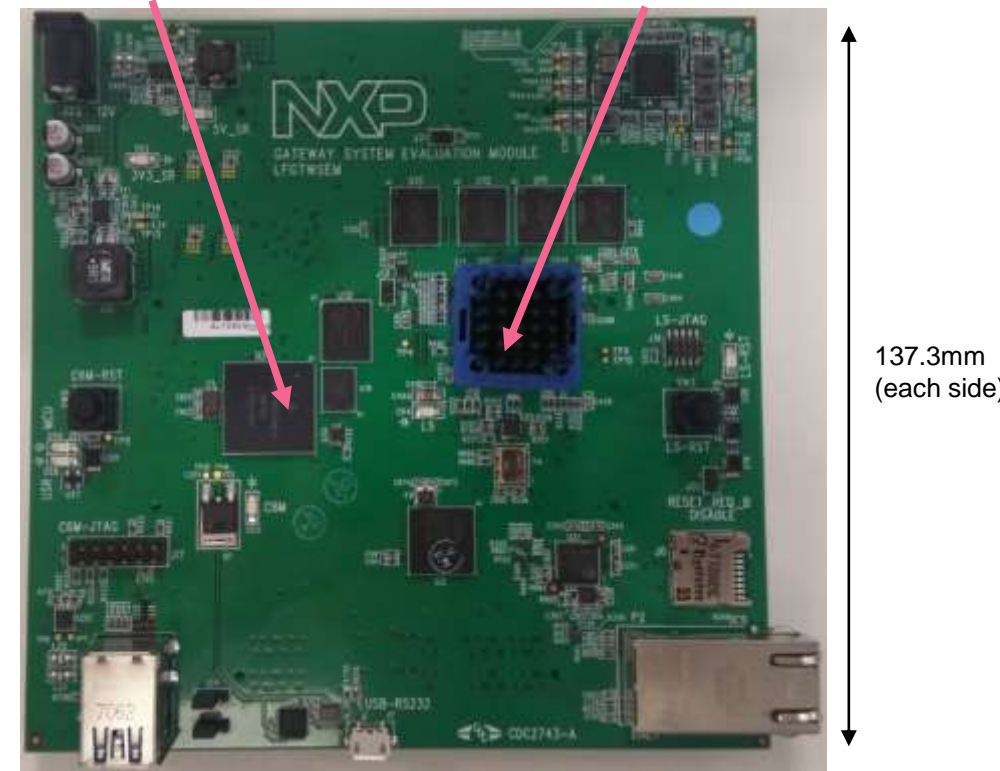
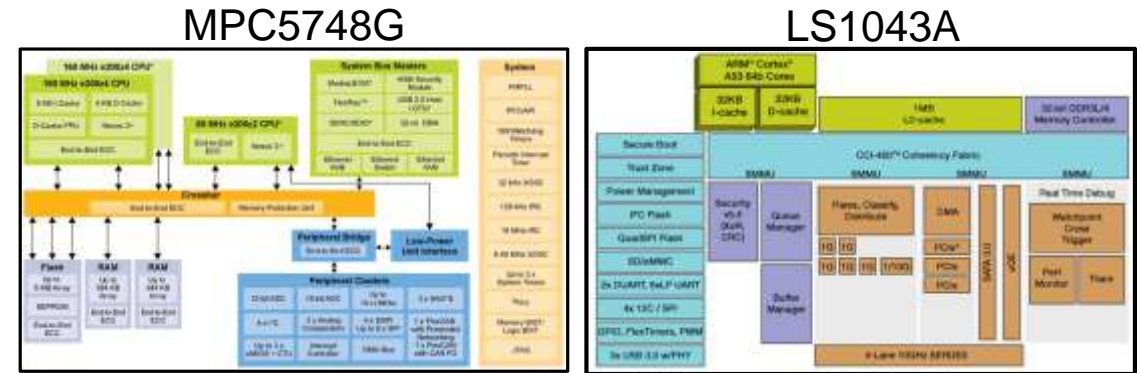


Hardware Enablement



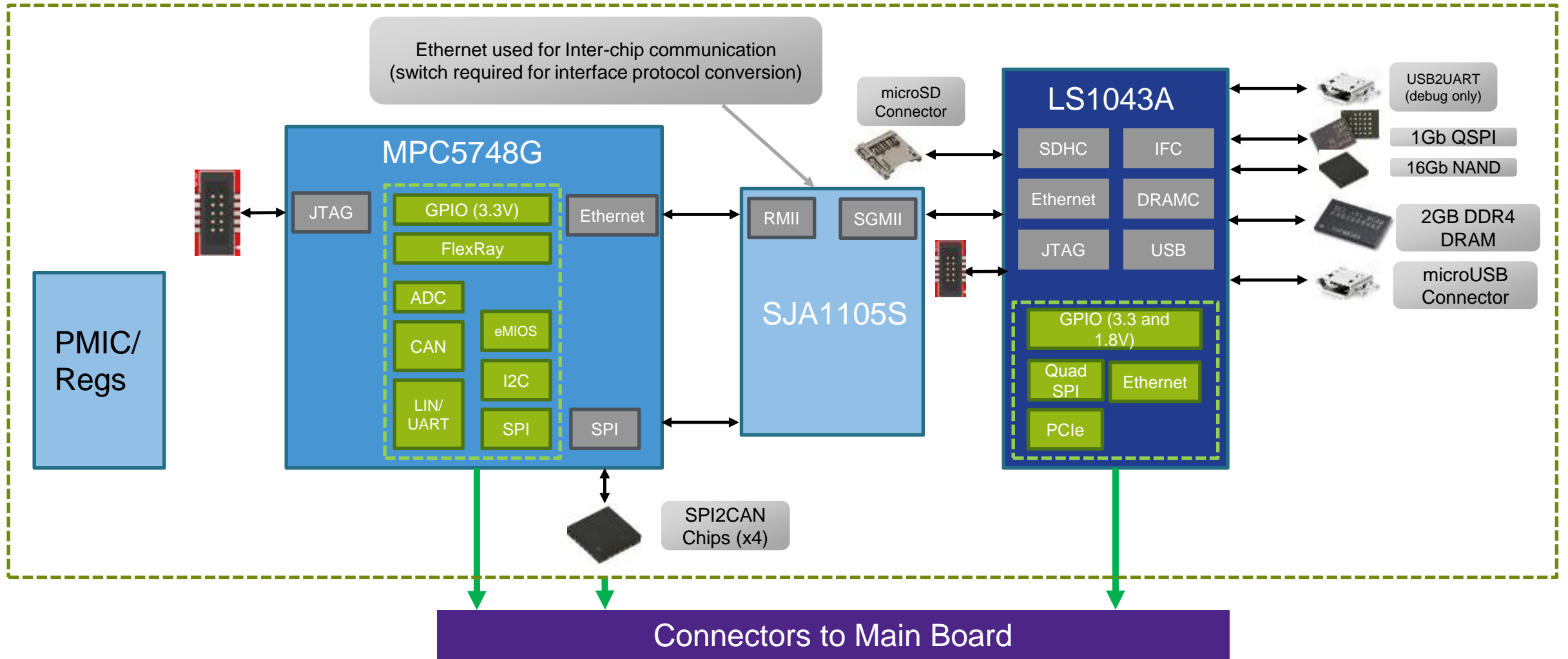
Dual Chip Module Overview

- Highlights
 - MPC5748G (Calypso6M) + LS1043A (Layerscape)
 - Standalone module. Can be used with customer hardware.
- MPC5748G (Calypso 6M) + LS1043A
 - 8x CAN FD (internal), external CAN device available for >8CHs (via SPI)
 - 2x e200z4 @ 160MHz, 1x e200z2 @ 80MHz, 6MB Embedded flash, 768KB RAM, low power modes
 - 4x Cortex-A53 @ 1.6GHz, DDR, Ethernet Routing Engine, PCIe, USB
 - Ethernet (RMII) based IPC between 2-chips (100Mbps raw)
- Modules available to support evaluation and software development now
- Module Part Number: **LFGTWSEM**



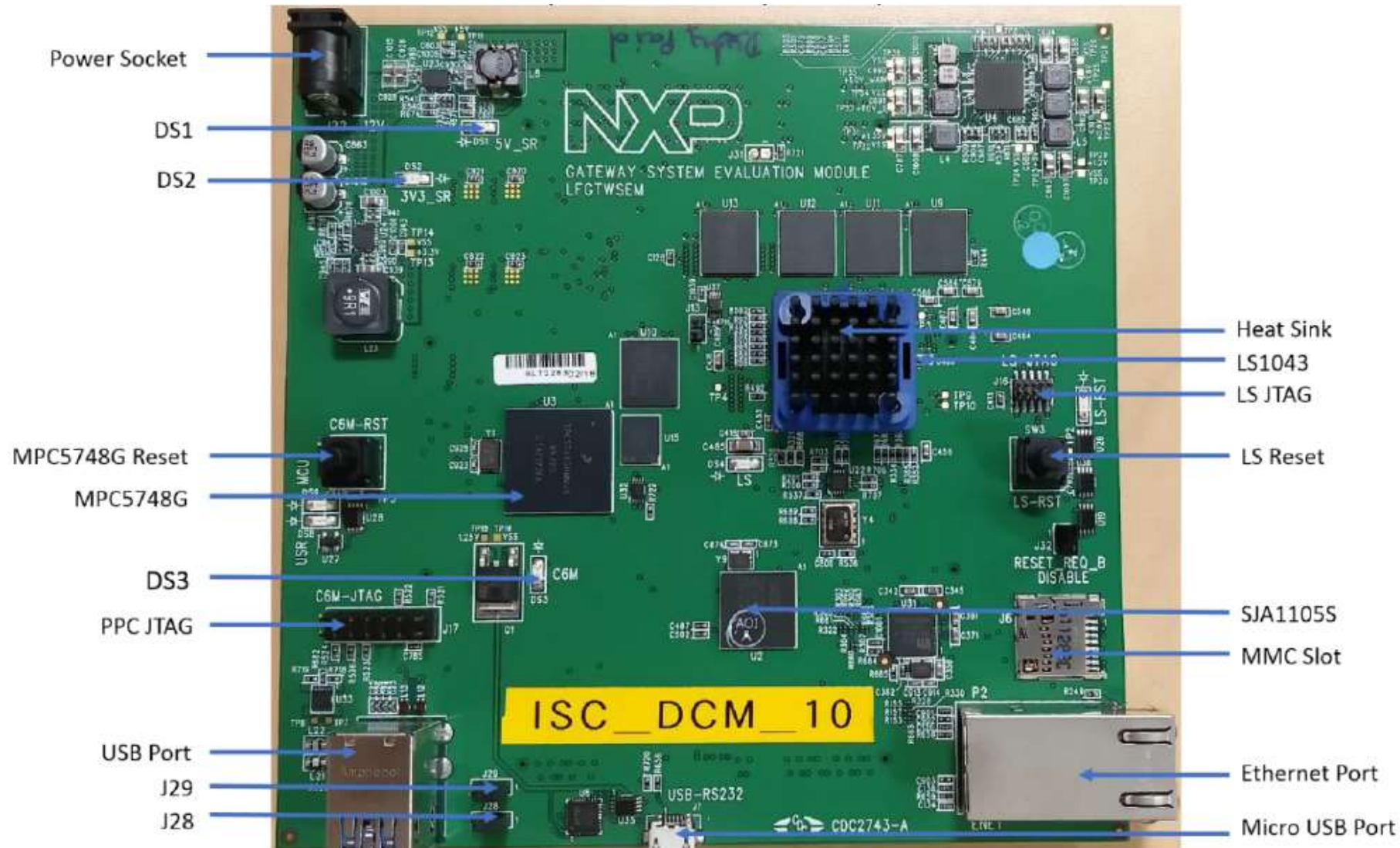
Dual Chip Module

Dual Chip Module Architecture



- Module I/O remains on daughter card
- Module I/O routed to main board

Dual Chip Module – Key Components



Dual Chip Module Back w/Connectors



Software Enablement



Dual Chip Module – Getting Started Kit

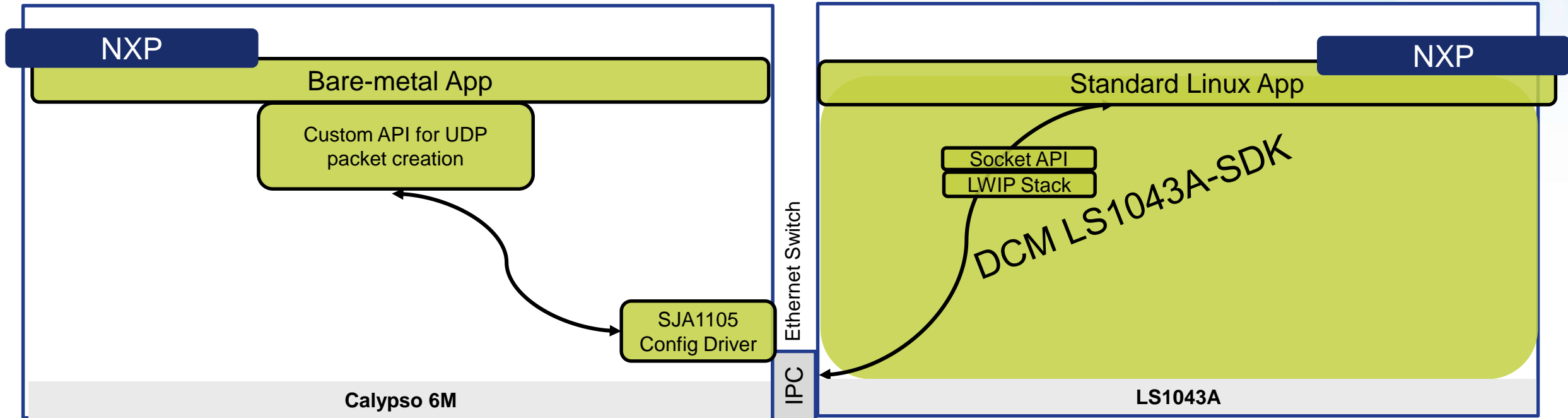
- Getting Started package is provided with the DCM board
 - Includes MPC5748G App integrated with LS1043A Linux SDK
- Content:
 - Binaries & Scripts
 - MPC5748G Bare-metal App Binary & Flashing Script
 - LS1043A Binaries: U-Boot, RCW, Frame Manager, Secure Firmware, Linux SDK
 - Documentation
 - Quick Start Guide
 - Getting Started Document
 - User Manual
 - Board Schematics
- The binaries are pre-flashed on DCM board

Dual Chip Module - Software Kit BOM

S.No	Domain	SW Details	Remarks
1	MPC5748G	Arccore AUTOSAR + NXP Switch Driver & IPCF SW	Customers looking for turnkey AUTOSAR solution S32DS based App with Switch Driver + MPC-LS communication
2	MPC5748G	NXP Baremetal Software	S32DS Rel 2017.R1 + PPC Lauterbach
3	MPC5748G	IDE/FlashTool	Rel 17.12 (Open Source)
4	LS1043A	LS SDK-Linux-Uboot	CW IDE Rel 11.2.3 + TAP & Probe Tip
5	LS1043A	IDE/FlashTool	ASK Build required for Demo Applications (NXP License, not free)
6	LS1043A	LS ASK-Linux	DCM SW Customizations on MPC5748G & LS1043A
7	MPC5748G + LS1043A	DCM Patches	Collaterals
8	MPC5748G + LS1043A	Collaterals	

DCM-MPC5748G:

NXP Bare-metal SW - High Level Overview



DCM-MPC5748G:

ARCCORE AUTOSAR SW - High Level Overview

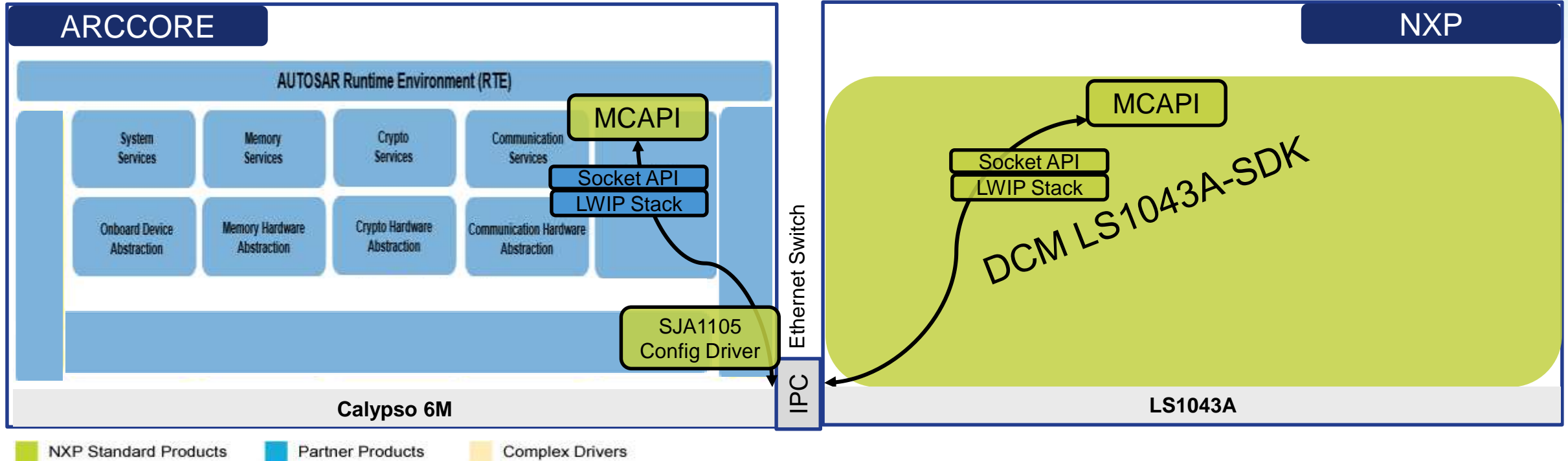
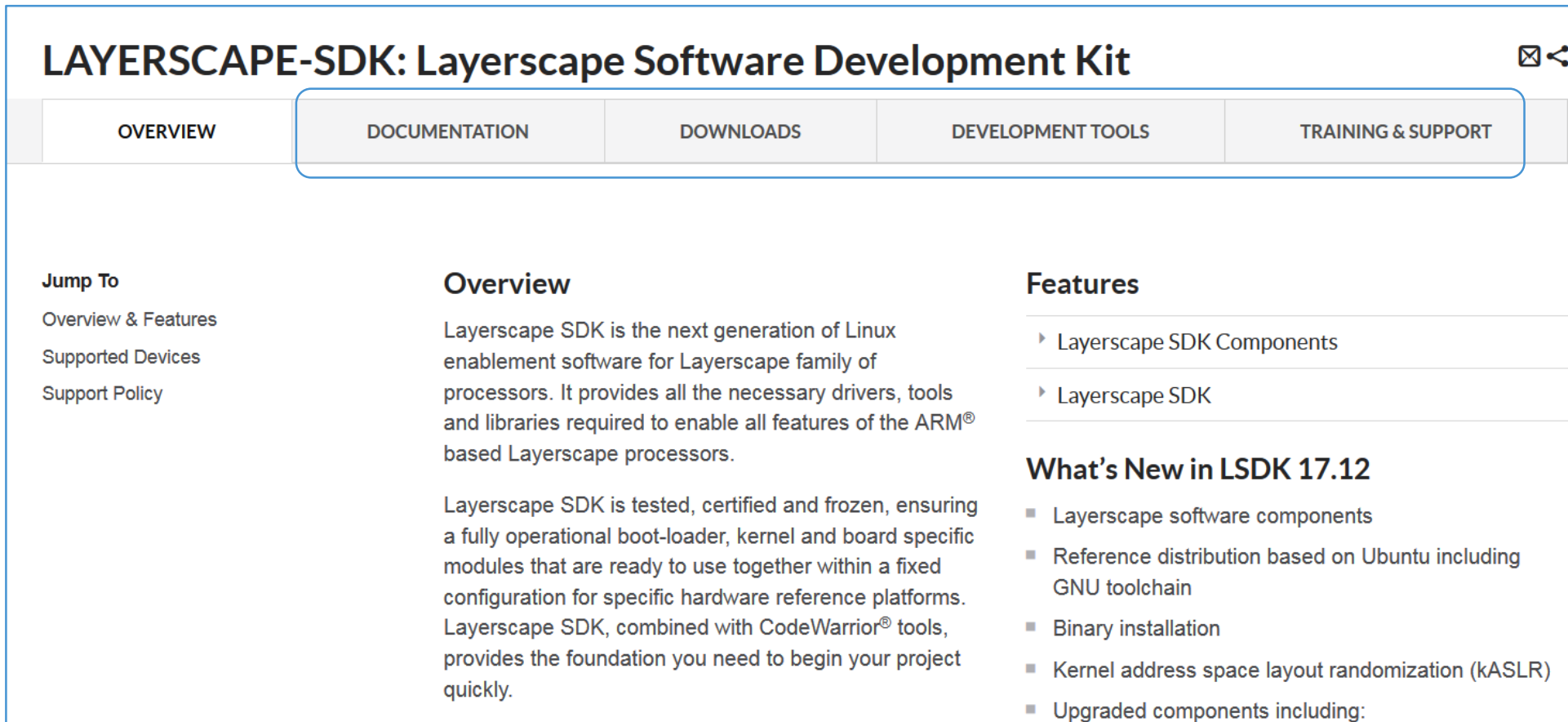


 Diagram for reference purpose only. For more details, contact AUTOSAR vendor

DCM-LS1043A: NXP SDK - High Level Overview

- [SDK URL](#)
- DCM SDK SW uses LSDK17.12
- Board specific customizations to be delivered as patches.



The screenshot displays the 'LAYERSCAPE-SDK: Layerscape Software Development Kit' website. The navigation bar includes 'OVERVIEW', 'DOCUMENTATION', 'DOWNLOADS', 'DEVELOPMENT TOOLS', and 'TRAINING & SUPPORT'. The 'OVERVIEW' page is active, featuring a 'Jump To' sidebar with links to 'Overview & Features', 'Supported Devices', and 'Support Policy'. The main content area is titled 'Overview' and describes the SDK as the next generation of Linux enablement software for Layerscape processors. It lists features such as Layerscape SDK Components and Layerscape SDK. A 'What's New in LSDK 17.12' section highlights updates like software components, Ubuntu-based reference distribution, binary installation, kASLR, and upgraded components.

LAYERSCAPE-SDK: Layerscape Software Development Kit

- OVERVIEW
- DOCUMENTATION
- DOWNLOADS
- DEVELOPMENT TOOLS
- TRAINING & SUPPORT

Jump To

- Overview & Features
- Supported Devices
- Support Policy

Overview

Layerscape SDK is the next generation of Linux enablement software for Layerscape family of processors. It provides all the necessary drivers, tools and libraries required to enable all features of the ARM® based Layerscape processors.

Layerscape SDK is tested, certified and frozen, ensuring a fully operational boot-loader, kernel and board specific modules that are ready to use together within a fixed configuration for specific hardware reference platforms. Layerscape SDK, combined with CodeWarrior® tools, provides the foundation you need to begin your project quickly.

Features

- Layerscape SDK Components
- Layerscape SDK

What's New in LSDK 17.12

- Layerscape software components
- Reference distribution based on Ubuntu including GNU toolchain
- Binary installation
- Kernel address space layout randomization (kASLR)
- Upgraded components including:

Dual Chip Module Setup (NXP Lab)

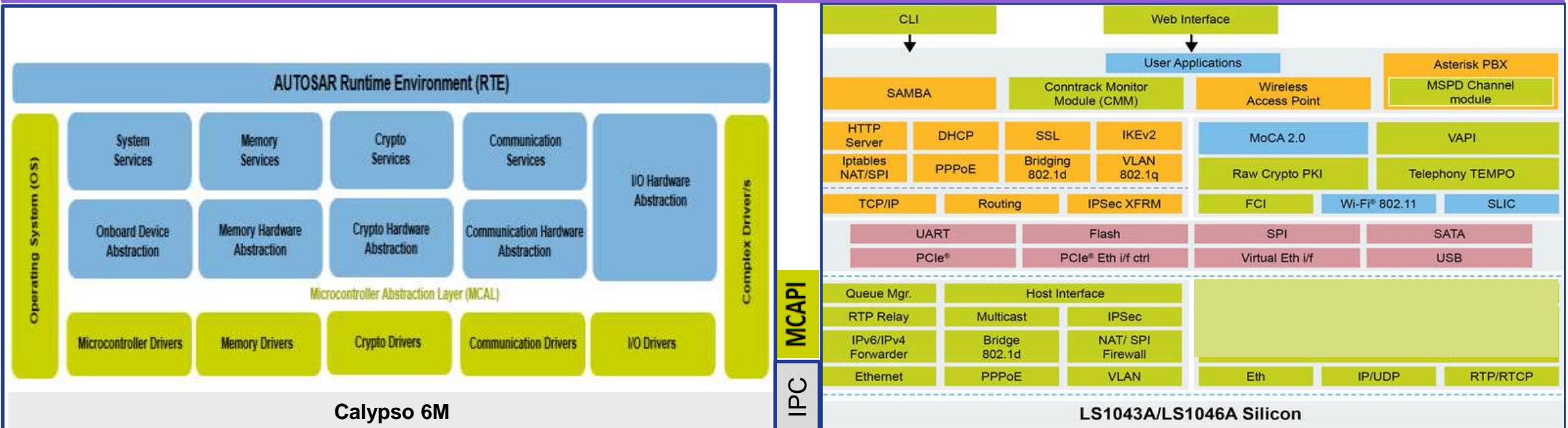
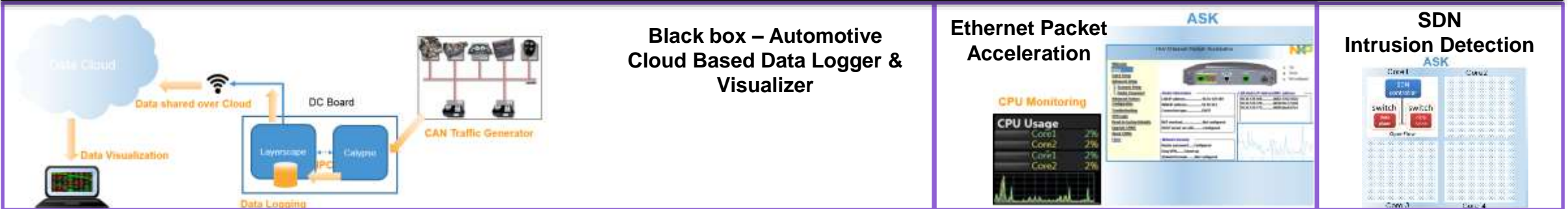


Demo Applications



Dual Chip Module Demo Applications Software

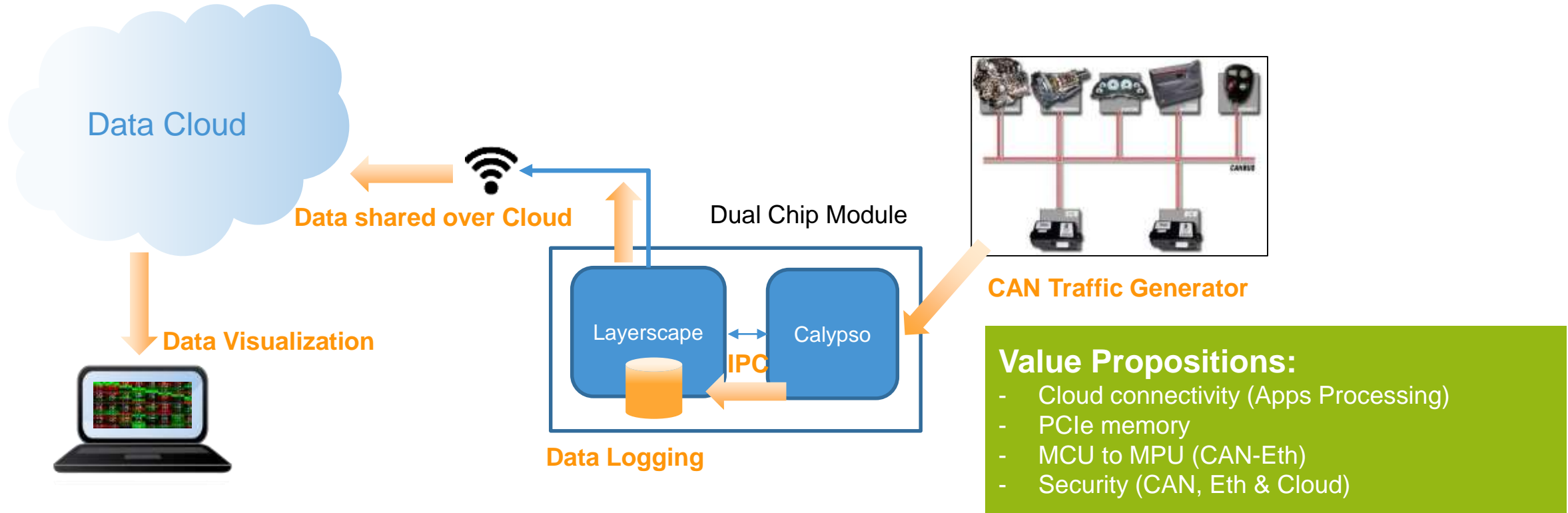
DEMO APPS



■ NXP Standard Products
 ■ Partner Products
 ■ Complex Drivers

■ NXP
 ■ Third-Party Components
 ■ Open-source SW
 ■ SDK Components

Automotive Data Logger

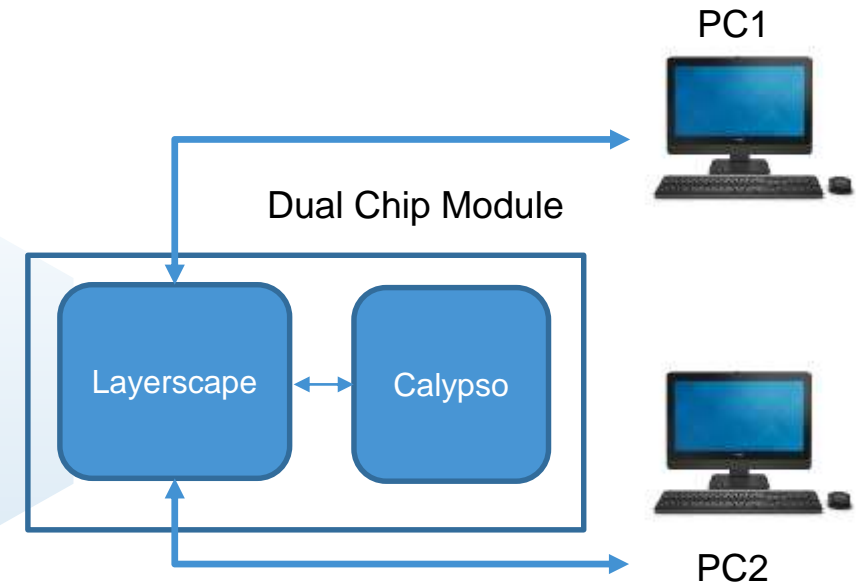
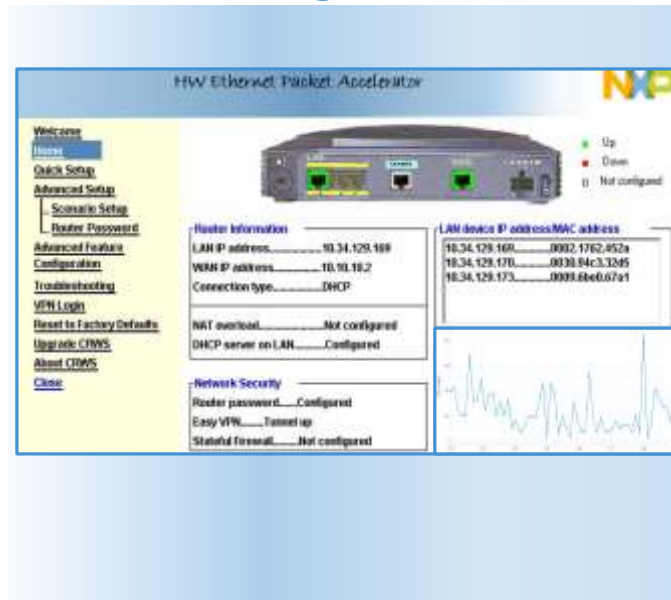
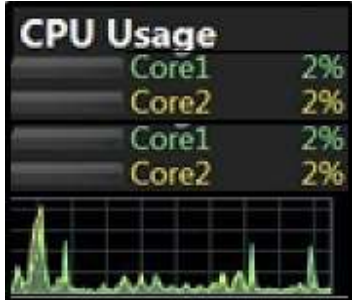


- Vehicle Health Parameters recorder - "relevant" data from Vehicle logged into a mass storage.
- Calypso receiving the CAN data from an external CAN traffic generator.
- Data transmitted via IPC to Layerscape for logging.
- Logged Data shared over cloud
- Data fetched from cloud for monitoring.

Ethernet Packet Acceleration

ASK

CPU Monitoring



Value Proposition:

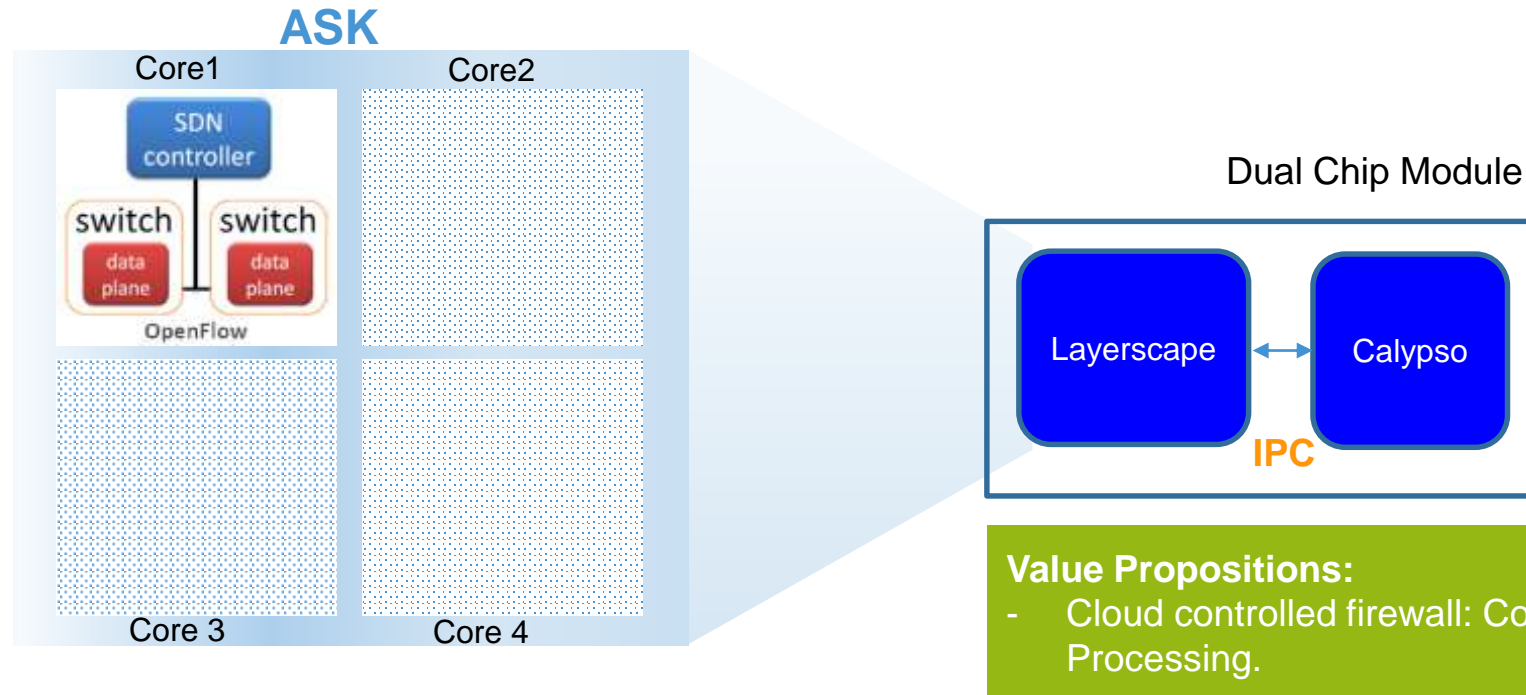
- Ethernet Packet Acceleration vs SW based competitor

Web based Application in ASK with below functionalities

- Demonstrating packet acceleration during network load
- Enabling and disabling of HW acceleration (Slow Path/Fast path with load on primary cores)
- Realtime CPU Load monitoring
- Router setup/configuration connecting two PCs

Note: App GUI shown is for illustration purpose. Actual one may differ.

Software Defined Network (SDN) in Vehicular Networks

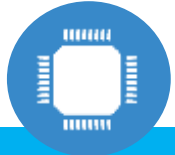


- Full functional SDN Stack showcased on one Arm Cortex-A53 core in Layerscape
- An application demonstrating OpenFlow switch with a Control Agent.
- Realtime CPU Load monitoring demonstrating three Cores near idle.

Future Solutions Brief



S32x Platform – Vehicle Network Processor – Key Values



Performance

- **Safe & Secure Single Chip, High-Performance MCU + MPU**

- + Low-latency MCU
- + High-bandwidth MPU
- + Performance extension via PCIe



Bandwidth

- **High-bandwidth Ethernet Accelerator**

- + Packet Forwarding Engine

- **Low Latency Hardware Accelerator for Automotive Interfaces**

- + System offload (interrupts + security) and time sync of CAN FD, FlexRay, LIN



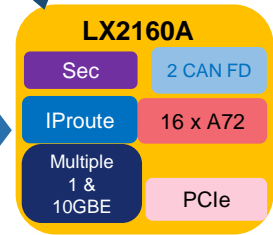
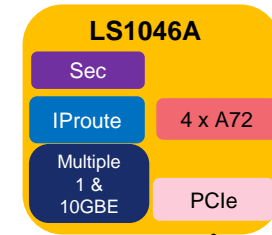
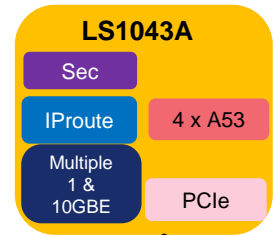
Security

- **Future Proof Security**

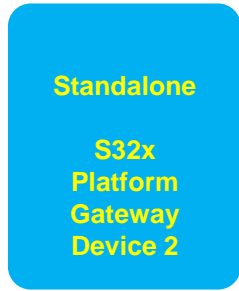
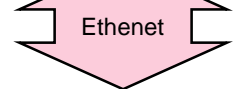
- + High-performance Hardware Security Engine (beyond SHE, HSM, EVITA)
- + Crypto (AES,ECC,SHE, RSA), updateable, life cycle, side channel protection...

Scalable Performance within the S32x Platform Gateway and beyond via PCIe Interface to a Layerscape Device

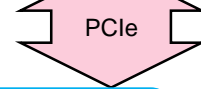
Great Single Chip performance
 Upgradable using Layerscape Family
 Scalable HW + SW



Increasing performance →



...



- **Dual Chip Solution**
 - Software compatible through API
 - Similar feature support as Next Gen

- **Scalable Single Chip Solutions**
 - Footprint and software compatible
 - Same interfaces and accelerators

- **Scalable Dual Chip Solutions**
 - PCIe attached, software compatible
 - Same interfaces and accelerators

Summary





Summary

- Next-Gen Gateways are adding new capabilities beyond a microcontroller as they become more service-oriented (applications)
 - High-level operating systems, virtualization, AUTOSAR Adaptive Platform, Gigabit Ethernet packet processing
- NXP has combined leadership in automotive gateway microcontrollers with leadership in digital networking to address these gateways
 - MPC5748G – Automotive Interfaces - Gateway Controller
 - Layerscape LS1043A – Communications/Applications Processor with Ethernet Packet Acceleration (Auto-Qualified)
- **NXP solution for Next-Gen Gateways is available today in production**
 - Supported by a module and software for rapid hardware and software development



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