Vehicle Network Processing with the MPC5748G MCU + LS1043A MPU

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FAE - Automotive Gateway

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Agenda

• Automotive Gateway Evolution
• NXP Next-Gen Gateway Solution
• Hardware Enablement
• Software Enablement
• Demo Applications
• Summary
Automotive Gateway Evolution
Next-Gen Gateway in Vehicle Network

Key Gateway Use Cases

- Protocol Translation
- Network Security
- OTA Updates Management
- Diagnostics / Prognostics
- Applications & Services
Next-Gen Gateways: More Processing and Networking

**Today’s Gateways**
- Basic Gateway
- Microcontroller
- < 1000 DMIPS performance
- 1 or 2, 100 Mbps Ethernet
- 5 – 8 CAN interfaces

**2020+ Gateways**
- Advanced Gateway with Services
- Microcontroller + Microprocessor
- 10,000+ DMIPS performance
- 3 – 5, Gigabit Ethernet
- >8 CAN / CAN FD interfaces

> 10x
Next-gen Gateway: Processing

- **1000’s of DMIPS performance** required for 2020+ gateway architectures

- **Applications and Services:** Feature deployment through software modules rather than new ECUs
  - ECU Consolidation
  - Advanced OTA updates
  - Vehicle Configuration
  - Data Logging

- **Big Data Analytics:** Leverage vehicle data through gateway - Descriptive / Diagnostics / Predictive
  - Security, safety & integrity of the vehicle & network
  - Data analytics

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<table>
<thead>
<tr>
<th>GW Feature</th>
<th>Processor Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applications and Services</td>
<td>- Application Processing (w/support for high-level OS – Linux, QNX… and hypervisors)</td>
</tr>
<tr>
<td>Big Data Analytics</td>
<td>- AUTOSAR Adaptive Platform for service-oriented gateways (services and APIs)</td>
</tr>
<tr>
<td>ECU Consolidation</td>
<td>- Compute Performance</td>
</tr>
<tr>
<td></td>
<td>- Scalability to higher performance (e.g., expansion via PCIe)</td>
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Next-gen Gateway: Networking

- Move toward an **Ethernet backbone** to connect domains to gateway
  - Bandwidth needs – Autonomous Platforms
  - Domain controller approach – simplifies logistics of deploying vehicle platform
  - **IP Routing, VLAN & >L3 firewalls** to Isolate & Protect Ethernet domains
  - Diagnostics over IP (DoIP) usage widespread

- **Hybrid Approach in 2020+**
  - Typical: 3-5 Ethernet domains + 8 or more CAN

- CAN channels increasing with majority of OEMs
  - Driven by domain isolation
  - Higher bandwidth needs move to CAN FD
  - 10 to 12 typical for 2020+

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<th>GW Feature</th>
<th>Processor Requirements</th>
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<tbody>
<tr>
<td>Ethernet Network Processing</td>
<td>- Packet Acceleration hardware</td>
</tr>
<tr>
<td></td>
<td>- Deep Packet Inspection driver need for higher processor performance</td>
</tr>
<tr>
<td></td>
<td>- Ethernet Intrusion Detection</td>
</tr>
<tr>
<td>CAN Network Processing</td>
<td>- &gt;8 CAN/CAN FD interfaces</td>
</tr>
<tr>
<td></td>
<td>- More performance for CAN Intrusion Detection</td>
</tr>
</tbody>
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**Connectivity**

- Ethernet
- Ethernet

**Infotainment**

- NA
- IVI

**Gateway**

- Body & Comfort
- Chassis & Safety
- Vehicle dynamics
- Ethernet
- CAN / FlexRay
- CAN / LIN
- Ethernet

**DC**

- Ethernet
- CAN / LIN

**IVI**

- Ethernet
- CAN / FlexRay
NXP Gateway Processor Roadmap

Leveraging NXP Digital Networking Expertise in Automotive
NXP Next-Gen Gateway Solution
Dual Chip Gateway Solution

- **Enables Next-gen CAN-Ethernet Gateways**
  - Automotive Gateway + Network Processing (Gigabit Ethernet Packet Routing) + Applications
  - MPC5748G (MCU) + LS1043A (MPU)
  - Available today

- **Feature Set**
  - CAN Signal Gateway (ASIL B)
  - 4x Arm Cortex-A53 (LS1043A) for Applications
  - Packet Forwarding Engine

- **OS Support**
  - AUTOSAR: Real-time CAN gateway
  - Linux / QNX: Ethernet routing, applications processing
MPC5748G Gateway Microcontroller

**Multicore architecture**
- 2x e200z4 + 1x z2 Power Architecture cores

**Floating Point Unit (FPU)**
- on z4 cores for additional computational algorithm support

**High performance**
- 160 MHz max e200z4 cores,
- 80 MHz e200z2 core

**Triple ported flash**
- and multiple RAM minimize access time to memory

**Part of Safe Assure**
- Functional Safety Program: Designed for ISO 26262 ASIL B systems

**Media Local Bus**
- Supports MOST for infotainment domain networking

**Robust security**
- Hardware Security Module (HSM) option supports both SHE and EVITA low/medium security specifications

**USB 2.0 (OTG and host module)**
- supports interfacing to both wireless modems and infotainment domain

**2 x Ethernet modules and Ethernet Switch**
- support 10/100 Mb/s for diagnostics, backbone and AVB applications

**Low-Power Unit (LPU)**
- provides CAN, LIN, SPI, ADC functionality in a new low power state

**Broad Communications**
- Multiple CAN, LIN, I2C, I2S for integrated BCM & Gateway applications

**System**
- FMPLL 16 MHz IRC
- RTC/API 8-40 MHz XOSC
- SW Watchdog Timers
- Periodic Interrupt Timer
- 32 kHz XOSC
- 128 kHz IRC

**Peripheral Clusters**
- 12-bit ADC
- 10-bit ADC
- 18 x LINFlex
- 9 x SAUPS
- 4 x CAN
- 3 x Analog Comparators
- 4 x SPI
- 6 x GPI
- 1 x FlexCAN with Pretended Networking
- 7 x FlexCAN with CAN FD

**System Bus Masters**
- MediaLB/SD
- FlexRay
- Ethernet: AVE
- SDHC/SDIO

**Peripheral Bridge**
- End-to-End ECC

**Crossbar**
- Memory Protection Unit

**Low Power Unit Interface**

**Flash**
- 6 MB Array
- EEPROM
- End-to-End ECC

**RAM**
- 256 KB Array
- End-to-End ECC

**System**
- Cores 3
- Flash 6 MB
- RAM 768 KB
- ETH/FR/ML/SD/USB 2/1/1/2
QorIQ Layerscape LS1043A

Auto quality
- AEC Q100 Grade 3 (105 Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Process & Package
- 28HPM, ~4-8W Thermal Max @ 105C
- 23x23mm, Unlidded FCBGA, .8mm pitch (780 pins)

Performance
- Arm Cortex-A53 x 4 @ 1.6 GHz
  - 19.5K DMIPS
  - SpecInt2k6 – 5.95, Rate -15
  - NEON SIMD in all CPUs
- 1x36b (including ECC) DDR3L/4 up to 1.6GT/s
  - 6.4GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen2 controllers
  - Multiple Ethernet MACs (up to 10G)

Functional Safety
- Target ASIL B (retroactive)
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security
- 10Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - Arm TrustZone
NXP MPC5748G + LS1043A Features

<table>
<thead>
<tr>
<th>MPC5748G+LS1043A</th>
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<tbody>
<tr>
<td>Microcontroller + Microprocessor</td>
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<tr>
<td>Six processor cores:</td>
</tr>
<tr>
<td>(2) PowerPC z4 + (1) PowerPC z2</td>
</tr>
<tr>
<td>(4) ARM Cortex-A53 @ 1.6 GHz</td>
</tr>
<tr>
<td>Up to 14,720 DMIPS processing</td>
</tr>
<tr>
<td>Ethernet Packet Acceleration</td>
</tr>
<tr>
<td>768 KB SRAM, 6MB embedded flash, DDR3L/DDR4 support</td>
</tr>
<tr>
<td>(2) 10/100 Ethernet (Calypso)</td>
</tr>
<tr>
<td>(4) Up to 10G Ethernet (Layerscape)</td>
</tr>
<tr>
<td>(8) CAN FD / (18) LIN</td>
</tr>
<tr>
<td>(1) USB 2.0, (3) USB 3.0, (3) Gen2 PCIe</td>
</tr>
<tr>
<td>HSM Security + SEC Security</td>
</tr>
<tr>
<td>ASIL B functional safety</td>
</tr>
<tr>
<td>Production: Now</td>
</tr>
</tbody>
</table>
NXP Dual Chip System Solution

- Secure Element (NCJ38A)
- Safety MCU (S32K)
- SBC (MC33909)
- SPHi-CAN Microchip
- CAN PHY TJA1046
- CAN PHY TJA1046
- FlexRay TJA1085
- LIN PHY TJA1022/24
- LIN PHY TJA1022/24
- 5-Port Ethernet Switch: SJA1105
- PMIC (34VR500)

MPC5748G Auto Gateway

- OBD TJA1046
- Ethernet PHY 100/1000 BASE-TX

LS1043A Network Processor

- 2 x 1 lanes
- PCIe Expansion
- Ethernet PHY 1000BASE-T1
- Cell Modem

- Digital IN
- Digital OUT
- QSPI NOR
- 32-bt DDR4
- eMMC

- Financial
- Automotive
- Industrial
- Infrastructure
- Security

- Production platform
- Architecture: MCU + MPU
- High-performance Apps Processor
- HW offload for Ethernet

NXP Device
Dual Chip Module Overview

- **Highlights**
  - MPC5748G (Calypso 6M) + LS1043A (Layerscape)
  - Standalone module. Can be used with customer hardware.

- **MPC5748G (Calypso 6M) + LS1043A**
  - 8x CAN FD (internal), external CAN device available for >8CHs (via SPI)
  - 2x e200z4 @ 160MHz, 1x e200z2 @ 80MHz, 6MB Embedded flash, 768KB RAM, low power modes
  - 4x Cortex-A53 @ 1.6GHz, DDR, Ethernet Routing Engine, PCIe, USB
  - Ethernet (RMII) based IPC between 2-chips (100Mbps raw)

- Modules available to support evaluation and software development now

- Module Part Number: **LFGTWSEM**
Dual Chip Module Architecture

- Module I/O remains on daughter card
- Module I/O routed to main board

- MPC5748G
  - Ethernet used for Inter-chip communication (switch required for interface protocol conversion)
  - JTAG
  - GPIO (3.3V)
  - FlexRay
  - ADC
  - CAN
  - LIN/UART
  - SPI

- SJA1105S
  - Ethernet
  - RMII
  - SGMII
  - SPI

- LS1043A
  - SDHC
  - IFC
  - Ethernet
  - DRAMC
  - JTAG
  - USB
  - SPI
  - CAN
  - I2C
  - LIN/UART

- Connectors to Main Board

- PMIC/Regs
  - GPIO (3.3V)
  - FlexRay
  - ADC
  - CAN
  - LIN/UART
  - SPI
  - SPI2CAN Chips (x4)

- Ethernet
- PCIe
- SPI

- USB2UART (debug only)
- 1Gb QSPi
- 16Gb NAND
- 2GB DDR4 DRAM
- microUSB Connector

- microSD Connector
- DDR4 DRAM
- PCIe
- SPI
- SPI2CAN
- CAN
- I2C
- LIN/UART
Dual Chip Module – Key Components
Dual Chip Module Back w/Connectors
Software Enablement
Dual Chip Module –
Getting Started Kit

• Getting Started package is provided with the DCM board
  ▪ Includes MPC5748G App integrated with LS1043A Linux SDK

• Content:
  ▪ Binaries & Scripts
    - MPC5748G Bare-metal App Binary & Flashing Script
    - LS1043A Binaries: U-Boot, RCW, Frame Manager, Secure Firmware, Linux SDK
  ▪ Documentation
    - Quick Start Guide
    - Getting Started Document
    - User Manual
    - Board Schematics

• The binaries are pre-flashed on DCM board
## Dual Chip Module - Software Kit BOM

<table>
<thead>
<tr>
<th>S.No</th>
<th>Domain</th>
<th>SW Details</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MPC5748G</td>
<td>Arccore AUTOSAR + NXP Switch Driver &amp; IPCF SW</td>
<td>Customers looking for turnkey AUTOSAR solution</td>
</tr>
<tr>
<td>2</td>
<td>MPC5748G</td>
<td>NXP Baremetal Software</td>
<td>S32DS based App with Switch Driver + MPC-LS communication</td>
</tr>
<tr>
<td>3</td>
<td>MPC5748G</td>
<td>IDE/FlashTool</td>
<td>S32DS Rel 2017.R1 + PPC Lauterbach</td>
</tr>
<tr>
<td>4</td>
<td>LS1043A</td>
<td>LS SDK-Linux-Uboot</td>
<td>Rel 17.12 (Open Source)</td>
</tr>
<tr>
<td>5</td>
<td>LS1043A</td>
<td>IDE/FlashTool</td>
<td>CW IDE Rel 11.2.3 + TAP &amp; Probe Tip</td>
</tr>
<tr>
<td>6</td>
<td>LS1043A</td>
<td>LS ASK-Linux</td>
<td>ASK Build required for Demo Applications (NXP License, not free)</td>
</tr>
<tr>
<td>7</td>
<td>MPC5748G + LS1043A</td>
<td>DCM Patches</td>
<td>DCM SW Customizations on MPC5748G &amp; LS1043A</td>
</tr>
<tr>
<td>8</td>
<td>MPC5748G + LS1043A</td>
<td>Collaterals</td>
<td></td>
</tr>
</tbody>
</table>
Diagram for reference purpose only. For more details, contact AUTOSAR vendor
DCM-LS1043A: NXP SDK - High Level Overview

- **SDK URL**
- DCM SDK SW uses LSDK17.12
- Board specific customizations to be delivered as patches.
Dual Chip Module Setup (NXP Lab)
Demo Applications
Dual Chip Module Demo Applications Software

DEMO APPS

Black box – Automotive Cloud Based Data Logger & Visualizer

Ethernet Packet Acceleration

SDN Intrusion Detection

AUTOSAR Runtime Environment (RTE)

Operating System (OS)

System Services

Memory Services

Crypto Services

Communication Services

I/O Hardware Abstraction

Onboard Device Abstraction

Memory Hardware Abstraction

Crypto Hardware Abstraction

Communication Hardware Abstraction

Calypso 6M

Microcontroller Abstraction Layer (CAL)

Microcontroller Drivers

Memory Drivers

Crypto Drivers

Communication Drivers

I/O Drivers

IPC

MCAPI

Host Interface

Queue Mgr.

UIC

PCIe

Dual Chip Module Demo Applications Software

NXP Standard Products

Partner Products

Complex Drivers

NXP

Third-Party Components

Open-source SW

SDK Components

COMPANY PUBLIC | 27
Automotive Data Logger

- Vehicle Health Parameters recorder - "relevant" data from Vehicle logged into a mass storage.
- Calypso receiving the CAN data from an external CAN traffic generator.
- Data transmitted via IPC to Layerscape for logging.
- Logged Data shared over cloud
- Data fetched from cloud for monitoring.

Value Propositions:
- Cloud connectivity (Apps Processing)
- PCIe memory
- MCU to MPU (CAN-Eth)
- Security (CAN, Eth & Cloud)
Ethernet Packet Acceleration

Web based Application in ASK with below functionalities

- Demonstrating packet acceleration during network load
- Enabling and disabling of HW acceleration (Slow Path/Fast path with load on primary cores)
- Realtime CPU Load monitoring
- Router setup/configuration connecting two PCs

Value Proposition:
- Ethernet Packet Acceleration vs SW based competitor

Note: App GUI shown is for illustration purpose. Actual one may differ.
Software Defined Network (SDN) in Vehicular Networks

• Full functional SDN Stack showcased on one Arm Cortex-A53 core in Layerscape
• An application demonstrating OpenFlow switch with a Control Agent.
• Realtime CPU Load monitoring demonstrating three Cores near idle.
Future Solutions Brief
S32x Platform – Vehicle Network Processor – Key Values

- **Safe & Secure Single Chip, High-Performance MCU + MPU**
  + Low-latency MCU
  + High-bandwidth MPU
  + Performance extension via PCIe

- **High-bandwidth Ethernet Accelerator**
  + Packet Forwarding Engine

- **Low Latency Hardware Accelerator for Automotive Interfaces**
  + System offload (interrupts + security) and time sync of CAN FD, FlexRay, LIN

- **Future Proof Security**
  + High-performance Hardware Security Engine (beyond SHE, HSM, EVITA)
  + Crypto (AES, ECC, SHE, RSA), updateable, life cycle, side channel protection…
Scalable Performance within the S32x Platform Gateway and beyond via PCIe Interface to a Layerscape Device

**Standalone S32x Platform Gateway Device 1**
- 4 x A53
- Multiple 1 & 10GBE
- PCIe
- Ethenet

**Standalone S32x Platform Gateway Device 2**
- 4 x A72
- Multiple 1 & 10GBE
- PCIe

**Standalone S32x Platform Gateway Device x**
- 16 x A72
- Multiple 1 & 10GBE
- PCIe

**LS1043A**
- Sec
- IProute
- 4 x A53
- Multiple 1 & 10GBE
- PCIe
- Ethenet

**LS1046A**
- Sec
- IProute
- 4 x A72
- Multiple 1 & 10GBE
- PCIe

**LX2160A**
- Sec
- IProute
- 16 x A72
- Multiple 1 & 10GBE
- PCIe

**Increasing performance**

- **Dual Chip Solution**
  - Software compatible through API
  - Similar feature support as Next Gen

- **Scalable Single Chip Solutions**
  - Footprint and software compatible
  - Same interfaces and accelerators

- **Scalable Dual Chip Solutions**
  - PCIe attached, software compatible
  - Same interfaces and accelerators

Great Single Chip performance
Upgradable using Layerscape Family
Scalable HW + SW
Summary
Summary

• Next-Gen Gateways are adding new capabilities beyond a microcontroller as they become more service-oriented (applications)
  - High-level operating systems, virtualization, AUTOSAR Adaptive Platform, Gigabit Ethernet packet processing

• NXP has combined leadership in automotive gateway microcontrollers with leadership in digital networking to address these gateways
  - MPC5748G – Automotive Interfaces - Gateway Controller
  - Layerscape LS1043A – Communications/Applications Processor with Ethernet Packet Acceleration
    (Auto-Qualified)

• NXP solution for Next-Gen Gateways is available today in production
  - Supported by a module and software for rapid hardware and software development