Getting Started with S32K Hands-on Workshop

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Automotive

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First, Things First...

We need all of the hardware (thumb drives, EVB's, etc.) to remain in the lab due to reuse across multiple hands-on sessions...

PUBLIC 1



Agenda

- Brief S32K Product & Roadmap Overview
- Introduction
 - Hello World (GPIO) Hands-On
 - Hello World + Clocks
 - Hello World + Interrupts Hands-On
 - DMA
 - Timed I/O (FTM)
 - ADC
 - UART Hands-On
 - SPI

- CAN 2.0
- CAN FD Hands-On
- Appendix: S32 Design Studio Blank Project Steps



Product Overview & Roadmap





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Solutions for Edge Nodes – Today and Tomorrow



Today

Distributed vehicle architectures Incompatible silicon and software Security and over-the-air update challenges Inefficient development Not easily upgraded or scaled

Tomorrow

High performance domain architectures Greater network capacity Secure, safe over-the-air updates Efficient to develop Upgradable and scalable platform, future proof



Common Chassis Scalability





General Purpose and Integrated Solutions

Target Markets

Products

Technology



S32K Value Proposition

ARM Cortex for Scalability



Future-proof Features





S32K1 / KEA Compatibility

Pin Compatibility:

- Within S32K1xx product series
- Similar pinout as **KEA** products

IP Compatibility:



• With MPC55xx/MPC56xxx/MPC57xxx product series: FlexCAN, ACMP, eDMA, QuadSPI

• With KEA products: FlexTimer, IIC, LSPI, UART, CRC, FlexIO

| Flash | Pin Count | | | | | | | | | |
|-------|-----------|---------|----------------------|--------------------|--------|----------|---------|---------|---------|--|
| | 16/24 | 32 | 48 | 64 | 80 | 100 LQFP | 100 BGA | 144 | 176 | |
| 2M | | | | | | | S32K148 | S32K148 | S32K148 | |
| 1M | | | | S32K146 | | S32K146 | S32K146 | S32K146 | | |
| 512K | | | | S32K144 | | S32K144 | S32K144 | | | |
| 256K | | | S32K142 * S32K118 | S32K142 S32K118 | | S32K142 | | | | |
| 128K | | S32K116 | S32K116 | KEAZ128 | KEA128 | | | | | |
| 64K | | KEAZN64 | | KEAZ(N)64 | KEAZ64 | | | | | |
| 32K | | KEAZN32 | | KEAZN32 | | | | | | |
| 16K | | KEAZN16 | | KEAZN16 | | | | | | |
| 8K | KEAZN8 | | | | | | | | | |

*: S32K142 48LQFP is for development only



S32K144: ASIL B 512K General Purpose MCU



Specifications:

- Cores: ARM Cortex-M4F @112 MHz max
- Memory: 512 KB Flash, 64 KB RAM (60 KB with ECC, 4 KB FlexRAM/EEPROM)
- **Temp Range:** Ta -40 to 125°C (Tj=135°C)
- Power Supplies: 2.7-5.5 V
- Packaging:10 x 10 mm, 0.5 mm pitch 64 LQFP (up to 58 usable pins). 11 x 11 mm, 1 mm pitch 100 MapBGA.(up to 89 usable pins). 14 x 14 mm, 0.5 mm pitch 100 LQFP (up to 89 usable pins)

Key Features:

- High Performance: Powerful ARM Cortex-M4F core
- Advanced Automotive Communication: CAN FD
- Functional Safety: Developed as per ISO 26262 with target ASIL B
- Security: HW security engine (SHE+ compliant)
- Low Power: Low leakage tech. Best in class STOP current: 25-40 uA (device dependent)
- Full solution offering: AUTOSAR, SDK, Design Studio IDE



2. Write or erase access to security (CSEc) or EEPROM is allowed only when device operating in RUN mode (up to 80MHz). No write or erase access to security and EEPROM allowed when device running at HSRUN mode (112MHz).



S32K Superior Performance





S32K Superior Code Density



- Higher speed leads to better cache efficency
- More space for application code



Industry Leading Low Power Performance

| | Ta (C) | VLPS (uA) | VLPR (mA) | Stop 1 (mA) | Run (mA) |
|------------|-----------|-----------|-----------|-------------|----------|
| S32K116 | 25 (typ) | 26 | 1.9 | 7 | tbd |
| S32K118 | 25 (typ) | 26 | 1.9 | 7 | tbd |
| S32K142 | 25 (typ) | 29 | 1.17 | 6.4 | 37.5 |
| 0001/4.4.4 | 25 (typ) | 29.8 | 1.48 | 7 | 39.6 |
| 532N144 | 105 (typ) | 256.3 | 1.8 | 7.8 | 40.5 |
| | 125 (max) | 1492 | 3.18 | 12.2 | 46 |
| S32K146 | 25 (typ) | 40 | 5 | 15 | tbd |
| S32K148 | 25 (typ) | 38 | 2.17 | 8.5 | 57.7 |







More Than a Standard EVB...



System Solutions – Released Already

Embedded

Firmware

NFC

Controlle

NFC

Antenn

а

S32k NCINCx3340

NFC

NCI Stack

MCU

ISELED Driver

- High-speed communication for creating dynamic lighting effects
- ISELED Driver for S32K
- Using FlexIO and SPI
- SDK and Autosar



Touch Sense library

- 1D Touch Library
- SDK and Autosar
- Single chip solution for **automotive** TS.
- Suitable for up to 10
 electrodes



NFC Stack

- Interface between MCU and NFC controller
- Specified by NFC Forum
- Eases integration of NFC controllers
- SDK and Autosar



BMS Reference Design

- Turnkey solution for Safety Applications up to ASIL-C 4 NXP Devices:
- S32K144
- KEA
- SBC
- Battery Cell Management





0. Start S32 Design Studio and Import the Labs



0

Open S32 Design Studio & Select a Workspace

1. Double click the S32 Design Studio 3.0 icon on the desktop

X

Cancel

PUBLIC

Select Workspace Directory

Select the workspace directory to use.

- 2. Create a folder on the desktop, to use as a workspace
- 3. Click "OK"

| ies Willson outer ork 711 PODS Tech Rvw demo new files |
|---|
| Willson outer ork 711 PODS Tech Rvw demo new files |
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| demo new files |
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| / |
| 2K |



Toolbar and Menubar





Import the Labs

1. File→ Import→ General→ Existing Projects into Workspace→ Next

| alast | |
|--|---|
| Create new projects from an archive file or directory. | Ľ |
| Select an import wizard: | |
| type filter text | |
| General Archive File Existing Projects into Workspace File System Preferences Projects from Folder or Archive C/C++ Git Install Processor Expert Remote Systems Run/Debug S32 Design Studio Team XML | |
| | |

2. Select Archive File \rightarrow Browse and select file

| Import Projects | | |
|---------------------------|---|--------------|
| Select a directory to sea | ch for existing Eclipse projects. | 17 |
| 6 | | - |
| C Select root directory: | | Browse |
| Select archive file: | C:\nsp\projects_S328\532D5\Cot + | Browse |
| Projects | | |
| S32K144_Project | ADC (Examples/S32K144_Project/S + | Select All |
| S32K144_Project | _Canif d (Examples/S32K144_Project, _CMP (Examples/S32K144_Project/S | Deselect All |
| S32K144_Project | Refresh | |
| S32K144_Project | EWM (Examples/S32K144_Project/1 | |
| S32K144_Project | FlexCan (Examples/S32K144_Projec | |
| (| Friendo (Exampleo 2024/244_Project) + | |
| Options | | |
| [2] Search for nexted pr | njech | |
| Copy projects into a | iorkopace | |
| Window netr | ready exist in the wondpace | |
| TT a set a set a | | |
| Add project to wor | ong sets | New |
| Waiting atto | * | Select |
| | | |
| | | |
| | | |
| (?) < Back | Net > Finish | Cancel |
| | | |





Take a Tour of S32 Design Studio







1. Hello World (GPIO)





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1. Hello World: Introduction

<u>Summary</u>: A GPIO input is continuously polled to detect a high or low level. A GPIO output is set corresponding to the level.





1. Hello World: Key Points

- Out of reset, clocks are not enabled to peripherals. (Done in PCC, Peripheral Clock Controller module)
- GPIO requires configuring
 - Input or output direction (Done in PTx, GPIO modules)
 - GPIO function (Done in PORTx, Port Control and Interrupts module)
- Hands on: Using next slides:
 - -browse a project from a bare metal code example that exists in S32 Design Studio,
 - -build, download to flash and run.



1. Hello World: Build 1 of 2

1. Select project "Hello"









1. Hello World: Debug Configuration

- The first time a project is built, a debug configuration is needed. Click Run→ Debug Configurations
- 2. Set up debug configuration: a. expand GDB PEMicro Interface,
 - b. select hello_Debug,
 - c. select Debugger tab,
 - d. verify OpenSDA selected
 - e. Verify Port is filled.
- 3. Click Debug on bottom right corner



1. Hello World: Debug Tip

If you get this error message at Debug, you likely need to fix your power configuration.

In this case, J107 Power Source Selection jumper (center of board) was configured to provide power from an external 12V source, but none was connected. Launching hello_Debug
 P&E Connection Assistant
 An error occured while connecting to the interface hardware or target specified in the Launch Configuration Dialog. For this launch, you may retry/re-specify the connection with the following parameters:
 OpenSDA - USB Port
 OpenSDA on USB1 (Name=5E271E57) (Autodetecter Refresh

Solution: connect J107 pins 2-3 (default) so power is routed from USB

J107: <u>move</u> jumper to right if external 12V is not connected





1. Hello World: Run a Project

Debug perspective: click "Resume" icon to execute code

| 🖆 – 🖩 🕼 👌 🕨 🛛 🖷 🙌 🍕 🕫 🕫 🖓 👘 🖓 🖉 🖉 🍅 | 𝒜 ▼ 🕖 ♥ 𝔅 |
|--|---|
| 🎄 Debug ⊠ 🦓 🙀 📩 🤿 🛛 🖬 | 🗱 Variables 💁 Breakpoints 🔀 🏘 Expressions 🔠 Registers 🚪 Peripherals 🛋 Modules 🕮 EmbSysReg View 🖓 🗖 |
| FTM_Debug [GDB PEMicro Interface Debugging] FTM.elf Phread #1 (Suspended : Breakpoint) main() at main.c:26 0x5dc C:\Freescale\S32_ARM_v1.2\eclipse\plugins\com.pemicro.debug.gdbjtag.pne_2.5.9.201609160049\win32\pegdbserver_cons arm-none-eabi-gdb Semihosting Console | ✓ |
| ۰ ۲ | → |
| i main.c ⊠ | 🖳 🗆 📴 Outline 🛛 🕞 🎝 💘 🗞 🔹 🗮 🖙 🗸 🗖 |
| <pre> • void PORT_init (void) { PCC->PCCn[PCC_PORTD_INDEX]]=PCC_PCCn_CGC_MASK; /* Enable clock for PORTD */ PCC->PCCn[PCC_PORTE_INDEX]]=PCC_PCCn_CGC_MASK; /* Enable clock for PORTE */ PORTE->PCR[3]]=PORT_PCR_MUX(2); /* Port E8: MUX = ALT2, FTM0CH6 */ PORTD->PCR[15]]=PORT_PCR_MUX(2); /* Port D15: MUX = ALT2, FTM0CH0 */ PORTD->PCR[16]]=PORT_PCR_MUX(2); /* Port D16: MUX = ALT2, FTM0CH1 */ } • void WDOG_disable (void) { WDOG->CNT=0xD928C520; /* Unlock watchdog */ WDOG->CS = 0x0000FFFF; /* Maximum timeout value */ WDOG->CS = 0x00002100; /* Disable watchdog */ } • int main(void) { </pre> | S32K144.h clocks_and_modes.h FTM.h PORT_init(void) : void WDOG_disable(void) : void main(void) : int |
| WDOG_disable(); /* Disable WDOG*/ | |



1. Hello World: Hands-On: Debug Basics

• Step



Step Over



Step Return



Resume ["go", "run"]



Suspend ["stop", "halt"]



Terminate [exit debugger]
 tor Navigate Search Project
 Image: Image:

Debug Basics: View & Alter Variables

- View in "Variables" tab in upper right of debug perspective.
- Click on a value to allow typing in a different value.

| (×)= Variables ⊠ | Breakpoints | 🔤 Registers 🛋 Modules | <u>*.</u> |
|------------------|-------------|-----------------------|-----------|
| Name | | Туре | Value |
| (x)= counter | | int | 8 |
| | | | <i>₽</i> |
| | | | |
| | | | |

Debug Basics: View & Alter Registers

- View CPU registers in the "Registers" tab
- Click on a value to allow typing in a different value

| (x)= Variables 💁 Breakpoints 🔤 Registers 😂 | 🛋 Modules |
|--|-----------|
| Name | Value |
| General Registers | |
| 1818 rO | 3 |
| 1000 r 1 | 5 |
| (1959 r2 | 536866944 |
| 1010 r3 | 8 |
| 1919 - 1 | 0 |

| (x)= Variables | ● _● Breakpoints | ିଙ୍କୁ Expressions | 1919 Registers | 🚡 Peripherals | 🛋 Modules | III EmbSysReg | x | | |
|----------------|----------------------------|-------------------|----------------|---------------|-----------|---------------|---|---|---|
| | | | | | | | 0 | 6 | Ę |

Project: [ADC] => Arch: cortex-m4 Vendor: Freescale Chip: S32K144

 View peripheral registers in the EmbSys Registers tab

| Register | Hex | Bin | Reset | Access | * |
|-----------------------------------|------------|---|------------|--------|---|
| ⊿ 👬 ADC0 | | | | | |
| ⊿ 🔚 SC1A | 0x0000009D | 000000000000000000000000000000000000000 | 0x000001F | RW | |
| ADCH (bits 4-0) | 0x1D | 11101 | | | |
| AIEN (bit 6) | 0x0 | 0 | | | Ξ |
| COCO (bit 7) | 0x1 | 1 | | | |
| ▷ 8889 SC1B | | | 0x000001F | RW | |
| ▷ ### SC1C | | | 0x000001F | RW | |
| ▷ 8889 SC1D | | | 0x0000001F | RW | |
| ▷ 8889 SC1E | | | 0x0000001F | RW | |
| N 1919 SC1 F | | | 0v000001 F | R/W | |





Debug Basics: View & Alter Memory

Add Memory Monitor

- Select Base Address
- to Start at : 4000000
- View Memory

| | | | executione | | anoly \sim | |
|---|--------------|---|---|---|---|--|
| Monitors | R X 3 | <u>k</u> | | | | |
| | Add Me | mory Mo | nitor | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| Monitor Memory | × | | | | | |
| Enter address or expression to a | moniton | | | | | |
| Enter address or expression to r | monitor: | | | | | |
| 40000000 | • | | | | | |
| | | | | | | |
| | | | | | | |
| ? Ок | Cancel | | | | | |
| Ок | Cancel | | | | | |
| ? ок | Cancel | | | | | |
| Console A Tasks Prob | Cancel | es 🚺 Memo | w x2 | | | |
| Console Z Tasks R Prob | Cancel | 25A00 <hex></hex> | ny ⊠ ≅ t New | Renderings) | | |
| Console Console Tasks Prob Ionitors | Cancel | es 🚺 Memo 25A00 <hex> 0 - 3</hex> | ny ⊠ ⊠ <mark>∳ New</mark> 4 - 7 | Renderings) 8 - B | C - F | |
| Console Tasks Prob Ionitors + X | Cancel | es 🚺 Memo 25A00 <hex> 0 - 3 00000000</hex> | ny ⊠ ≅ <mark>∳</mark> New 4 - 7 00000000 | Renderings 8 - B 00000000 | C - F 00000000 | |
| Console Tasks Prob Ionitors Prob | Cancel | es 🚺 Memo 25A00 <hex> 0 - 3 00000000 00000000</hex> | ny ⊠ ≅ <mark>∳</mark> New 4 - 7 00000000 00000000 | Renderings 8 - B 00000000 00000000 | C - F 00000000 00000000 | |
| Console Tasks Prob Ionitors Prob | Cancel | es Memo 25A00 <hex> 0 - 3 00000000 00000000 00000000</hex> | y ⊠ | Renderings 8 - B 00000000 00000000 00000000 | C - F 00000000 00000000 00000000 | |
| Console Tasks Prob Aonitors + X | Cancel | es Memo 25A00 <hex> 0 - 3 00000000 00000000 00000000 00000000 0000</hex> | y ⊠ | Renderings 8 - B 00000000 00000000 00000000 00000000 | C - F 00000000 00000000 00000000 00000000 | |
| Console Tasks Prob Aonitors + X | Cancel | es Memo 25A00 <hex> 0 - 3 00000000 00000000 00000000 00000000 0000</hex> | y ⊠ | Renderings 8 - B 00000000 00000000 00000000 00000000 0000 | C - F 00000000 00000000 00000000 00000000 0000 | |
| OK Console Tasks Prob Monitors + X 4000000 | Cancel | es Memo 25A00 <hex> 0 - 3 00000000 00000000 00000000 00000000 0000</hex> | y ⊠ | Renderings 8 - B 00000000 00000000 00000000 00000000 0000 | C - F 00000000 00000000 00000000 00000000 0000 | |



Debug Basics: Breakpoints

Add Breakpoint: Point and Click

Light blue dot represents debugger breakpoint





Debug Basics: Reset & Terminate Debug Session

Reset program counter



Terminate Ctl+F2





Always terminate a debug session when finished.







3. Hello World + Interrupts: Introduction

Summary An interrupt is implemented to service the LPIT counter match function.





3. Hello World + Interrupts: Startup Code



- Reset source handling

- startup_S32K144.S
 - interrupt table
 - flash configuration field
 - reset handler
 - CPU initialization
 - jump to main()
- startup.c
 - RAM initialization
 - DATA table copying



3. Hello World + Interrupts: Vector # vs Interrupt

| Address | Contents in Big Endian memory view | Contents as Little Endian format addresses ¹ | Vector # | IRQ # (NVIC interrupt source) | Symbol in file startup_S32K144.S, section .isr_vector, isr_vector | Description |
|-------------|--|---|-------------|---|--|--|
| 0x0000 0000 | 0070 0020 | 2000 7000 | 0 | | StackTop | Initial stack pointer |
| 0x0000 0004 | 1104 0000 | 0000 4010 | 1 | | Reset_Handler | Initial Program Counter |
| 0x0000 0008 | 4004 0000 | 0000 044C | 2 | | NMI Handler | Non-maskable IRQ (NMI) Vector |
| 0x0000 003C | 4D04 0000 | 0000 044C | 15 | | SysTick_Handler | Sys tick timer (Sys Tick) Vector |
| 0x0000 0040 | 4D04 0000 | 0000 044C | 16 | 0 | DMA0_IRQHandler | Interrupt # 0 Vector: DMA Channel 0 transfer complete |
| 0x0000 0044 | 4D04 0000 | 0000 044C | 17 | 1 | DMA1_IRQHandler | Interrupt # 1 Vector DMA Channel |
| l | | 1 | | ••• | 1 | |
| 0X0000 0100 | 5906 0000 | 0000 0658 | 64 | 48 | LPIT0_Ch0_IRQHandler | Interrupt #48 Vector: LPIT0 Ch. 0 |



Quick look at S32K Reference Manual (Interrupt tables, memory map, etc.)





3. Hello World + Interrupts: Interrupt Handlers

Location of vector table in S32 Design Studio project: startup_S32K144.s



LPIT0 channel 0 interrupt handler definition



3. Hello World + Interrupts: "weak" Handlers

Startup_S32K144.S



| def | irq_handler | |
|-----|-------------|--|
| def | irq_handler | |
| def | irq_handler | |
| def | irg_handler | |
| def | irq_handler | |
| def | irq_handler | |
| | | |

RTC_Seconds_IRQHandler LPIT0_Ch0_IRQHandler LPIT0_Ch1_IRQHandler LPIT0_Ch2_IRQHandler LPIT0_Ch3_IRQHandler PDB0_IRQHandler Main.c

Source of the second sec

Overrides the "weak" default handler



3. Hello World + Interrupts: Interrupt initialization

The Nested Vector Interrupt Controller (NVIC) is used to initialize an interrupt:

- <u>Clear any prior pending</u> interrupt (in case there was one)
 - Write a 1 to the interrupt # bit in Interrupt Clear Pending Register (ICPR)
- Enable the desired interrupt
 - Write a 1 to the interrupt # bit in the Interrupt Set Enable Register (ISER)
- <u>Set the interrupt's priority</u>
 - Write a priority from 0 to 15 to the appropriate Interrupt Priority register (IP)

```
Example for IRQ # 48:
```

```
      S32_NVIC->ICPR[1] = 1 << (48 % 32);</td>
      /* IRQ48-LPIT0 ch0: clear any pending IRQ*/

      S32_NVIC->ISER[1] = 1 << (48 % 32);</td>
      /* IRQ48-LPIT0 ch0: enable IRQ */

      S32_NVIC->IP[48] = 0xA0;
      /* IRQ48-LPIT0 ch0: priority 10 of 0-15*/
```



3. Hello World + Interrupts

1. Be sure C/C++ perspective is selected, otherwise click on it to get it selected.

- 2. Double click on HelloInterrupts project
- 3. Click on Build icon
- 4. Click on Debug icon
 - Create debug connection... Go...





3. Hello World + Interrupts: View, Modify Registers

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- 1. Use Resume to run, Suspend to halt
- 2. Disable LPIT channel 0:
 - 1. Click EmbSys Registers tab
 - 2. Scroll down list about half way and expand LPIT & LPIT0
 - 3. Expand register TCTRL0
 - 4. Click on hex value (0x1) to change to 0x0, disabling counter
- 3. Use Resume to run again. Note LED stopped blinking



4. Click Terminate.

| • • • | | | | | | Quick Access | 🗐 🗟 C/C++ 🚺 Debug |
|---|--------------|---------|----------------|---------|------------|----------------------------------|---|
| 👓 Variables 🐁 Breakpoints 😤 Perij | pheral 🔤 Er | nbSys P | Registers 💷 | | | | 800 |
| Project: [hello_interrupts] => Arch: cort | tex-m4 Vendo | r: Free | scale Chip: 53 | 2K144 8 | ioard: nor | e (Double) | click on register to read values) |
| Register | Hex | Bin | Reset | Acce | Address | Description | |
| A Con LPIT | | | | | | Low Power Period | ic Interrupt Timer (LPIT) |
| · 計計 LPTTO | | | | | | Low Power Period | ic Interrupt Timer (LPIT) |
| # ## VERID | | | 0x01000000 | RO | 0%40037000 | Version ID Registe | A. Carlos and a second s |
| IIII PARAM | | | 0x00000404 | RO | 0x40037004 | Parameter Registe | 5 |
| D IIII MCR. | | | 0x00000000 | RW | 0x40037008 | Module Control Register | |
| IIII MSR | | | 0x00000000 | RW | 0x4003700C | Module Status Register | |
| IIII MER | | | 0x00000000 | RW | 0x40037010 | Module Interrupt Enable Register | |
| ### SETTEN | | | 0x00000000 | RW | 0x40037014 | Set Timer Enable Register | |
| > WI CLRTEN | | | 0x00000000 | RW | 0x40037018 | Clear Timer Enable Register | |
| I IN TVALO | 0x02625A00 | 000 | 0x00000000 | RW | 0x40037020 | Timer Value Regis | ter |
| 1 H H CV | 0x00EA70FA | 000 | OxFFFFFFFFF | RO | 0x40037024 | Current Timer Vali | ie . |
| - uff 15760 4 | 0x0000001 | 000 | 0x00000000 | RW | 0x40037028 | Timer Control Reg | jister |
| T_EN (bit 0) | 0x1 | 1. | | | | 1: Timer Chann | el is enabled |
| CHAIN (bit 1) | 0x0 | 0.4% | | | | O: Channel Chai | ning is disabled. Channel Time. |
| MODE (bits 3-2) | 0x0 | 00 | | | | O: 32-bit Period | ic Counter |
| TSOT (bit 16) | 0x0 | 0 | | | | O: Timer starts ! | to decrement immediately bas. |
| TSOI (bit 17) | 0x0 | 0 | | | | 🕸 0: Timer does r | ot stop after timeout |
| TROT (bit 18) | 0x0 | 0 | | | | O: Timer will no | t reload on selected trigger |
| TRG_SRC (bit 23) | 0x0 | 0 | | | | O: Trigger sour | ce selected in external |
| TRG_SEL (bits 27-24) | 0x0 | 0000 | | | | Olixe: Timer cha | nnel 0 - 3 trigger source is sel. |
| IIII TVAL1 | | | 0x00000000 | RW | 0x40037030 | Timer Value Regis | te/ |
| UII CVAL1 | | | 0xFFFFFFFF | RO | 0x40037034 | Current Timer Vali | Je |
| IIII TCTFL1 | | | 0x00000000 | RW | 0x40037038 | Timer Control Reg | pster |

How to Break an ARM

- Uninitialized clock sources will result in a CPU Hard Fault
- ARM Cortex-M generally allows each peripheral to enable/disable the clock to its register file

- Power-saving feature!

- Exercise: Hard Fault handler
 - Remove the line of code that enables port clock
 - Observe results
 - -Use debugger to find the offending line of code
 - Register View



How to Break an ARM

Set compiler optimization (-O2); Clean; Build; Debug



After

void LPIT0_Ch0_IRQHandler (void)
{
 /* Perform read-after-write to ensure flag clears before ISR exit */
 lpit0_ch0_flag_counter++; /* Increment LPIT0 timeout counter */
 PTD->PTOR |= 1<<0; /* Toggle output on port D0 (blue LED) */
LPIT0->MSR |= LPIT_MSR_TIF0_MASK; /* Clear LPIT0 timer flag 0 */
}



Guidelines for ISR's

- Clear the peripheral interrupt flag first
- Perform memory R/M/W afterward
- Use __attribute__((optimize("O0"))) to override gcc compiler flags

```
void __attribute__((optimize("00"))) LPIT0_Ch0_IRQHandler (void)
{
   LPIT0->MSR |= LPIT_MSR_TIF0_MASK; /* Clear LPIT0 timer flag 0 */
   PTD->PTOR |= 1<<0; /* Toggle output on port D0 (blue LED) */
   lpit0_ch0_flag_counter++; /* Increment LPIT0 timeout counter */
}</pre>
```







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9. Classic CAN & CAN-FD

9. CAN 2.0: Introduction

Summary

- FlexCAN module is initialized for 500K bps based on an 8 MHz crystal
- Two boards can be used to communicate using an CAN cable (CAN HI, CAN LO, ground)
- Software builds are to be configured for:
 - Node A or B
 - SBC MC33903 or UJS1169





10. CAN FD: Introduction

Summary

- FlexCAN module is initialized for 500K bps/ 2 MHz based on an 8 MHz crystal
- Two boards can be used to communicate using an CAN cable (CAN HI, CAN LO, ground)
- Software builds are to be configured for:
 - Node A or B
 - SBC MC33903 or UJS1169





10. CAN FD Frame Overview

- CAN FD stands for CAN with Flexible Data-Rate
- CAN FD was a proposal by Bosch to:
 - Increase the baud rate of the data portion of a CAN message
 - Increase the number of data bytes that can be sent in a single CAN message to up to 64 bytes
 - No changes to arbitration field allow for existing physical layers to be used



10. CAN FD: Key Points

- Key design parts described:
 - -CAN 2.0 vs CAN FD (ISO) initialization comparison.
 - CAN FD timing calculations for arbitration and data phases
 - New message buffer structure for larger data frames
 - Transceiver Delay Compensation (TDC) for faster baud rates
- Modify FlexCAN.h file for Node A/B and two SBCs:

| SBC (data phase) | Node A | Node B |
|-------------------------|------------------------|------------------------|
| MC33903 | #define NODE_A | // #define NODE_A |
| (max. 1 MHz) | #define SBC_MC33903 | #define SBC_MC33903 |
| UJA1169 | #define NODE_A | // #define NODE_A |
| (max. 2 MHz) | // #define SBC_MC33903 | // #define SBC_MC33903 |



10. CAN FD: Board Connections, Defines

- Move power supply selection jumper to use external 12V (away from CAN connector; see red arrows for jumper)
- Connect CAN, power cables as shown
- USB cable can still be connected for downloads, debug.

- Program Node A and Node B.
- High level summary:
 - Node B (Power up this EVB first)
 - Loop: For every received message from Node A, one is transmitted back.
 - Node A
 - Transmits initial message to Node B
 - Loop: For every received message from Node B, one is transmitted back.





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