QorIQ T1040 and T2081 Communication Processors Compatible Design Guidelines

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Agenda

- Hardware Compatibility
- Software Compatibility
- Pinout comparision
- Session Review and Wrap-Up

Use a common board

With the introduction of the T1040 and T2081, customers can now create common boards for both devices.

- T1040 and T2081 are pin compatible
- One common board design would reduce design time and save cost
- Make migration much faster and easier

Hardware Compatibility

- Hardware Compatibility
- Commonality and difference
- Overcome the difference

Device Comparison – T1040 and T2081

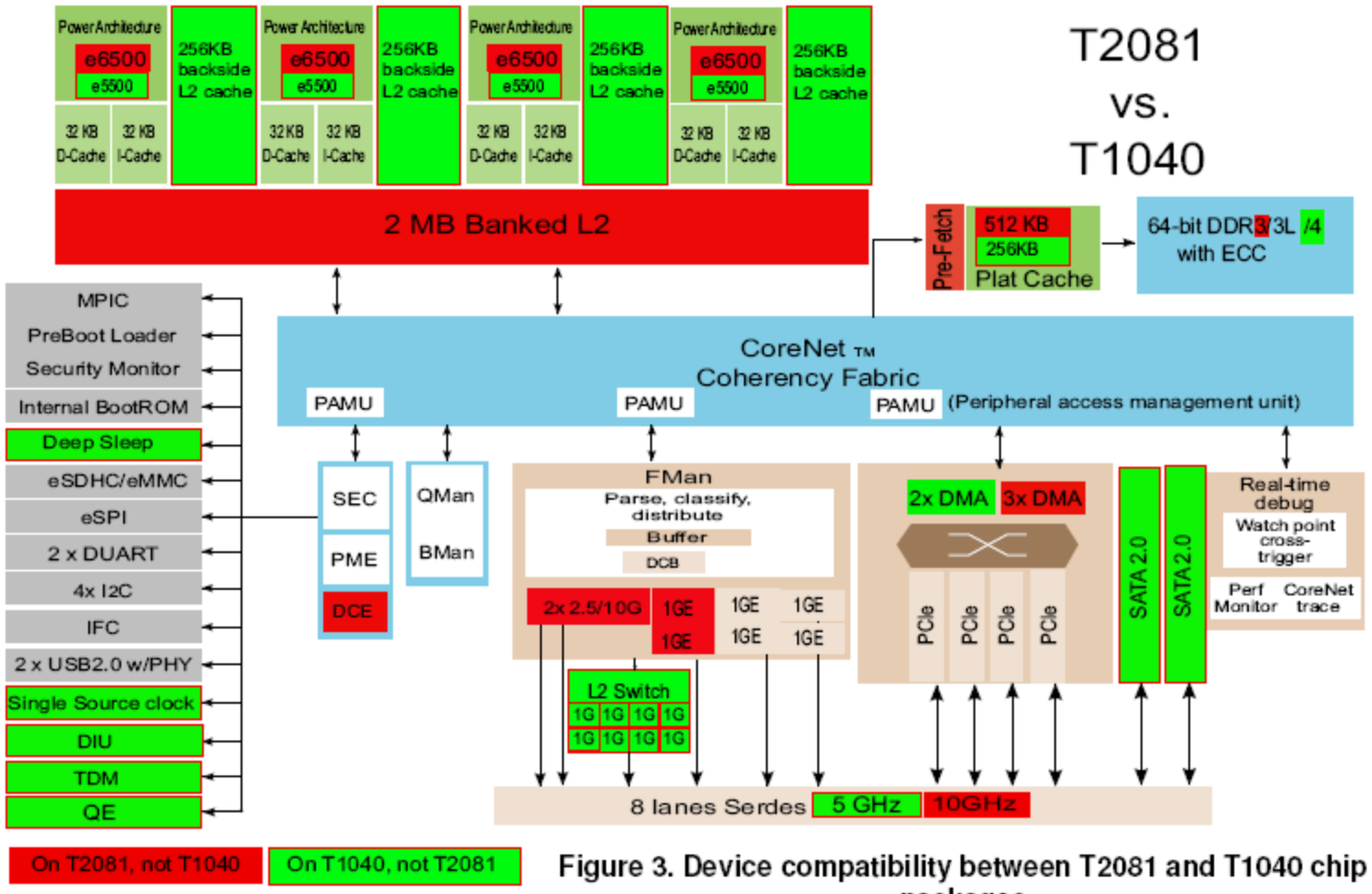


Figure 3. Device compatibility between T2081 and T1040 chip packages

Commonality and Difference

Features	T2081	T1040	T1042
Cores			
Number of cores	4 × e6500 dual threaded Power Architecture	4 × e5500 Power Architecture	4 x e5500 Power Architecture
Architecture width	64-bit	64-bit	64-bit
Max frequency (MHz)	1800	1400	1400
DMIPS/MHz	6	3	3
Memory Size			
L1 cache	32 KB I/D	32 KB I/D	32 KB I/D
L2 cache	Shared 2MB	256KB per core backside	256KB per core backside
CoreNet platform cache (CPC)	512KB frontside	256KB frontside	256KB frontside
Cache-line size	64 bytes	64 bytes	64 bytes
Main memory type	1 × DDR3/3L 2133 MT/s	1 × DDR3L/4 1600 MT/s	1 DDR3L/4 1600 MT/s
Maximum size of main memory	32 GB (1Gbit x8 device)	32 GB (1Gbit x8 device)	32 GB (1Gbit x8 device)

Commonality and Difference (continue)

I/O			
Ethernet controllers	2× 10Gbps XFI; 6x 1Gbps SGMII; 2x 2.5Gbps SGMII; 2x RGMII	2× 5Gbps QSGMII; 6x 1Gbps SGMII; 2x RGMII; 1x MII	5x 1Gbps SGMII; 2x 2.5Gbps SGMII; 2x RGMII; 1x MII
SerDes lanes	8 lanes at up to 10 GHz	8 lanes at up to 5 GHz	8 lanes at up to 5 GHz
PCI Express controllers	3 × Gen 2.0 controllers; 5 Gbps and 1× Gen 3.0 controllers; 8 Gbps	4 × Gen 2.0 controllers; 5 Gbps	4 × Gen 2.0 controllers; 5 Gbps
SATA	None	2 x SATA controllers upto 3.0Gbps operation	2 x SATA controllers upto 3.0Gbps operation
TDM	None	Full duplex serial port	Full duplex serial port
Display Interface Unit	None	12 bit dual data rate	12 bit dual data rate
CoreNet	700 MHz at 256 bits	600 MHz at 128 bits	600 MHz at 128 bits
L2 switch	None	8 Port	None
QE	None	HDLC, Transparent UART, TDM/SI	HDLC, Transparent UART, TDM/SI
Integrated Flash Controller (IFC)	8-/16-bit data width, 32-bit address width	8-/16-bit data width, 32-bit address width	8-/16-bit data width, 32-bit address width

Hardware Compatibility

- Identical Interfaces
- DDR Controller
- eSDHC Controller
- TEST_SEL Pin
- Sense Pin
- Power Sequencing
- Power Supply
- Sysclk

Identical interfaces

The following interfaces are identical between the T2081 and T1040:

- Integrated Flash Controller (IFC)
- Enhanced SPI controller (eSPI)
- DUART controller
- USB controller

DDR Controller

The T2081 supports DDR3/3L DDR controller, T1040 supports DDR3L/4 DDR controller. As DDR3L is common to both T2081 and T1040, it should be used for common board design.

Table 4. DDR calibration resistor values

	MDIC[0]	MDIC[1]
T1040	162 ohm 1%	162 ohm 1%
T2081	187 ohm 1%	187 ohm 1%

eSDC Controller

3.3 eSDHC controller recommendations

Both T2081 and T1040 support SD 3.0 specification introducing higher capacity upto 2 TB and frequency up to 208 MHz.

In order to support these modes, dynamic switching of I/O voltage from 3.3 V to 1.8 V is required. This dynamic switching is not supported on T2081 and board level shifters are required for common board design.

Figures below shows the SD card connections for T2081 compatibility for different modes.

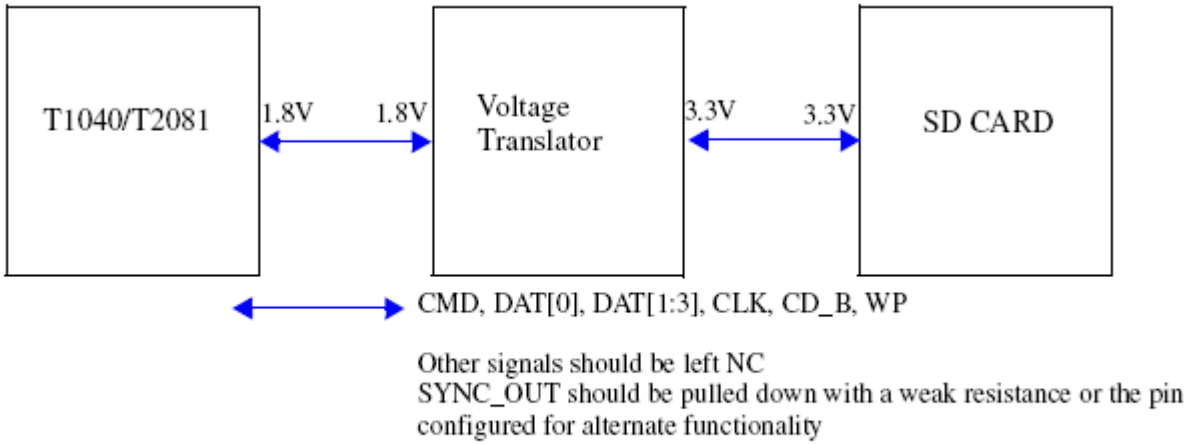


Figure 4. SD card connections for T2081 compatability (DS and HS modes)

SD Card Connection example

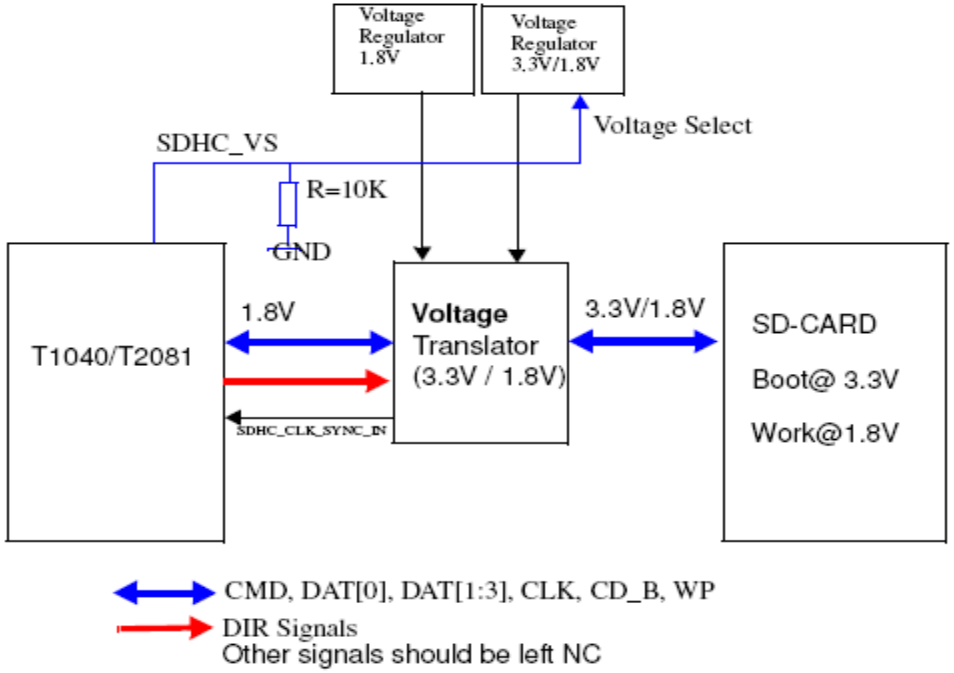


Figure 5. SD card connections for T2081 compatability (SDR 12, 25, 50, 104 and DDR50 modes)

NOTE

In Figure 5,

- SYNC_OUT should be pulled-down with a weak resistor or the pin should be configured for alternate functionality
- SYNC_IN connection is needed in DDR50 mode only
- In SDR50, DDR50 modes, all the input signals are sampled with respect to SYNC_IN
- Resistor R is only needed when RCW loading is required to be done from SD card

TEST_SEL_B pin

3.11 TEST_SEL_B requirements

When migrating between the T1020 and T1040, the connection of TEST_SEL_B needs to be considered. This table lists the different TEST_SEL_B connection requirements for each chip.

Table 13. TEST_SEL_B pin connection requirements

Device	TEST_SEL_B pin requirement
T1040, T1042	Pull to $O1V_{DD}$
T1020, T1022	Pull to GND
T2081	Pull to OV_{DD}

Sense Pins

3.9.4 SENSE Pins requirements

If sense pins are to be used for the regulators, $SENSEV_{DD}$ should be used. $SENSEV_{DDC}$ can be left floating.

Table 12. Regulator sense-pin source

Ball	T2081	T1040
G19	$SENSEV_{DD}$	$SENSEV_{DD}$
AB9	RSVD28	$SENSEV_{DDC}$

Power Sequencing

3.10 Power Sequencing requirements

T1040 requires its power rails to rampup in a specific sequence, whereas T2081 has no such requirement. Common board should follow T1040 hardware specification for the Power sequencing requirements.

Power Supply for Core

3.9.1 Core Power island requirements

T1040 has V_{DD} and V_{DDC} power domains for Core and platform supply whereas there is only V_{DD} power domain for core and platform supply in T2081. For a common board design, it is recommended to use a single rail for V_{DD} and V_{DDC} in T1040.

Table 10. V_{DD} configuration

T2081	T1040	Recommnedation
V_{DD}, USB_SV_{DD}	V_{DD}, V_{DDC}, USB_SV_{DD}	V_{DD} and V_{DDC} should be connected to a common rail.

Power Supply for I/O

3.9.3 I/O Power island requirements

The table below summarizes the Power island requirements for T2081 and T1040 and provides recommendations for common board design.

Table 11. I/O Power island configuration

Supply	T2081	T1040	Recommendation for a common board design	Interface wise recommendation	Interfaces
$O1V_{DD}$	—	1.8V	Use Single regulator for OV_{DD} and $O1V_{DD}$ on T1040 at 1.8V	eSDHC interface of T2081 is on OV_{DD} supply while IO power supply of eSDHC in T1040 is fed by EV_{DD}. If eSDHC is used, EV_{DD} and OV_{DD} should be connected to 1.8V. On board level shifters are required to support SD 3.0 modes.	Common: MPIC, GPIO, System Control, Debug, Clocks, JTAG I/O, IFC, RTC and power management I/O's, T2081 only: eSDHC
OV_{DD}	1.8V	1.8V			

I/O Power Supply (continue)

Supply	T2081	T1040	Recommendation for a common board design	Interface wise recommendation	Interfaces
DV_{DD}	2.5V 1.8V	3.3V 2.5V 1.8V	Use 2.5V or 1.8V only for DV_{DD} supply	DIU and TDM are supported at 3.3V so voltage translators may be required on a common board. QE interface is supported at 2.5V and 3.3V, restricting DV_{DD} to 2.5V for common board.	Common: DUART, I2C, DMA, MPIC T1040 only: QE, TDM, DIU
CV_{DD}	2.5V 1.8V	3.3V 1.8V	Use 1.8V for CV_{DD} supply	—	Common: eSPI, SDHC_DAT[4:7]
EV_{DD}	—	3.3V 1.8V	Use OV_{DD} supply for EV_{DD}	SDHC_DAT[0:3], SDHC_CMD and SDHC_CLK are the signals on EV_{DD} supply in T1040. These signals are on OV_{DD} supply in T2081. See OV_{DD} supply for details.	Common: eSDHC See Note
$G1V_{DD}$	1.5V 1.35V	1.35V 1.2V	Use $G1V_{DD}$ at 1.35V	Use DDR3L only	Common:DDR3L T1040: DDR4 T2081: DDR3
$L1V_{DD}$	—	3.3V 2.5V 1.8V	Use Single regulator for LV_{DD} and $L1V_{DD}$ on T1040 It can support 2.5V or 1.8V	Use RGMII interface at 2.5V only.	Common:GPIO, RGMII@2.5V T1040: MII, RGMII@1.8V
LV_{DD}	2.5V 1.8V	3.3V 2.5V 1.8V			

Sysclk

4 Internal clocking differences

T1040 supports additional clocking schemes and differences are summarised in the table below.

Table 14. T2081/T1040 clocking comparison

Clocking scheme	T2081	T1040	Recommendation
Single Reference clock mode	No	Yes	T1040: Supported through DIFF_SYSCLK/DIFF_SYSCLK_B clock input pair
Multiple reference clock mode	**Yes**	Yes	Through separate oscillators for SYSCLK, DDRCLK, USBCLK, SDREF_CLKn inputs. Recommended mode for common board design.

NOTE

For a common board design, use SYSCLK as the system clock input and leave the differential pair as floating or connect through 10K resistor to GND

Exceptions

2.2 Pin-compatibility considerations

Exceptions and recommendations in regards to pin compatibility between the T2081 and T1040 processor family are as follows:

- T1040 supports MII interfaces on EC1 which is not supported by T2081. Only RGMII interfaces should be used for EC1 and EC2.
- T2081 supports XFI interface, while T1040 does not.
- T1040 supports an 8 port L2 switch, while T2081 does not.
- T1040 supports up to two QSGMII interfaces, while T2081 does not.
- T1040 has four PCI Express controllers supporting PCI Express 2.0 protocol while the T2081 has three PCI express controllers supporting PCI Express 2.0 protocol and one PCI Express controllers supporting PCI Express 3.0 protocol at 8 Gbps.
- T1040 supports two SATA 2.0 interfaces, while T2081 does not.
- T1040 supports TDM or HDLC over uQE interface. uQE is not supported on T2081.
- T1040 supports 12 bit DIU interface, while T2081 does not.
- T1040 supports Deep sleep, a low power state, this state is not supported by T2081.
- TEST_SEL pin connection requirements vary per device family derivative; see Section 3.11, "TEST_SEL_B requirements."

Software Compatibility

- e6500 and e5500mc
- RGMII
- Serdes configurations
- RCW

e6500 and e500mc Compatibility

- User code runs equally well on e6500 or e500mc
  - Interrupts per thread
  - Soft reset per thread (hard reset per core only)
  - Debug state per thread
- Changes are hidden by OS
  - L2 initialization uses a different register
  - Cache locking controlled differently
- P4080 SDK, emulated for e6500, didn’t require changes.
- Additional enablement for new features not present on e500mc: 64b, drowsy power manager, Altivec.

e500mc/e6500 Caching Structure Differences

	e500mc	e6500	Implication
L1	32kB. Can lock per core	32kB. Can lock per core.	e6500 doesn't lock per thread.
L2	128kB per core	2MB shared	There will be a somewhat different latency profile, overall improved for e6500
L3	512MB for SC4080	512kB	

- Cache changes are transparent to user application.
- L1 locking is less granular in e6500.

RGMII

3.8 Ethernet MACs options

While the two RGMII interfaces are pin compatible, the configurations for RGMII mode are different between the T2081 and T1040 devices. This table lists the RGMII configuration options and the assigned FMan/MACx on both T2081 and T1040.

Table 8. Configuration for RGMII mode

Configuration	RGMII assignment		
	T2081	T1040	
RCW[EC1] = 0b00	FMan MAC3	FMan MAC4	MAC2_GMII_SEL = 0b0
		FMan MAC2	MAC2_GMII_SEL = 0b1
RCW[EC2] = 0b00	FMan MAC4	FMan MAC5	—
RCW[EC2] = 0b01	FMan MAC10	—	

Additonally T1040 also supports MII interface on EC1 Interface. When using MII interface, $L1V_{DD}$ and LV_{DD} are restricted to 3.3V and RGMII cannot be supported on EC1 or EC2.

Serdes configurations

T1040 SRDS_PRCTL_S1	A	B	C	D	E	F	G	H	T2081 SRDS_PRTCL_S1
0x00 (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2/5)				PEX2 (5/2.5)				0xAA (2 RGMII; FMAN MAC3 & MAC4/10)
	PEX3 (5/2.5)				PEX4 (8/5/2.5)				
0x40 (2 RGMII; FMAN MAC4 & MAC5)	PEX1 (5/2.5)		sg.m1 (1.25)	sg.m2 (1.25)	PEX2 (5/2.5)				0xBC (2 RGMII; FMAN MAC3 & MAC4/10)
	PEX3 (5/2.5)		SG1 (1.25)	SG2 (1.25)	PEX4 (8/5/2.5)				
0xA5 (0 RGMII)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (3.125)	sg.m2 (3.125)	PEX2 (5/2.5)		sg.m4 (1.25)	sg.m5 (1.25)	0xC8 (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (3.125)	SG2 (3.125)	PEX4 (5/2.5)		SG5 1.25)	SG6 (1.25)	
0xAA (0 RGMII)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (3.125)	sg.m2 (3.125)	PEX2 (5/2.5)	PEX3 (5/2.5)	sg.m4 (1.25)	sg.m5 (1.25)	0xFA (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (3.125)	SG2 (3.125)	PEX4 (5/2.5)	PEX1 (5/2.5)	SG5 (1.25)	SG6 (1.25)	
0x85 (0 RGMII)	PEX1 (5/2.5)	sg.m3 (1.25)	sg.m1 (1.25)	sg.m2 (1.25)	PEX2 (5/2.5)		sg.m4 (1.25)	sg.m5 (1.25)	0xD6 (2 RGMII; FMAN MAC3 & MAC4)
	PEX3 (5/2.5)	SG10 (1.25)	SG1 (1.25)	SG2 (1.25)	PEX4 (8/5/2.5)		SG5 (1.25)	SG6 (1.25)	

Reset Configuration Word

RCW are mostly compatible, detail listed in T1040 and T2080 reference manual.

Table 10. Reset Configuration Word Comparison (continued)

RCW Bit(s)	P4 Function	P5 Function	Notes
8–9	MEM_PLL_CFG		—
10–14	MEM_PLL_RAT		Cutoff frequencies for the P4 and P5 differ. 19:1 async mode setting is available for P5.
15–63	Reserved		
64–65	CC1_PLL_CFG		0b01 is not a valid setting for P5
66–70	CC1_PLL_RAT		Synchronous mode ratios are available for P5. 17:1 async mode setting is available for P5.
71	Reserved		
72–73	CC2_PLL_CFG		0b01 is not a valid setting for P5
74–78	CC2_PLL_RAT		Synchronous mode ratios are available for P5. 17:1 async mode setting is available for P5.

Pinout Comparison

Pin	T2081	T1040	Compatible connection
Ethernet MI 2 pins			
L6	**EMI2_MDC**	RSVD10	All the Ethernet PHY's to be used with T1040 should be managed through the EMI1 interface.
M6	**EMI2_MDIO**	RSVD11	
Ethernet Cont. 1 pins			
AC4	RSVD34	**EC1_TX_ER**	EC1 Interface on T1040 also supports MII interface (**see Section 3.8, "Ethernet MACs options"**)This output pin can be left floating if not used.
AC2	RSVD33	**EC1_RX_ER**	Tie low through a 2-10 kohm resistor if not used.
AC1	RSVD32	**EC1_COL**	
Differential SYSCLK pins (see Section 4, "Internal clocking differences")			
G14	RSVD07	**DIFF_SYSCLK**	Differential SYSCLK input is available only in T1040. These can be left floating or connected to GND if unused.
F14	RSVD05	**DIFF_SYSCLK_B**	

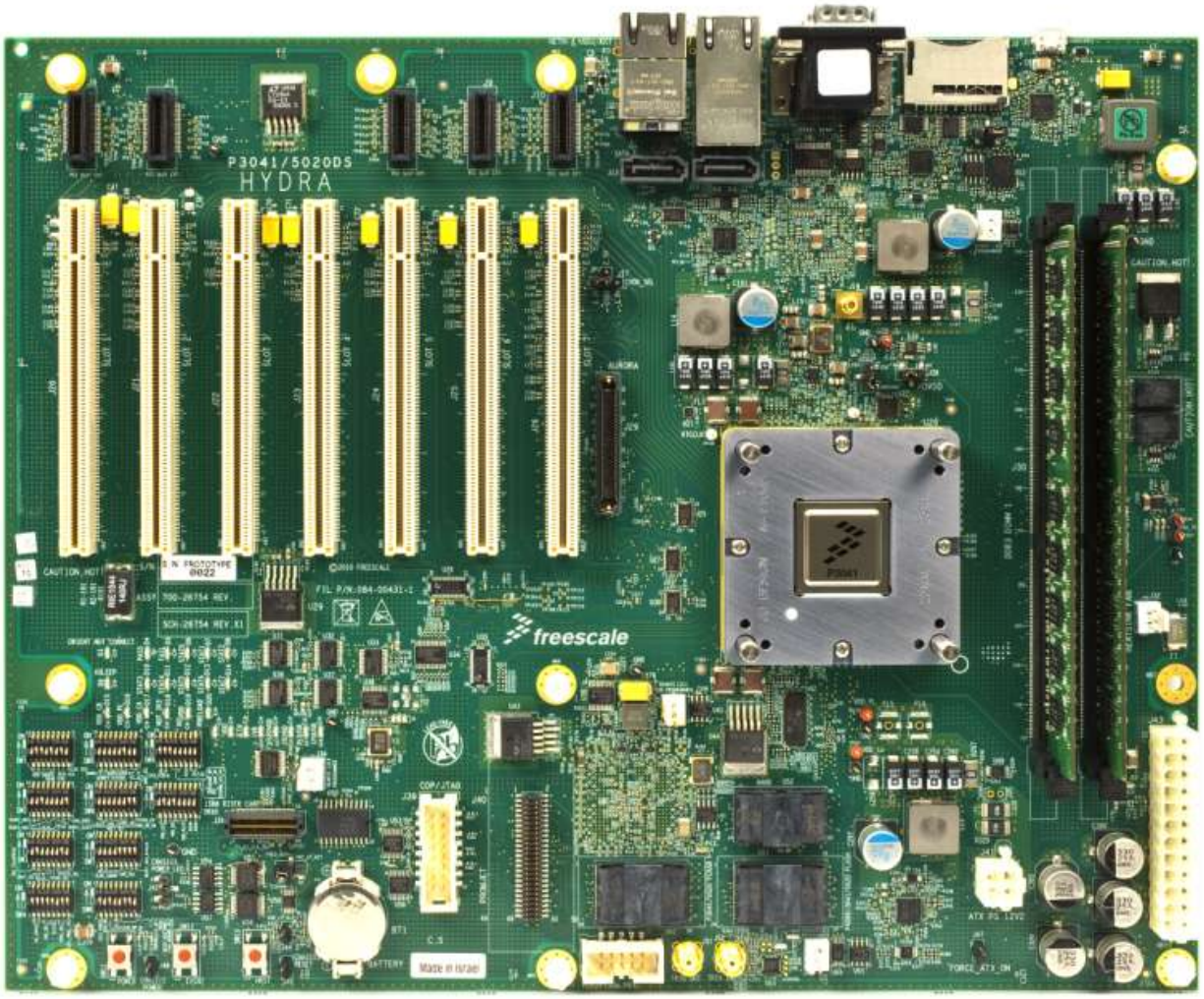
Software Development Kit (need to update)

- The Software Development Kit (SDK) 1.5 was released for T1040 and T2080 on Feb. 14, 2014. The components (described in more detail in the SDK product brief for the P4080) are:
  - T2080 rev. 1 silicon + QDS
  - Bare-metal support
  - U-boot debug
  - Register details
  - Linux Kernel and Application Debug

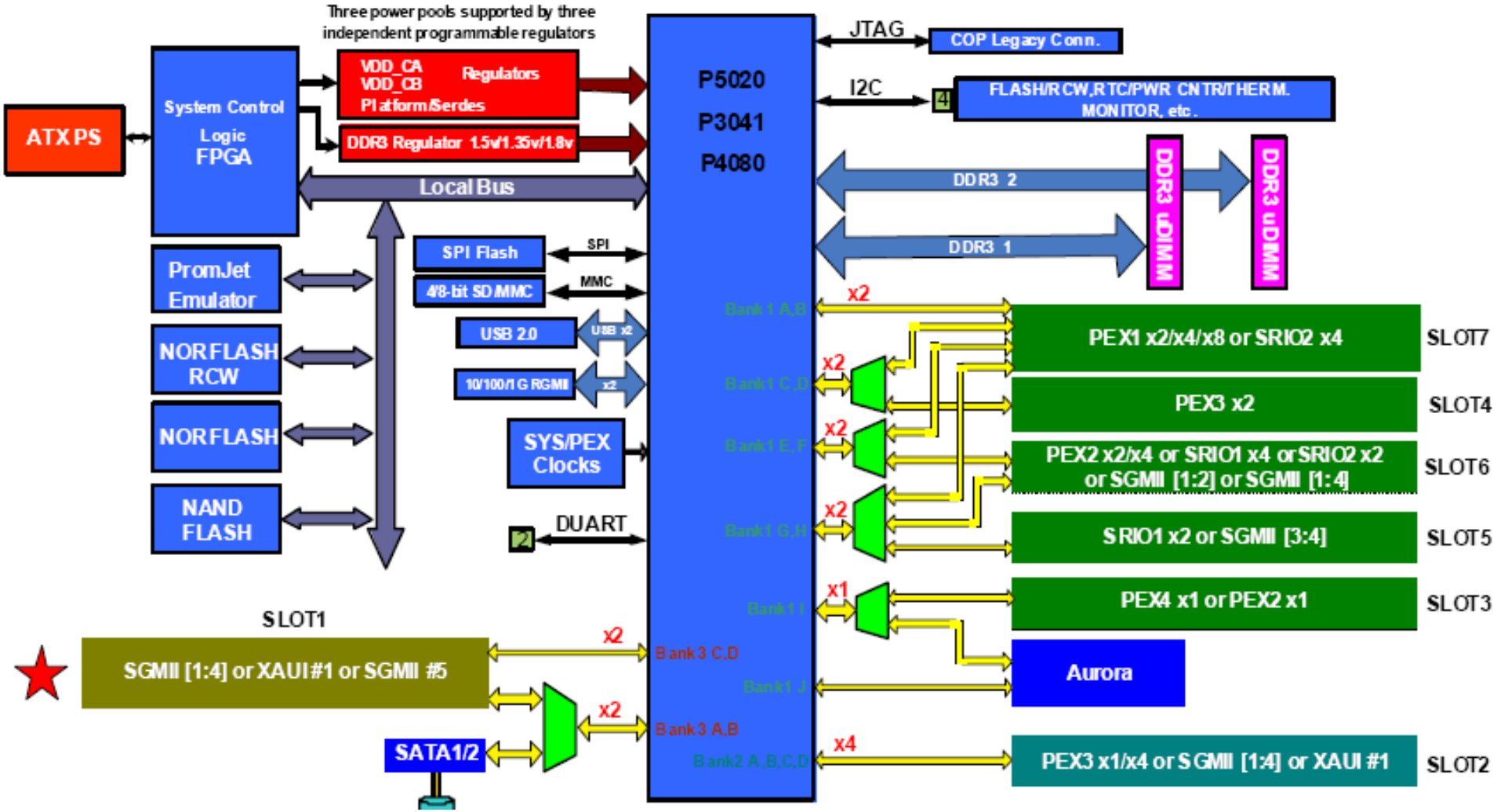
CodeWarrior

- CodeWarrior for Power Architecture v10.3.3 Service pack 2 product with T1040 and T2080 support are available along with first silicon. It features the next generation of CodeWarrior tools based on the Eclipse framework:
  - T2080 rev. 1 silicon + QDS
  - Bare-metal support
  - U-boot debug
  - Register details

T1040/T2081 Development System (need to update with T1040 RDB picture)



T1040 Development System Block Diagram (need to update with T1040 RDB)



Reference Documentation

- T1040 Hardware Specification and Reference Manual
- T2081 Hardware Specification and Reference Manual
- Application note (AN4733) T1040 to T2081 Migration Guide
- T1040/T2081 Design Checklist
- T1040 RDB User Manual
- T1040 RDB Schematic

Session Closing

- By now, you should be able to:
  - Use Freescale's design collateral to aid your own T1040 and T2081 designs
  - Understand the commonality and difference between these devices
  - Understand the unique challenges facing P4, P5 and P3 common design and the solutions to overcome them

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