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Schematic Design Guidelines, MAC-to-MAC MII Interface Connections

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MAC-to-MAC MII Interface Connections

Purpose

This design guide is supplied to our customers to facilitate the design of a robust PCB for their LAN application. This guide is intended for the review of new designs as well as existing PCB troubleshooting efforts. This design guide, however, should not be the ***only*** source of information in designing a PCB with an SMSC product. This particular design guide simply covers the circuit connections when using two MACs through the MII Bus Interface; an all-inclusive PCB design may or may not include additional information concerning our products. The system designer should also review the material listed below to assure a successful design effort:

- Specific SMSC Product Data Sheet
- Specific SMSC Product Reference Schematic
- Specific SMSC Bill of Material
- Any Applicable SMSC Product Application Note
- Specific SMSC Product LANCheck Schematic Checklist
- Specific SMSC Product LANCheck Component Placement Checklist
- Specific SMSC Product LANCheck Routing Checklist
- General PCB Design Guidelines

All the information above can be obtained from our website. If any of the above documentation is not available by that means, simply contact any SMSC FAE or SMSC Representative and they should be able to furnish any documentation required.

Schematic Design Guidelines

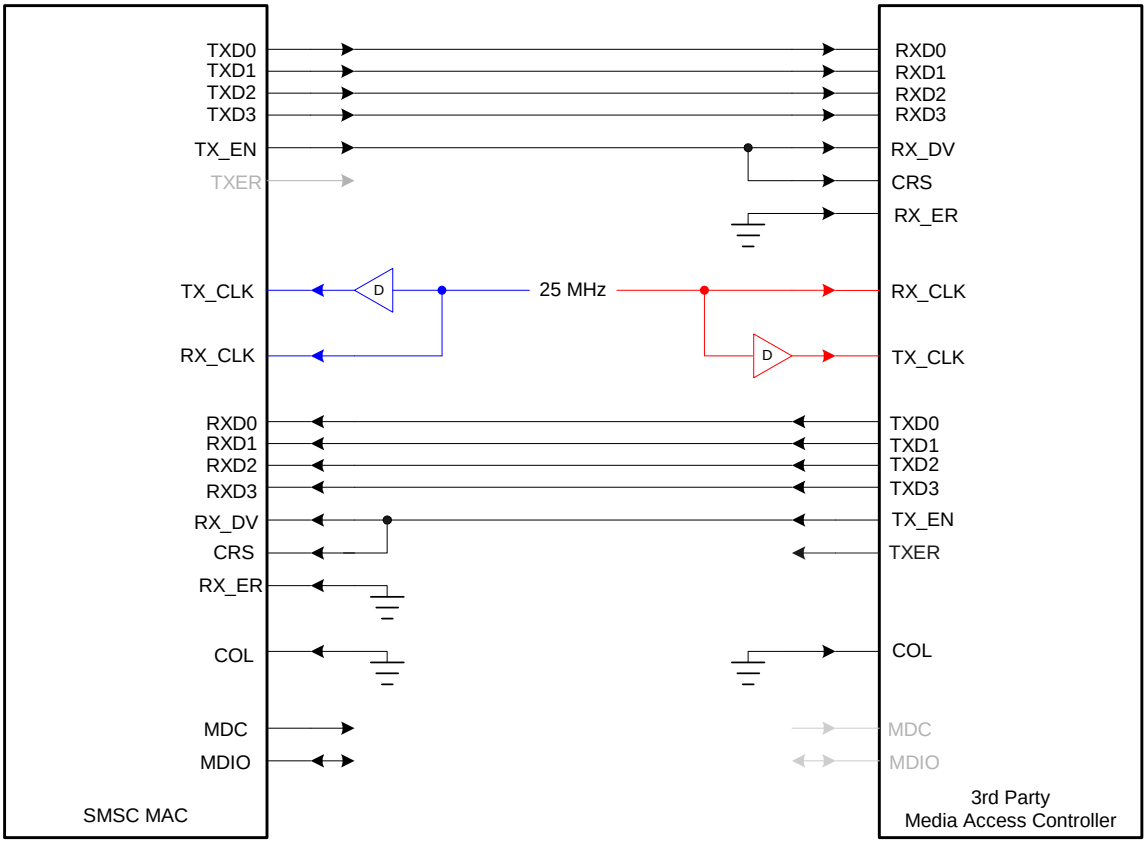
This schematic design note is provided to our SMSC LAN customers in an effort to expedite and simplify their design cycle. The information is provided with the understanding that any circuit suggested or designed by our customers must be evaluated and verified by the customer in an engineering lab environment. Subtle differences between components, PCB designs and specific applications require verification of each circuit designed.

The information contained herein should be used in combination with any applicable SMSC reference schematic, application note, and schematic checklist available. Upon detailed investigation, the designer may come to realize that in order to operate properly, different LAN devices may require more or less components and/or information than what is presented in this design note. This note should provide useful information and may explain the basis for certain component selection and/or circuit design.

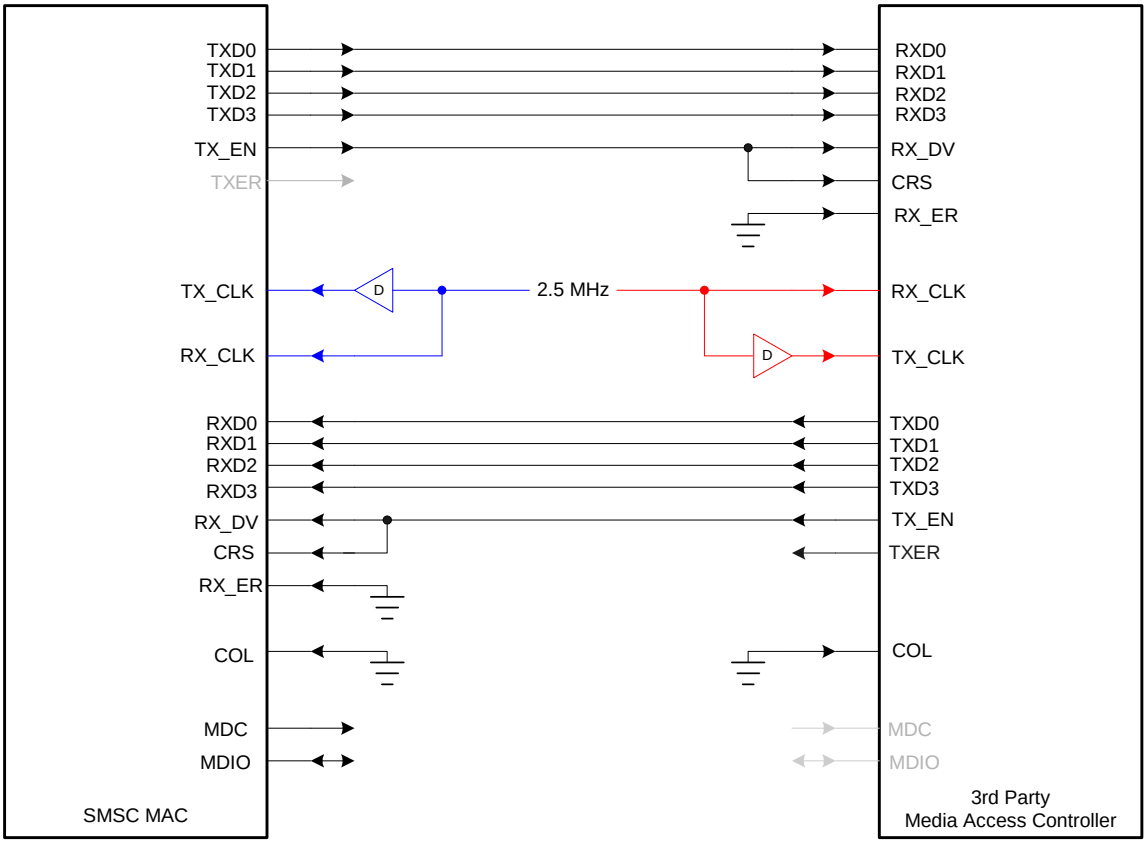
MAC-to-MAC MII Interface Connections

Typical applications for this type of architecture in a customer's design is when the designer wants to take advantage of SMSC's LAN devices ability to connect to a Local Bus Interface on the system processor. From the processor, through our part, the designer can connect up through the MII Interface to any other LAN device with an IEEE compliant MII Interface. Typical applications we see are customer's products that need 2 or 4 port switches. Typical switch chips only have an MII Interface and the 2 or 4 Twisted Pair Interfaces. Using one of SMSC's LAN devices with an MII Interface allows the switch chip to connect to the system processor.

The following two pages depict the recommended connections for two MAC-to-MAC MII Interface connections. The difference between the two is the speed that is supported. A Fast Ethernet (100BASE-TX) connection requires a 25.000 MHz source for the clocks. An Ethernet (10BASE-T) connection requires a slower 2.500 MHZ clock. Both applications are run in Full Duplex operational mode.



100BASE-TX Speed in Full Duplex Mode



10BASE-T Speed in Full Duplex Mode

There are two design points that should be considered by the design engineer. As noted in the schematics, the TX_CLK signals may require an amount of delay in order to meet the receiver's minimum input hold time of 10 nS. This situation comes about due to the atypical application of the MAC-to-MAC MII Interface. In the standard MAC-to-Phy MII Interface, the Phy supplies an RX_CLK that is recovered from the received data. Since the MAC-to-MAC MII Interface application is not supplying a recovered clock, some adjustments may be necessary.

The second design point worth considering is the use of series terminations on all driving signals. Depending upon the distances involved in the particular application, series resistors may be necessary to ensure proper signal integrity. Both output driver impedance and PCB trace impedance should be considered when developing this circuit. In particular, all clock signals should be checked for glitch-free and reflection-free signal characteristics.

In summation, the designer can use the information in this design note to connect two MACs together through the MII Interface. Upon hardware verification, it is the responsibility of the design engineer to check this circuit for accuracy and make any necessary adjustments. All timing relationships with the MII Interface should be verified to guarantee a robust Ethernet product.