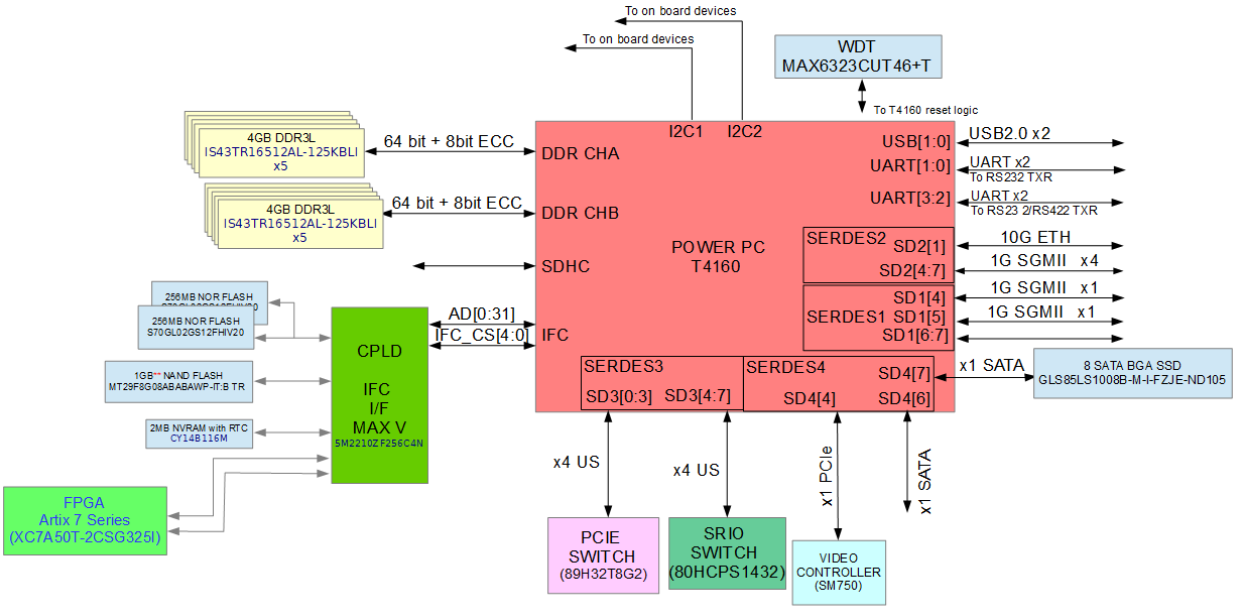
1.1 NXP T4160

The board uses NXP's QorIQ T4160 processor based on the Power PC architecture.

Features of T4160

Cores (Dual Threaded): 8
L2 Cache: 4 MB
CoreNet Platform Cache: 1 MB
DDR Controllers: 2
SerDes Lanes: 24
Max 10 Gbit/s Ethernet: 2
Max 1 Gbit/s Ethernet: 13
PCIe Controllers: 3

Interfaces used: DDR3L dual channel, IFC, USB x2, I2C x2, SDHC, UART x4.
Serdes used: PCIe x5, SRIO x4, SGMII x8, XFI x1, SATA x2



Configuration straps

IFC_TE - IFC external transceiver enable polarity select

Value	Implication
0	IFC drives logic 1 for TE assertion
1	IFC drives logic 0 for TE assertion

IFC_TE signal is not used in design. It is a signal used as the enable for any external transceivers used on the IFC bus.

ASLEEP - Serdes XVDD voltage select

Value	Implication
0	1.5V
1	1.35V

In this design, XVDD is powered by 1.35V power rail.

IFC_AD21 - DRAM type select

Value	Implication
0	DDR3 technology
1	DDR3L technology

In this design DDR3L technology is used. T4160's DDR controller GVDD and DDR memory chips are powered from 1.35V

RCW source selection - {IFC[8:15],IFC_CLE} -> cfg_rcw_src[0:8]

Switches are provided to realise different configurations. The configuration can also be driven by the CPLD

The required configurations for cfg_rcw_src[0:8] are

NOR flash - 0x37

Cfg_rcw_src[0:4] – 00011-> 32-bit NOR flash is used

0_0011_xxxx	32-bit NOR Flash cfg_rcw_src[5:8] encodings are the same as those described for 0_0001_xxxx (8-bit NOR Flash)

The last 4 bits are as follows

Cfg_rcw_src[5] – 0 -> There is no address shift in this design, this bit is don't care.

Cfg_rcw_src[6:7] – 11 -> There is no address shift.

Cfg_rcw_src[8] – 1 -> Simple asynchronous NOR device used.

0_0001_xxxx	8-bit NOR Flash cfg_rcw_src[5]: 0 Address shift "left" (most significant bits are IFC_AD[0:n-1] 1 Address shift "right" (least significant bits are IFC_AD[0:n-1] cfg_rcw_src[6:7]:
	00 Shift left by 10 OR shift right by 10 (depending on the value of cfg_rcw_src[5]/ IFC_MODE[5] to provide 22b addressability. Note that this option is not valid for pinouts supporting 32b of addressability. 01 Shift left by 7 OR shift right by 7 (depending on the value of cfg_rcw_src[5]/ IFC_MODE[5]) to provide up to 25b addressability. . 10 Shift left by 4 OR shift right by 4 (depending on the value of cfg_rcw_src[5]/ IFC_MODE[5]) to provide up to 28b addressability. 11 Shift left by 0 OR shift right by 0 (depending on the value of cfg_rcw_src[5]/ IFC_MODE[5]]) to provide up to 32b addressability. cfg_rcw_src[8]: 0 CS before ALE (supports internal latch based asynchronous NOR devices) 1 ALE before CS (supports simple asynchronous NOR devices)

Hardcoded RCW (COP emulator) - 0x9A

0_1001_1010[1] 0_1001_1100[1] 0_1001_1110[1]	Hard-coded RCW options (See Hard Coded RCW Options, for more information.)

Serdes options selected

Serdes 1

SD1_RX/TX[4:7] – SGMII

Table A-7. SerDes1

SerDes1							
SRDS_PRTCL_S1		EC2 (RGMII)	E	F	G	H	Per Lane PLL mapping
Decimal	Hex						
1	1	r1.5	XAUI1.10				1111
2	2	r1.5	HiGig[2]1.10 (3.125)				1111
4	4	r1.5	*HiGig[2]1.10 (3.75)*				1111
27	1B	r1.5	sg1.1	sg1.2	sg1.3	sg1.4	1111
35	23	r1.5	*sg1.1*	*sg1.2*	*sg1.3*	*sg1.4*	2222
37	25	r1.5			qs1a		xx1x

SRDS_PRTCL_S1 – 0x1B

Serdes 2

SD2_RX/TX1 – XFI

SD2_RX/TX[4:7] – SGMII

SRDS_PRTCL_S2 – 0x37

Table A-8. SerDes2 (continued)

SerDes2											
SRDS_PRTCL_S2		EC1 (RGMII)	A	B	C	D	E	F	G	H	Per Lane PLL mapping
Decimal	Hex										
35	23		sg2.5	sg2.6	sg2.10	sg2.9	*sg2.1*	*sg2.2*	*sg2.3*	*sg2.4*	11112222
37	25				qs2.b				qs2.a		xx1xxx1x
39	27		sg2.5	sg2.6	sg2.10	sg2.9			qs2.a		1111xx1x
45	2D		sg2.5	sg2.6	*sg2.10*	*sg2.9*			qs2.a		1111xx1x
47	2F		*sg2.5*	*sg2.6*	*sg2.10*	*sg2.9*			qs2.a		1111xx2x
49	31	r2.5	XAUI2.9						qs2.a		1111xx2x
51	33	r2.5	HiGig[2]2.9 (3.125)						qs2.a		1111xx2x
53	35	r2.5	*HiGig[2]2.9 (3.75)*						qs2.a		1111xx2x
55	37	r2.5		XFI1.10	XFI2.10		sg2.1	sg2.2	sg2.3	sg2.4	x11x2222
57	39	r2.5		XFI1.10	XFI2.10		*sg2.1*	*sg2.2*			x11x22xx

Serdes 3

SD3_RX/TX[0:3] – PCIe

SD3_RX/TX[4:7] – SRIO

Table A-9. SerDes3

SerDes 3										
SRDS_PRTCL_S3		A	B	C	D	E	F	G	H	Per lane PLL mapping
Decimal	Hex									
1	1	PCIe1 (5/2.5)								11111111
3	3	PCIe1 (5/2.5)				PCIe2 (8/5/2.5)				11111111
5	5	PCIe1 (5/2.5)				SRIO1 (5/2.5)				11111111
7	7	PCIe1 (8/5/2.5)				SRIO1 (3.125)				11112222
10	A	InterLaken (6.25)								11111111
11	B					PCIe2 (8/5/2.5)				11112222
13	D	InterLaken (6.25)				PCIe2 (8/5/2.5)				11112222

SRDS_PRTCL_S3 – 0x05 default, 0x07

When SRDS_PRTCL_S3 option 0x07 is used 125Mhz clock connected to PLL2 will be used and the speed setting in SRIO switch must be changed from 0x011 (5Gbps) to 0x101 (3.125Gbps)

Serdes 4

SD4_RX/TX4 – PCIe4

SD4_RX/TX[4:7] – SATA

SRDS_PRTCL_S4 – 0x09

Table A-10. SerDes4

SerDes 4						
SRDS_PRTCL_S4		E	F	G	H	Per lane PLL mapping
Decimal	Hex					
3	3	PCIe4 (8/5/2.5)				1111
5	5	SRIO2 (5/2.5)				1111
7	7	SRIO2 (3.125)				2222
9	9	PCIe4 (5/2.5)		SATA1 (3/1.5)	SATA2 (3/1.5)	1122
11	B	Aurora (5/2.5)		SATA1 (3/1.5)	SATA1 (3/1.5)	1122
13	D	Aurora (5/2.5)		SRIO2 (5/2.5)		1111
15	F	Aurora (3.125)		SRIO2 (3.125)		2222

Processors IRQ lane connections

Processor IRQ pin	Net name	IRQ source
IRQ00	SRIO_SW_IRQ	SRIO switch

IRQ01	FPGA_IRQ1	FPGA
IRQ02	RTC_INT_OUT	NVRAM
IRQ03	VDD_CORE_SMB_ALERT_1	VDD_CORE power controller
IRQ04	FPGA_IRQ2	FPGA
IRQ05	FPGA_IRQ3	FPGA

1.2 DDR3 Memory

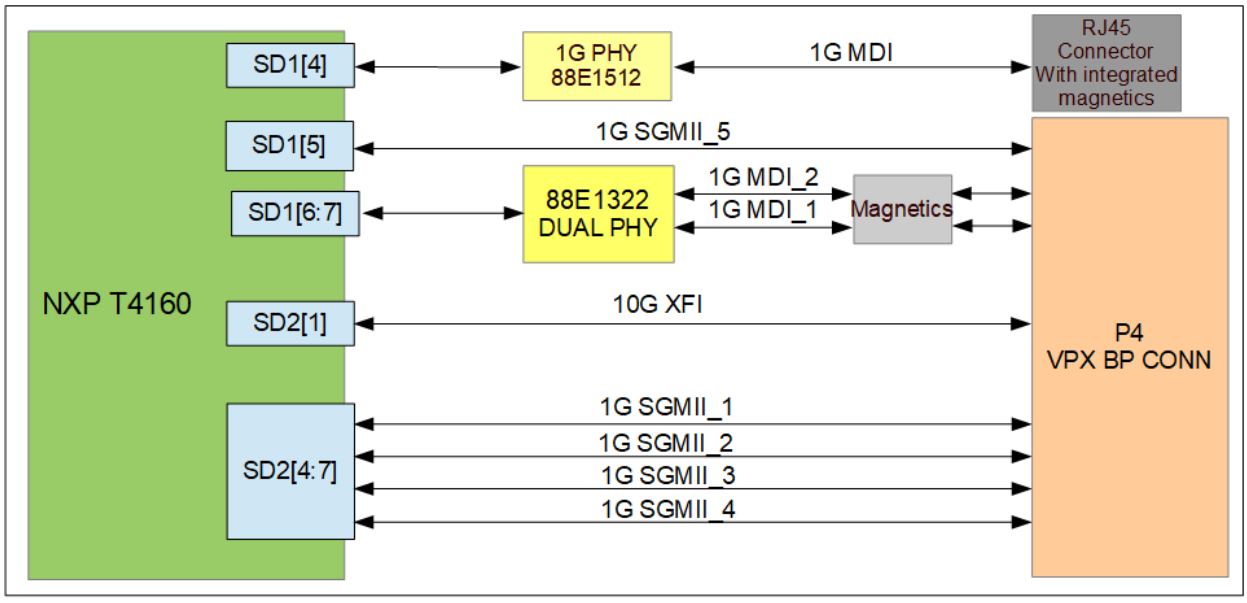
NXP T4160 has two memory controllers.

DDR3 memory of 4GB is connected to each controller with ECC as discrete chips. Discrete chip used is ISSI IS43TR16512AL-125KBLI, a 512M x16 chip. DDR3L mode of operation is used in system and selected by T4160 strap pin IFC_AD21, which has been already described in previous section

A total memory of 8GB is available in the board.

1.3 Ethernet

Ethernet connectivity in the VPX board is shown in below figure



The VPX board has a total of Eight 1G ethernet interface, out of which five 1G SGMII signals are connected to the VPX backplane connector P4 and the other three SGMII is connected through a PHY. Out of the three PHY SGMII signals, two are connected to a dual phy(Marvell 88E1322)and the MDI signals connected to the backplane connector P4 through magnetics, and one SGMII is connected to a single phy(Marvell 88E1512) and it's MDI signals connected to front panel RJ45 connector on board.

Of the 5 SGMII ports connected to Backplane, 1port is connected to single phy(Marvell 88E1512) and 4 ports are connected to Quad PHY (Marvell 88E1340).

PHY address corresponding to each SD port is given below,

Sl. No.	Port Name	PHY Address (Hex)	PHY used
1	SD1 [4]	0x0	Marvell 88E1512
2	SD1[5]	0x1	Marvell 88E1512
3	SD1[6]	0x5	Marvell 88E1322
4	SD1[7]	0x7	Marvell 88E1322
5	SD2 [4]	0x18	Marvell 88E1340
6	SD2[5]	0x19	Marvell 88E1340
7	SD2[6]	0x1a	Marvell 88E1340
8	SD2[7]	0x1b	Marvell 88E1340

10G interface from T4160 is routed to the backplane connector P4.

1.3.1 Dual phy (88E1322)

The device has two clock sources. Selection is through CLK_SEL[1:0] pins. Default selection is 0b11 which sources clock from 25Mhz crystal. 125Mhz clock is also connected to the phy and there is provision to change CLK_SEL[1:0] to set to 125MHz REF_CLKP/N

51 50	CLK_SEL[1] CLK_SEL[0]	I	Reference Clock Selection 00 = Use 156.25 MHz REF_CLKP/N 01 = Use 125 MHz REF_CLKP/N 10 = Use 25 MHz XTAL_IN/XTAL_OUT[1] 11 = Use 25 MHz XTAL_IN/XTAL_OUT CLK_SEL[1:0] must be connected to VDDOR for configuration high.

Ethernet management interface MDIO/MDC is connected to T4160's EMI1 interface with the PHYAD selection as 0b00101 and 0b00111

Hardware configuration pins

The details of each config pin selection and alternate provisions provided in VPX board are highlighted below.

Note: If there is an alternate setting for a parameter, it is repeated twice and the default selection highlighted in bold.

```
CONFIG_0: 0001/0000
    0000 - Phy addresses 0b00000 - 0b00011
    0001 - Phy addresses 0b00100 - 0b00111
    PHY_ORDER: 0 = Phy address order is Port 0-00,1-01,2-10,3-11

CONFIG_1: 1111/0111 /0011 /1011
      SEL_MS: 1 = Prefer master
      SEL_MS: 0 = Prefer slave (DEPOP option)
      ENA_PAUSE: 1 = Advertise pause and asymmetric pause
      ENA_PAUSE: 0 = Do not advertise pause and asymmetric
      pause
      C_ANEG[O:1]: Advertise all ethernet capabilities

CONFIG_2: 0110/1110
    S_ANEG: SGMII/1000BASE-X Auto-negotiations OFF
    S_ANEG: SGMII/1000BASE-X Auto-negotiations ON
    (DEPOP option)
    ENA_XC: Default enable auto-crossover
    DIS_SLEEP: Default energy detect OFF
    PDOWN: Default power up port
CONFIG_3: 0001
  MODE[2:0]: 001 SGMII(System) to copper
```

1.3.2 Single Phy (Frontpanel) (88E1312)

Ethernet management interface MDIO/MDC is connected to T4160's EMI1 interface with the PHYAD selection as 0x0

Hardware configuration pins

VDDO setting

VDDO_SEL = Tie to GND -> VDDO=2.5V/3.3V

In VPX board VDDO is connected to 2.5V

CONFIG pin selection

CONFIG pin selection

Tie to FP_PHY_LED1
PHYAD[0] = 0
VDDO_LEVEL = 2.5V/1.8V

Tie to FP_PHY_LED0
PHYAD[0] = 1
VDDO_LEVEL = 2.5V/1.8V

1.3.3 Single Phy RTM (88E1312)

Ethernet management interface MDIO/MDC is connected to T4160's EMI1 interface with the PHYAD selection as 0x1

Hardware configuration pins

VDDO setting

VDDO_SEL = Tie to GND -> VDDO=2.5V/3.3V

In VPX board VDDO is connected to 2.5V

CONFIG pin selection

1.3.4 RTM Quad phy (88E1340)

The device has two clock sources. Selection is through CLK_SEL[1:0] pins. Default selection is 0b11 which sources clock from 25Mhz crystal. 125Mhz clock is also connected to the phy and there is provision to change CLK_SEL[1:0] to set to 125MHz REF_CLKP/N

51 50	CLK_SEL[1] CLK_SEL[0]	I	Reference Clock Selection 00 = Use 156.25 MHz REF_CLKP/N 01 = Use 125 MHz REF_CLKP/N 10 = Use 25 MHz XTAL_IN/XTAL_OUT[1] 11 = Use 25 MHz XTAL_IN/XTAL_OUT CLK_SEL[1:0] must be connected to VDDOR for configuration high.

Ethernet management interface MDIO/MDC is connected to T4160's EMI1 interface with the PHYAD selection as 0b11000, 0b11001, 0b11010, and 0b11011

Hardware configuration pins

The details of each config pin selection and alternate provisions provided in VPX board are highlighted below.

Note: If there is an alternate setting for a parameter, it is repeated twice and the default selection highlighted in bold.

CONFIG0 = 0110:

PHY_ADDR[4:2] = 110
PHY_ORDER = 0; Low->High

CONFIG1 = 1111:

C_ANEG[1:0] = 11: Advertise all capabilities
ENA_PAUE=1; advertise Pause
SEL_MS=1 -> Prefer Master

CONFIG2 = 1110:

PDOWN=0 -> Default power up port
DIS_SLEEP=1 -> Default energt detect off
ENA_XC=1 -> Default enable Auto-Crossover
S_ANEG=1 -> SGMII/1000BaseX Auto-Neg on
Q_ANEG=1 -> SGMII Auto-Neg on QSGMII on

CONFIG3 = 0001:

MODE[2:0] = 001 ->SGMII to Copper
PTP_EN = 0 -> PTP Disable

PHY ID of each chip is given below

88E1312 :

Table 77: PHY Identifier 1
Page 0, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 78: PHY Identifier 2
Page 0, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI Lsb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24
9:4	Model Number	RO	Always 011101	Always 011101	Model Number 011101
3:0	Revision Number	RO	See Descr	See Descr	Rev Number. Contact Marvell® FAEs for information on the device revision number.

For both 88E1322 and 88E1340

Table 116: PHY Identifier 1
Page 0, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 117: PHY Identifier 2
Page 0, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	0x03	0x03	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24
9:4	Model Number	RO	0x1C	0x1C	Model Number 011100
3:0	Revision Number	RO	See Descr	See Descr	Rev Number Contact Marvell FAEs for information on the device revision number.

1.4 NAND Flash, NOR Flash, NVRAM

The IFC bus connects to 4 different types of memory devices. The connections to the devices are through a CPLD, which acts as latch to separate address and data signals and as a voltage translator. The CS mapping is as follows

IFC_CS0 - NOR flash
IFC_CS1 - NAND flash
IFC_CS2 - NVRAM
IFC_CS3 - FPGA memory 1
IFC_CS4 - FPGA memory 2

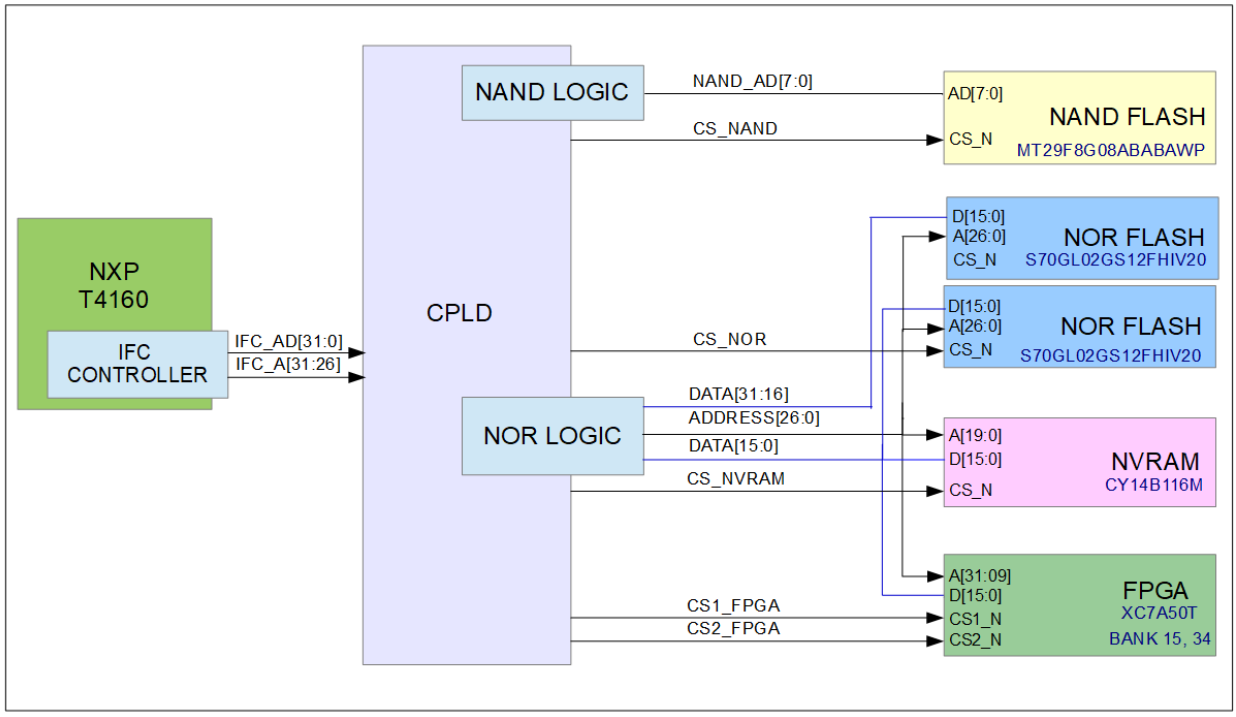
1GB NAND Flash is provided on board. IFC controller is interfaced to the CPLD and through the logic implemented in CPLD. NAND Flash is connected to multiplexed address/data and control signals implemented in CPLD. The part used is MT29F8G08ABABAWP. T4160 CS1 corresponds to NAND flash.

512MB NOR Flash is provided on the board. Here also the IFC controller of T4160 is connected the CPLD and the logic is implemented on the CPLD. Two 256MB NOR flash parts are used in parallel to achieve 512 MB capacity. The part used is S70GL02GS12FHIV20. A NOR flash HAS address[26:0]/data[15:0]. The address signals are common to both NOR flash, but NOR flash 1 has data

signals DATA[15:0] and NOR flash 2 has DATA[31:16]. The control signals are same for both the NOR flash parts. T4160 CS0 corresponds to NOR flash.

NVRAM used in the board is CY14B116M. This chip is interfaced to the CPLD NOR Logic where address pins [19:0], data[15:0] and control signals are used. T4160 CS2 corresponds to NVRAM.

FPGA has internal logic/memory array. It has address[22:0] and data[15:0]. This interface is also interfaced to the CPLD NOR logic. T4160 CS2 and CS3 corresponds to FPGA.

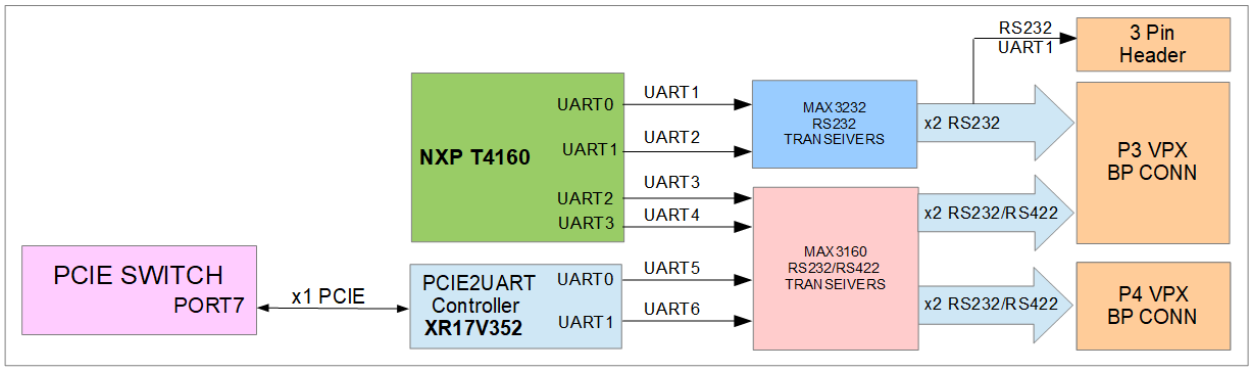


1.5 UART/RS232/RS422

Total of 6 UART interfaces are there. Out of this, 2 are used as RS232 Interface and 4 as selectable between RS232/RS422 signaling modes.

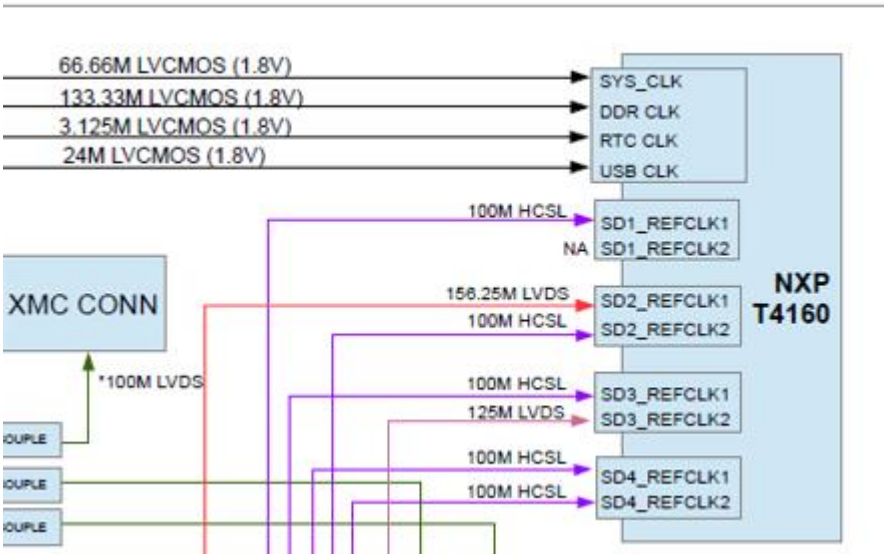
Four of the UART outputs are from NXP T4160. Out of that UART1 and UART2 are converted to RS232 signaling through MAX3232. The MAX3232 outputs are connected to P3 VPX backplane connector. UART1 out of MAX3232 is also connected to a 3-pin header on board. UART3 and UART4 are converted to selectable RS232/RS422 signaling mode through MAX4160. MAX4160 outputs are connected to P3 VPX backplane connector.

2 UART outputs UART5 and UART6 are generated from a PCIe based UART controller. UART5 and UART6 are converted to selectable RS232/RS422 signaling mode through MAX4160. MAX4160 outputs are connected to P4 VPX backplane connector.

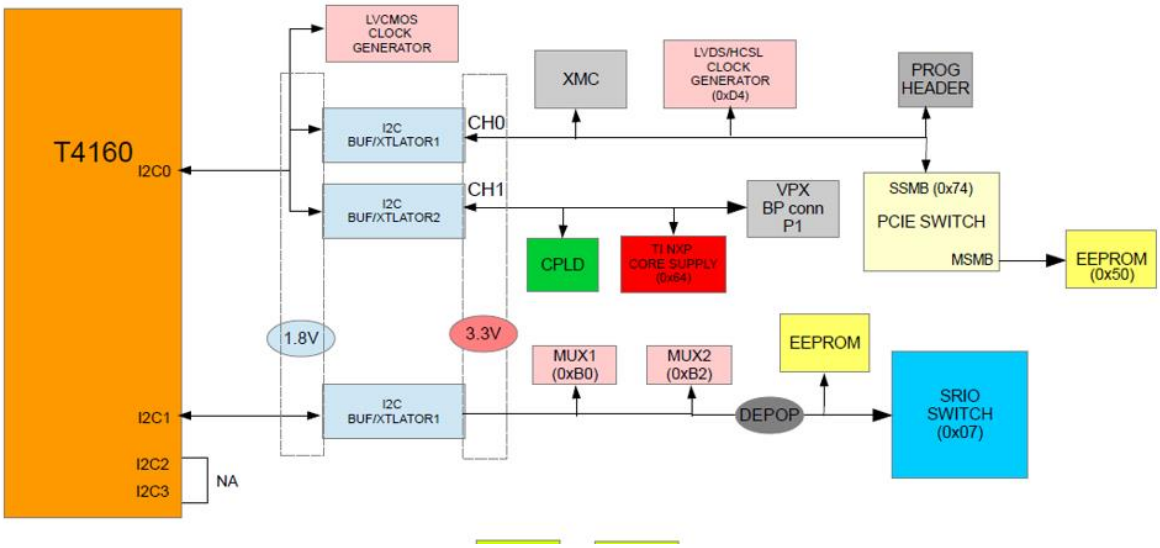


1.6 T4160 clock

5P49V5935B000LTGI is used as an LVCMOS clock generator to provide clocks to NXP T4160 processor. There are 4 clock outputs which connect to T4160, which are SYSCLK(133.33Mhz), DDRCLK(66.66Mhz), RTCCLK(3.125MHZ), USBCLK(24MHz).



1.7 I2C


T4160
I2C0
I2C1
I2C2
I2C3
NA
LVCMOS CLOCK GENERATOR
I2C BUF/XTLATOR1
I2C BUF/XTLATOR2
I2C BUF/XTLATOR1
CH0
CH1
XMC
LVDS/HCSL CLOCK GENERATOR (0xD4)
PROG HEADER
VPX BP conn P1
SSMB (0x74)
PCIE SWITCH
MSMB
EEPROM (0x50)
CPLD
TI NXP CORE SUPPLY (0x64)
1.8V
3.3V
MUX1 (0xB0)
MUX2 (0xB2)
EEPROM
DEPOP
SRIO SWITCH (0x07)