◆DESCRIPTION

The Ramaxel RMT3150ED58E8W-1600 memory module family are low profile Unbuffered SODIMM modules with 30.00mm height based DDR3 technology. DIMMs are available as No-ECC (x64) modules.

The module family based on 8(x64) x8 DDR3 DRAM components, and the DIMMs feature serial presence detect based on a serial EEPROM device.

◆FEATURE

- 204-pin Dual-in-line DDR3 memory module.
- JEDEC Standard with 1.5 V (±0.075 V) power supply
- 1 Rank Organizations based x8 DDR3 DRAM components
- Fast data transfer rates: PC3-12800
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK,CK#)
- Commands entered on each rising CK edge
- Eight-bit pre-fetch architecture
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Data mask (DM) for masking write data
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- Concurrent auto pre-charge option is supported
- Auto Refresh (CBR) and Self Refresh Mode
- ZQ calibration
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- For contact pads, electrolytic gold plating 0.38 micrometer minimum.
- Halogen-free

◆**PART NUMBER DECODER**

R M T 315 0 E D 58 E 8 W- 1600

Ramaxel Module

Module Type

R:240pin DDR3 Unbufferd DIMM

PCB Number

ECC:

0: Without ECC

1: With ECC

DRAM Vendor:

M: Micron

H: Hynix

S: Infineon

L: Longmax

E: Elpida

K: Samsung

DRAM DIE Revision

(Refer to DRAM manufacturer)

DRAM Density:

18: 128Mb (16M*8b)

28: 256Mb (32M*8b)

38: 512Mb (64M*8b)

48: 1Gb (128M*8b)

58: 2Gb (256M*8b)

Speed: 800：PC3-6400

1066: PC3-8500

1333:PC3-10600

1600：PC3-12800

1866：PC3-14900

DRAM Package:

F: FBGA

W: WBGA

Module Density

5: 256MB

6: 512MB

7: 1GB

8: 2GB

SSTL:

C: 25V D:1.8V E:1.5V

◆ **PINOUT, PIN LOCATION and FUNCTIONAL DESCRIPTION**

PINOUT

DDR3 SDRAM SO-DIMM Pinout.

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	$V_{REF}DQ$	2	Vss	53	DQ19	54	Vss	105	V_{DD}	106	V_{DD}	157	DQ42	158	DQ46
3	Vss	4	DQ4	55	Vss	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	161	Vss	162	Vss
7	DQ1	8	Vss	59	DQ25	60	Vss	111	V_{DD}	112	V_{DD}	163	DQ48	164	DQ52
9	Vss	10	$\overline{DQS0}$	61	Vss	62	$\overline{DQS3}$	113	$\overline{WE}$	114	$\overline{S0}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	167	Vss	168	Vss
13	Vss	14	Vss	65	Vss	66	Vss	117	V_{DD}	118	V_{DD}	169	$\overline{DQS6}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13[3]	120	ODT1	171	DQS6	172	Vss
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S1}$	122	NC	173	Vss	174	DQ54
19	Vss	20	Vss	71	Vss	72	Vss	123	V_{DD}	124	V_{DD}	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	$V_{REF}CA$	177	DQ51	178	Vss
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	Vss	128	Vss	179	Vss	180	DQ60
25	Vss	26	Vss	77	NC	78	A15[3]	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{DQS1}$	28	DM1	79	BA2	80	A14[3]	131	DQ33	132	DQ37	183	DQ57	184	Vss
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	Vss	134	Vss	185	Vss	186	$\overline{DQS7}$
31	Vss	32	Vss	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS4}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	Vss	189	Vss	190	Vss
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	Vss	140	DQ38	191	DQ58	192	DQ62
37	Vss	38	Vss	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	Vss	195	Vss	196	Vss
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	Vss	146	DQ44	197	SA0	198	$\overline{EVENT}$
43	Vss	44	Vss	95	A3	96	A2	147	DQ40	148	DQ45	199	VDD_{SPD}	200	SDA
45	$\overline{DQS2}$	46	DM2	97	A1	98	A0	149	DQ41	150	Vss	201	SA1	202	SCL
47	DQS2	48	Vss	99	V_{DD}	100	V_{DD}	151	Vss	152	$\overline{DQS5}$	203	Vtt	204	Vtt
49	Vss	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$	155	Vss	156	Vss				

1. NC = No Connect, NU = Not Useable, RFU = Reserved Future Use
2. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
3. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

◆ FUNCTIONAL DESCRIPTION

Symbol	Type	Polarity	Function
CK0/$\overline{CK0}$, CK1/$\overline{CK1}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$[1:0]	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	—	Selects which DDR3 SDRAM internal bank of eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
A[9:0], A10/AP, A11 A12/$\overline{BC}$, A[15:13]	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped)
DQ[63:0]	In/Out	—	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	In/Out	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.
V_{DD}, V_{DD}SPD, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REF}DQ, V_{REF}CA	Supply	—	Reference voltage for SSTL15 inputs.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to V_{DD}SPD on the system planar to act as a pull up.
SCL	Input	—	This pin is used to clock data into and out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SCL bus line to V_{DD}SPD on the system planar to act as a pull up
SA[1:0]	Input	—	Address pins used to select the Serial Presence Detect and Temp sensor base address.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).

Symbol	Type	Polarity	Function
$\overline{EVENT}$	Wire-OR Out	Active Low	This pin is an output of the Thermal Sensor to indicate critical module temperature. A resistor must be connected from $\overline{EVENT}$ bus line to VDDSPD on the system planar to act as a pullup.
$\overline{RESET}$	In	Active Low	This signal resets the DDR3 SDRAM

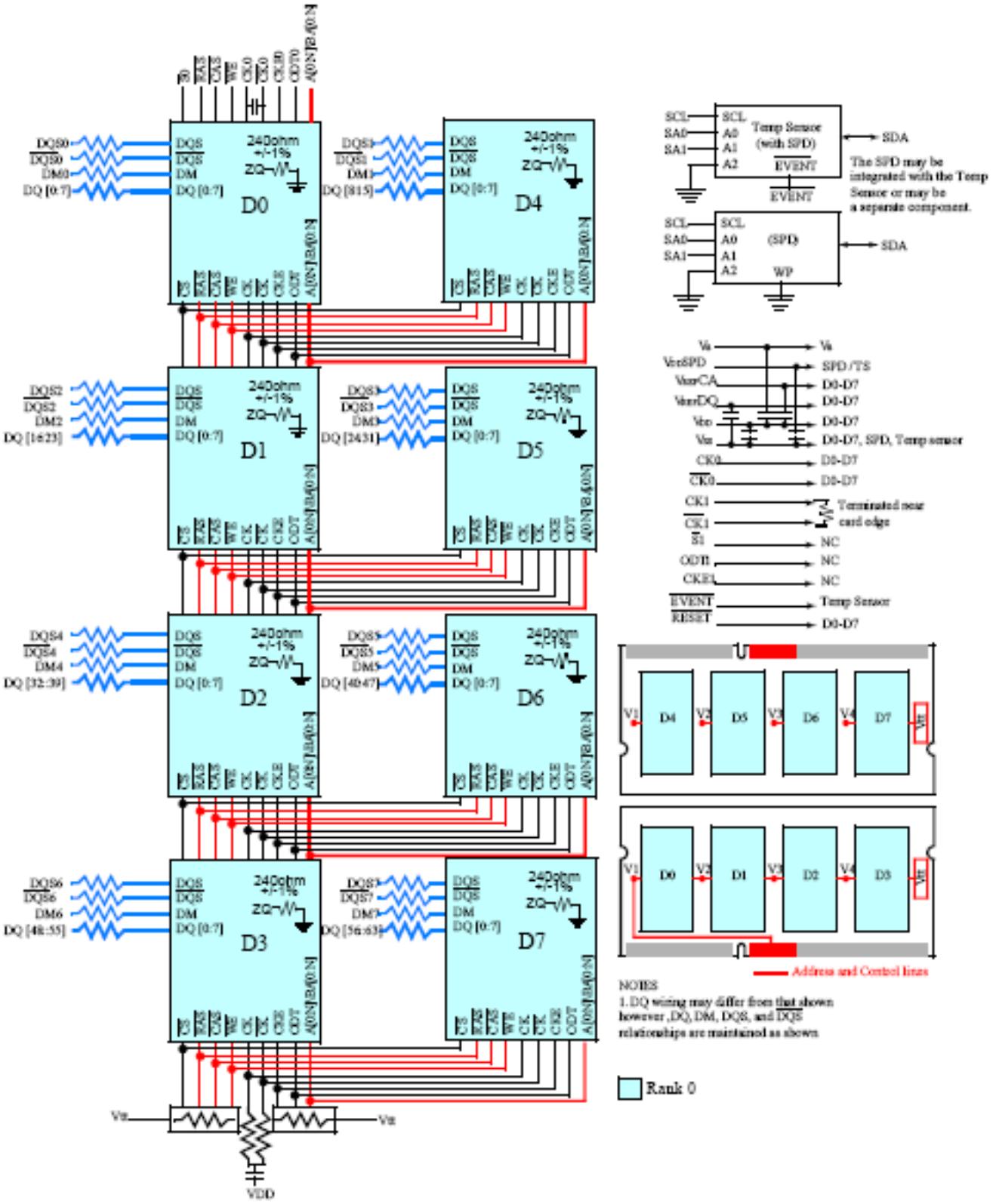
◆ COMMAND TRUTH TABLE

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA3	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7,8,9,12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:
1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registerng any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

◆**BLOCK DIAGRAM**

Block Diagram: Raw Card Version B(Populated as 1rank of x8 SDRAMs)



◆ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

◆OPERATING TEMPERATURE and DC/AC OPERATING CONDITION

OPERATING TEMPERATURE

Parameter	Symbol	Rating	Units	Notes
Operating case temperature	TC	0 to +95	℃	1、2、3

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0° C to +85° C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85° C and +95° C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. (This double refresh requirement may not apply for some devices.)
b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Note: Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM for measurement conditions.

DC/AC OPERATING CONDITION

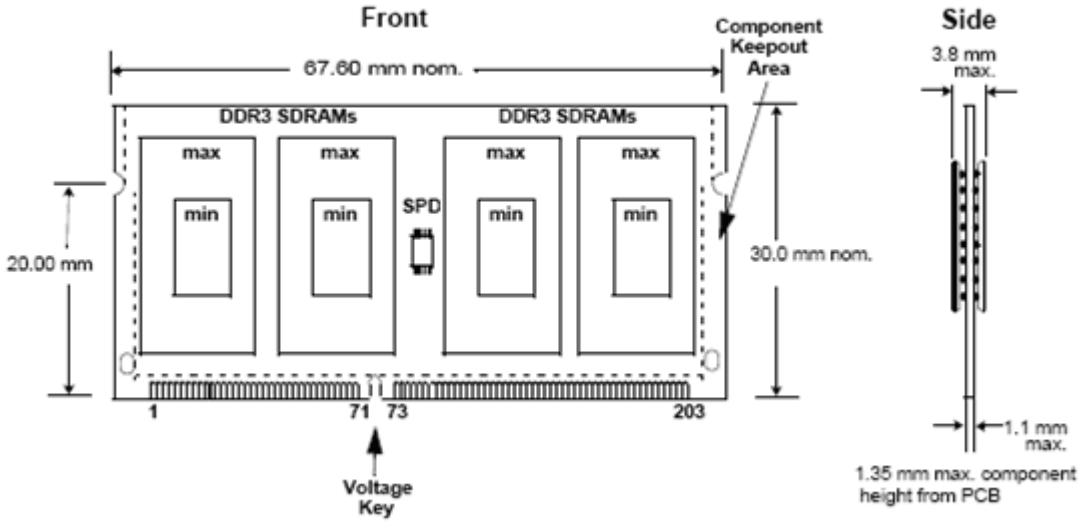
Symbol	Parameter	Rating			Unit	Notes
		Min	Typ	Max		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1, 2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1, 2

Notes:
1.Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

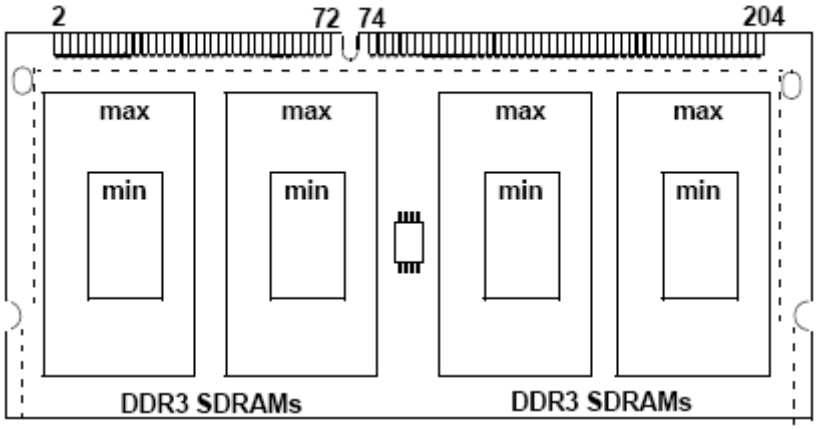
Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL(DC)	DC input logic low	VSS	Vref - 0.100	V	1
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low	-	Vref - 0.175	V	1, 2
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:
1. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
2. See 9.6 "Overshoot and Undershoot Specifications" on page 113.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{Ref(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

◆**DIMENSIONS (Unit: mm)**

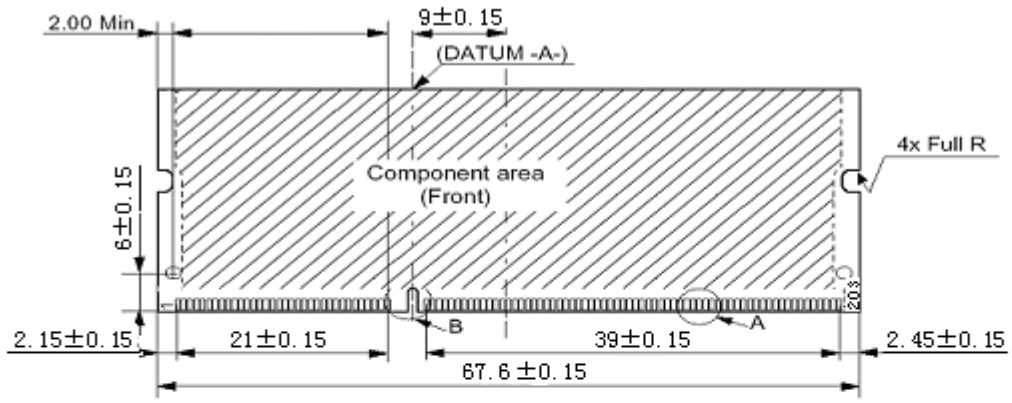


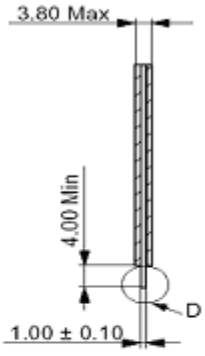
Rear View



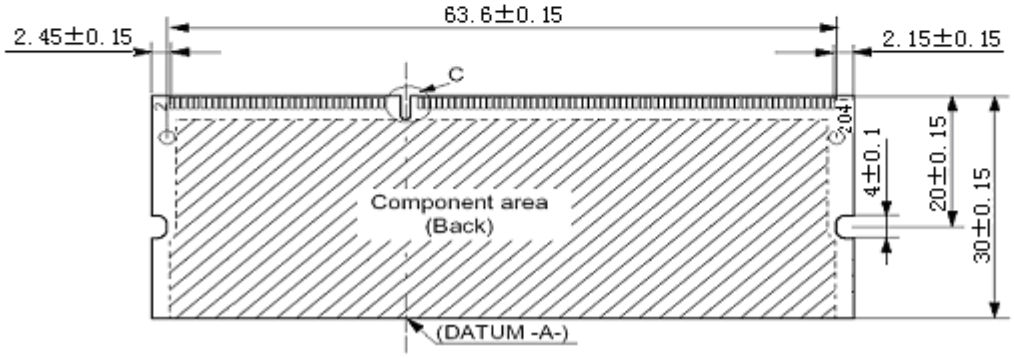
Unit: mm

Front side

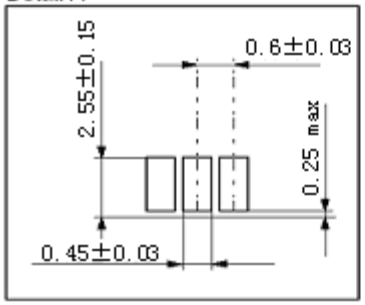




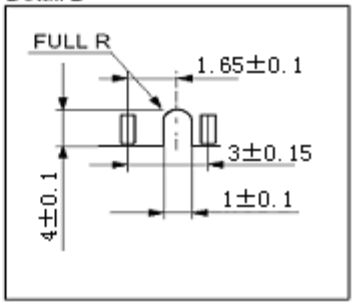
Back side



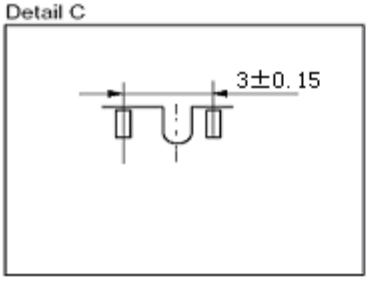
Detail A



Detail B



Detail C



Detail D