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MM912_634 - Die to Die Interface (D2D) Software Setting Recommendation

Featuring the MM912_634 Product Family of Relay Drivers with LIN

1 Introduction

This application note clarifies for users the correct software setting of the Die-to-Die (D2D) interface, in order to avoid encountering increased current consumption when the device is placed into STOP mode.

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2 Description of the Potential Problem

As is well documented in the associated data sheets, the MM912_634 are a family of System-in-Package (SiP) Relay Driver solutions implemented with a digital MCU die and an Analog driver die. Communication between the dice is accomplished through the Die-to-Die (D2D) interface block.

The Die-To-Die (D2D) interface block is composed of:

- Eight bidirectional data bus lines (D2DDAT0…D2DDAT7)
- One clock signal line coming from the MCU (D2DCLK)
- One interrupt line coming from the Analog Die (D2DINT)

The D2D interface was designed to be used to implement a 4-bit or 8-bit data bus transfer.The appropriate data bus transfer width is configured through the D2DCW bit in D2DCTL0 register.

For the MM912_634 SMARTMOS product family, only the first four (4) bidirectional data lines (D2DDAT0…D2DDAT3) are physically connected between the MCU die and the Analog die.

The other four (4) data lines, D2DDAT4 to D2DDAT7, are unused.

When not used as bidirectional data bus lines for the D2D interface, the D2DDAT4…7 pins act as GPIO connections.

DDRD register allows to configure GPIO:

- as bidirectional data line (high impedance)
- or as output

When entering in stop mode, D2DDATx configured as bidirectional data bus lines for the D2D interface, and D2DDATx configured as GPIO output are explicitly pulled down.

D2DDATx configured as default GPIO (bidirectional data line) stay floating

For the MM912_634 family, when going into STOP mode, D2DDAT0…D2DDAT3 are pulled low. However, D2D data lines D2DDAT4…D2DDAT7, in their default state, are not configured as OUTPUT GPIOs.

Therefore, when entering STOP mode, these D2DDAT4…D2DDAT7 pins enter an undefined high impedance floating state (not pulled low). The voltage on these lines can increase over time, leading to increased current consumption in the device while in STOP mode because these connections are in a high impedance state.

When this phenomena occurs in a device in STOP mode, a user may observe an additional 20-30 µA of current consumption over short (~10s) or longer time periods.

3 Proposed Application Solution

In order to avoid the possible occurrence of increased current consumption, users should explicitly configure the D2D data lines D2DDAT4…D2DDAT7 as OUTPUTS by writing xF0 to the DDRD register (0X0007).

Refer to the data sheet chapter describing "Port D Data Direction Register (DDRD) for more details.

Table 241. Port D Data Direction Register (DDRD)

Address 0x0007 Access: User read/write[166]

	7	6	5	4	3	2	1	0
R W	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset	0	0	0	0	0	0	0	0

Note:
166. Read: Anytime.
Write: Anytime.

Table 242. PTD Register Field Descriptions

Field	Description
7-0 DDRD	**Port D Data Direction** This register controls the data direction of pins 7 through 0. The D2DI function controls the data direction for the associated pins. In this case, the data direction bits do not change. When operating a pin as a general purpose I/O, the associated data direction bit determines whether it is an input or an output. 1. Associated pin is configured as an output. 0. Associated pin in configured as a high-impedance input.

Figure 1. Port D Data Direction Register (DDRD)

4 References

Following are URLs where you can obtain information on related Freescale products and application solutions:

Document Number and Description	URL
MM912_634D1 - Data Sheet	http://www.freescale.com/files/analog/doc/data_sheet/MM912_634D1.pdf
MM912F634 - Data Sheet	http://www.freescale.com/files/analog/doc/data_sheet/MM912F634.pdf
Freescale.com Support Pages	**URL**
MM912_634 - Product Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MM912_634
Analog Home Page	http://www.freescale.com/analog

5 Revision History

Revision	Date	Description
1.0	6/2015	• Initial release

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