S32V234-EVB2
QUICK START GUIDE
REV 2. FEBRUARY 2018

SECURE CONNECTIONS
FOR A SMARTER WORLD
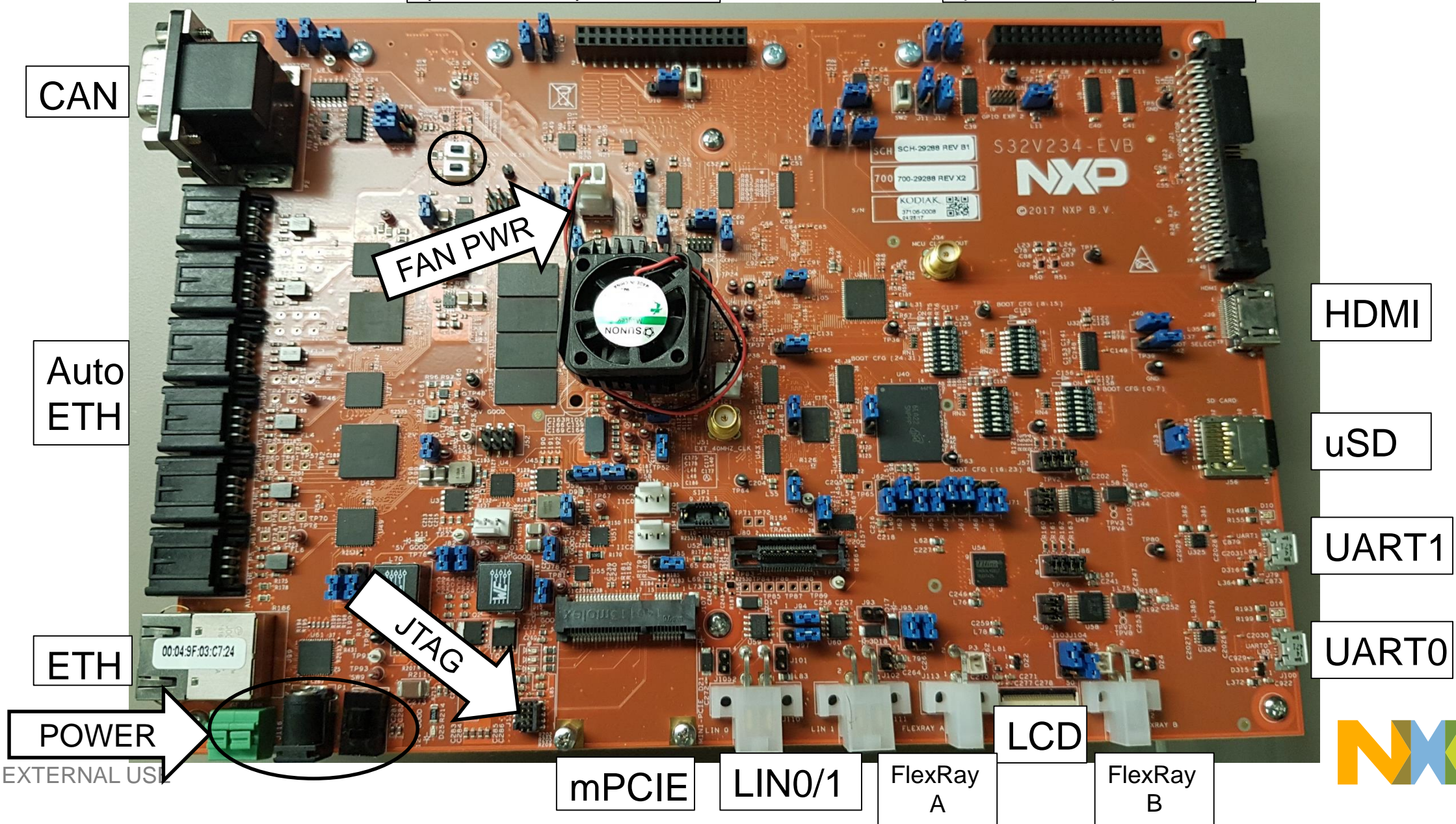
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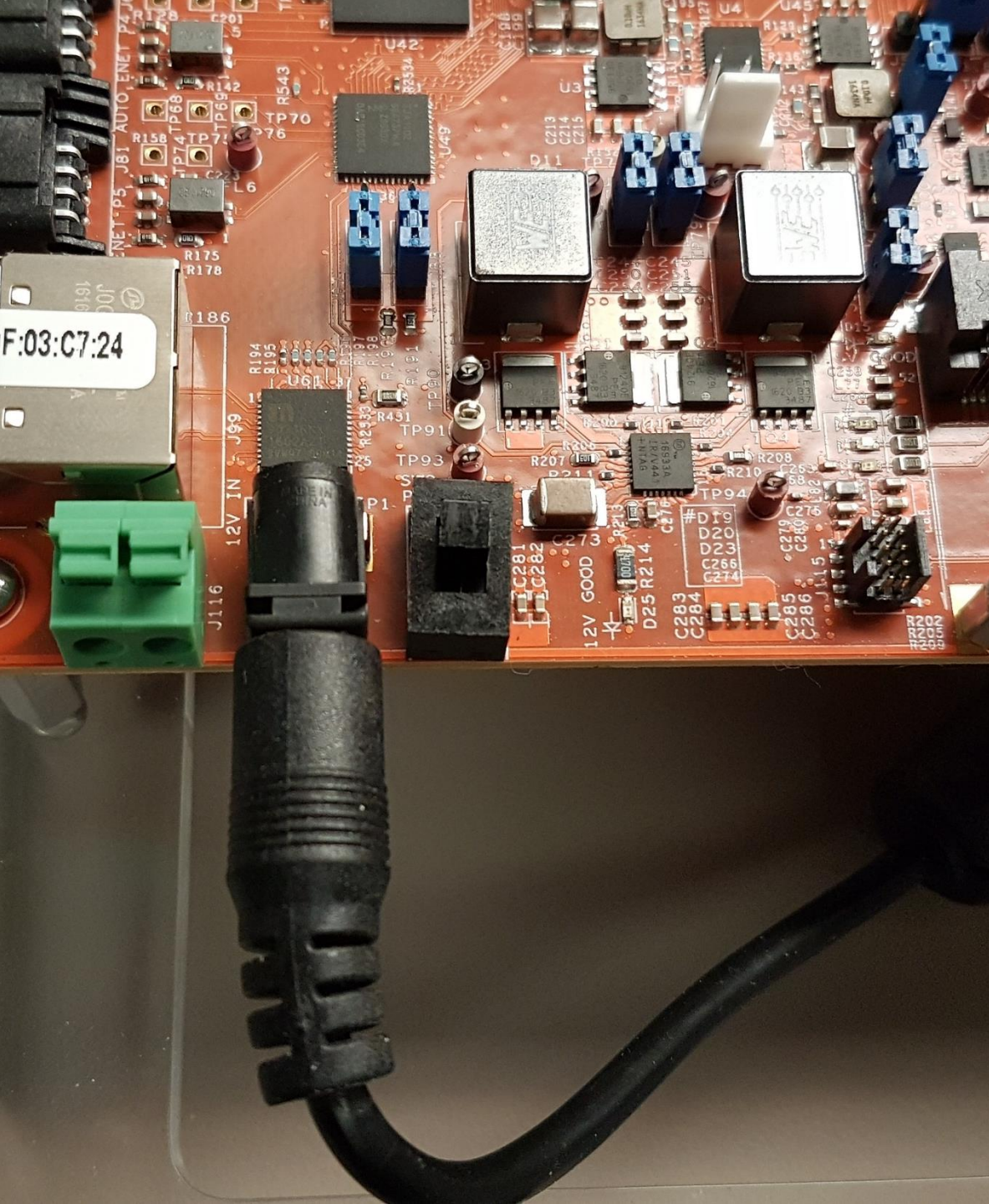- Boot sources and boot configurations

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# Board Overview

(On back) MIPI 1

(On back) MIPI 0

CAN

FAN PWR

Auto ETH

JTAG

ETH

POWER

HDMI

uSD

UART1

UART0

mPCIE

LIN0/1

FlexRay A

LCD

FlexRay B

Power

- EVB2 uses 12V barrel jack power supply, or wire-ended jack

- ***DO NOT USE BOTH SIMULATENOUSLY OR YOU WILL LIKELY DAMAGE YOUR BOARD***

- 12V hot goes to Pin 1 of Barrel jack or wire-end plug. See rear of board for pin marking

- Dual position SW (SW9) controls power flow

- Red TP93 available for measuring 12V prior to main power SW (SW9)
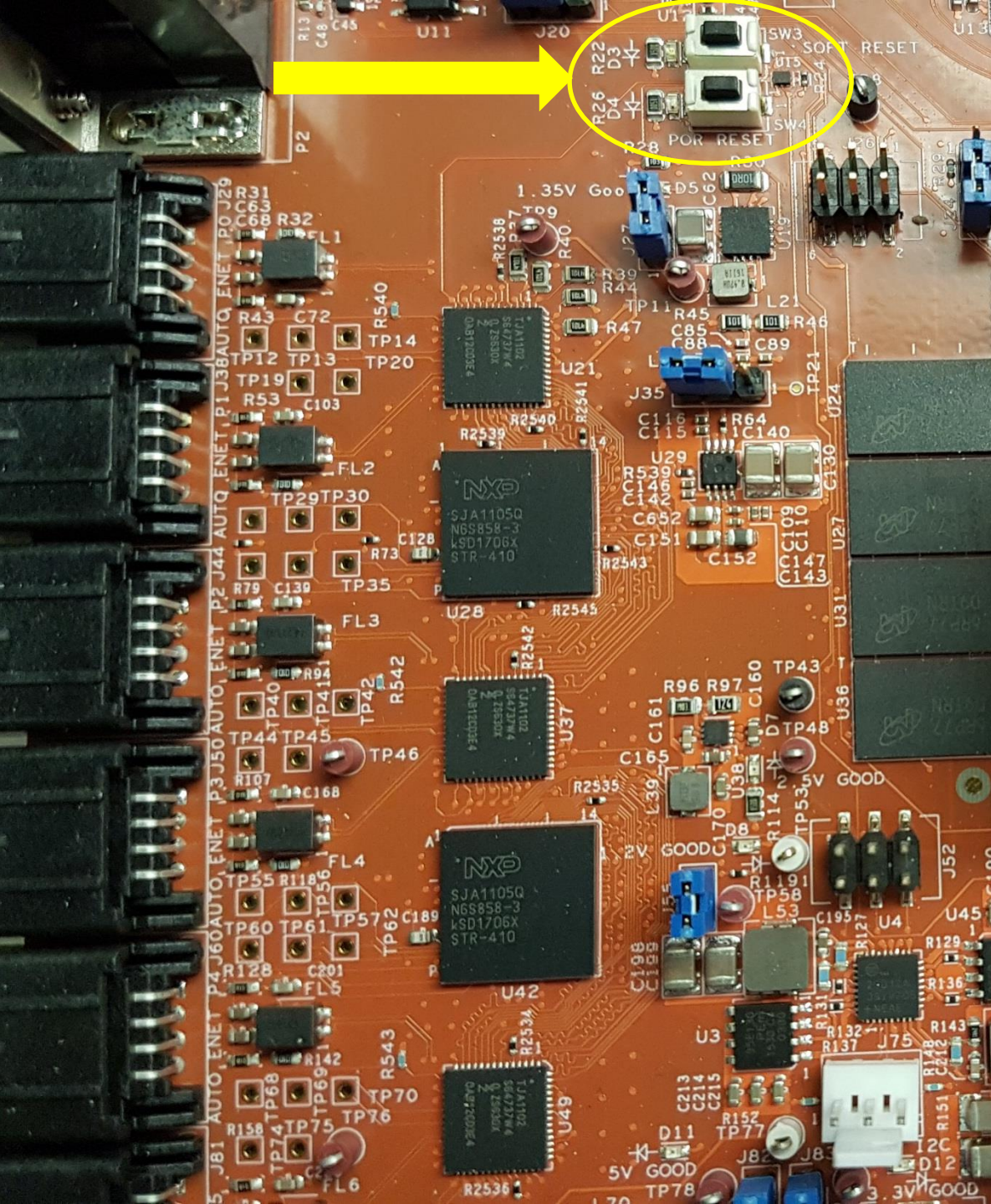
Reset

- EVB2 provides "SOFT RESET" and "POR RESET" buttons

- Pressing "POR RESET" pulls active low "EXT_POR" signal on S32V234 chip to GND

- Pressing "SOFT RESET" pulls active low "RESET" signal on S32V234 chip to GND

- Refer to S32V234 Reference Manual for specifics on levels of reset and device reset flow
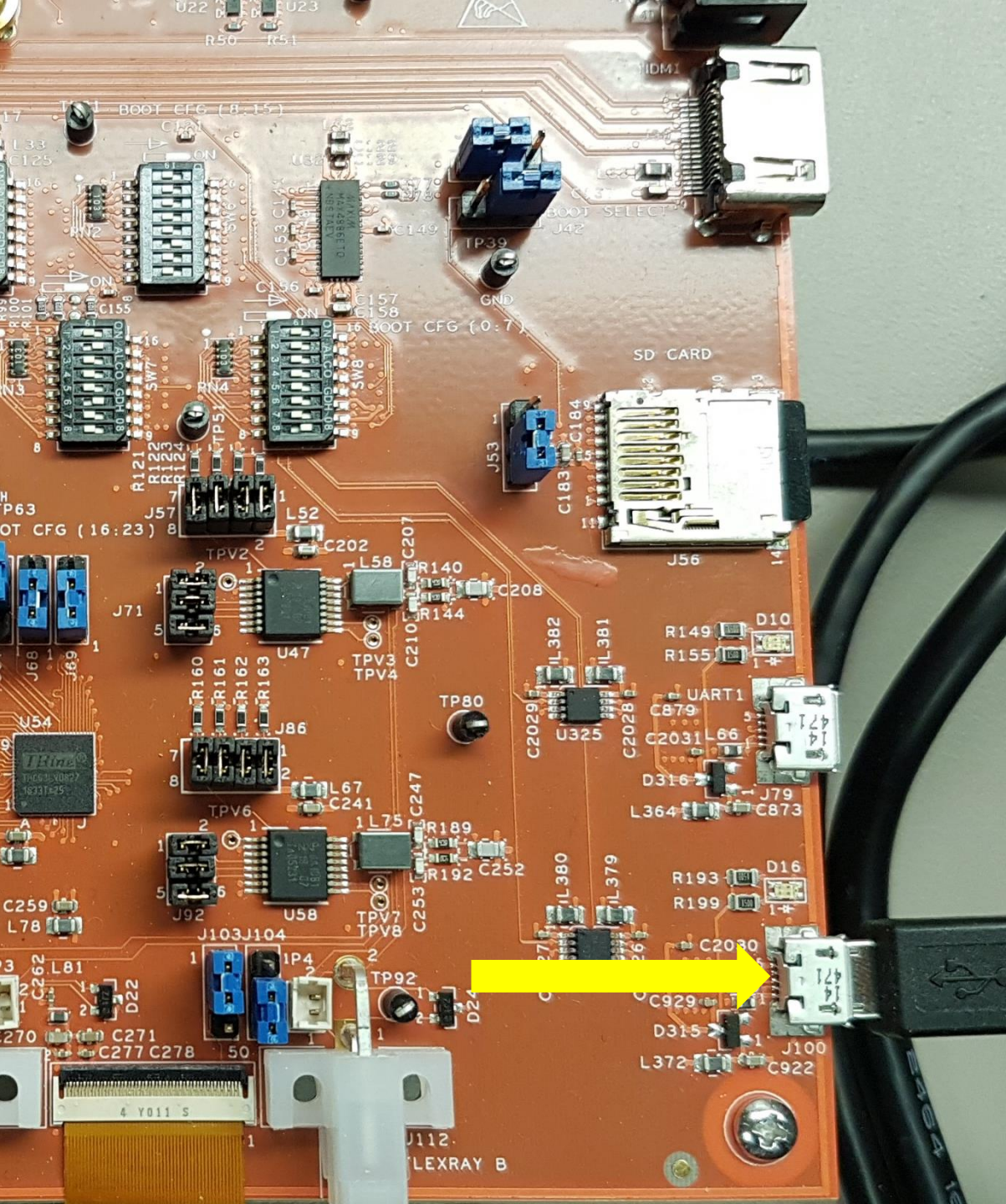
Serial Communications

- EVB2 has an FTDI chip to convert UART signals to USB friendly format, to be connected to host PC

- UART 0 (with arrow) is default serial output for Linux BSP boot images.

- Default comms rate is 115200 baud with 8 data bits, 1 stop bit, no parity.

- Use a program such as puTTy, TeraTerm or Minicom on host PC to communicate with board

- Lack of serial output on boot can indicate corrupt (or missing) boot medium, or improper baud rate. Activity LED is present near each USB port to indicate serial communication

Boot configurations

- The S32V234 has are three 'Boot modes':
  - Serial download: Allows external tool to use CAN or UART to download code into RAM and start execution. Code must be redownloaded on every reset in this mode. Uses 48kbps baud rate, see S32V234 reference manual, system boot chapter, for specifics.
  - Boot from fuses: Configures device to boot according to the internal eFuse values programmed at factory, generally not used for evaluation boards due to lack of custom fuse programming.
  - Boot from RCONs: the most common configuration, allows customization of boot configuration via the 4 8-bit DIP switches on EVB2 (circled in picture).

- The modes are selected by 'BOOT_MODE0/1' signals controlled by jumpers J40(Boot_Mode[0]) & J42(Boot_Mode[1]), and are read at reset. By default, the EVB2 is configured to use 'Boot from RCONs' mode. Refer to reference manual 'System Boot' chapter for more details on boot modes.

- By default, the board boots from RCON switches, which allow choosing boot core, and SD card modes for advanced use cases. (*Table to be provided at end of slides.*)

- Using Jumpers J48 and J49, the EVB2 can be configured to boot from SD card, EMMC, or QSPI. Booting from SD card is the factory default setting.

- Boot from SD: J48=1&2,J49=1&2, SW8 = 0x80
- Boot from EMMC: J48=1&2, J49=2&3, SW8 = 0xC0
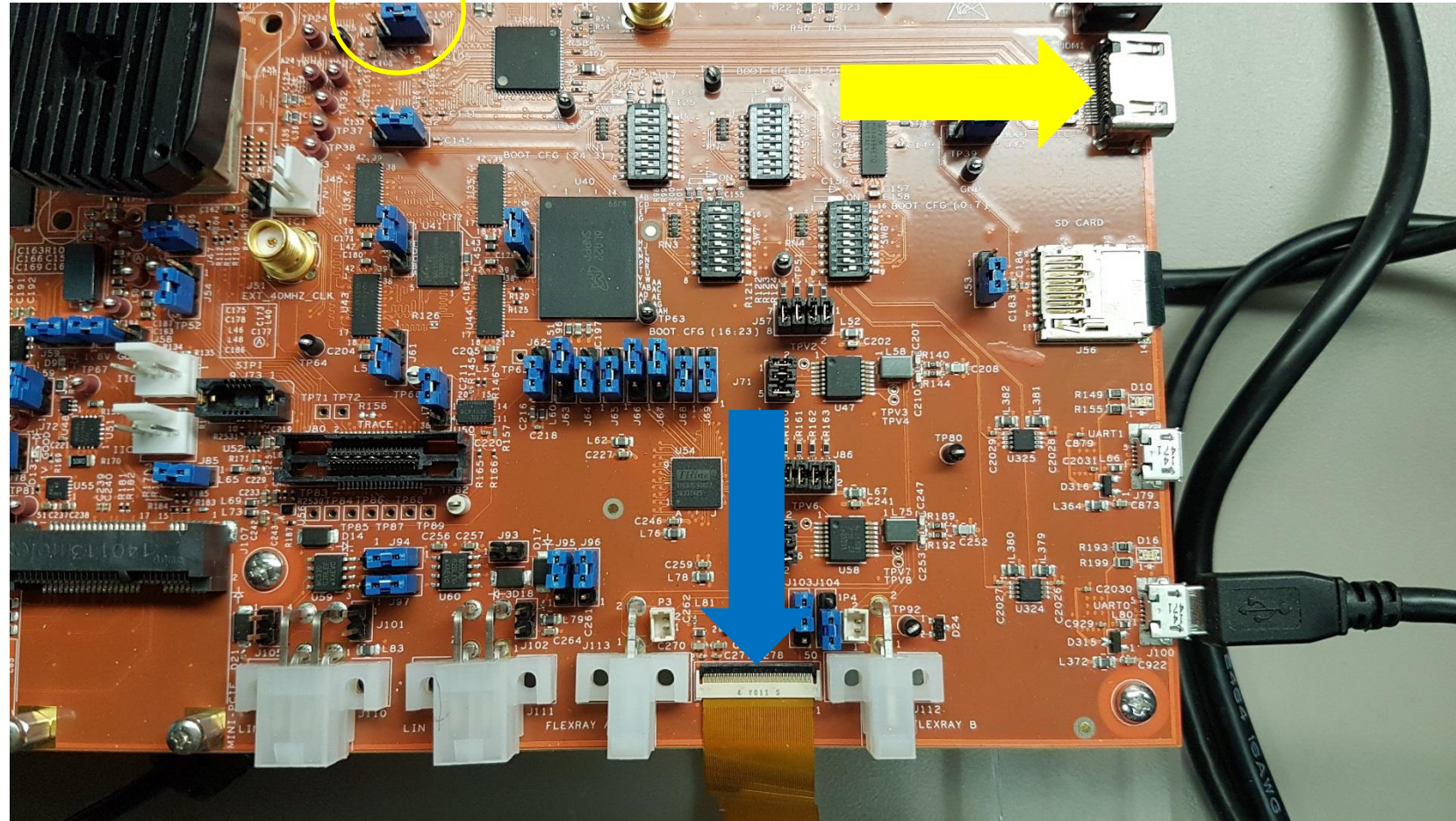- Boot from QSPI: J48=2&3, SW8 = 0x01
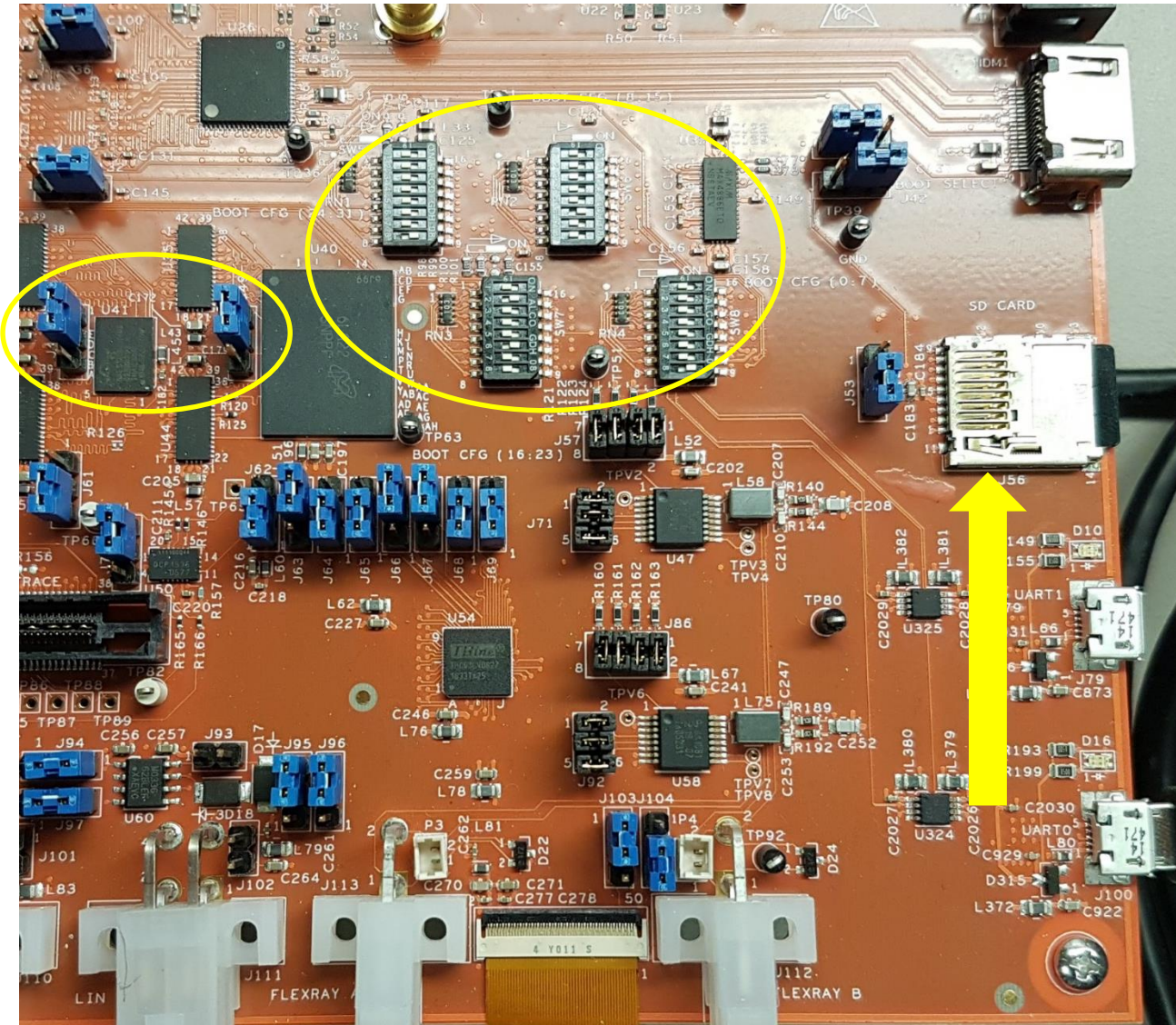
Note: Not all configurations of switches are supported by Linux BSP. Please refer to Linux BSP User Manual for validated modes.

Display

- EVB2 has TFT display or HDMI. Jumper J36 (circled) set to 1&2 for HDMI (yellow arrow), 2&3 for LVDS (blue arrow)

- *NOTE: Power off board before changing any jumpers or switches.*

Camera inputs

- EVB2 two MIPI camera inputs, and two VIU (parallel) inputs

- NXP and distributors sell MIPI cameras designed for use with this board

- Additionally can be added and 5V/12V external power can be provided (see schematics for pinout)

- *WARNING: Power off board before changing any jumpers or switches.*

- *Configuring optional voltage:* For 5V on Cameras 0/1, set jumpers J7/J5 to 2&3 respectively. For 12V, set to 1&2 respectively.

- *Enabling/Disabling optional voltage:* To enable opt. voltage for cameras 0/1, set jumpers J6/J4 to 1&2 respectively. To disable opt. voltage, set J6/J4 to 2&3 respectively.

- *NOTE: If you aren't sure if your camera requires optional voltage, keep it disabled and refer to schematics/data sheet for your camera and EVB2.*
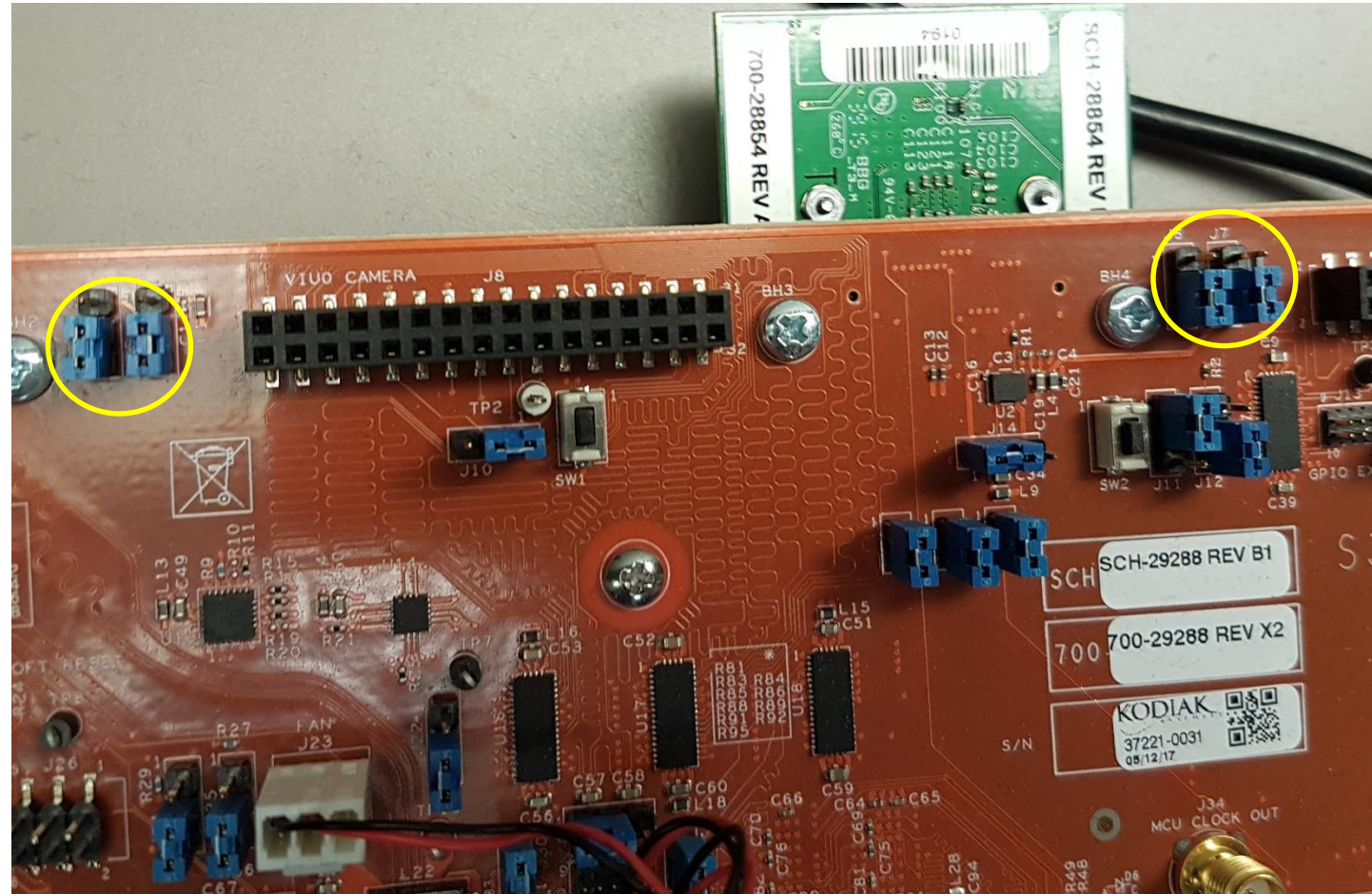
Camera configurations

- By default, jumpers J6 & J4 should be set to 2&3 to keep optional voltage disabled.

- This configuration is suitable for most MIPI cameras that do not require additional voltage supply. It is also the safest configuration when using a new camera.

- Two NXP-endorsed MIPI cameras use this configuration: the OV10640 module (picture) and the Sony IMX224 camera.
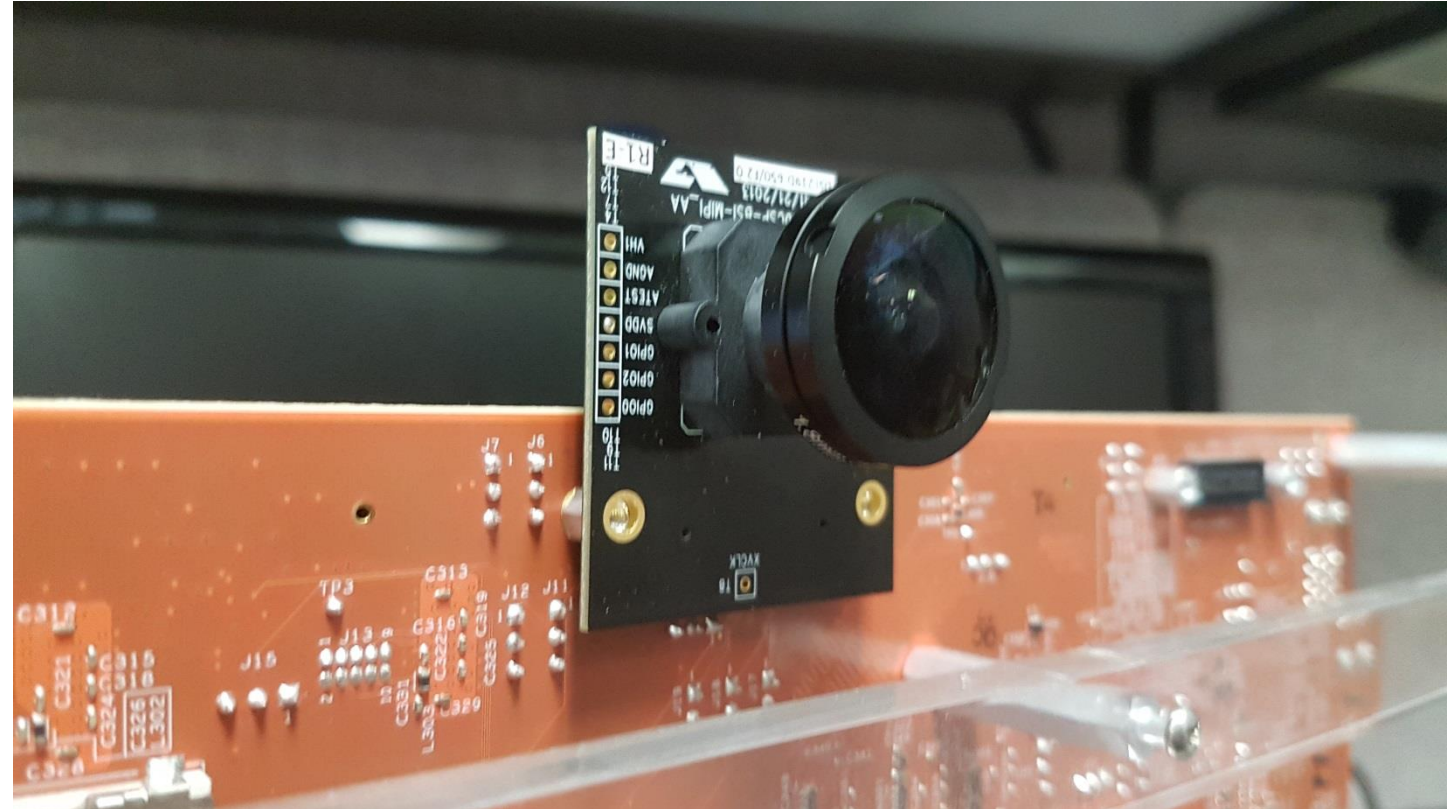
Camera configurations

- Another NXP-endorsed camera module is the OV10635/10640 with MAXIM 9271 Serializer, paired with the MAXIM 9286 Deserializer (both pictured). This camera set requires the optional 12V to be enabled.

- To prepare to use the MAX9271/86 Ser/Des setup, first ensure power is off and unplugged from the board. Then, choose between MIPI 0 or 1 and configure only J7 or J5 respectively to 1&2 to select 12V. Then, set jumpers J6 or J4 to 1&2 to enable optional voltage.

- Lastly, confirm that the MAX9286 deserializer board is configured to use board power by setting its jumper JU4 to the position shown (For Rev A deserializer boards). For other revisions, refer to deserializer schematic to find required configuration.

- Once all of these are set and cameras are connected, power can be turned on. Be sure to power off before removing cameras or components.
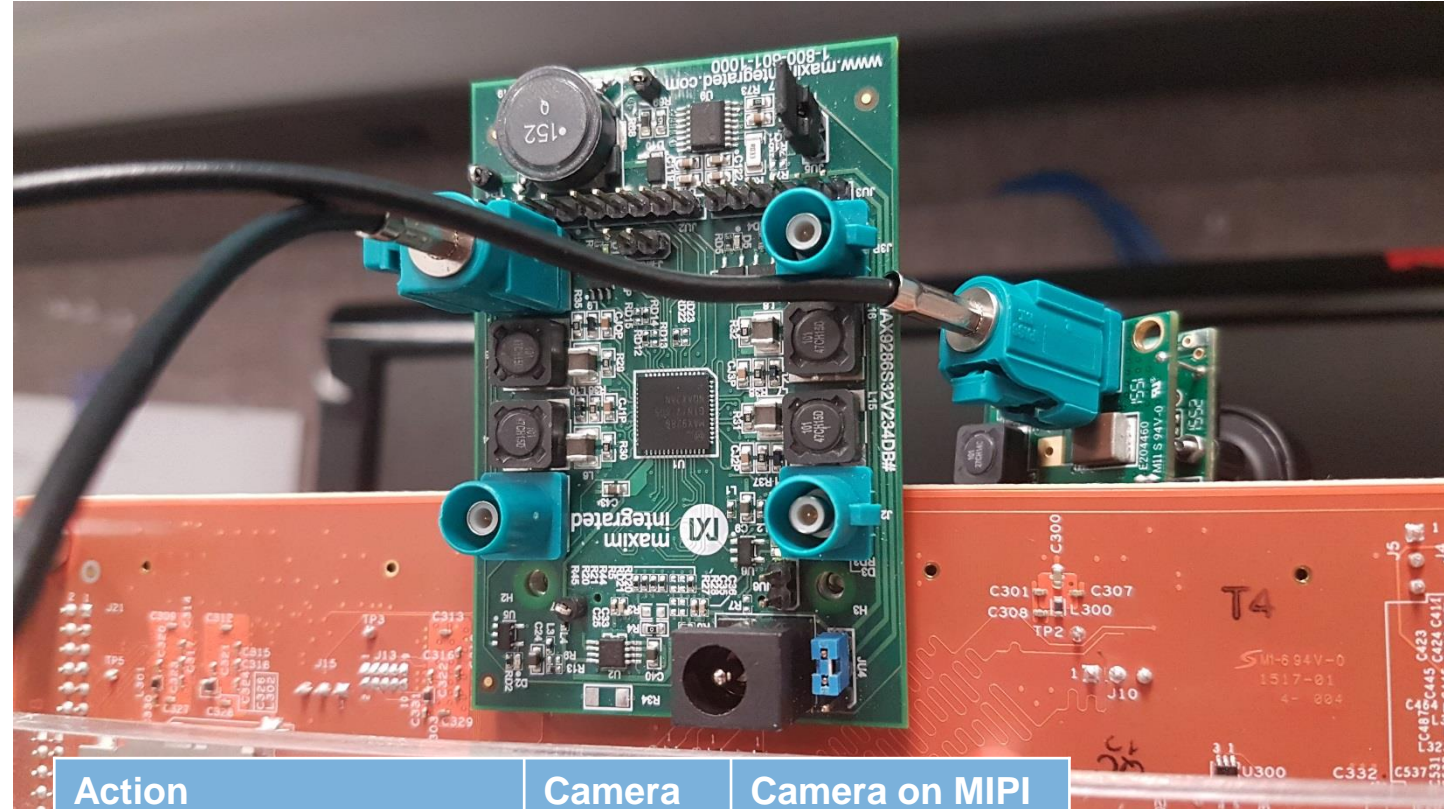
Action	Camera on MIPI 0	Camera on MIPI 1
Set to 12V	J7=1&2	J5=1&2
Enable voltage	J6=1&2	J4=1&2
Disable voltage	J6=2&3	J4=2&3

RCON Table

Block 1

	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1
RCON Pins	RCON31	RCON30	RCON29	RCON28	RCON27	RCON26	RCON25	RCON24
QSPI	BOOT_CA53 1 - Boot from CA53[0] 0 - Boot from CM4							
SD/eSD		MMC_DLL_DLY[6:0]						
MMC/eMMC								
Reserved								

Block 2

	PC0	PB15	PB14	PB13	PB12	PB11	PB10	
RCON Pins	RCON23	RCON22	RCON21	RCON20	RCON19	RCON18	RCON17	
QSPI								
SD/eSD	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	XOSC Transconductance (Serial Boot) XOSC[2]	Wait Period 000: No Wait 74 Clock Cycles 001: 50ms 010:100ms 011:200ms 100:300ms 101:Reserved 101: Reserved 111:500ms (max) (only for SD/eSD/MMC/eMMC Configuration)			XOSC Transconductance (Serial Boot) XOSC[1]	
MMC/eMMC								
Reserved								

Block 3

	PB9	PB8	PB7	PB6	PB5	PB3	PB2	PB1
RCON Pins	RCON16	RCON15	RCON14	RCON13	RCON12	RCON11	RCON10	RCON9
QSPI	Reserved						TDH(Serial flash Data In hold time) 00:Data aligned at PosEdge 01:Data aligned with 2X Clock 10: Data aligned with 4X Clock	
SD/eSD	SD Calibration Step '00' - 1		SD Bus Width: 0 - 1-bit 1 - 4-bit	XOSC Transconductance (Serial Boot) XOSC[0]			DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eSD	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC
MMC/eMMC	MMC Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.				eMMC 4.4 - RESET TO PRE-IDLE STATE 1- Enable 0 - Disable	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC
Reserved								

Block 4

	PB0	PA15	PA14	PA13	PA12	PA11	PA9	PA8	PA7
RCON Pins	RCON8	RCON7	RCON6	RCON5	RCON4	RCON3	RCON2	RCON1	RCON0
QSPI	Override Pad Settings (using PAD_SETTINGS value)	0	0		OTFAD Key Blob 0 - Disable 1 - Eanble	OTFAD Key Scramble 0- Disable 1- Enable	OTFAD Key Blob CRC 0- Disable 1- Enable	QSPI MODE 00: QSPI Mode 01: RPC Mode 1x: Reserved	
SD/eSD	Override Pad Settings (using PAD_SETTINGS value)	1	0	SD VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	Override Pad Settings (using PAD_SETTINGS value)	1	1	SD VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
Reserved		0	1						

See schematics for RCON to BOOTCFG switch mapping.

Note: The Linux BSP has only been validated on certain configurations. Please see the User Manual for more information on validated settings.