

MPC5775K EVB User Guide

by: Andrew Robertson
Applications Engineering
Freescale EKB, UK

1 Introduction

This user's manual details the setup and configuration of the Freescale MPC5775K Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the MPC57xx family of microprocessors, and to facilitate hardware and software development.

At the time of writing this document, the MPC57xx family will consist of the 55nm safety and powertrain devices. For the latest product information, please speak to your Freescale representative or consult the MPC57xx website at www.freescale.com.

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

1.1 List of Acronyms

Table 17 provides a list and description of acronyms used throughout this document.

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Table Of Contents

| | |
|--|----|
| MPC5775K EVB User Guide..... | 1 |
| 1 Introduction | 1 |
| 1.1 List of Acronyms | 2 |
| 1.2 Modular Concept | 2 |
| 1.3 Daughter Card Availability | 3 |
| 2 EVB Features | 3 |
| 3 Configuration | 4 |
| 3.1 Power Supply Configuration | 5 |
| 3.2 CAN Configuration..... | 7 |
| 3.3 RS232 Configuration | 9 |
| 3.4 LIN Configuration..... | 10 |
| 3.5 FlexRAY Configuration | 11 |
| 3.6 Ethernet Configuration..... | 12 |
| 3.7 Motherboard | 13 |
| 4 Configuration – Daughter card..... | 14 |
| 4.1 MCU Power | 15 |
| 4.2 Reset Circuit..... | 17 |
| 4.3 MCU External Clock Circuit | 18 |
| 4.4 JTAG | 18 |
| 4.5 Nexus Aurora | 19 |
| 4.6 Serial Interprocessor Interface (SIPI) | 19 |
| 4.7 Test Points - Daughter Card | 20 |
| 4.8 Daughter Card - Standalone Use | 19 |
| 4.9 Configure External VREG Mode | 20 |
| 4.10 Configure Internal VREG Mode | 20 |
| 5 Board Interface Connector..... | 23 |
| 6 Default Jumper Summary Table | 30 |
| 6.1 Default Jumper Table - Motherboard | 30 |
| 6.2 User Area..... | 34 |
| 6.3 Known Bugs | 30 |

Table 17. List of Acronyms

| Acronym | Description |
|----------------|---|
| 1.25V_SR | Supply voltage from the 1.25V switching regulator |
| 3.3V_SR | Supply voltage from the 3.3V switching regulator |
| 5V_LR | Supply voltage from the 5.0V linear regulator |
| 5V_SR | Supply voltage from the 5.0V switching regulator |
| ADC | Analog-to-Digital converter |
| RESET_B | External signal reset |
| EVB | Evaluation board |
| FEC | Fast ethernet controller module |
| GND | Ground |
| HV | High voltage (3.3V and/or 5V) |
| LED | Light emitting diode |
| LV | Low voltage (1.25V) |
| MCU | Microcontroller |
| OSC | Oscillator |
| P12V | 12V EVB supply power domain |
| VREG_POR_B | Power-on reset |
| PWR | Power |
| RX | Receive |
| SIPI | Serial Interprocessor Interface |
| TBD | To be defined |
| TX | Transmit |
| VSS | Ground |

1.2 Modular Concept

For maximum flexibility and simplicity, the EVB has been designed as a modular development platform. The EVB main board does not contain an MCU. Instead, the MCU is fitted to an MCU daughter card (occasionally referred to as an adapter board). This approach means that the same EVB platform can be used for multiple packages and MCU derivatives within the MPC57xx family. High density connectors provide the interface between the EVB and MCU daughter cards as shown in the diagram below. See chapter 3.7 for more details on the daughter cards and 4.7 for more details on the interface connectors.

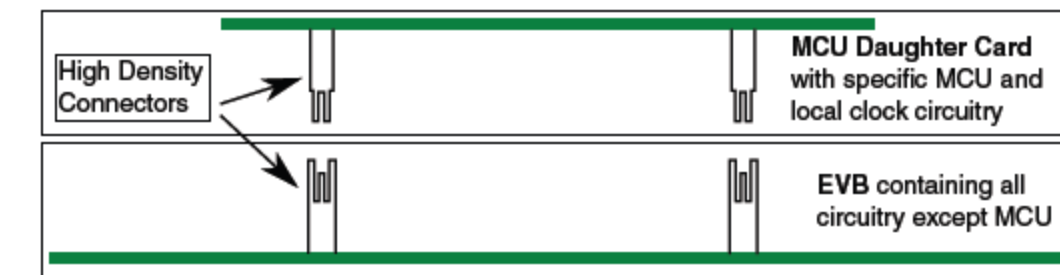


Figure 2. Modular concept – Mother board and MCU daughter card

Please consult the MPC57xx website at www.freescale.com or speak to your Freescale representative for more details on the availability of MCU daughter cards.

NOTE

For details on your specific daughter card, please consult the instructions included with the daughter card.

The EVB is designed to use the motherboard and the daughter card in conjunction. However, it is possible to use the daughter cards standalone.

1.3 Daughter Card Availability

A number of compatible daughter cards are available for the motherboard across a number of devices. Table 18 gives an overview of daughter cards that can be used with MPC57xx motherboard and associated devices, package sizes and part numbers.

Table 18. Daughter card overview

| Daughter card number | Device | Package | Socket | Nexus |
|----------------------|----------|---------|--------|-------|
| MPC5775K-356DS | MPC5775K | 356BGA | Yes | Yes |
| | | | | |

All daughter cards will be similar in design and concept. For details on the daughter cards please refer to chapter 3.7.

2 EVB Features

The EVB system consists of a motherboard and a daughter card, both with distinct features.

The **mother board** provides the following key features:

- Support provided for different MPC57xx MCUs by utilising MCU daughter cards
- Single 12V external power supply input with four on-board regulators providing all of the necessary EVB and MCU voltages; Power supplied to the EVB via a 2.1mm barrel style power jack or a 2-way level connector; 12V operation allows in-car use if desired
- Master power switch and regulator status LEDs

- Two 240-way high-density daughter card expansion connectors allowing connection of the MCU daughter card or a custom board for additional application specific circuitry
- All MCU signals readily accessible at a port-ordered group of 0.1" pitch headers
- RS232/SCI physical interface and standard DB9 female connector
- FlexRAY interface
- LINFlexD interface
- 2 CAN interfaces, one configurable to be connected to one out of two CAN modules, and one connected to a dedicated third CAN module
- Ethernet interface
- Variable resistor, driving between 5V and ground
- 4 user switches and 4 user LEDs, freely connectable
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB

The **daughter cards** provide the following features:

- MCU (soldered or through a socket)
- Flexible MCU clocking options allow provision of an external clock via SMA connector or 40MHz EVB clock oscillator circuit. Jumpers on the daughter card allow selection between these external clocks. SMA connector on CLKIN signal for easy access.
- User reset switch with reset status LEDs
- Standard 14-pin JTAG debug connector and 34-pin Nexus Aurora connector
- 10-pin Serial Interprocessor Interface (SIPI) connector
- Liberal scattering of ground and test points (surface mount loops) placed throughout the EVB

NOTE

To alleviate confusion between jumpers and headers, all EVB jumpers are implemented as 2mm pitch whereas headers are 0.1inch (2.54mm). This prevents inadvertently fitting a jumper to a header.

CAUTION

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board. Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

3 Configuration

This section details the configuration of each of the EVB functional blocks.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

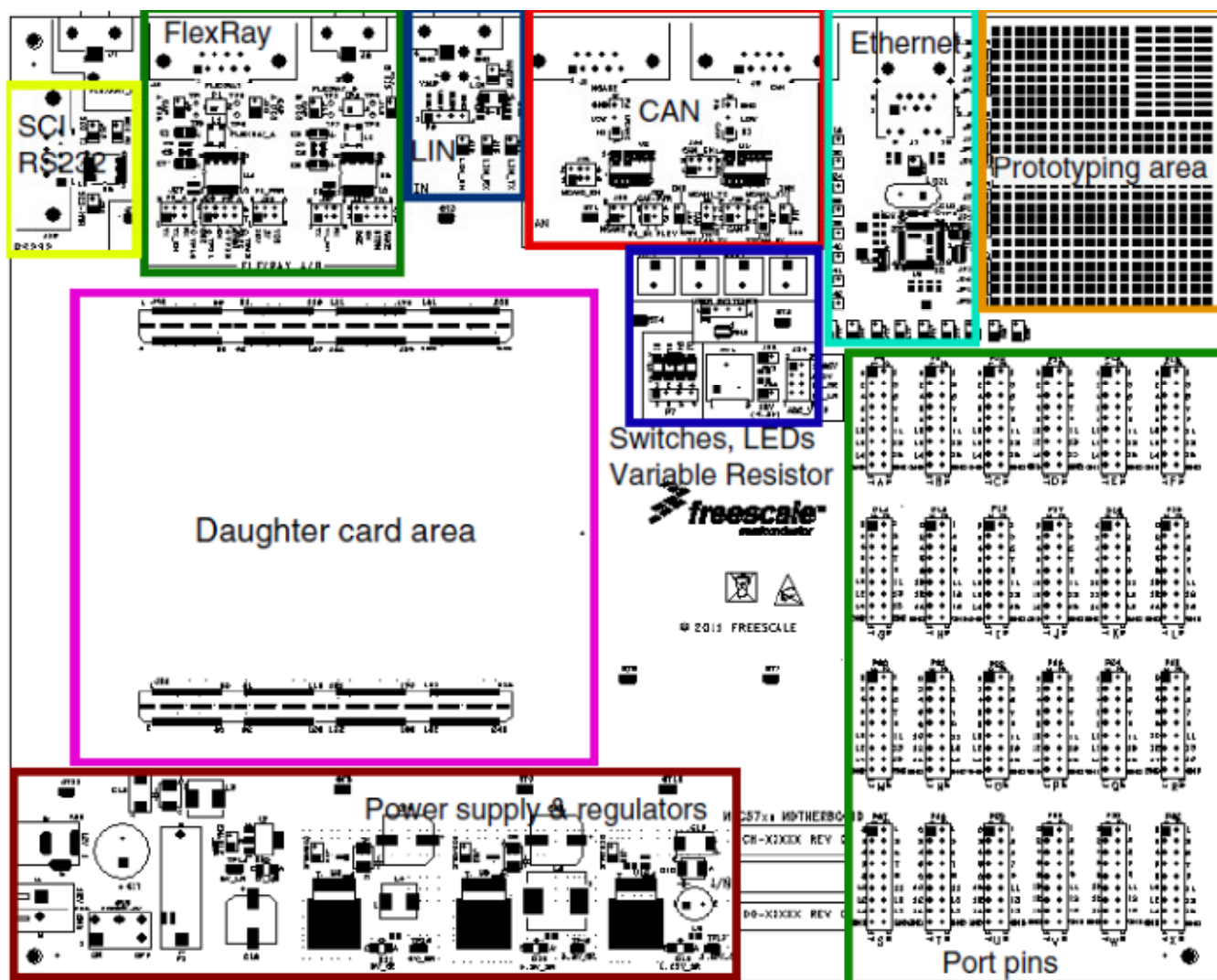


Figure 3. EVB Functional Blocks

3.1 Power Supply Configuration

The EVB requires an external power supply voltage of 12V DC, minimum 1A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using three switching regulators to provide the necessary EVB and MCU operating voltages of 5.0V, 3.3V and 1.25V, and one 5V linear regulator for the ADC supplies and references.

For flexibility there are two different power supply input connectors on the motherboard as detailed below. There is also a power supply option on the daughter card to use the daughter card in standalone mode. Please refer to section 4.1.2 for details on the daughter card power input.

3.1.1 Motherboard Power Supply Connectors

2.1mm Barrel Connector – P28:



Figure 4. 2.1mm Power Connector

2-Way Lever Connector – P32:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

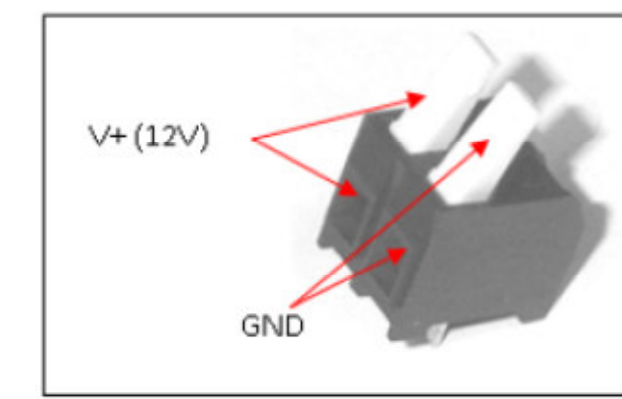


Figure 5. 2-Lever Power Connector

3.1.2 Regulator Power Jumpers

There are four power regulator circuits on the MPC57xx motherboard that supply the required voltages to operate the MCUs:

- 1.25V_SR: 1.25V switching regulator to supply the core voltage
- 5V_SR: 5V switching regulator to supply the power management controller, I/O and peripherals
- 3.3V_SR: 3.3V switching regulator for Ethernet, FlexRAY, debug and I/O
- 5V_LR: 5V linear regulator for ADC supply and reference

All of the regulators have the option of being disabled/enabled if they are not required. By default (jumpers are off), all of the switching regulators are enabled and the 5V linear regulator is disabled. The regulators can be enabled individually by the following jumper settings:

- Connecting J57 enables the 5V linear regulator
- Disconnecting J58 enables the 5V switching regulator
- Disconnecting J59 enables the 3.3V switching regulator
- Disconnecting J60 enables the 1.25V switching regulator

The regulators supply power to the daughter cards through the board connector. The individual selection and configuration of the MCU supplies are done on the daughter cards.

NOTE

Not all the supported daughter card MCUs require all the supplies to be switched on. Please refer to the individual daughter card user guide for details.

3.1.3 Power Switch, Status LEDs and Fuse

The main power switch (slide switch SW5) can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from connector P33) will turn the EVB on
- Moving the slide switch to the left (towards connector P33) will turn the EVB off

When power is applied to the EVB, four green power LEDs adjacent to the voltage regulators show the presence of the supply voltages as follows:

- LED D9 – Indicates that the 5.0V linear regulator is enabled and working correctly
- LED D11 – Indicates that the 5.0V switching regulator is enabled and working correctly
- LED D12 – Indicates that the 3.3V switching regulator is enabled and working correctly
- LED D13 – Indicates that the 1.25V switching regulator is enabled and working correctly

If no LED is illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW5 is in the “OFF” position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a 20mm 1.5A fast blow fuse.

3.2 CAN Configuration

The EVB has two NXP TJA1041T high speed CAN transceivers and two female standard DB9 connectors to provide physical CAN interfaces for the MCU.

The pinout of the DB9 connector (J2) is shown in Figure 5.

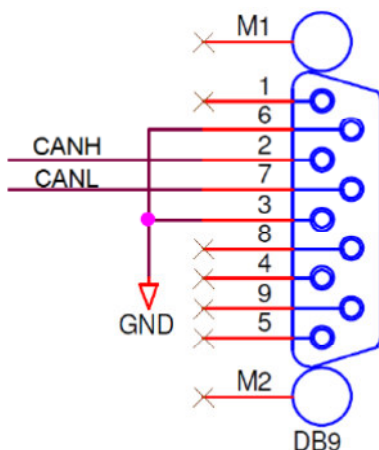


Figure 6. CAN DB9 connector pinout

For flexibility, the CAN transceiver I/Os are also connected to two standard 0.1" connectors (P4 and P5) at the top side of the PCB. The pin-out for these connectors is shown in Figure 7.

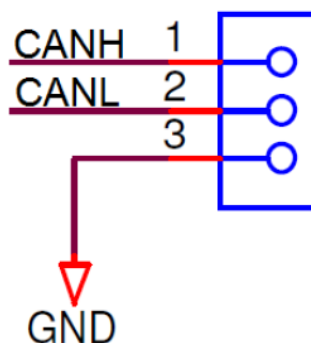


Figure 7. CAN 3pin header interface connector

By default the CAN interfaces are not enabled. To enable the CAN interfaces the jumpers detailed in Table 19 need to be placed.

Table 19. CAN control jumpers

| Jumper | Label | Description |
|--------|---------|---|
| J23 | CAN2_EN | PHY U2 configuration 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V |
| J32 | CAN2 | 1-2: PHY TX to MCU 3-4: PHY RX to MCU |
| J33 | CAN-PWR | 1-2: 5.0V_SR to PHY U2 V _{CC} 3-4: 12V to PHY U2 V _{BAT} |
| J34 | - | PHY U2 signal out 1: ERR 2: INH |
| J21 | CAN_EN | PHY U1 configuration 1-2: WAKE to GND 3-4: STB to 5V |

| Jumper | Label | Description |
|--------|-------|--|
| | | 5-6: EN to 5V |
| J35 | CAN | 1-2: 5.0V _{SR} to PHY U1 V _{CC} 3-4: 12V to PHY U1 V _{BAT} |
| J37 | CAN | PHY U1 TX to MCU 1-2: TTCAN TX 2-3: MCAN1 TX |
| J38 | - | PHY U1 RX to MCU 1-2: TTCAN RX 2-3: MCAN1 RX |
| J36 | - | PHY U1 signal out 1: ERR 2: INH |

3.3 RS232 Configuration

Female DB9 connector J19 and MAX3221E RS232 transceiver device provide a physical RS232 interface, allowing a direct RS232 connection to a PC or terminal.

The pin-out of these connectors is detailed in Figure 8. Note that hardware flow control is not supported on this implementation.

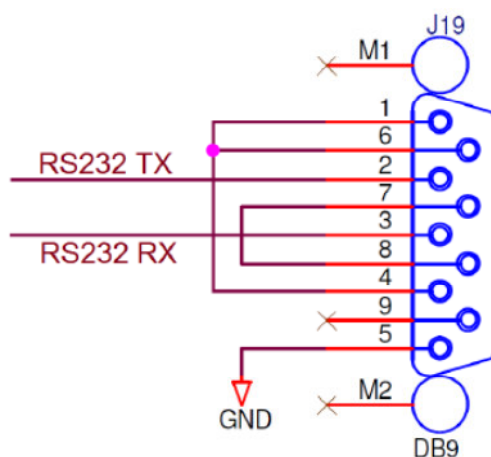


Figure 8. RS232 physical interface connector

On default the RS232 interface is not enabled. To enable the RS232 interface the user needs to place the jumpers detailed in Table 20.

Table 20. RS232 control jumpers

| Jumper | Label | Description |
|--------|---------|----------------------|
| J13 | SCI TX | TX enable |
| J14 | SCI RX | RX enable |
| J25 | SCI_PWR | Transceiver power on |

3.4 LIN Configuration

The EVB is fitted with a Freescale MC33661F LIN transceiver (U50) and two different style connectors: A standard LIN Molex connector (J14) at the edge of the board and a standard 0.1" connector (P3).

The pin-out of the Molex connector J4 is shown in Figure 9.

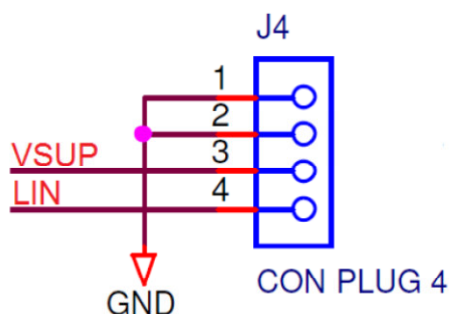


Figure 9. LIN Molex connector

For flexibility, the LIN transceiver is also connected to a standard 0.1" connector (P3) at the top side of the PCB as shown in Figure 10. For ease of use, the 12V EVB supply is fed to pin1 of P3 and the LIN transceiver power input to pin2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of connector P3 using a 0.1" jumper shunt.

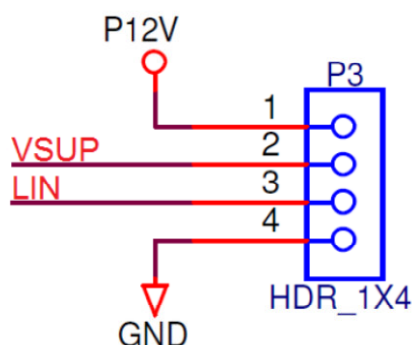


Figure 10. LIN 4pin header interface connector

By default the LIN interface is not enabled. To enable the LIN interface the jumpers detailed in Table 21 need to be placed.

Table 21. LIN control jumpers

| Jumper | Label | Description |
|--------|--------|----------------------|
| J15 | LIN_EN | LIN PHY (U50) enable |
| J16 | LIN_RX | LIN RX enable |
| J17 | LIN_TX | LIN TX enable |

3.5 FlexRAY Configuration

The EVB is fitted with two FlexRAY transceivers, a female DB9 connector (for both transceivers) and two alternative connectors. Jumpers J27 and J30 are provided to route the respective MCU signals to the physical interfaces.

The pin-out of the DB9 connector (J2) is shown in Figure 11.

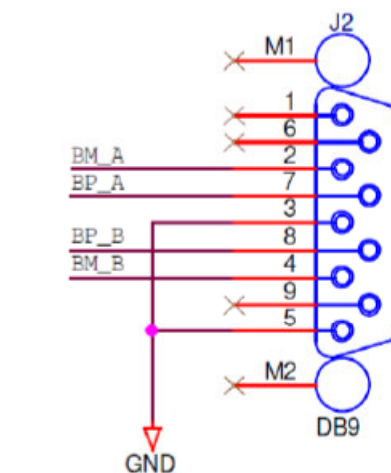


Figure 11. FlexRAY DB9 connector pinout

For flexibility, the FlexRAY transceiver is also connected to two FlexRAY connectors (P1 & P2) and two 2pin Molex connectors (J1 & J3, not populated by default) at the top side of the EVB. Figure 12 shows the connections for both types of connectors.

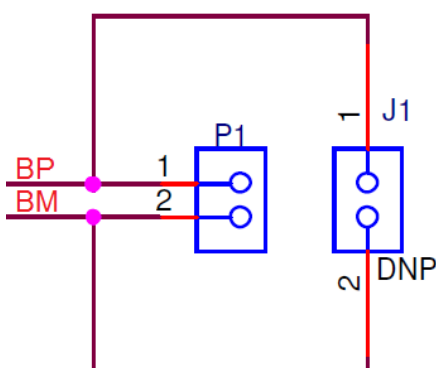


Figure 12. FlexRAY alternative connector pin-outs

By default the FlexRAY interface is not enabled. To enable the FlexRAY interface the jumpers detailed in Table 22 need to be placed.

Table 22. FlexRAY control jumpers

| Jumper | Label | Description |
|--------|--------|--|
| J29 | FR_PWR | FlexRay transceiver VIO selection 1-2: 12V to V _{BAT} 3-4: 5V _{SR} to V _{CC} and V _{BUF} 5-6: 3.3V _{SR} to V _{IO} |

| Jumper | Label | Description |
|--------|-------|--|
| J27 | FR_A | 1-2: PHY U4 TX to MCU 3-4: PHY U4 TXEN to MCU 5-6: PHY U4 RX to MCU |
| J28 | FR_A | PHY U4 configuration: 1-2: 3.3V (V _{IO}) to BGE 3-4: 3.3V (V _{IO}) to EN 5-6: 3.3V (V _{IO}) to STBY 7-8: GND to WAKE |
| J30 | FR_B | 1-2: PHY U5 TX to MCU 3-4: PHY U5 TXEN to MCU 5-6: PHY U5 RX to MCU |
| J31 | FR_B | PHY U5 configuration: 1-2: 3.3V (V _{IO}) to BGE 3-4: 3.3V (V _{IO}) to EN 5-6: 3.3V (V _{IO}) to STBY 7-8: GND to WAKE |

3.6 Ethernet Configuration

The EVB is fitted with a standard RJ45 Ethernet connector (J7) and a DP83848C 10/100 Ethernet transceiver (U6).

By default the Ethernet interface is not enabled. To enable the Ethernet interface the jumpers detailed in Table 23 need to be placed.

Table 23. Ethernet control jumpers

| Jumper | Description |
|--------|---|
| J22 | PHY power on (jumper placed on default) |
| J18 | RXCLK |
| J20 | CRS_LEDCFG |
| J24 | RXER_MDIXEN |
| J26 | RXDV_MIIMODE |
| J39 | RXD0_PHYAD1 |
| J40 | RXD1_PHYAD1 |
| J41 | RXD2_PHYAD2 |
| J42 | RXD3_PHYAD3 |
| J44 | COL_PHYAD0 |
| J45 | TXEN |
| J46 | TXCLK |
| J47 | TXD0 |
| J48 | TXD1 |
| J49 | TXD2 |
| J50 | TXD3_SNIMODE |

MPC5775K EVB Users Manual, Rev2.0

| Jumper | Description |
|--------|-------------|
| J51 | MDC |
| J52 | MDIO |

3.7 Motherboard

A number of test points of different shape and functionality is scattered around the EVB to allow easy access to MCU and reference signals. This chapter summarizes and describes the available test points. Motherboard test points are listed and detailed in Table 24.

Table 24. Test points - motherboard

| Signal | TP name | Shape | Description |
|----------|---------|---------------|--------------------|
| GND | GT1 | Hook | Ground reference |
| GND | GT2 | Hook | Ground reference |
| GND | GT3 | Hook | Ground reference |
| GND | GT4 | Hook | Ground reference |
| GND | GT5 | Hook | Ground reference |
| GND | GT6 | Hook | Ground reference |
| GND | GT7 | Hook | Ground reference |
| GND | GT8 | Hook | Ground reference |
| GND | GT9 | Hook | Ground reference |
| GND | GT10 | Hook | Ground reference |
| GND | GT11 | Hook | Ground reference |
| 1.25V_SR | JP1 | User Area Pin | 1.25V_SR reference |
| 1.25V_SR | JP2 | User Area Pin | 1.25V_SR reference |
| 1.25V_SR | JP3 | User Area Pin | 1.25V_SR reference |
| 1.25V_SR | JP4 | User Area Pin | 1.25V_SR reference |
| 3.3V_SR | JP5 | User Area Pin | 3.3V_SR reference |
| 3.3V_SR | JP6 | User Area Pin | 3.3V_SR reference |
| 3.3V_SR | JP7 | User Area Pin | 3.3V_SR reference |
| 3.3V_SR | JP8 | User Area Pin | 3.3V_SR reference |
| 5V_SR | JP9 | User Area Pin | 5V_SR reference |
| 5V_SR | JP10 | User Area Pin | 5V_SR reference |

| Signal | TP name | Shape | Description |
|-----------|---------|---------------|--------------------|
| 5V_SR | JP11 | User Area Pin | 5V_SR reference |
| 5V_SR | JP12 | User Area Pin | 5V_SR reference |
| GND | JP13 | User Area Pin | Ground reference |
| GND | JP14 | User Area Pin | Ground reference |
| GND | JP15 | User Area Pin | Ground reference |
| GND | JP16 | User Area Pin | Ground reference |
| 5V_SR | TP15 | Hook | 5V_SR reference |
| 5V_LR | TP14 | Hook | 5V_LR reference |
| 3.3V_SR | TP16 | Hook | 3.3V_SR reference |
| 1.25V_SR | TP17 | Hook | 1.25V_SR reference |
| FRA-INH2 | TP5 | Pad | FlexRAY |
| FRA-INH1 | TP1 | Pad | FlexRAY |
| FRA-ERRN | TP2 | Pad | FlexRAY |
| FRA-RXEN | TP6 | Pad | FlexRAY |
| FRB-INH2 | TP7 | Pad | FlexRAY |
| FRB-INH1 | TP3 | Pad | FlexRAY |
| FRB-ERRN | TP4 | Pad | FlexRAY |
| FRB-RXEN | TP8 | Pad | FlexRAY |
| FR_DBG0 | TP10 | Pad | FlexRAY debug0 |
| FR_DBG1 | TP11 | Pad | FlexRAY debug1 |
| FR_DBG2 | TP12 | Pad | FlexRAY debug2 |
| FR_DBG3 | TP13 | Pad | FlexRAY debug3 |
| FEC 25MHz | TP9 | Pad | Ethernet clock |

4 Configuration – Daughter card

This section details the configuration of each of the daughter card's functional blocks.

The daughter card has been designed with ease of use in mind and has been segmented into functional blocks as shown in Figure 13. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

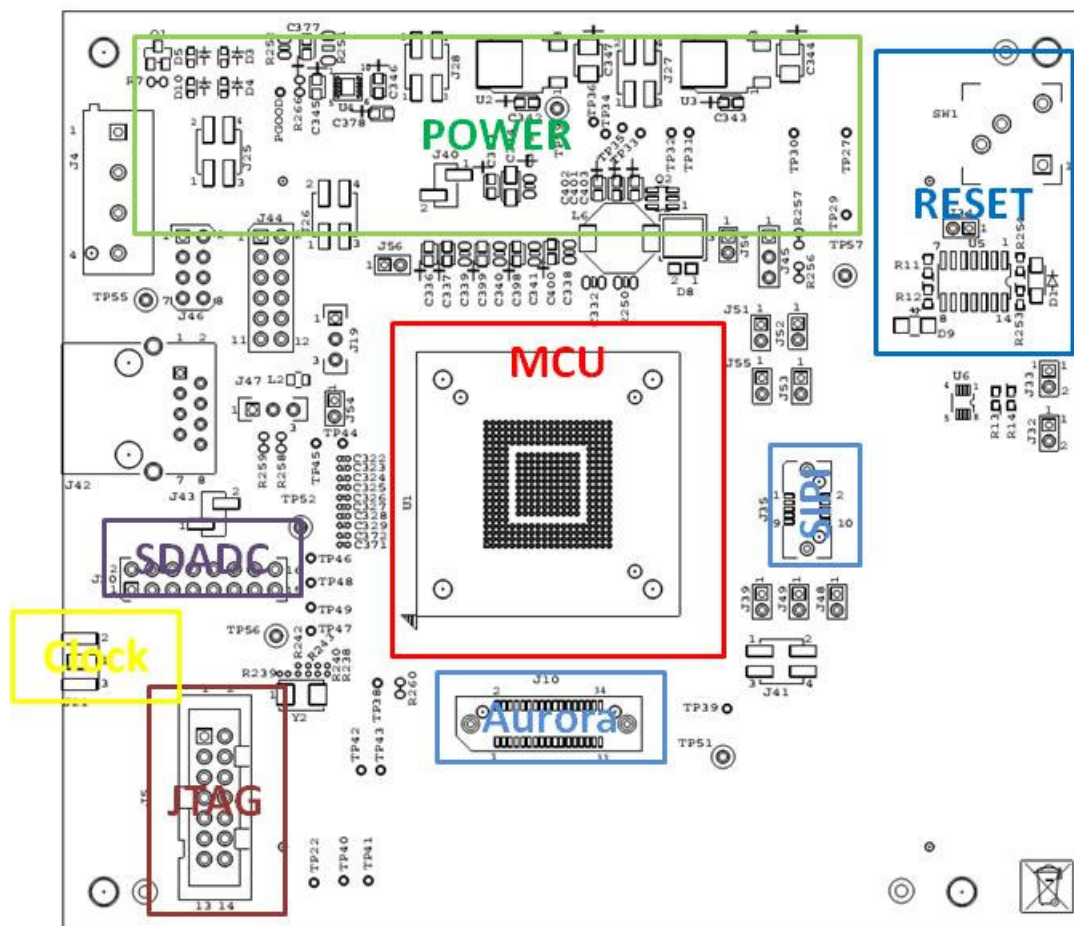


Figure 13. Daughter card - functional blocks

4.1 MCU Power

4.1.1 Supply Routing and Jumpers

The different MCU supply inputs are connected to the regulators on the motherboard through the interface connector. Figure 14 shows how the MCU power domains are connected to the regulators.

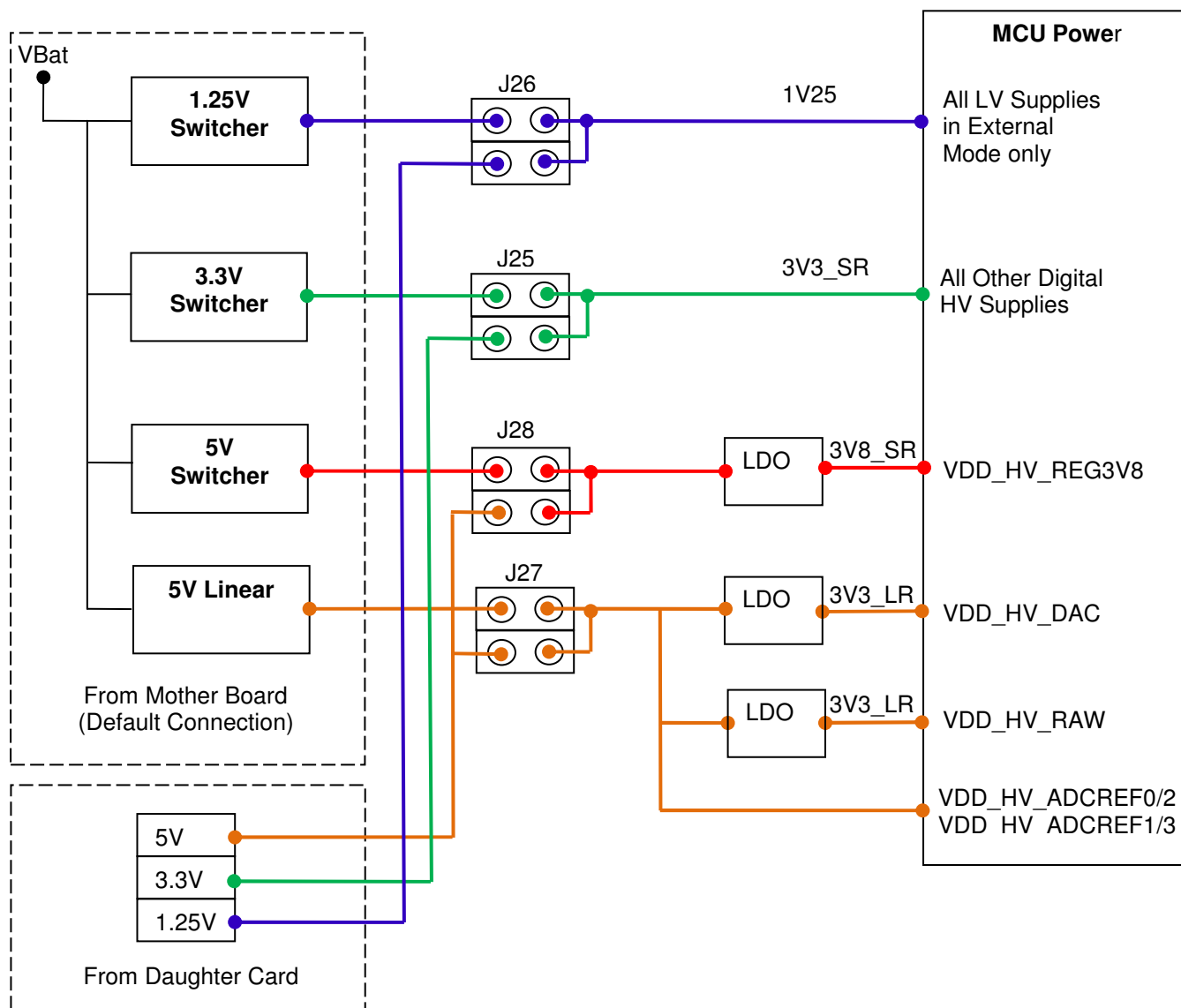


Figure 14. Daughter card power distribution

The connection of any power domain to a regulator has to be enabled by a dedicated jumper as described in Table 25.

Table 25. MCU power selection jumpers

| Jumper | Description |
|--------|--|
| J25 | Connects Digital HV supplies to 3.3V_SR |
| J26 | Connects Digital LV supplies to 1.25V_SR |
| J27 | Connects AFE Supply to 3.3V_LR via LDO |
| J28 | Connects AFE Supply to 3.8V_SR via LDO |

4.1.2 Daughter Card Standalone Power Input

A terminal power input is provided on the daughter card to enable use of the daughter card without the motherboard.

The connections of the power terminal are detailed in Figure 15.

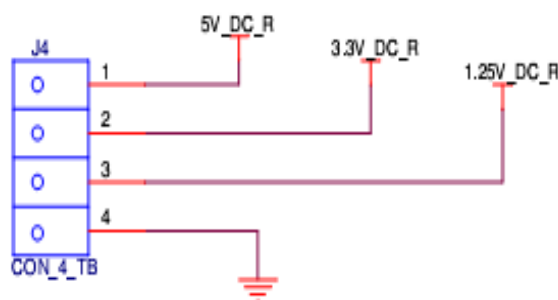


Figure 15. Terminal power input connections

NOTE

The power terminal does not connect to the 5.0V_LR power rail which is powered by the 5V linear regulator when used with the motherboard. This rail is powering the VDD_HV_DAC (DAC supply), VDD_HV_RAW (AFE supply) and VDD_HV_ADCCREFxx (ADC reference voltage). When using the daughter card standalone (without the motherboard) it is required to connect the 5.0V_LR and the 5.0V_SR rail in order for the microcontroller to come out of reset. Refer to section 4.8 for more information.

4.2 Reset Circuit

To enable standalone use the reset circuitry is placed on the daughter card. It consists of a reset switch that is connected to both reset pins, RESET_B and VREG_POR_B, via jumpers. It is also connected to the signal RST-SW that is connected to the motherboard to reset peripherals. Additionally LEDs are used to indicate the individual reset situations.

Due to the existence of chip internal low voltage detect (LVD) and high voltage detect (HVD) circuits the EVB does not provide external voltage monitoring.

The EVB reset circuit provides the following functionality: It is indicated if the device is in reset through the red LED D9. The reset switch SW1 can be used to reset the MCU when jumper J34 is set. The reset switch signal is connected to the MCU reset signals RESET_B (through jumper J32) and VREG_POR_B (through jumper J33) and the connections can be released by lifting the according jumper. Pushing the reset switch will also reset peripherals that are connected to the board reset signal RST-SW. LED D1 indicates when this signal is driven low by the reset switch.

Table 26. Reset circuit jumper settings

| Jumper | Description |
|--------|---|
| J32 | Connect reset switch circuit to RESET_B pin |

| Jumper | Description |
|--------|--|
| J33 | Connect reset switch circuit to VREG_POR_B pin |
| J34 | Connect reset switch (SW1) to reset circuit |

4.3 MCU External Clock Circuit

In addition to the internal 16 MHz oscillator, the MCU can be clocked by different external sources. The EVB system supports two possible MCU clock sources:

1. 40MHz crystal Y2 (The MCU only has a 40Mhz input)
2. External clock input to the EVB via the SMA connector (J21), driving the MCU EXTAL signal

The clock circuitry for the 40MHz crystal is shown in Figure 16.

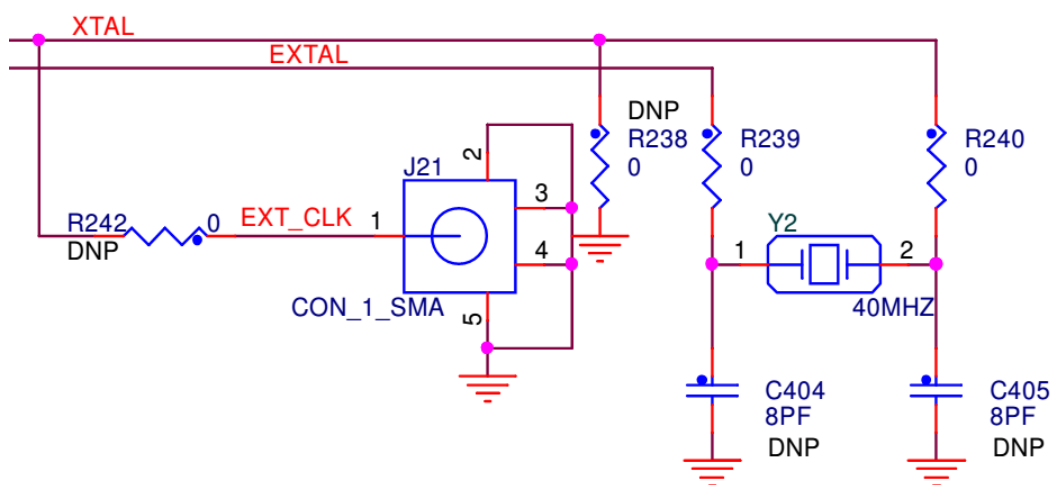


Figure 16. 40MHz crystal circuit

4.4 JTAG

The EVB is fitted with 14-pin JTAG debug connector. The following diagram shows the 14-pin JTAG connector pinout (0.1" keyed header).

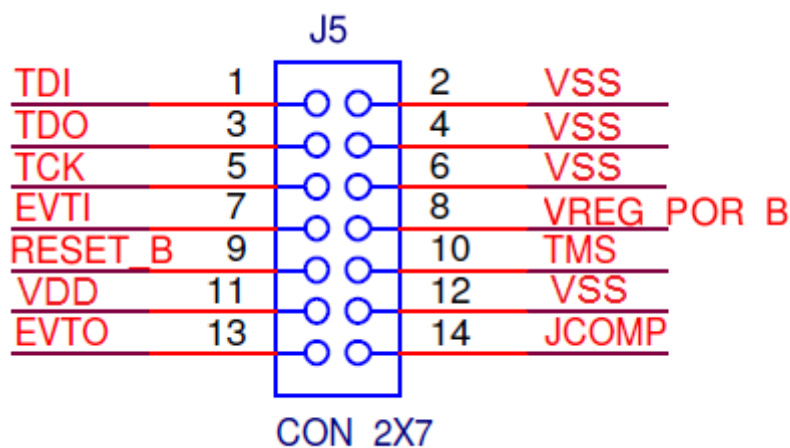


Figure 17. JTAG connector pinout

4.5 Nexus Aurora

Table 27 shows the pinout of the 34-pin Samtec connector for the MPC5775K.

Table 27. Aurora Trace connector pinout

| Pin No | Function | Pin No | Function |
|--------|-------------------|--------|------------------|
| 1 | TX0+ | 2 | VREF |
| 3 | TX0- | 4 | TCK/TCKC/DRCLK |
| 5 | VSS | 6 | TMS/TMSC/TxDataP |
| 7 | TX1+ | 8 | TDI/TxDataN |
| 9 | TX1- | 10 | TDO/RxDataP |
| 11 | VSS | 12 | JCOMP/RxDataN |
| 13 | TX2+ | 14 | EVTI1 |
| 15 | TX2- | 16 | EVTI0 |
| 17 | VSS | 18 | EVTO0 |
| 19 | TX3+ | 20 | VREG_POR_B |
| 21 | TX3- | 22 | RESET_B |
| 23 | VSS | 24 | VSS |
| 25 | TX4+ ¹ | 26 | CLK+ |
| 27 | TX4+ ¹ | 28 | CLK- |
| 29 | VSS | 30 | VSS |
| 31 | TX5+ ¹ | 32 | EVTO1/RDY |
| 33 | TX5+ ¹ | 34 | N/C |
| GND | VSS | GND | VSS |

4.6 Serial Interprocessor Interface (SIPI)

A dedicated SIPI interface connector is provided on the daughter card. For signal integrity the SIPI signals are not routed to the mother board. Test points are provided on the signals so they can be accessed if required to be used as a different function.

A 10pin Samtec connector (J20: ERF8-005-05.0-LDV-L-TR) is used for the SIPI interface. The pin-out of the connector is shown in **Error! No bookmark name given..**

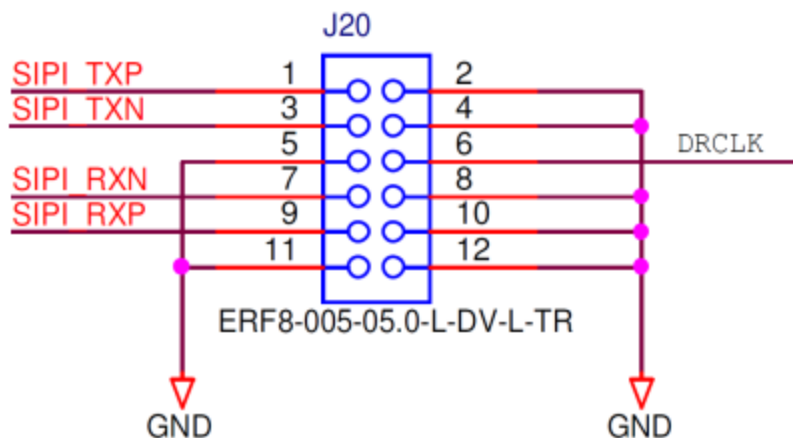


Figure 18. SIPI connector pinout

4.7 Test Points - Daughter Card

Daughter card test points are listed and detailed in Table 28.

Table 28. Test points – daughter card

| Signal | TP name | Shape | Description |
|--------|---------|-------|----------------------|
| VDD_LV | TP39 | Pad | 1V25 Reference |
| VDD_HV | TP44 | Pad | 3V3 HV DAC reference |
| VDD_HV | TP38 | Pad | 3V3 HV RAW Reference |
| VDD_LV | TP45 | Pad | 2V6 LV DAC Reference |
| VDD_LV | TP48 | Pad | 1V4 Radar Reference |
| VDD_LV | TP47 | Pad | 1V4 Radar Reference |
| VDD_LV | TP49 | Pad | 1V4 SDADC Reference |
| GND | TP57 | Pad | Ground Reference |
| GND | TP56 | Pad | Ground Reference |
| GND | TP55 | Pad | Ground Reference |
| GND | TP51 | Pad | Ground Reference |
| GND | TP52 | Pad | Ground Reference |
| VDD_HV | TP59 | Pad | 3V8 HV Reg Reference |
| GND | TP46 | Pad | AFE Filter Reference |

4.8 Configuring the Daughter Card for Standalone Use

It is possible to use the daughter cards without the motherboard to run code on the microcontroller. Power to the daughter cards must be supplied through the terminal power connector 'J4 – PWR_IN'. It is required to connect all three voltages (1.25V, 3.3V and 5V) and ground.

Jumpers positions must be moved to allow the J4 to supply the EVB.

J27 must move to position 1-2 (5V_DC_R)

J26 must move to position 1-2 (1.25V_DC_R)

J28 must move to position 1-2 (5V_DC_R)

J25 must move to position 1-2 (3.3V_DC_R)

4.9 Configuring External VREG Mode

Table 274 shows the jumper configuration for the EVB when in external VREG mode, this is the default position for the EVB when delivered.

| Jumper Number | Default position | Function |
|---------------|------------------|---|
| R302 | on | Resistor supplies 1.25v to the core |
| J45 | 2-3 | Determine internal or external Vreg Mode |
| J27 | 3-4 | 5.0v Linear supply from Motherboard for SAR ADC Reference voltage |
| J26 | 3-4 | 1.25v supply |
| J28 | 3-4 | 5.0v supply to create 3.8v for the AFE Regulator |
| J25 | 3-4 | 3.3v supply for the device |
| R304 | off | Resistor to supply to transistor |
| R303 | on | 3.8v supply to MCU |
| J49 | on | 1.25v PLL |
| J39 | on | 1.25v Reserved |
| J48 | on | 1.25v Aurora |
| J50 | on | 3.3v PWM |
| J52 | on | 3.3v PMU |
| J54 | on | 3.3v PDI |
| J51 | on | 3.3v FLA |
| J53 | on | 3.3v IO |
| J41 | 1-2 3-4 | ACD Ref |
| J32 | on | Disable Reset |
| J33 | on | Disable Reset |
| J34 | on | Disable Reset |
| J43 | off | ETH (ENET) |
| J19 | 2-3 | VPP TEST (always GND) |
| | Headers | |
| J44 | off | CTE output |
| J46 | off | WGM output |
| J35 | off | SIPI Interface |

MPC5775K EVB Users Manual, Rev2.0

| | | |
|-----|-----|----------------|
| J5 | off | JTAG Interface |
| J20 | off | SD ADC output |
| J47 | off | DAC output |

4.10 Configuring Internal VREG Mode

Table 275 shows the jumper configuration for the EVB when in internal VREG mode. Only 2 jumper are required to be changed J55 and J45

| Jumper Number | Default position | Function |
|---------------|------------------|---|
| R302 | off | Resistor removes supplies 1.25v to the core |
| J45 | 1-2 | Determine internal or external Vreg Mode |
| J27 | 3-4 | 5.0v Linear supply from Motherboard for SAR ADC Reference voltage |
| J26 | 3-4 | 1.25v supply |
| J28 | 3-4 | 5.0v supply to create 3.8v for the AFE Regulator |
| J25 | 3-4 | 3.3v supply for the device |
| R304 | on | Resistor to supply to transistor |
| R303 | on | 3.8v supply to MCU |
| J49 | on | 1.25v PLL |
| J39 | on | 1.25v Reserved |
| J48 | on | 1.25v Aurora |
| J50 | on | 3.3v PWM |
| J52 | on | 3.3v PMU |
| J54 | on | 3.3v PDI |
| J51 | on | 3.3v FLA |
| J53 | on | 3.3v IO |
| J41 | 1-2 3-4 | ACD Ref |
| J32 | on | Disable Reset |
| J33 | on | Disable Reset |
| J34 | on | Disable Reset |
| J44 | off | CTE output |
| J46 | off | WGM output |
| J35 | off | SIPI Interface |
| J5 | off | JTAG Interface |
| J20 | off | SD ADC output |
| J43 | off | Reserved |
| J47 | off | DAC output |
| J19 | 2-3 | VPP TEST (always GND) |

5 Board Interface Connector

This chapter provides a useful cross reference to see the connection from the motherboard to the board interface connector, and what MCU pins are connected to the interface connector on the daughter card.

Table 29 lists all the connections to the board interface connector on both motherboard and daughter card. The table on the left lists the 240 connections for the first interface connector (J43), the table on the right lists the 240 connections for the second interface connector (J56):

- The column 'Motherboard' shows the motherboard connections to the interface connectors like power supply connections and user area port pins.
- The column 356 BGA shows the connections from the MCU pins to the interface connector on daughter card for the 356 BGA package. It is ensured that the MCU port pins are routed to the associated user area port pin on the motherboard. Some pins are multiplexed and can have different uses that can be determined from the device reference manual.
- Green fields indicate power signals, power signals are connected to all the appropriate pins on the MCU
- Red fields indicate MCU signals that are not connected to the motherboard through the interface connector (usually to retain signal integrity).
- Grey fields indicate MCU signals that have dedicated connections to the motherboard peripherals through the interface connector (such as the Ethernet, CAN, FlexRay and LIN connectors).
- Ground signals are not listed here. A solid ground connection is achieved through the middle bar of the interface connector.

Table 29. Board interface connector details

| Connector | Motherboard | 356 BGA | Connector | Motherboard | 356 BGA |
|-----------|-------------|------------|-----------|-------------|-----------------------|
| A-1 | 1.25V_SR | 1.25V_SR | B-240 | 1.25V_SR | 1.25V_SR |
| A-2 | 1.25V_SR | 1.25V_SR | B-239 | 1.25V_SR | 1.25V_SR |
| A-3 | 1.25V_SR | 1.25V_SR | B-238 | 1.25V_SR | 1.25V_SR |
| A-4 | 1.25V_SR | 1.25V_SR | B-237 | 1.25V_SR | 1.25V_SR |
| A-5 | PA0 | ADC0_AN[0] | B-236 | PB0 | ADC1_AN[0] |
| A-6 | PA1 | ADC0_AN[1] | B-235 | PB1 | ADC1_AN[1] |
| A-7 | PA2 | ADC0_AN[2] | B-234 | PB2 | ADC1_AN[2] |
| A-8 | PA3 | ADC0_AN[3] | B-233 | PB3 | ADC1_AN[3] |
| A-9 | PA4 | ADC0_AN[4] | B-232 | PB4 | ADC1_AN[4]/ADC3_AN[3] |
| A-10 | PA5 | ADC0_AN[5] | B-231 | PB5 | ADC1_AN[5]/ADC3_AN[4] |
| A-11 | PA6 | ADC0_AN[6] | B-230 | PB6 | ADC1_AN[6]/ADC3_AN[5] |
| A-12 | PA7 | ADC0_AN[7] | B-229 | PB7 | ADC1_AN[7]/ADC3_AN[6] |
| A-13 | PA8 | ADC0_AN[8] | B-228 | PB8 | ADC1_AN[8]/ADC3_AN[7] |
| A-14 | PA9 | NC# | B-227 | PB9 | ADC2_AN[0]/ADC3_AN[0] |
| A-15 | PA10 | CAN2_TXD | B-226 | PB10 | ADC2_AN[1]/ADC3_AN[1] |
| A-16 | PA11 | CAN2_RXD | B-225 | PB11 | ADC2_AN[2]/ADC3_AN[2] |

MPC5775K EVB Users Manual, Rev2.0

5 Board Interface Connector

| | | | | | |
|------|---------|-------------------------|-------|---------|----------|
| A-17 | PA12 | ADC0_AN[11]/ADC1_AN[11] | B-224 | PB12 | NC# |
| A-18 | PA13 | ADC0_AN[12]/ADC1_AN[12] | B-223 | PB13 | NC# |
| A-19 | PA14 | ADC0_AN[13]/ADC1_AN[13] | B-222 | PB14 | NC# |
| A-20 | PA15 | ADC0_AN[14]/ADC1_AN[14] | B-221 | PB15 | NC# |
| A-21 | 5.0V_SR | 5.0V_SR | B-220 | 5.0V_SR | 5.0V_SR |
| A-22 | 5.0V_SR | 5.0V_SR | B-219 | 5.0V_SR | 5.0V_SR |
| A-23 | 5.0V_SR | 5.0V_SR | B-218 | 5.0V_SR | 5.0V_SR |
| A-24 | 5.0V_SR | 5.0V_SR | B-217 | 5.0V_SR | 5.0V_SR |
| A-25 | PC0 | NC# | B-216 | PD0 | NC# |
| A-26 | PC1 | NC# | B-215 | PD1 | NC# |
| A-27 | PC2 | ETHERNET_0_MDIO | B-214 | PD2 | NC# |
| A-28 | PC3 | ETHERNET_0_MDC | B-213 | PD3 | NC# |
| A-29 | PC4 | NC# | B-212 | PD4 | NC# |
| A-30 | PC5 | NC# | B-211 | PD5 | NC# |
| A-31 | PC6 | NC# | B-210 | PD6 | NC# |
| A-32 | PC7 | NC# | B-209 | PD7 | NC# |
| A-33 | PC8 | CAN0_RXD | B-208 | PD8 | NC# |
| A-34 | PC9 | CAN0_TXD | B-207 | PD9 | NC# |
| A-35 | PC10 | ETHERNET_0_RX_CLK | B-206 | PD10 | NC# |
| A-36 | PC11 | NC# | B-205 | PD11 | NC# |
| A-37 | PC12 | ETHERNET_0_RX_D0 | B-204 | PD12 | LIN3_TXD |
| A-38 | PC13 | ETHERNET_0_RX_D1 | B-203 | PD13 | LIN3_RXD |
| A-39 | PC14 | ETHERNET_0_TX_EN | B-202 | PD14 | LIN1_TXD |
| A-40 | PC15 | ETHERNET_0_TX_D0 | B-201 | PD15 | LIN1_RXD |
| A-41 | 3.3V_SR | 3.3V_SR | B-200 | 3.3V_SR | 3.3V_SR |
| A-42 | 3.3V_SR | 3.3V_SR | B-199 | 3.3V_SR | 3.3V_SR |
| A-43 | 3.3V_SR | 3.3V_SR | B-198 | 3.3V_SR | 3.3V_SR |
| A-44 | 3.3V_SR | 3.3V_SR | B-197 | 3.3V_SR | 3.3V_SR |
| A-45 | PE0 | IIC0_DATA | B-196 | PF0 | NC# |
| A-46 | PE1 | CTU0_EXT_TGR | B-195 | PF1 | NC# |
| A-47 | PE2 | FCCU_F0 | B-194 | PF2 | NC# |
| A-48 | PE3 | FCCU_F1 | B-193 | PF3 | NC# |
| A-49 | PE4 | GPIO 98 | B-192 | PF4 | NC# |
| A-50 | PE5 | CAN1_TXD | B-191 | PF5 | NC# |
| A-51 | PE6 | LIN0_RXD | B-190 | PF6 | NC# |
| A-52 | PE7 | LIN0_TXD | B-189 | PF7 | NC# |
| A-53 | PE8 | WKUP_NMI | B-188 | PF8 | NC# |
| A-54 | PE9 | MC_CGL_CLK_OUT | B-187 | PF9 | NC# |
| A-55 | PE10 | SWG_ANAOUT | B-186 | PF10 | NC# |
| A-56 | PE11 | RST-SW | B-185 | PF11 | NC# |
| A-57 | PE12 | ETHERNET_0_TX_D1 | B-184 | PF12 | NC# |

5 Board Interface Connector

| | | | | | |
|------|----------|----------|-------|----------|----------------|
| A-58 | PE13 | NC# | B-183 | PF13 | NC# |
| A-59 | PE14 | NC# | B-182 | PF14 | NC# |
| A-60 | PE15 | NC# | B-181 | PF15 | NC# |
| A-61 | 1.25V_SR | 1.25V_SR | B-180 | 1.25V_SR | 1.25V_SR |
| A-62 | 1.25V_SR | 1.25V_SR | B-179 | 1.25V_SR | 1.25V_SR |
| A-63 | 1.25V_SR | 1.25V_SR | B-178 | 1.25V_SR | 1.25V_SR |
| A-64 | 1.25V_SR | 1.25V_SR | B-177 | 1.25V_SR | 1.25V_SR |
| A-65 | PG0 | NC# | B-176 | PH0 | NC# |
| A-66 | PG1 | NC# | B-175 | PH1 | NC# |
| A-67 | PG2 | NC# | B-174 | PH2 | NC# |
| A-68 | PG3 | NC# | B-173 | PH3 | FLEXRAY_TXD_B |
| A-69 | PG4 | NC# | B-172 | PH4 | FLEXRAY_TXEN_B |
| A-70 | PG5 | NC# | B-171 | PH5 | NC# |
| A-71 | PG6 | NC# | B-170 | PH6 | NC# |
| A-72 | PG7 | NC# | B-169 | PH7 | FLEXRAY_TXD_A |
| A-73 | PG8 | NC# | B-168 | PH8 | FLEXRAY_TXEN_A |
| A-74 | PG9 | NC# | B-167 | PH9 | FLEXRAY_CA_RX |
| A-75 | PG10 | NC# | B-166 | PH10 | FLEXRAY_CB_RX |
| A-76 | PG11 | NC# | B-165 | PH11 | NC# |
| A-77 | PG12 | NC# | B-164 | PH12 | NC# |
| A-78 | PG13 | NC# | B-163 | PH13 | NC# |
| A-79 | PG14 | CAN1_RXD | B-162 | PH14 | NC# |
| A-80 | PG15 | NC# | B-161 | PH15 | NC# |
| A-81 | 5.0V_SR | 5.0V_SR | B-160 | 3.3V_SR | 3.3V_SR |
| A-82 | 5.0V_SR | 5.0V_SR | B-159 | 3.3V_SR | 3.3V_SR |
| A-83 | 5.0V_SR | 5.0V_SR | B-158 | 3.3V_SR | 3.3V_SR |
| A-84 | 5.0V_SR | 5.0V_SR | B-157 | 3.3V_SR | 3.3V_SR |
| A-85 | PI0 | PDI_D0 | B-156 | PJ0 | PDI_HSYNC |
| A-86 | PI1 | PDI_D1 | B-155 | PJ1 | PDI_VSYNC |
| A-87 | PI2 | PDI_D2 | B-154 | PJ2 | PDI_CLK |
| A-88 | PI3 | PDI_D3 | B-153 | PJ3 | NC# |
| A-89 | PI4 | PDI_D4 | B-152 | PJ4 | NC# |
| A-90 | PI5 | PDI_D5 | B-151 | PJ5 | NC# |
| A-91 | PI6 | PDI_D6 | B-150 | PJ6 | NC# |
| A-92 | PI7 | PDI_D7 | B-149 | PJ7 | NC# |
| A-93 | PI8 | PDI_D8 | B-148 | PJ8 | NC# |
| A-94 | PI9 | PDI_D9 | B-147 | PJ9 | NC# |
| A-95 | PI10 | PDI_D10 | B-146 | PJ10 | NC# |
| A-96 | PI11 | PDI_D11 | B-145 | PJ11 | NC# |
| A-97 | PI12 | PDI_D12 | B-144 | PJ12 | NC# |
| A-98 | PI13 | PDI_D13 | B-143 | PJ13 | NC# |

5 Board Interface Connector

| | | | | | |
|-------|---------|-------------------|-------|---------|--------------|
| A-99 | PI14 | PDI_D14 | B-142 | PJ14 | NC# |
| A-100 | PI15 | PDI_D15 | B-141 | PJ15 | NC# |
| A-101 | NC# | NC# | B-140 | NC# | NC# |
| A-102 | NC# | NC# | B-139 | NC# | NC# |
| A-103 | NC# | NC# | B-138 | NC# | NC# |
| A-104 | NC# | NC# | B-137 | NC# | NC# |
| A-105 | PK0 | DSPI0_CS0 | B-136 | PL0 | ETIMER1_ETC0 |
| A-106 | PK1 | DSPI0_CS1 | B-135 | PL1 | ETIMER1_ETC1 |
| A-107 | PK2 | DSPI0_SCK | B-134 | PL2 | ETIMER1_ETC2 |
| A-108 | PK3 | DSPI0_SIN | B-133 | PL3 | ETIMER1_ETC3 |
| A-109 | PK4 | DSPI0_SOUT | B-132 | PL4 | ETIMER1_ETC4 |
| A-110 | PK5 | DSPI2_CS0 | B-131 | PL5 | ETIMER1_ETC5 |
| A-111 | PK6 | DSPI2_CS1 | B-130 | PL6 | ETIMER2_ETC0 |
| A-112 | PK7 | DSPI2_SCK | B-129 | PL7 | ETIMER2_ETC1 |
| A-113 | PK8 | DSPI2_SIN | B-128 | PL8 | ETIMER2_ETC2 |
| A-114 | PK9 | DSPI2_SOUT | B-127 | PL9 | NC# |
| A-115 | PK10 | NC# | B-126 | PL10 | NC# |
| A-116 | PK11 | NC# | B-125 | PL11 | NC# |
| A-117 | PK12 | NC# | B-124 | PL12 | NC# |
| A-118 | PK13 | NC# | B-123 | PL13 | NC# |
| A-119 | PK14 | ETHERNET_0_TX_CLK | B-122 | PL14 | NC# |
| A-120 | PK15 | ETHERNET_0_RX_D3 | B-121 | PL15 | NC# |
| A-121 | 5.0V_LR | | B-120 | 5.0V_LR | 5.0V_LR |
| A-122 | 5.0V_LR | | B-119 | 5.0V_LR | 5.0V_LR |
| A-123 | 5.0V_LR | | B-118 | 5.0V_LR | 5.0V_LR |
| A-124 | 5.0V_LR | | B-117 | 5.0V_LR | 5.0V_LR |
| A-125 | PM0 | ETHERNET_0_RX_DV | B-116 | PN0 | NC# |
| A-126 | PM1 | ETHERNET_0_RX_D2 | B-115 | PN1 | NC# |
| A-127 | PM2 | NC# | B-114 | PN2 | NC# |
| A-128 | PM3 | NC# | B-113 | PN3 | NC# |
| A-129 | PM4 | ETHERNET_0_TX_D2 | B-112 | PN4 | NC# |
| A-130 | PM5 | ETHERNET_0_TX_D3 | B-111 | PN5 | NC# |
| A-131 | PM6 | NC# | B-110 | PN6 | NC# |
| A-132 | PM7 | NC# | B-109 | PN7 | NC# |
| A-133 | PM8 | NC# | B-108 | PN8 | NC# |
| A-134 | PM9 | NC# | B-107 | PN9 | NC# |
| A-135 | PM10 | NC# | B-106 | PN10 | NC# |
| A-136 | PM11 | NC# | B-105 | PN11 | NC# |
| A-137 | PM12 | NC# | B-104 | PN12 | NC# |
| A-138 | PM13 | NC# | B-103 | PN13 | NC# |
| A-139 | PM14 | NC# | B-102 | PN14 | NC# |

5 Board Interface Connector

| | | | | | |
|-------|----------------|-------------|-------|----------|----------|
| A-140 | PM15 | NC# | B-101 | PN15 | NC# |
| A-141 | RST-SW | RST-SW | B-100 | NC# | NC# |
| A-142 | VDD_HV_IO_FLEX | 3.3v_SR_LDO | B-99 | NC# | NC# |
| A-143 | VDD_HV_IO_FLEX | 3.3v_SR_LDO | B-98 | NC# | NC# |
| A-144 | VDD_HV_IO_FLEX | 3.3v_SR_LDO | B-97 | NC# | NC# |
| A-145 | PO0 | NC# | B-96 | PP0 | NC# |
| A-146 | PO1 | NC# | B-95 | PP1 | NC# |
| A-147 | PO2 | NC# | B-94 | PP2 | NC# |
| A-148 | PO3 | NC# | B-93 | PP3 | NC# |
| A-149 | PO4 | NC# | B-92 | PP4 | NC# |
| A-150 | PO5 | NC# | B-91 | PP5 | NC# |
| A-151 | PO6 | NC# | B-90 | PP6 | NC# |
| A-152 | PO7 | NC# | B-89 | PP7 | NC# |
| A-153 | PO8 | NC# | B-88 | PP8 | NC# |
| A-154 | PO9 | NC# | B-87 | PP9 | NC# |
| A-155 | PO10 | NC# | B-86 | PP10 | NC# |
| A-156 | PO11 | NC# | B-85 | PP11 | NC# |
| A-157 | PO12 | NC# | B-84 | PP12 | NC# |
| A-158 | PO13 | NC# | B-83 | PP13 | NC# |
| A-159 | PO14 | NC# | B-82 | PP14 | NC# |
| A-160 | PO15 | NC# | B-81 | PP15 | NC# |
| A-161 | 1.25V_SR | 1.25V_SR | B-80 | 1.25V_SR | 1.25V_SR |
| A-162 | 1.25V_SR | 1.25V_SR | B-79 | 1.25V_SR | 1.25V_SR |
| A-163 | 1.25V_SR | 1.25V_SR | B-78 | 1.25V_SR | 1.25V_SR |
| A-164 | 1.25V_SR | 1.25V_SR | B-77 | 1.25V_SR | 1.25V_SR |
| A-165 | PQ0 | NC# | B-76 | PR0 | NC# |
| A-166 | PQ1 | NC# | B-75 | PR1 | NC# |
| A-167 | PQ2 | NC# | B-74 | PR2 | NC# |
| A-168 | PQ3 | NC# | B-73 | PR3 | NC# |
| A-169 | PQ4 | NC# | B-72 | PR4 | NC# |
| A-170 | PQ5 | NC# | B-71 | PR5 | NC# |
| A-171 | PQ6 | NC# | B-70 | PR6 | NC# |
| A-172 | PQ7 | NC# | B-69 | PR7 | NC# |
| A-173 | PQ8 | NC# | B-68 | PR8 | NC# |
| A-174 | PQ9 | NC# | B-67 | PR9 | NC# |
| A-175 | PQ10 | NC# | B-66 | PR10 | NC# |
| A-176 | PQ11 | NC# | B-65 | PR11 | NC# |
| A-177 | PQ12 | NC# | B-64 | PR12 | NC# |
| A-178 | PQ13 | NC# | B-63 | PR13 | NC# |
| A-179 | PQ14 | NC# | B-62 | PR14 | NC# |
| A-180 | PQ15 | NC# | B-61 | PR15 | NC# |

5 Board Interface Connector

| | | | | | |
|-------|----------------|-------------|------|----------------|-------------|
| A-181 | 5.0V_SR | 5.0V_SR | B-60 | 5.0V_SR | 5.0V_SR |
| A-182 | 5.0V_SR | 5.0V_SR | B-59 | 5.0V_SR | 5.0V_SR |
| A-183 | 5.0V_SR | 5.0V_SR | B-58 | 5.0V_SR | 5.0V_SR |
| A-184 | 5.0V_SR | 5.0V_SR | B-57 | 5.0V_SR | 5.0V_SR |
| A-185 | PS0 | NC# | B-56 | PT0 | NC# |
| A-186 | PS1 | NC# | B-55 | PT1 | NC# |
| A-187 | PS2 | NC# | B-54 | PT2 | NC# |
| A-188 | PS3 | NC# | B-53 | PT3 | NC# |
| A-189 | PS4 | NC# | B-52 | PT4 | NC# |
| A-190 | PS5 | NC# | B-51 | PT5 | NC# |
| A-191 | PS6 | NC# | B-50 | PT6 | NC# |
| A-192 | PS7 | NC# | B-49 | PT7 | NC# |
| A-193 | PS8 | NC# | B-48 | PT8 | NC# |
| A-194 | PS9 | NC# | B-47 | PT9 | NC# |
| A-195 | PS10 | NC# | B-46 | PT10 | NC# |
| A-196 | PS11 | NC# | B-45 | PT11 | NC# |
| A-197 | PS12 | NC# | B-44 | PT12 | NC# |
| A-198 | PS13 | NC# | B-43 | PT13 | NC# |
| A-199 | PS14 | NC# | B-42 | PT14 | NC# |
| A-200 | PS15 | NC# | B-41 | PT15 | NC# |
| A-201 | 3.3V_SR | 3.3V_SR | B-40 | 3.3V_SR | 3.3V_SR |
| A-202 | 3.3V_SR | 3.3V_SR | B-39 | 3.3V_SR | 3.3V_SR |
| A-203 | 3.3V_SR | 3.3V_SR | B-38 | 3.3V_SR | 3.3V_SR |
| A-204 | 3.3V_SR | 3.3V_SR | B-37 | 3.3V_SR | 3.3V_SR |
| A-205 | PU0 | NC# | B-36 | PV0 | NC# |
| A-206 | PU1 | NC# | B-35 | PV1 | NC# |
| A-207 | PU2 | NC# | B-34 | PV2 | NC# |
| A-208 | PU3 | NC# | B-33 | PV3 | NC# |
| A-209 | PU4 | NC# | B-32 | PV4 | NC# |
| A-210 | PU5 | NC# | B-31 | PV5 | NC# |
| A-211 | PU6 | NC# | B-30 | PV6 | NC# |
| A-212 | PU7 | NC# | B-29 | PV7 | NC# |
| A-213 | PU8 | NC# | B-28 | PV8 | NC# |
| A-214 | PU9 | NC# | B-27 | PV9 | NC# |
| A-215 | PU10 | NC# | B-26 | PV10 | NC# |
| A-216 | PU11 | NC# | B-25 | PV11 | NC# |
| A-217 | PU12 | NC# | B-24 | PV12 | NC# |
| A-218 | PU13 | NC# | B-23 | PV13 | NC# |
| A-219 | PU14 | NC# | B-22 | PV14 | NC# |
| A-220 | PU15 | NC# | B-21 | PV15 | NC# |
| A-221 | VDD_HV_IO_MAIN | 3.3v_SR_LDO | B-20 | VDD_HV_IO_MAIN | 3.3v_SR_LDO |

| | | | | | |
|-------|----------------|-------------|------|----------------|-------------|
| A-222 | VDD_HV_IO_MAIN | 3.3v_SR_LDO | B-19 | VDD_HV_IO_MAIN | 3.3v_SR_LDO |
| A-223 | VDD_HV_IO_MAIN | 3.3v_SR_LDO | B-18 | VDD_HV_IO_MAIN | 3.3v_SR_LDO |
| A-224 | VDD_HV_IO_MAIN | 3.3v_SR_LDO | B-17 | VDD_HV_IO_MAIN | 3.3v_SR_LDO |
| A-225 | PW0 | NC# | B-16 | PX0 | NC# |
| A-226 | PW1 | NC# | B-15 | PX1 | NC# |
| A-227 | PW2 | NC# | B-14 | PX2 | NC# |
| A-228 | PW3 | NC# | B-13 | PX3 | NC# |
| A-229 | PW4 | NC# | B-12 | PX4 | NC# |
| A-230 | PW5 | NC# | B-11 | PX5 | NC# |
| A-231 | PW6 | NC# | B-10 | PX6 | NC# |
| A-232 | PW7 | NC# | B-9 | PX7 | NC# |
| A-233 | PW8 | NC# | B-8 | PX8 | NC# |
| A-234 | PW9 | NC# | B-7 | PX9 | NC# |
| A-235 | PW10 | NC# | B-6 | PX10 | NC# |
| A-236 | PW11 | NC# | B-5 | PX11 | NC# |
| A-237 | PW12 | NC# | B-4 | PX12 | NC# |
| A-238 | PW13 | NC# | B-3 | PX13 | NC# |
| A-239 | PW14 | NC# | B-2 | PX14 | NC# |
| A-240 | PW15 | NC# | B-1 | PX15 | NC# |

Some of the port pins on the mother board share functionality with other peripherals like communication interfaces. Table 30 shows what port pins are used for peripherals on the motherboard.

Table 30. Port pins alternate function - on motherboard

| Port Pin | Function | Alternate Function |
|------------|----------------------|------------------------------------|
| PE1 | CTU0_EXT_TGR | Multiplexed with Pin J23 (GPIO 62) |
| PG0 | wgm.D0 | Multiplexed with PDI D0 |
| PG1 | wgm.D1 | Multiplexed with PDI D1 |
| PG2 | wgm.D2 | Multiplexed with PDI D2 |
| PI0 | Removed PDI_D0 | multiplexed with WGM.D0 |
| PI1 | Removed PDI_D1 | multiplexed with WGM.D1 |
| PI2 | Removed PDI_D2 | multiplexed with WGM.D2 |
| PL8 | Removed ETIMER2_ETC2 | Multiplexed with Ethernet |

Some of the port pins of the MCU have dedicated functionality or require short trace lengths to improve signal integrity . Therefore these signal have been routed to jumper or connectors on the daughter card.

1. JTAG - (J5)
2. Nexus Aurora – (J10)
3. SIPI – (J35)
4. Sigma Delta ADC – (J20)
5. DAC – (J47)
6. WGM – (J46)
7. CTE – (J44)

6 Default Jumper Summary Table

The details for the DEFAULT jumper configuration of the EVB as set up on delivery can be found in table 4.10.

6.1 Default Jumper Table - Motherboard

On delivery the motherboard comes with a default jumper configuration. Table 31 lists and describes briefly the jumpers on the MPC57xx motherboard and indicates which jumpers are on/off on delivery of the board.

Table 31. Default Jumper Table - Motherboard

| Jumper | Default Pos | PCB Legend | Description |
|--------|-------------|------------|---|
| J8 | Off | MASTER | LIN Master/Slave select |
| J9 | Off | CAP A DIS | Disable capacitor circuitry for FlexRAY_A signals |
| J10 | Off | CAP A DIS | Disable capacitor circuitry for FlexRAY_A signals |
| J11 | Off | CAP B DIS | Disable capacitor circuitry for FlexRAY_B signals |
| J12 | Off | CAP B DIS | Disable capacitor circuitry for FlexRAY_B signals |
| J13 | Off | SCI TX | Connect SCI TX signal |
| J14 | Off | SCI RX | Connect SCI RX signal |
| J15 | Off | LIN_EN | Enable LIN PHY U50 |
| J16 | Off | LIN_RX | Connect LIN RX signal |
| J17 | Off | LIN_TX | Connect LIN TX signal |
| J18 | Off | - | Ethernet signal: RXCLK |
| J20 | Off | - | Ethernet signal: CRS_LEDCFG |
| J21 | Off | CAN2_EN | PHY U2 configuration: 1-2: WAKE to GND |

MPC5775K EVB Users Manual, Rev2.0

Default Jumper Summary Table

| Jumper | Default Pos | PCB Legend | Description |
|--------|-------------|------------|--|
| | | | 3-4: STB to 5V 5-6: EN to 5V |
| J22 | On | - | Ethernet phy power-on |
| J23 | Off | CAN-EN | PHY U1 configuration: 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V |
| J24 | Off | - | Ethernet signal: RXER_MDIXEN |
| J25 | Off | SCI-PWR | SCI phy power-on |
| J26 | Off | - | Ethernet signal: RXDV_MIIMODE |
| J27 | Off | FR-A | 1-2: PHY U4 TX to MCU 3-4: PHY U4 TXEN to MCU 5-6: PHY U4 RX to MCU |
| J28 | Off | FR-A | PHY U4 configuration: 1-2: 3.3V (V _{IO}) to BGE 3-4: 3.3V (V _{IO}) to EN 5-6: 3.3V (V _{IO}) to STBY 7-8: GND to WAKE |
| J29 | Off | FR_PWR | FlexRAY transceiver VIO selection 1-2: 12V to V _{BAT} 3-4: 5V _{SR} to V _{CC} and V _{BUF} |
| J30 | Off | FR_B | 1-2: PHY U5 TX to MCU 3-4: PHY U5 TXEN to MCU 5-6: PHY U5 RX to MCU |
| J31 | Off | FR_B | PHY U5 configuration: 1-2: 3.3V (V _{IO}) to BGE 3-4: 3.3V (V _{IO}) to EN 5-6: 3.3V (V _{IO}) to STBY 7-8: GND to WAKE |
| J32 | Off | CAN2 | 1-2: PHY TX to MCU 3-4: WAKE to GND |
| J33 | Off | CAN-PWR | 1-2: 5V _{SR} to PHY U2 V _{CC} 3-4: 12V to PHY U2 V _{BAT} |
| J34 | Off | - | MCAN2 signal out: 1: ERR 2: INH |
| J35 | Off | CAN | 1-2: 5V _{SR} to PHY U1 V _{CC} 3-4: 12V to PHY U1 V _{BAT} |
| J36 | Off | - | CAN PHY U1 signal out |
| J37 | Off | - | CAN TX connect |
| J38 | Off | - | CAN RX connect |
| J39 | Off | - | Ethernet signal: RXD0_PHYAD1 |
| J40 | Off | - | Ethernet signal: RXD1_PHYAD1 |
| J41 | Off | - | Ethernet signal: RXD2_PHYAD2 |

| Jumper | Default Pos | PCB Legend | Description |
|--------|-------------|------------|--|
| J42 | Off | - | Ethernet signal: RXD3_PHYAD3 |
| J44 | Off | - | Ethernet signal: COL_PHYAD0 |
| J45 | Off | - | Ethernet signal: TXEN |
| J46 | Off | - | Ethernet signal: TXCLK |
| J47 | Off | - | Ethernet signal: TXD0 |
| J48 | Off | - | Ethernet signal: TXD1 |
| J49 | Off | - | Ethernet signal: TXD2 |
| J50 | Off | - | Ethernet signal: TXD3_SNIMODE |
| J51 | Off | - | Ethernet signal: MDC |
| J52 | Off | - | Ethernet signal: MDIO |
| J53 | Off | RV1 | Connect RV1 to analog input AN0 |
| J54 | Off | ADC_VSUP | Connect EVB supply voltages to analog inputs |
| J55 | Off | 12V (4.3V) | Connect 12V (scaled to 4.3V) EVB power to analog input |
| J57 | On | ENABLE | Enable 5V linear regulator |
| J58 | Off | DISABLE | Disable 1.25V switching regulator |
| J59 | Off | DISABLE | Disable 3.3V switching regulator |
| J60 | Off | DISABLE | Disable 5.0V switching regulator |

6.2 User Area

There is a rectangular prototype area on the EVB's top right corner, consisting of a 0.1inch pitch array of through-hole plated pads. Power from all the three switching regulators is readily accessible along with GND through JP1 – JP16 next to the prototyping area. This area is ideal for the addition of any custom circuitry.

There are four active low user LEDs D2, D3, D4 and D5, these are driven by connecting a logic 0 signal to the corresponding pin on 0.1" header P7 (USER LEDS). The LED inputs are pulled to VDD_HV_IO_MAIN through 10kOhm resistors.

There are 4 active high pushbutton switches SW1, SW2, SW3 and SW4 which will drive 5V onto the respective pins on 0.1" connector P6 when pressed. The switch outputs are pulled to GND via 10kOhm.

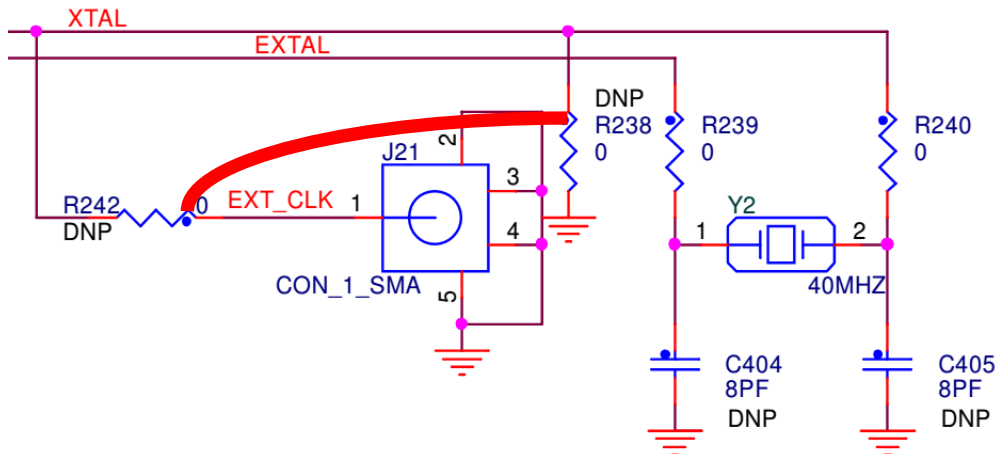
Potentiometer RV1 can be connected to port pin PB[0] and is adjustable between GND and 5V from the linear regulator. Power from all regulators can be connected to port pins as through J54:

- 1-2: 1.25V_SR to PB[1]
- 3-4: 3.3V_SR to PB[2]
- 5-6: 5V_SR to PB[3]
- 7-8: 5V_LR to PB[4]

The P12V rail from the 12V input is scaled to 4.3V through the voltage divider of R81 and R82 and the scaled voltage can be connected to PB[5] via J55.

6.3 Known Issues

The SMA connector for the External Clock source should be connected to EXTAL not XTAL, if you require to use an external clock source connect a wire from R242 to R238 as seen below.



How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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