S32K324 DUAL CORES DEBUG WITH P&E MULTILINK





SECURE CONNECTIONS FOR A SMARTER WORLD

EXTERNAL USE

- Debug S32K324 Project when "CM7_1_ENALBE=1"
- Debug S32K324 Project when "CM7_1_ENALBE=0"

Example application used in this document





Debug S32K324 Project when "CM7_1_ENALBE=1"

- CM7_1 is enabled during boot. Debugger can connect to it during the debug launch.
- Check CM7_0 and CM7_1 projects debug settings

Launch Group

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Debug S32K324 dual-core projects

Default settings are OK for debugging s32k 324.
 The target elf file can also be manually changed.

	Name: s32k324_dual_core_demo_M7_0_Debug_FONV ONE COIE
type filter text	📔 Main 🕸 Debugger 🕟 Startup 🦗 Source 🔲 Common 🕮 OS Awareness 🔤 SVD Support
€ C/C++ Application ▲ C/C++ Remote Application ● Eclipse Application ● Eclipse Application ● GDB Hardware Debugging ✓ GDB PEMicro Interface Debugging ✓ S32k324_dual_core_demo_M7_0_Debug_FLASH_PNE ✓ s32k324_dual_core_demo_M7_0_Release_FLASH_PNE ✓ s32k324_dual_core_demo_M7_1_Debug_FLASH_PNE ✓ s32k324_dual_core_demo_M7_1_Debug_FLASH_PNE ✓ s32k324_dual_core_demo_M7_1_Debug_RAM_PNE ✓ s32k324_dual_core_demo_M7_1_Release_FLASH_PNE ✓ s32k324_dual_core_demo_M7_1_Release_FLASH_PNE ✓ s32k324_dual_core_demo_M7_1_Release_RAM_PNE ✓ s32k324_dual_core_demo_M7_1_R	Project: Specify the number of additional object files you wish to program. I Generate Object File Fields Specify Additional Object File 1: Specify Additional Object File 1: Stproject_loc:s32k324_dual_core_demo_M7_0)//s32k324_dual_core_demo_M7_1/Debug_FL Browse Object File offset (hex) 1: C/C++ Application: Debug_FLASH/s32k324_dual_core_demo_M7_0.elf Debug_FLASH/s32k324_dual_core_demo_M7_0.elf
✓ ➡ Launch Group ➡ s32k324 dual core demo Debug ELASH PNE group	<u>V</u> ariables Searc <u>h</u> Project B <u>r</u> owse
	 You can launch this configuration to debug CM7 0 only You can launch this configuration to debug CM7_1 after CM7_0 is already connected by the debugger



Debug S32K324 dual-core projects

If a P&E multilink debugger or an OpenSDA debugger is

- Default settings are OK for debugging s32k324. connected to yowr PC, it can be
- The target device type can be changed in the seen in this drop-down list.

debugger settings page.	Name: s32k324_dual_core_demo_M7_0_Debug_FLASH_PNE			
type filter text	📄 Main 🏇 Debugger 🔪 🔈 Startup 🦆 Source 🔲 Common 🔤 SVD Support 💭 OS Awareness			
 C/C++ Application C/C++ Remote Application Eclipse Application GDB Hardware Debugging C GDB PEMicro Interface Debugging 	Software Registration Please register your software to remove this message. Register now			
Image: s32k324_dual_core_demo_M7_0_Debug_FLASH_PNE Image: s32k324_dual_core_demo_M7_0_Debug_RAM_PNE	PEMicro Interface Settings Interface: USB Multilink, USB Multilink FX, Embedded OSBDM/OSJTAG - USB Port V Compatible Hardw			
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Debug S32K324 dual-core projects

• Default settings are OK for debugging s32k324.

• The target device type can be changed in the

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eate, manage, and run configurations	Create, manage, and run configurations
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Debug S32K324 dual-core projects – launch debug process





Debug S32K324 Dual-Core project in S32DS with PE Multilink





Debug S32K324 Project when "CM7_1_ENALBE=0"

• Assumption:

- -CM7_1 is NOT enabled during boot. Debugger cannot work before it is launched. CM7_1 is started in CM7_0 application code.
- Use the same Debug Configuration as debugging "CM7_1_ENABLE=1".
- Procedure:
 - Download CM7_0 elf and CM7_1 elf into the flash with Group Launch

type filter text	Paths and Symbo	ls		$\langle \neg \neg \neg \rangle$	Ψ.
 C/C++ Build C/C++ General Code Analysis Documentation File Types Formattor 	Configuration: Del	oug_FLASH [Active] rraries ൙ Library Paths 😂 Soui	✓ Mana rce Location 🔒 R	age Configuratio	ons.
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Debug S32K324 Dual-Core project when CM7_1_ENALBE=0

	WorkspaceS32DS.3.4 - s32k324_dualcore_demo_M7_0/src/mai	in.c - S32 Design Studio for S32 Platform				
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Core1 is not started at this moment, you can't debug Core1.	 Image: Signature of the system of the system	<pre>157 */ 158@int main(void) 159 { 160 OsIf_Init(NULL); 161 Clock_Ip_Init(&Mcu_aClockConfigPB[0]); 162 Siul2_Port_Ip_Init(NUM_OF_CONFIGURED_PINS0, g_pin_mux_InitConfigArr0); 163 164 /* If previous reset is caused by FCCU fault state, the LPUART GPI0 mi 165 /* LPUART initialization */ 166 Console_SerialPort_Init(); 167 168 169 169 160 160 160 160 160 160 160 160 160 160</pre>				
	 main() at main.c:160 0x4015f0 C:\NXP\S32DS.3.4\eclipse\plugins\com.pemicro.debuc arm-none-eabi-gdb Semihosting Console 	<pre>107 print((r(n)), 168 printf("********* MCU reset occurred ********* \r\n"); 169 170 /* XRDC initialization */ 171 Xrdc_Ip_Init(&Xrdc_Config_BOARD_INITPERIPHERALS);</pre>				
	 S32k324_dualcore_demo_M7_1_Debug_FLASH_PNE [GDB S32k324_dualcore_demo_M7_1.elf Thread #1 (Running : User Request) arm-none-eabi-gdb Samibacting Consola 	<pre>172 /* XBIC initialization */ 173 Xbic_Ip_Init(&Xbic_Config_BOARD_INITPERIPHERALS); 174 /* Semaphore initialization */ 175 Sema42_Ip_Init(0); 176</pre>				
		<pre>177 /* After IntCtrl is enabled, the FCCU Alarm ISR is allowed to run */ 178 IntCtrl_Ip_ConfigIrqRouting(&intRouteConfig); 170 IntCtrl_IP_ConfigIrqRouting(&intRouteConfig);</pre>				



Debug S32K324 Dual-Core project when CM7_1_ENALBE=0

Debug Core0 step by step, after calling Mcme_Start_Core1 to start Core1, you will find the start address of Core1 could be showed at left side, then you could debug Core1 now.

📓 workspaceS32DS.3.4 - s32k324_dualcore_demo_M7_0/src/main.c - S32 Design Studio for S32 Platform				
ile Edit Source Refactor Navigate Search Project ConfigTools Run PEMicro FreeRTOS Window Help				
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🎋 Debug 🛛 🎦 Project Explorer 🛛 🗮 🗱 🖬 😫 🖓 🗖	🛅 S32K344_COM 🖻 RegLockMacros.h 🔹 main.c 🕺 🖻 main.c 🗈 Siul2_Dio_lp.c 🏻 🔭 🗖			
 \$32k324_dualcore_demo_Debug_FLASH_PNE_group [Laur C:\NXP\S32DS.3.4\eclipse\plugins\com.pemicro.debuc arm-none-eabi-gdb Semihosting Console arm-none-eabi-gdb 	<pre>184 Pit_ip_initChannel(Pii_0_IP_INSTANCE_NUMBER, &Pii_0_ChannelConfig_PB[0_ 185 /* Start PITO channel0 */ 186 Pit_ip_StartChannel(PIT_0_IP_INSTANCE_NUMBER, 0, 4000000); 187 /* Enable PITO channel0 interrupt */ 188 Pit_ip_EnableChannelInterrupt(PIT_0_IP_INSTANCE_NUMBER, 0); 189</pre>			
 Semihosting Console Isa2k324_dualcore_demo_M7_0_Debug_FLASH_PNE [GDB s32k324_dualcore_demo_M7_0.elf mrherad #1 (Suspended : Step) 	<pre>190 #if ENABLE_DUAL_CORE_DEMO 191</pre>			
 main() at main.c:205 0x401686 C:\NXP\S32DS.3.4\eclipse\plugins\com.pemicro.debuc arm-none-eabi-gdb Semihosting Console 	<pre>195 /* Core0 use SEMA42 Gate0 to notify Core1 init ready */ 196 Sema42_Ip_LockGate(SEMA42_INSTANCE, SEMA42_GATE0, CORE_DOMAIN_ID); 197 198 /* Core0 use shared variable to notify Core1 that Core0 is ready */</pre>			
 S32k324_dualcore_demo_M7_1_Debug_FLASH_PNE [GDB \$32k324_dualcore_demo_M7_1.elf 	<pre>199 core0Status = CORE_STATUS_INIT_DONE; 200 201</pre>			
Thread #1 (Suspended : Signal : SIGINT:Interrupt) start() at startup_cm7.s:154 0x600420	202 Mcme_Start_Core1(CORE1_START_ADDR); 203			
arm-none-eabi-gdb Semihosting Console	<pre>204 /* Core0 wait for Core1 initialization done. */ 205 while(core1Status != CORE_STATUS_INIT_DONE){} 206</pre>			



Debug S32K324 Dual-Core project when CM7_1_ENALBE=0

If the start address is still 0 after started Core1 in Core0 project, please check if there is similar log in Console window.

Open this folder, delete / rename the file 'S32K324.mac' to another name. Then debug again the dual-core project. Issue should be disappeared. There is no side effect to delete / rename this file 'S32K324.mac'.







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