T2080QDS features

	Specification	Description
Processor Support	Core Processors	4x64-bit up to 1.8 GHz Power Architecture Book E-compliant cores
	HS Serial Port (SerDes)[1]	• 16 lanes, up to 10.3125 GHz SerDes, divisible into combinations • Supports Aurora debug, PEX3.0, SATA2.0, SGMII, sRIO2.0, XFI, XAUI, and HiGig
	DDR	• Supports one DDR3/DDRL 32-/64-bit memory controller • T2080QDS supports 64-bit DDR3/DDR3L controller connected to single uDIMM socket • Default DIMM module - DDR3, 72-bit, ECC, 2 GB up to 2100MT/s, 1.5V • Optional DDR3L DIMM module could be <= 8 GB, 72-bit, ECC up to 1866MT/s, 1.35V
	EtherNet	• Dual 10/100/1000 Mbit/s port uses onboard RTL8211EG-VB-CG PHY's in RGMII mode.
	1588 PTP	• Support through on-board header J28
	Dual USB 2.0, Internal PHY	Two high speed onboard USB 2.0 connectors
	IFC	• One in-socket 128 MB NOR flash 16-bit data bus • One 512 MB NAND flash with ECC support • IFC Test Port • PromJet debug Port
	eSDHC	PEX x1 Right Angle connector (J4) is used for the following add-in card types: • 1-/4-/8-bit MMC Legacy CARD • 1-/4-/8-bit MMC Card • 4-bit eMMC Card Rev 4.4 • 8-bit eMMC Card Rev 4.5 • SD Card Rev 2.0 and Rev 3.0
	SPI	• 16 MB high-speed flash Memory for boot code and storage (up to 108MHz) • 8 MB high-speed flash Memory (up to 104 MHz) • 512 MB low-speed flash Memory (up to 40 MHz) • All memory operate at 1.8V
	Multimaster Serial Computer Bus, I^2C,	Four controllers
	DUART (2/channel)	Two 4-pin or four 2-pin serial ports at up to 115.2 Kbit/s
	SATA (2 channels)	Two SATA onboard connectors
	Debug Features	• Legacy, COP/JTAG, and Aurora support • Event and EVT support
	Package	• 896-pin, Flip-Chip PBGA of 25x25mm pitch 0.8mm • Supports attached socket and solder

T2080QDS features

	Specification	Description
System Logic	ProASIC3E FPGA	• Manages the following: – system reset sequencing – system and SerDes clock speed selections – boot and RCW source selection • Implements registers for system control and monitoring • Internal Cortex-M1 Soft Processor allows independent Vcore/temperature monitoring and reconfiguration • Supports legacy TMT test features • (PORt, IRS, SYSCLK synchronous assertion) • General fault monitoring and logging • Runs from ATX-PS Hot power rails, allowing operation while system is off
Clocks	SYSCLK	• Switch selectable to one of 16 common settings in the range of (64-166) MHz • Software programmable in 1MHz increments from (1-200) MHz
	SerDes	• Supports four domains • 100 (Spread Spectrum optionally), 125, and 156.25 MHz configurations support PEX, SATA, SGMII, sRIO, XFI, XAUI, HiGig and Aurora debug
	EtherNet	• Supports 125 MHz ethernet clocks for T2080, on-board RGMII PHY and 1588 test connector
	USB	• Supports 24MHz T2080 USB clock input
Power Supplies	One dedicated programmable regulator supply T2080 core domain and DDR power pools. Set of independent DC/DC and LDO power supplies	• PMBus control • Power: – 1.0V for USB Core – 1.89V for T2080 PROG_SFP and PROG_MTR (POVDD) – 1.5V for FPGA Core – 1.35/1.5V XVDD – 1.0V SVDD – 1.8V for T2080 Gen.I/O, SerDes MUX (OVDD) and USB OVDD – 2.5V for Ethernet PHY IO (LVDD) – 1.8/2.5/3.3V UART/I2C (DVDD) – 3.3V switchable regulator for FPGA – 3.3V for USB HVDD – VTT/VREF for DDR3 – 1.8/2.5V for eSPI, eSDHC (CVDD) – 1.0V for Secure monitor (VDD_LP)

T2080QDS block diagram