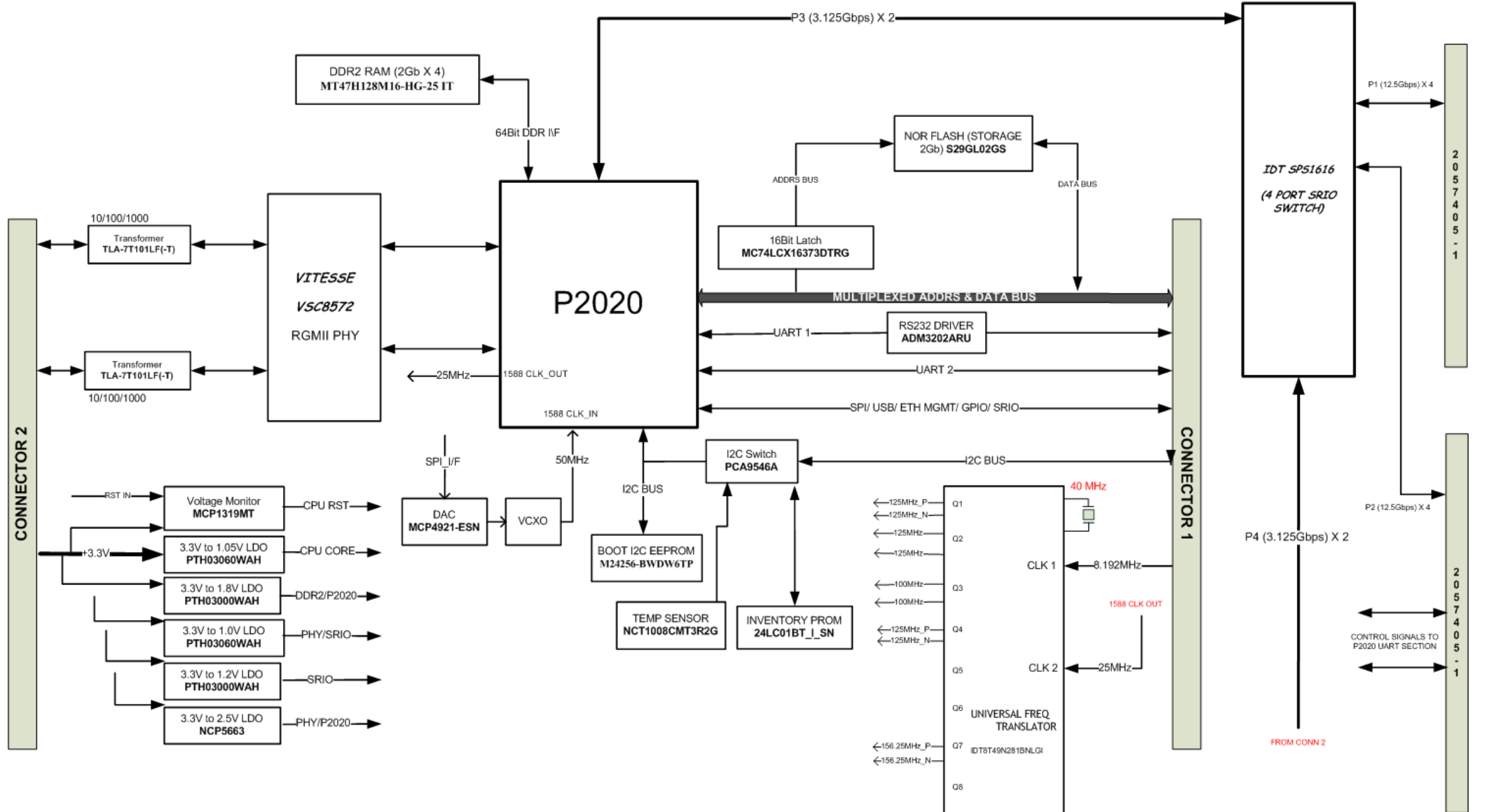
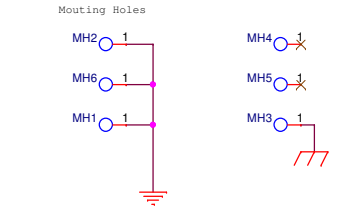
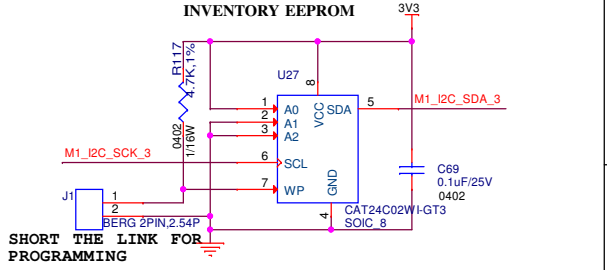
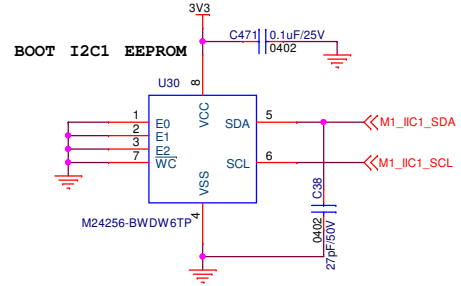
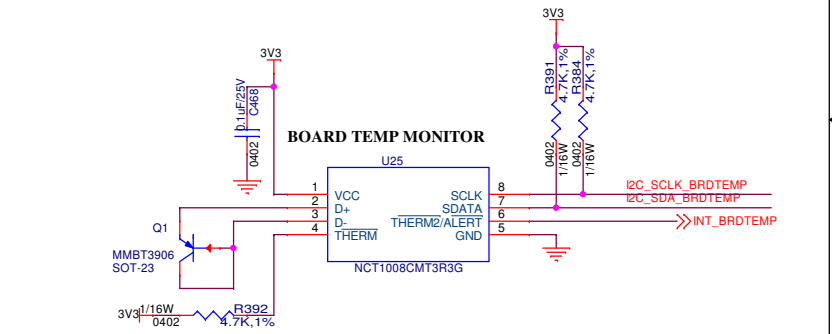
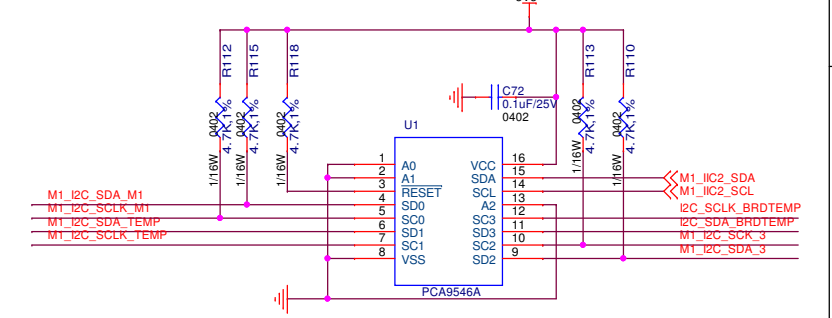
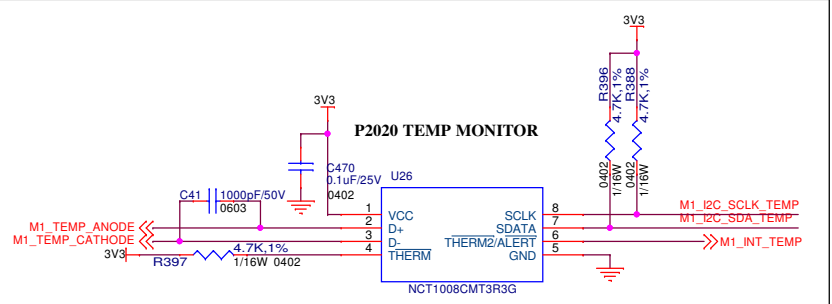
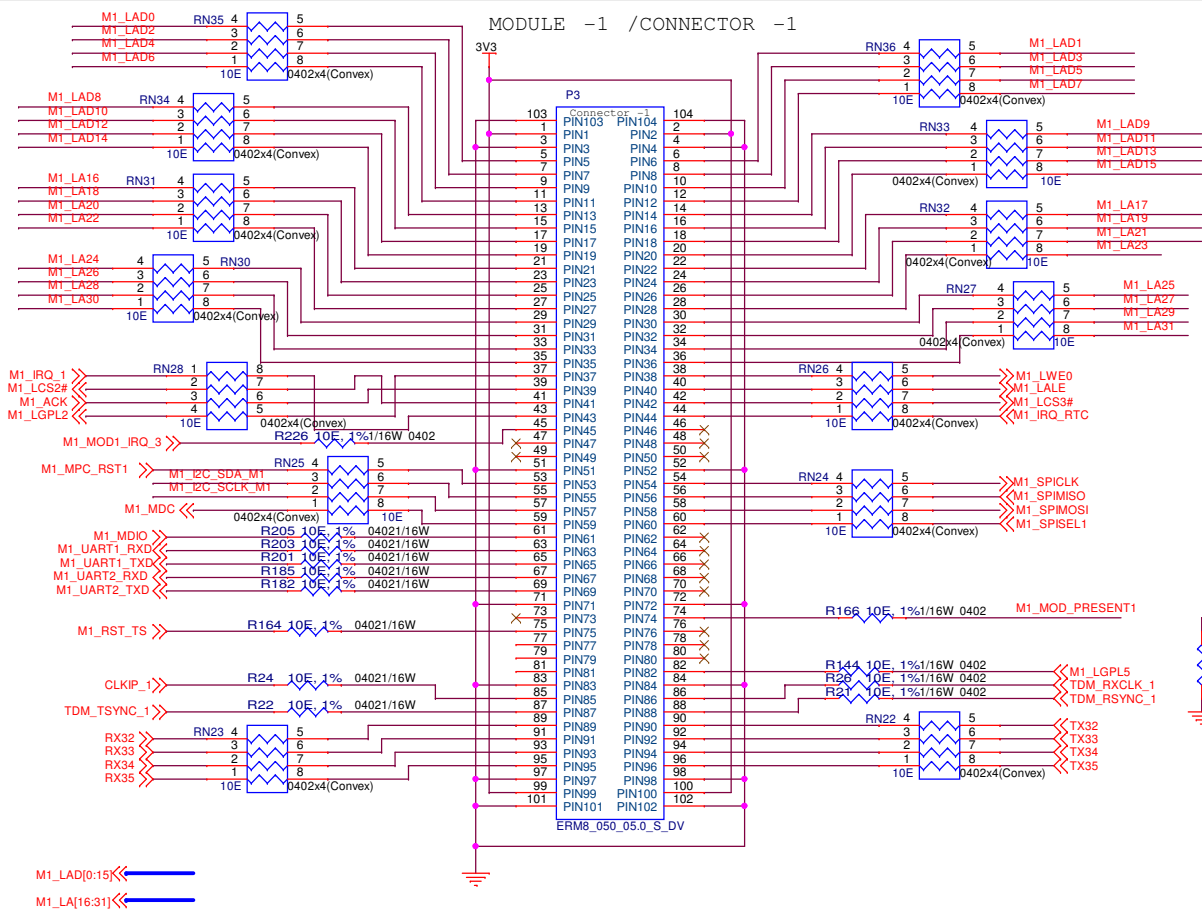


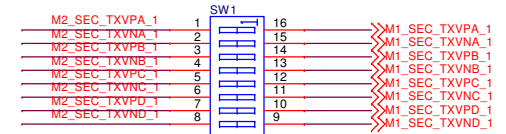
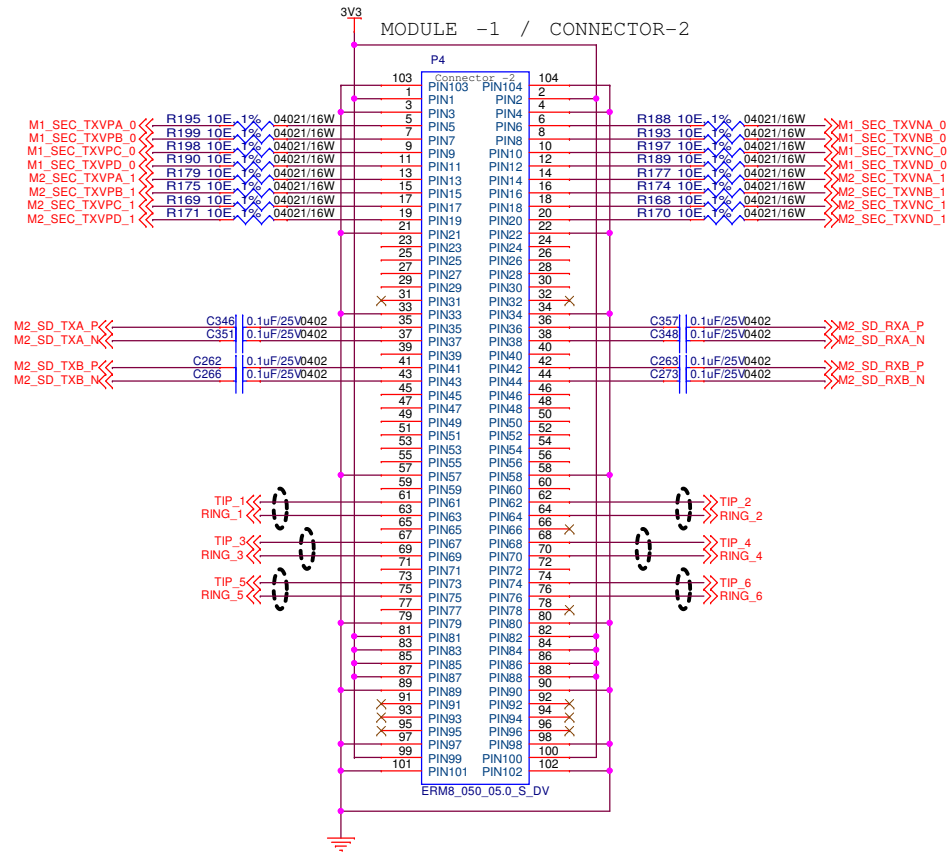
# HIGH SPEED CPU MODULE REV 2.0




<b>TATA POWER SED</b>												
TITLE : <b>NETWORK PROCESSOR CARD</b>												
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX						
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112						
		APR	XXX	DD/MM/YYYY	SECTION	BLOCK DIAGRAM						
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	1	OF	40	A3	REV	1.0



TATA POWER SED												
TITLE : NETWORK PROCESSOR CARD												
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX						
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112						
		APR	XXX	DD/MM/YYYY	SECTION	STACKING CONNECTOR-1						
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	2	OF	40	A3	REV	1.0



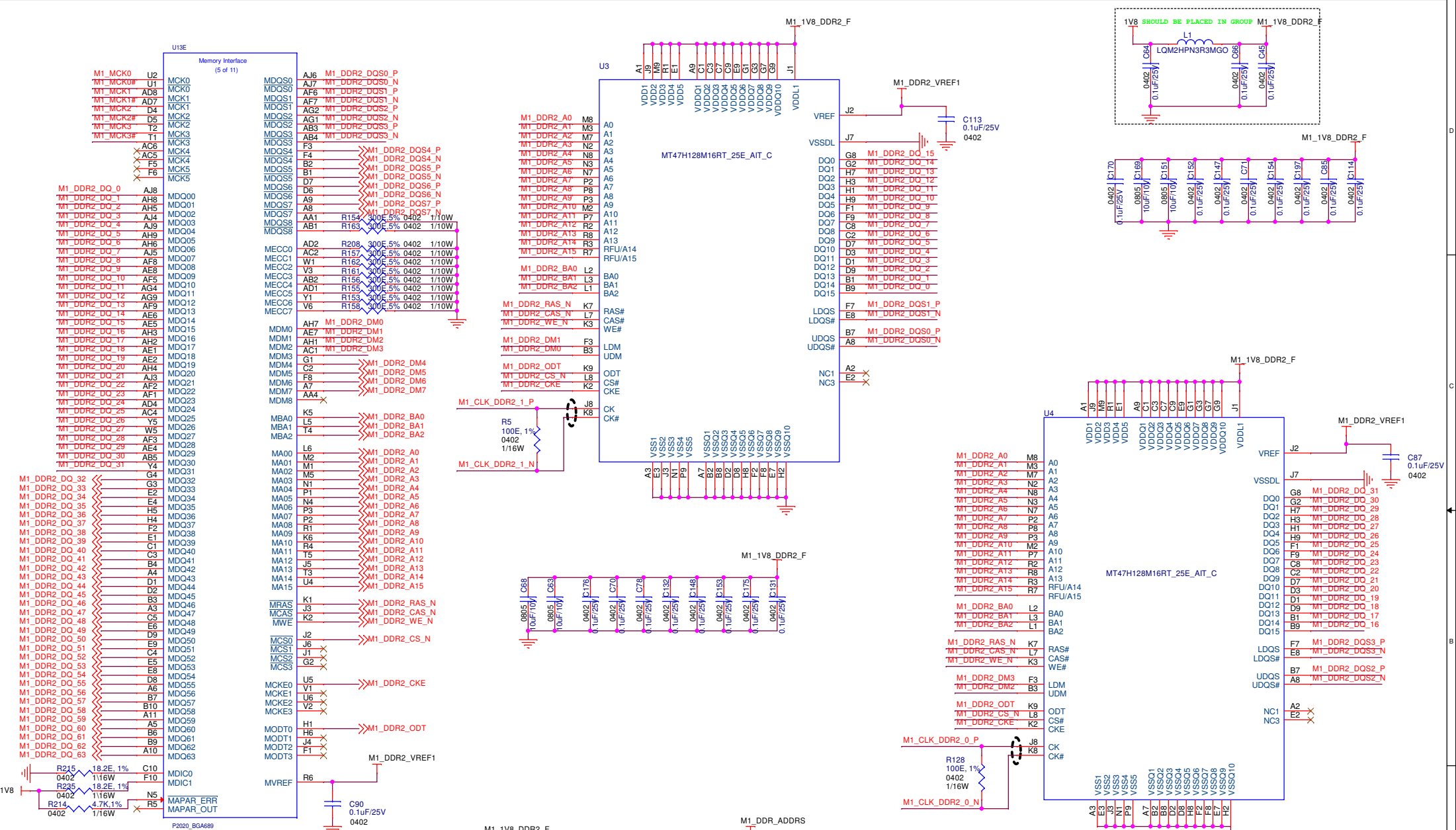
A6HF-8102 SMD\_1.27mm  
 Switch "ON" For P2020 Ethernet Port  
 Switch "OFF" For extended module Ethernet Port




**TATA POWER SED**

**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	STACKING CONNECTOR-2
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 3 OF 40 A3 REV 1.0

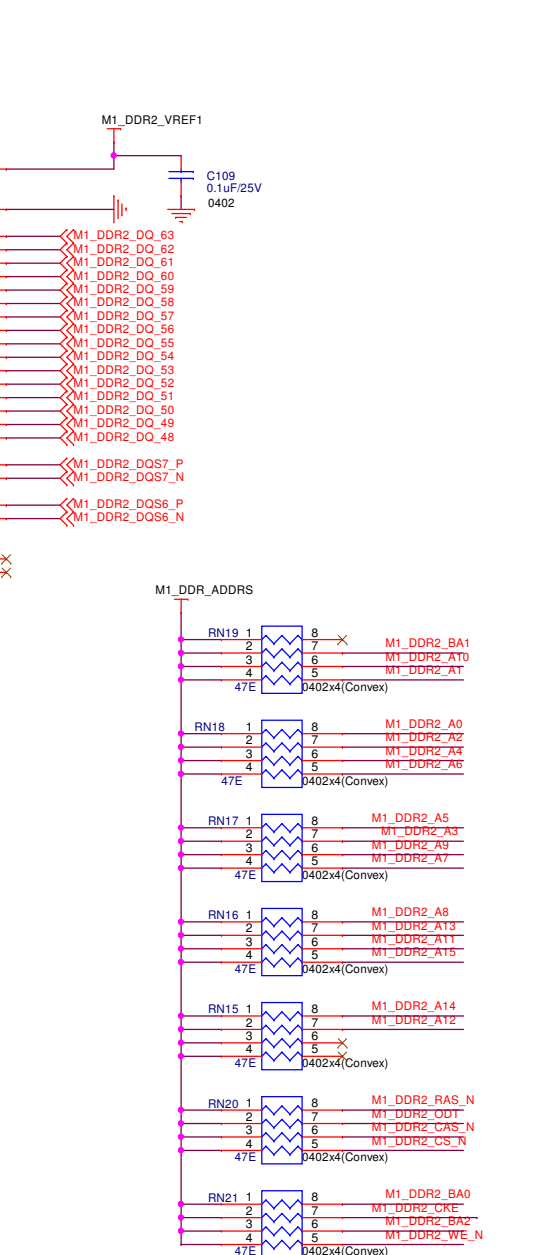
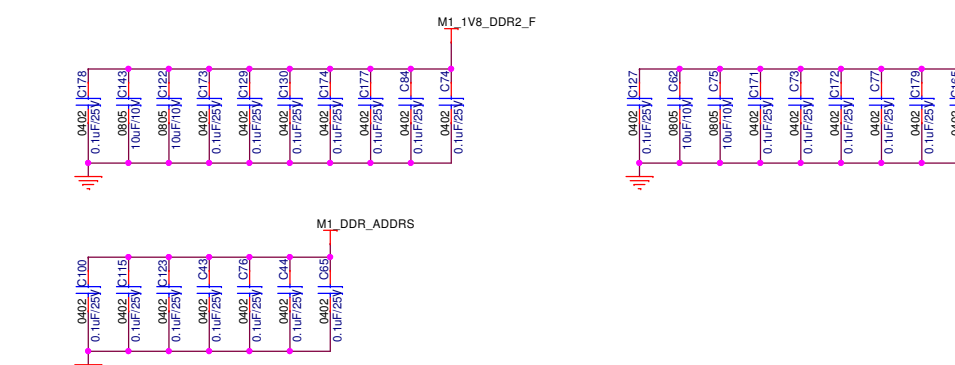
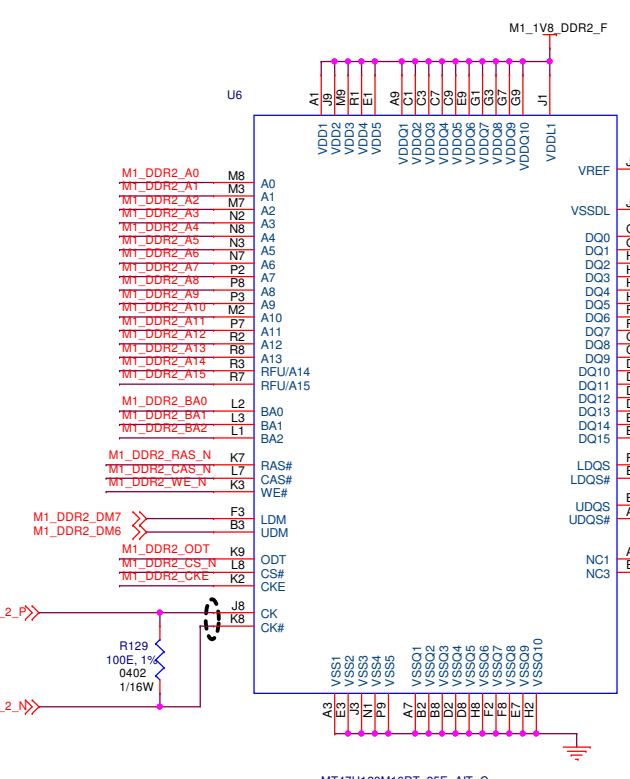
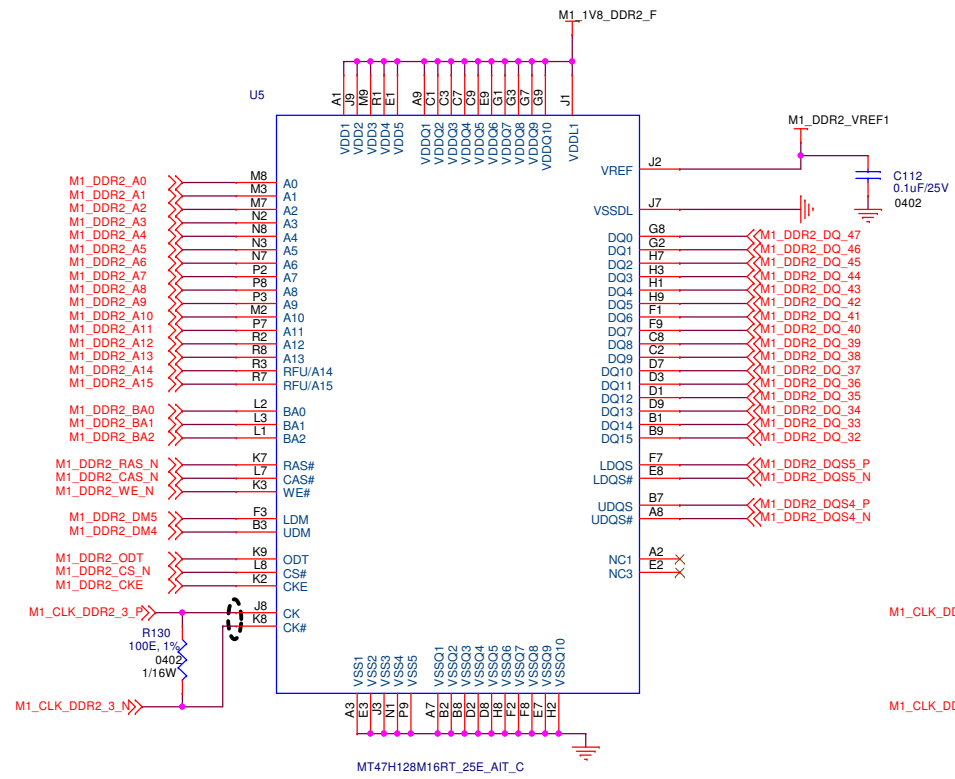


CM No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	DDR2_1&2
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 4 OF 40 A3 REV 1.0



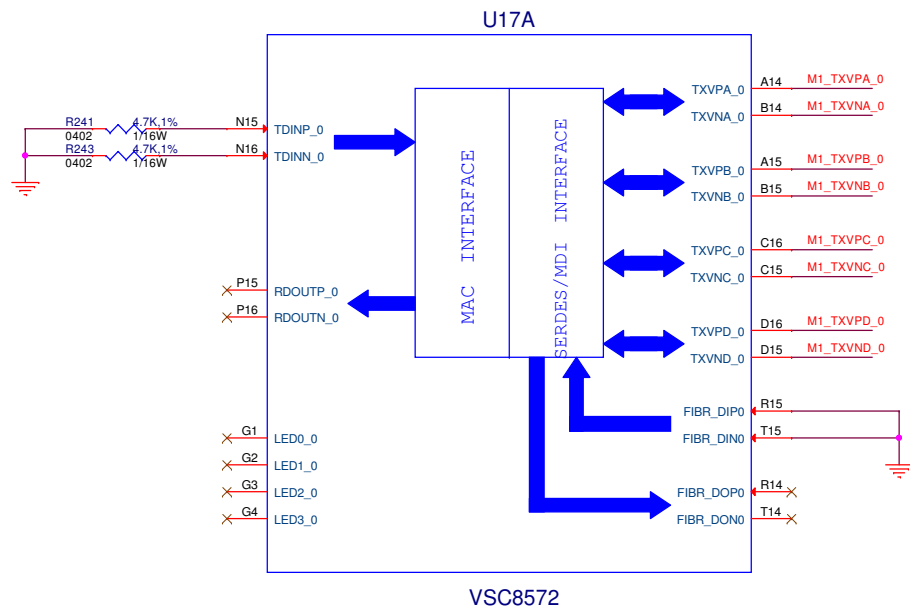
**TATA POWER SED**

TITLE : NETWORK PROCESSOR CARD						
CM No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	DDR2_1&2
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 4 OF 40 A3 REV 1.0

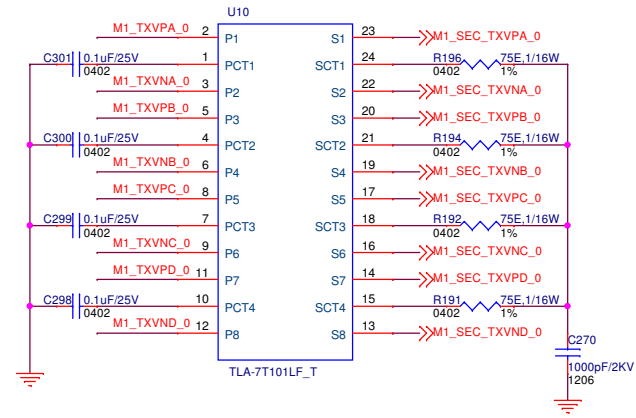


This Capacitors to be placed closer to the resistor network, (one each for every network)

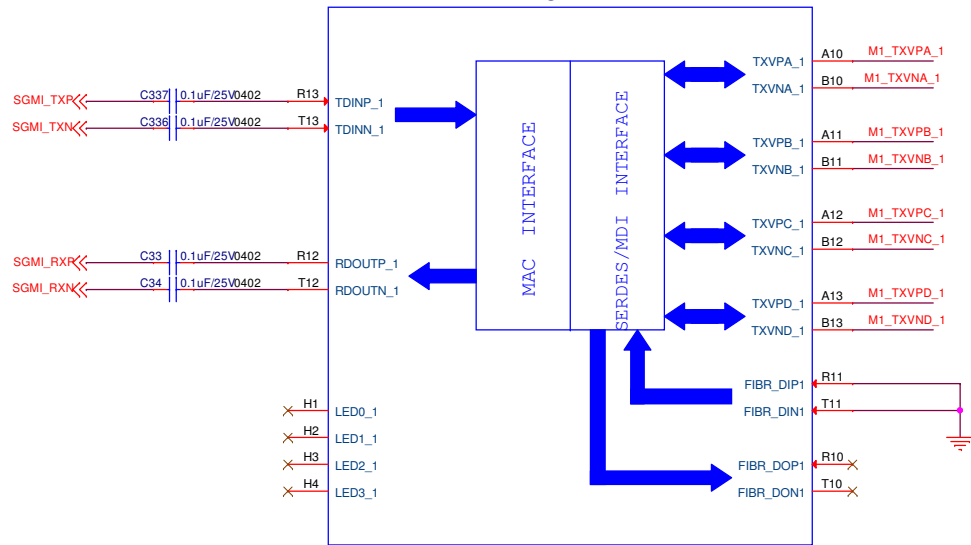
<b>TATA POWER SED</b>									
<b>TITLE : NETWORK PROCESSOR CARD</b>									
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX			
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112			
		APR	XXX	DD/MM/YYYY	SECTION	DDR2_3&4			
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	5 OF 40	A3	REV 1.0



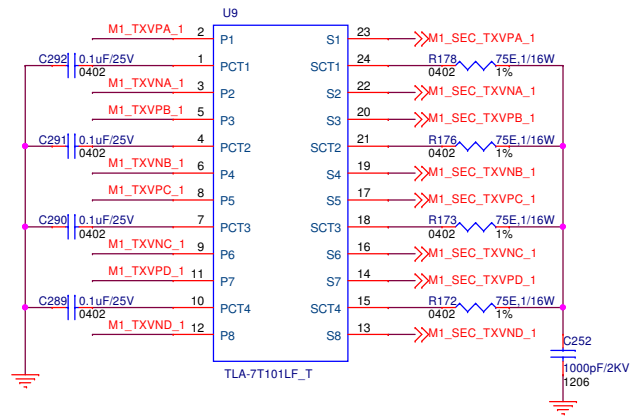
VSC8572



U17B



VSC8572

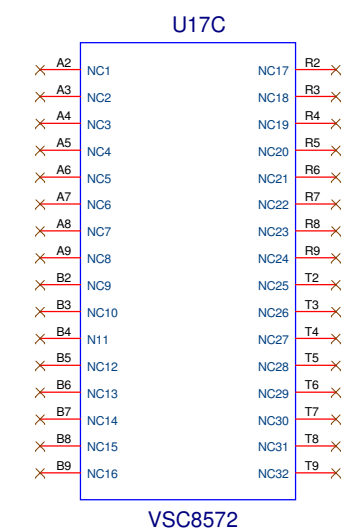
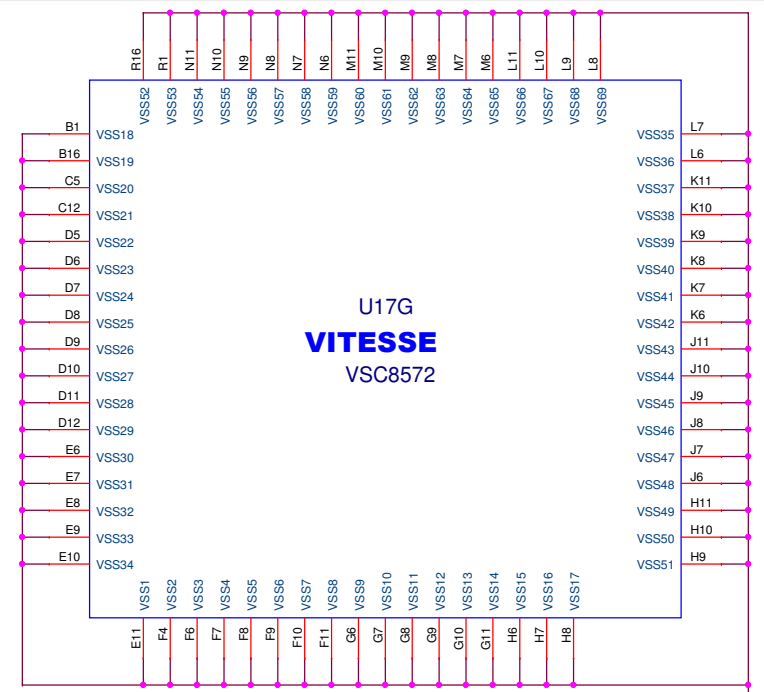
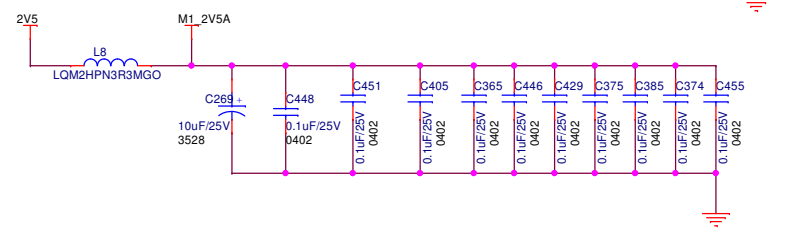
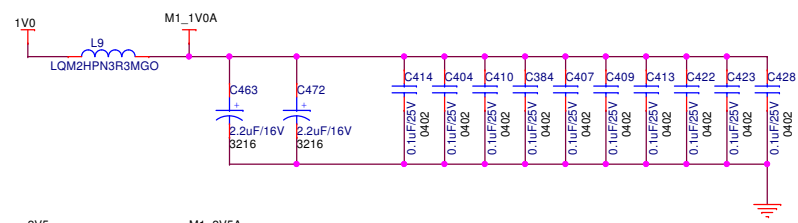
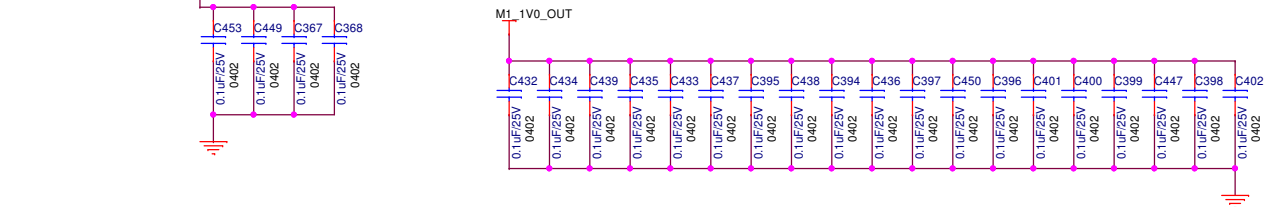
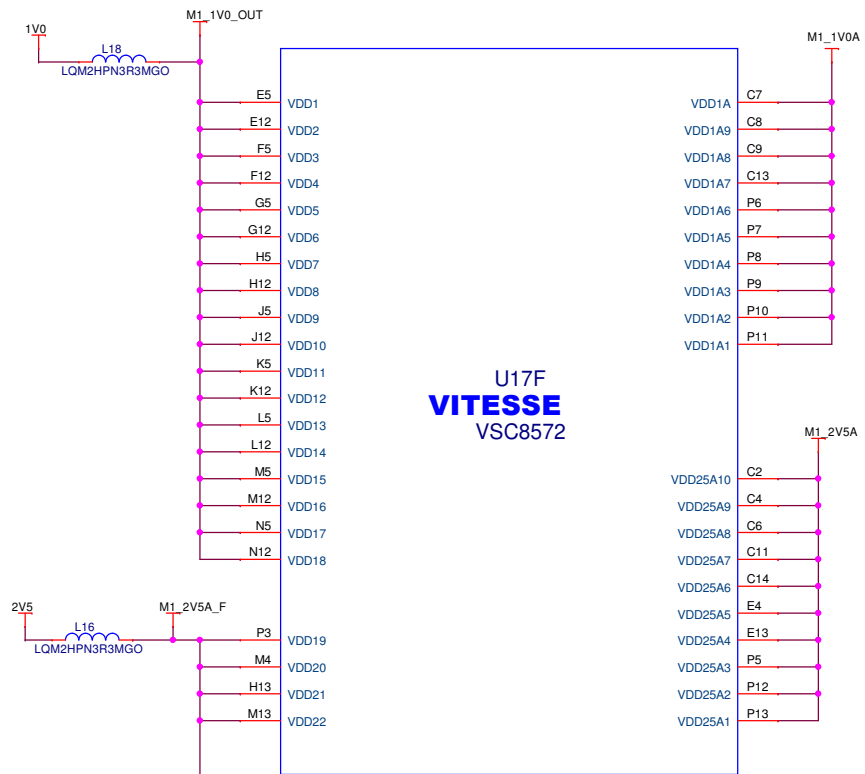


TATA POWER SED

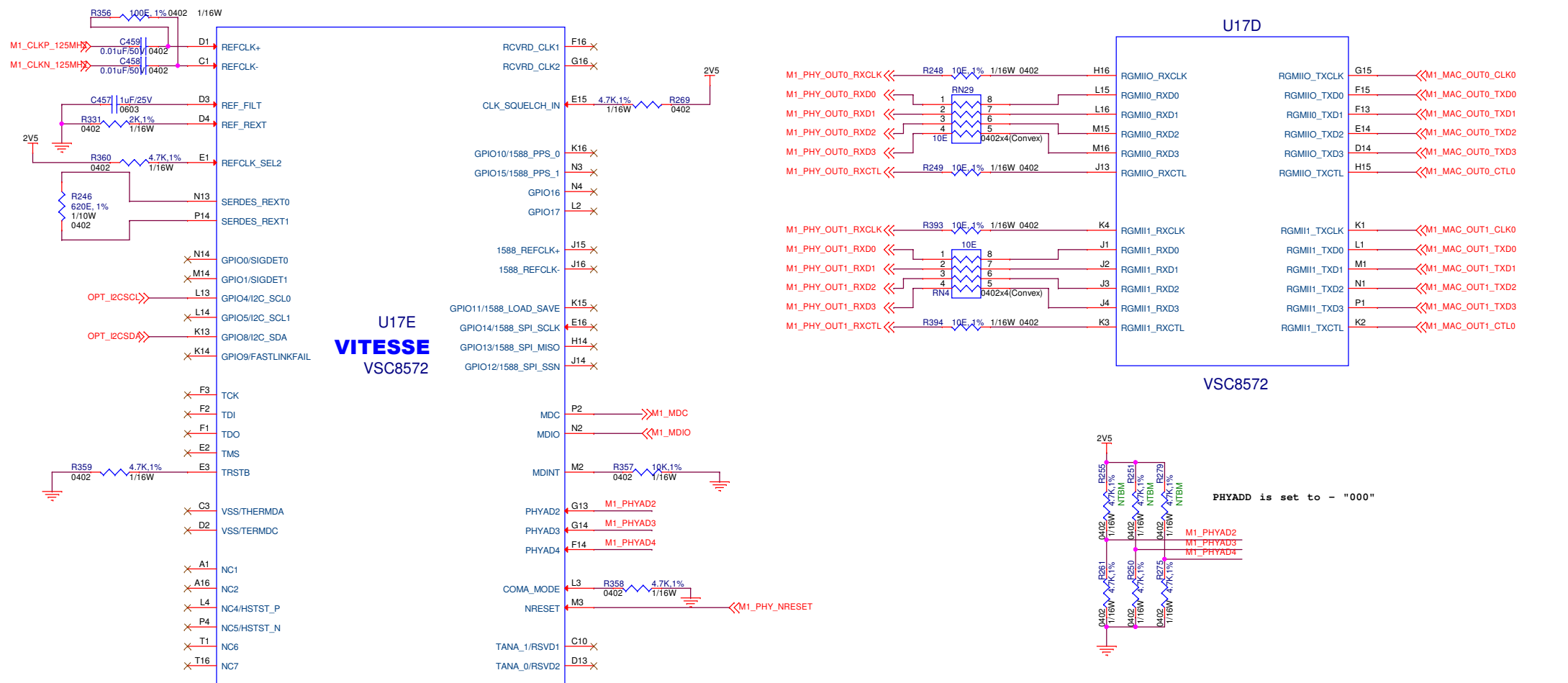


TITLE : NETWORK PROCESSOR CARD

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	PHY INTERFACE_1
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 6 OF 40 A3 REV 1.0



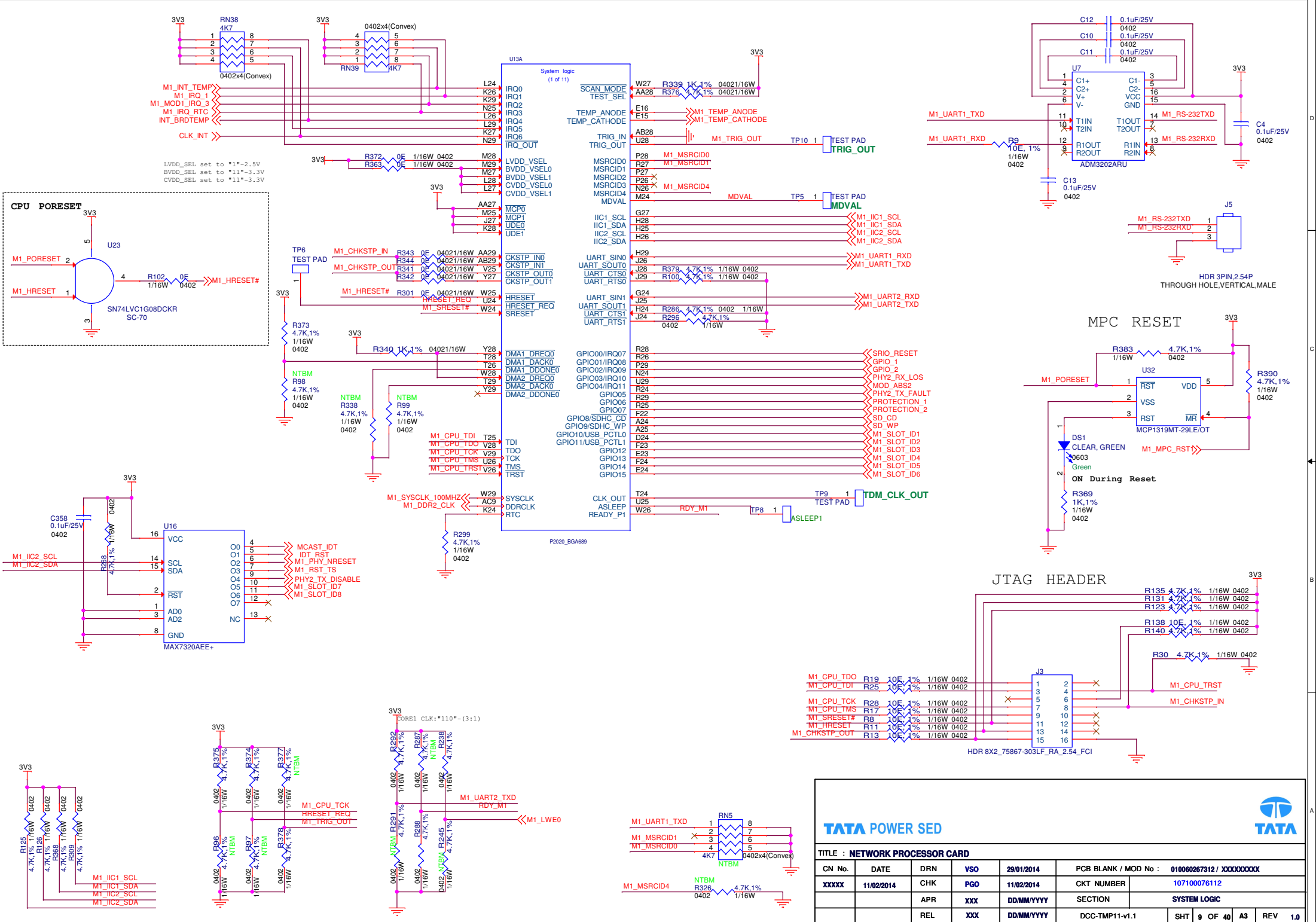
				<b>TITLE : NETWORK PROCESSOR CARD</b>				
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX		
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112		
		APR	XXX	DD/MM/YYYY	SECTION	PHY POWER & GND		
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	7 OF 40	A3 REV 1.0



PHYADD is set to - "000"

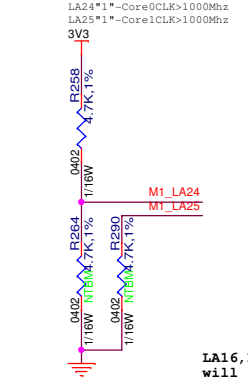
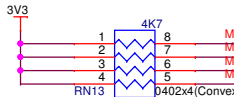
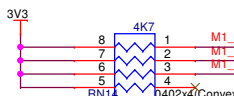
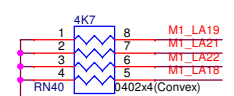
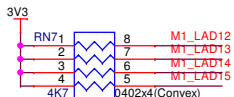
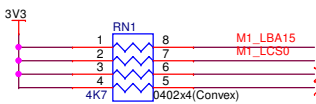
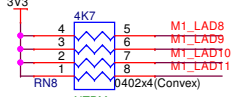
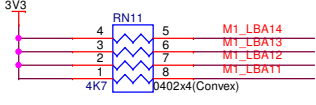
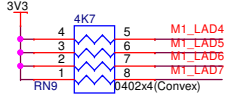
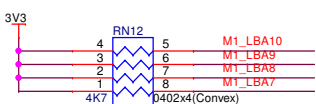
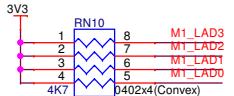
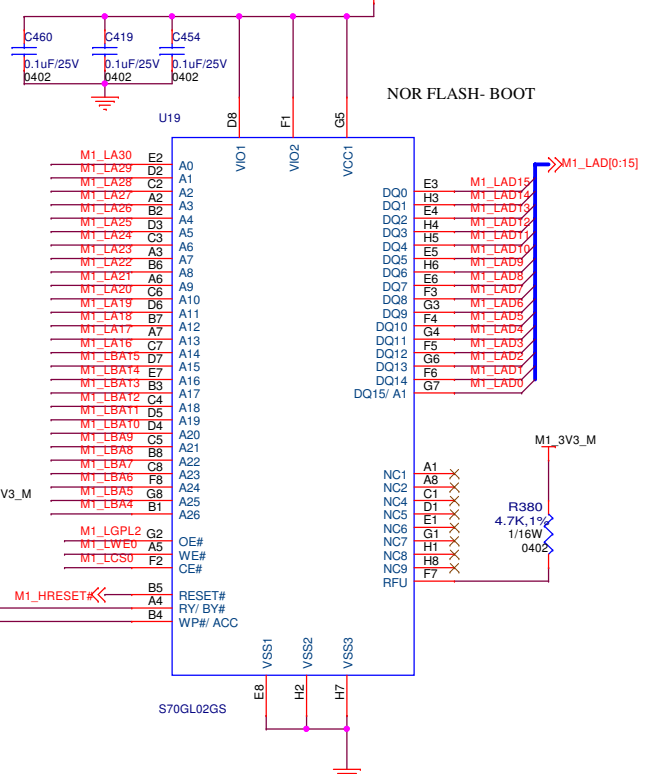
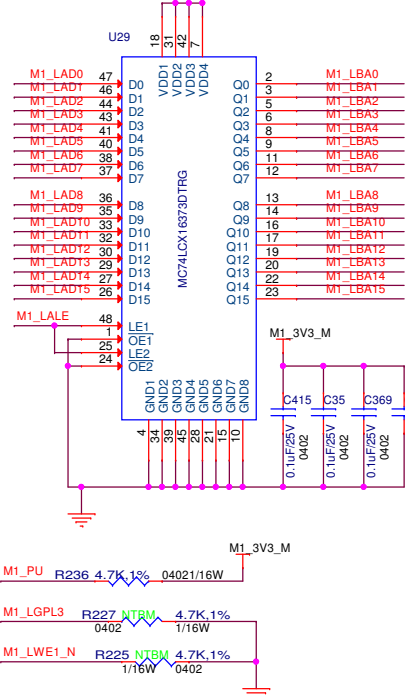
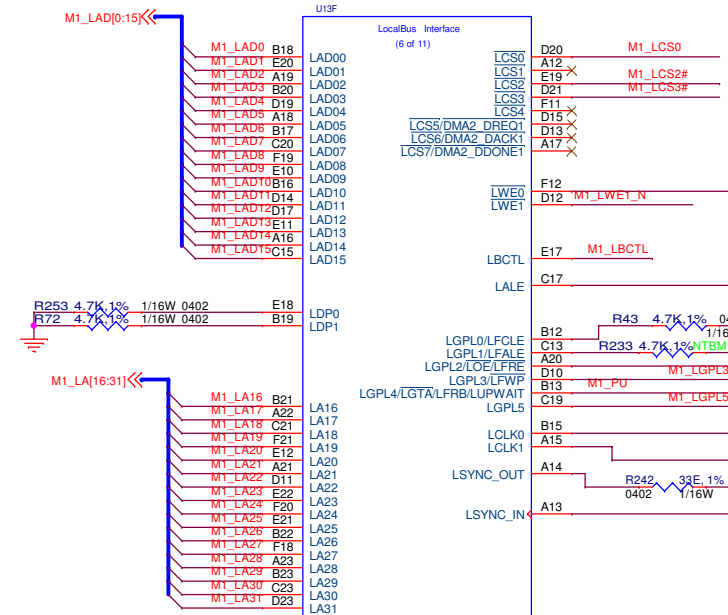
<b>TATA POWER SED</b>							
TITLE : <b>NETWORK PROCESSOR CARD</b>							
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX	
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112	
		APR	XXX	DD/MM/YYYY	SECTION	PHY INTERFACE_2	
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	8 OF 40 A3 REV 1.0



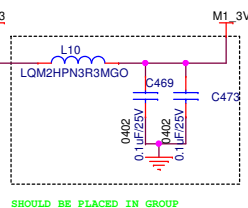
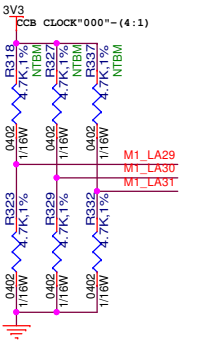
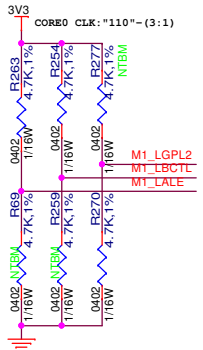
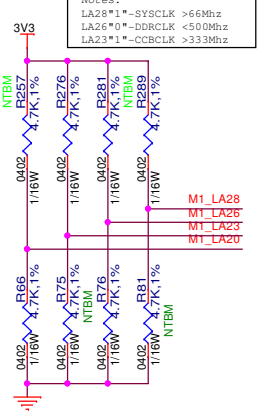


<b>TATA POWER SED</b>									
<b>TITLE : NETWORK PROCESSOR CARD</b>									
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX			
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112			
		APR	XXX	DD/MM/YYYY	SECTION	SYSTEM LOGIC			
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	9 OF 40	A3	REV 1.0

ADDRESS LATCH A [15:0]

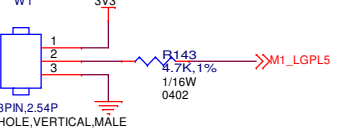


LA16,LA27"11"-Both the cores will boot independently



SHOULD BE PLACED IN GROUP

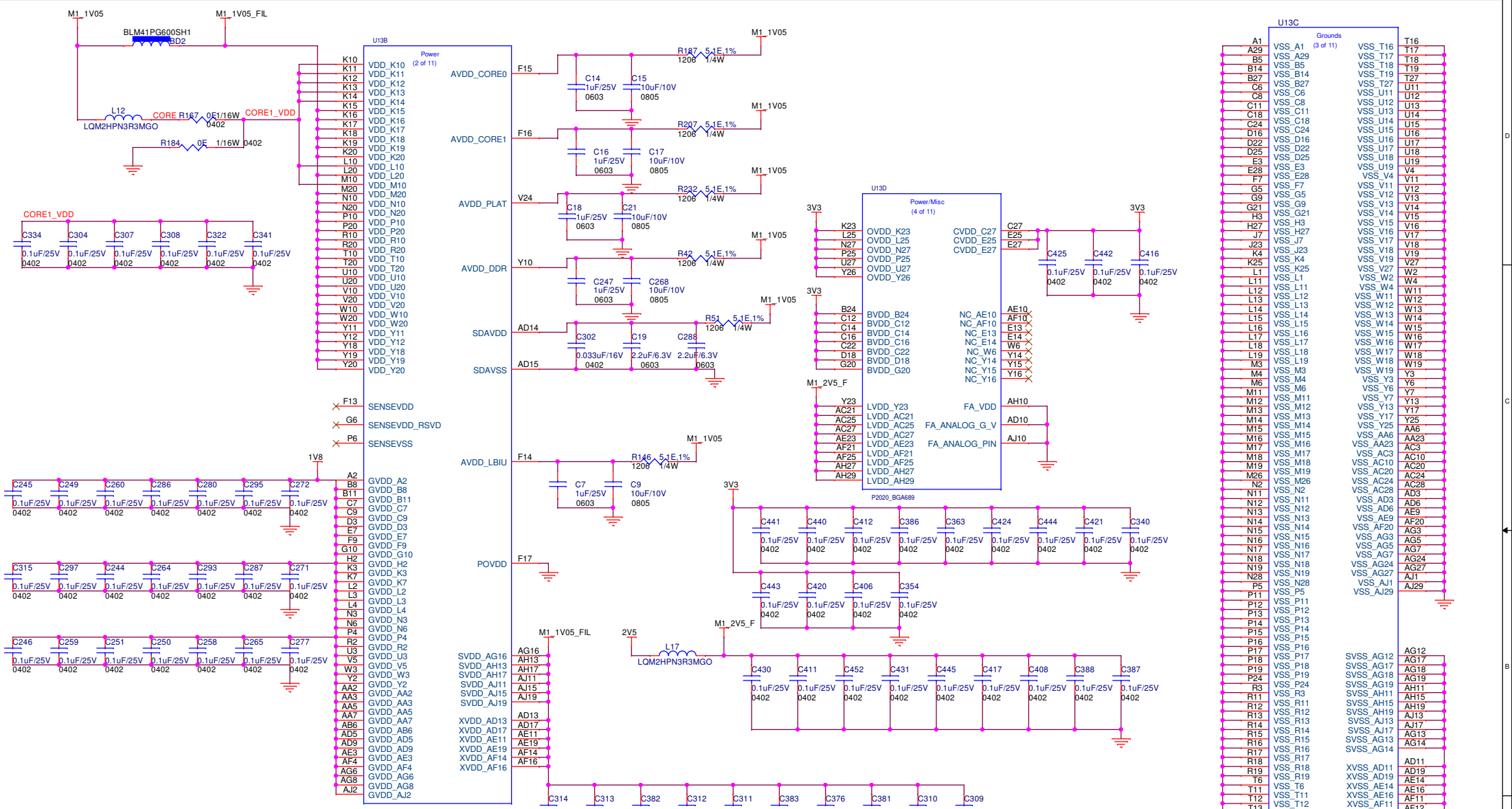
CONFIGURATION BOOT SEQ



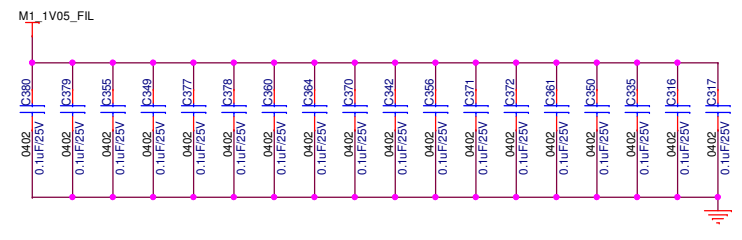
**TATA POWER SED**


TABLE TITLE : **NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	MEMORY INTERFACE
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 10 OF 40 A3 REV 1.0



Note: All Decoupling to be placed close to the Pin

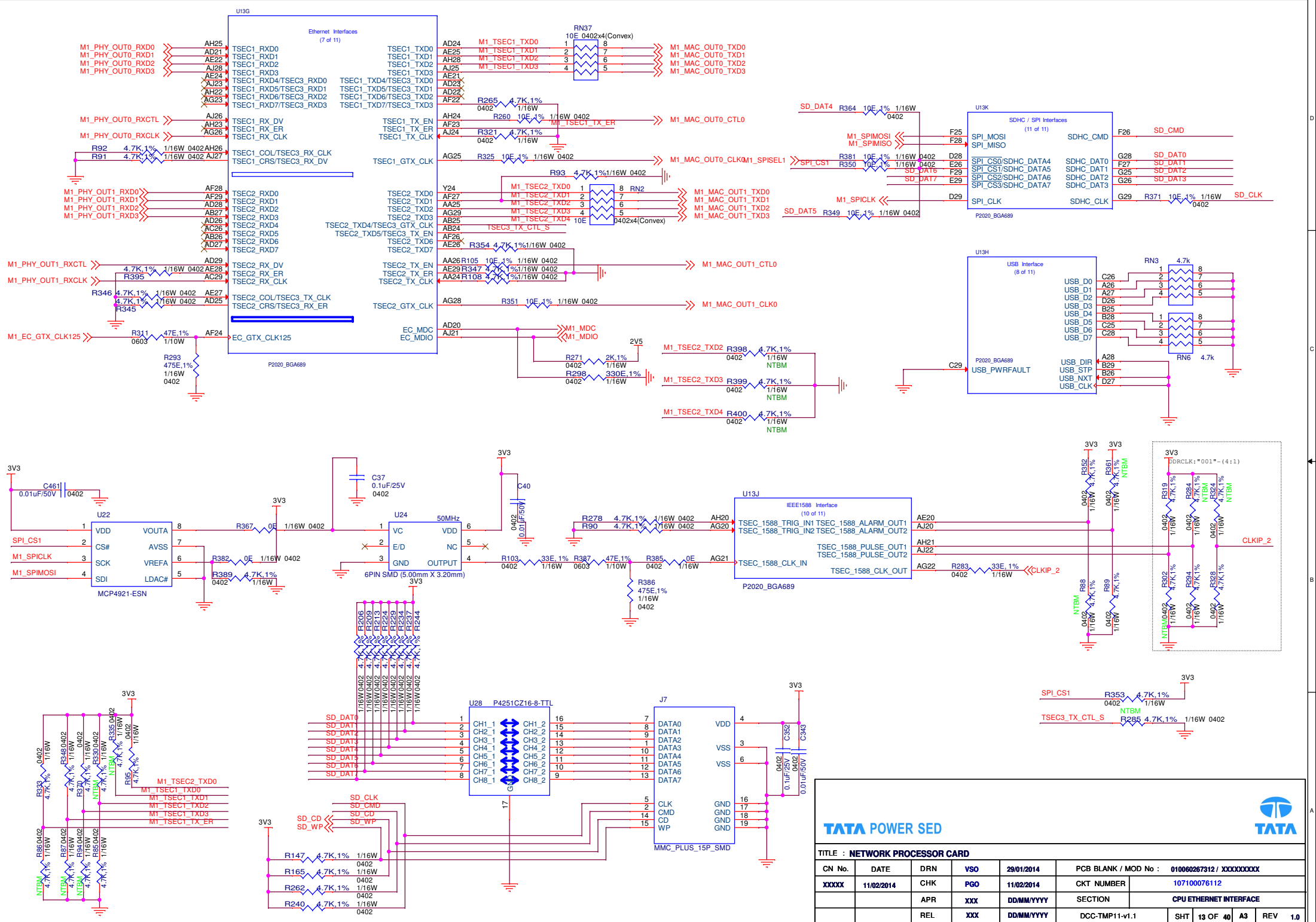




**TATA POWER SED**

**TITLE : NETWORK PROCESSOR CARD**

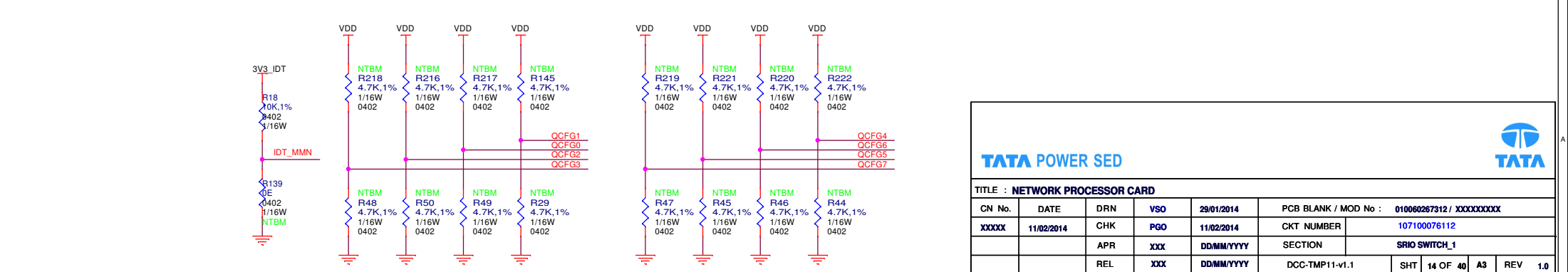
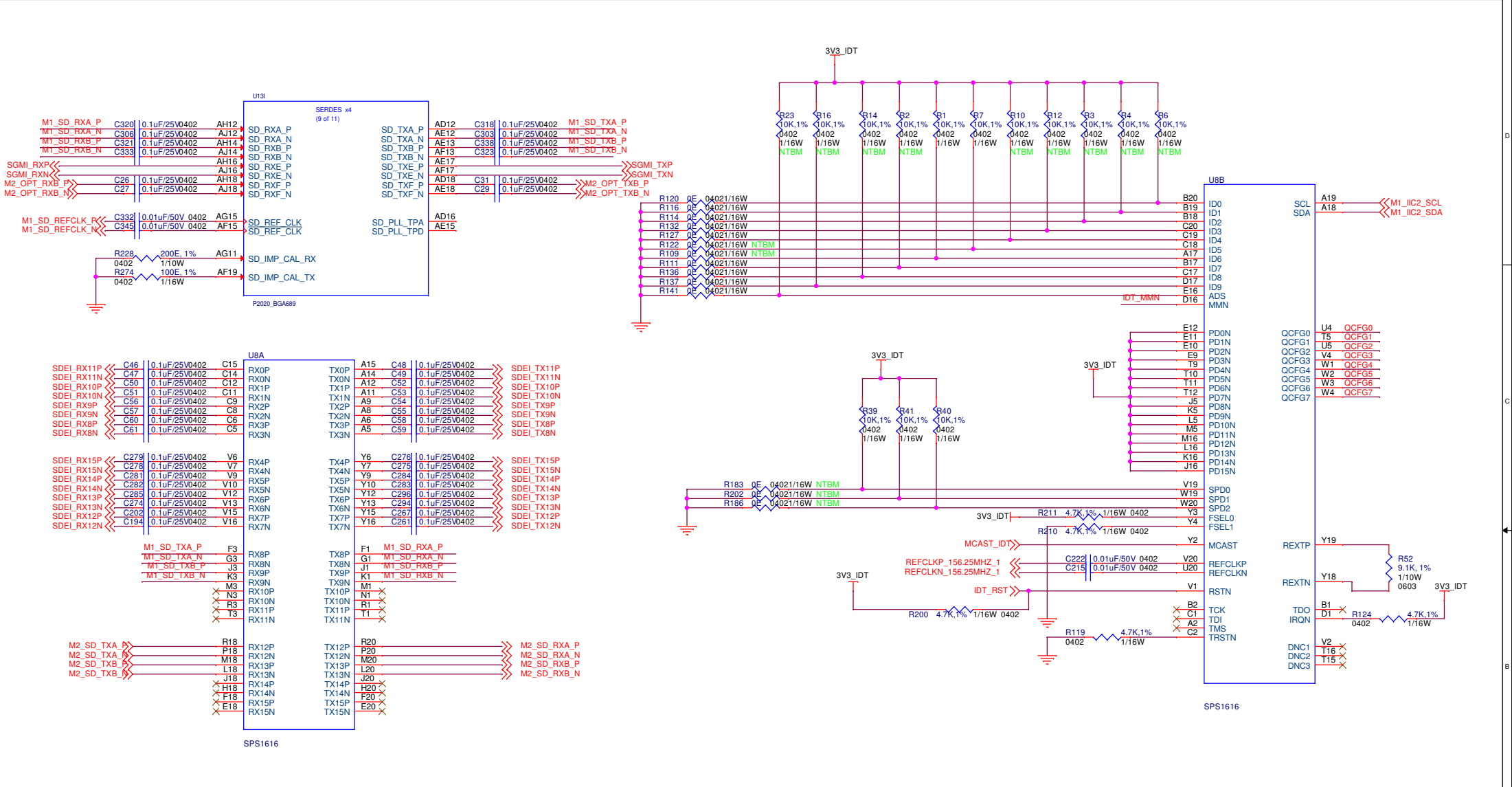
CM No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	CPU POWER
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 12 OF 40 A3 REV 1.0



**TATA POWER SED**

**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	CPU ETHERNET INTERFACE
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 13 OF 40 A3 REV 1.0

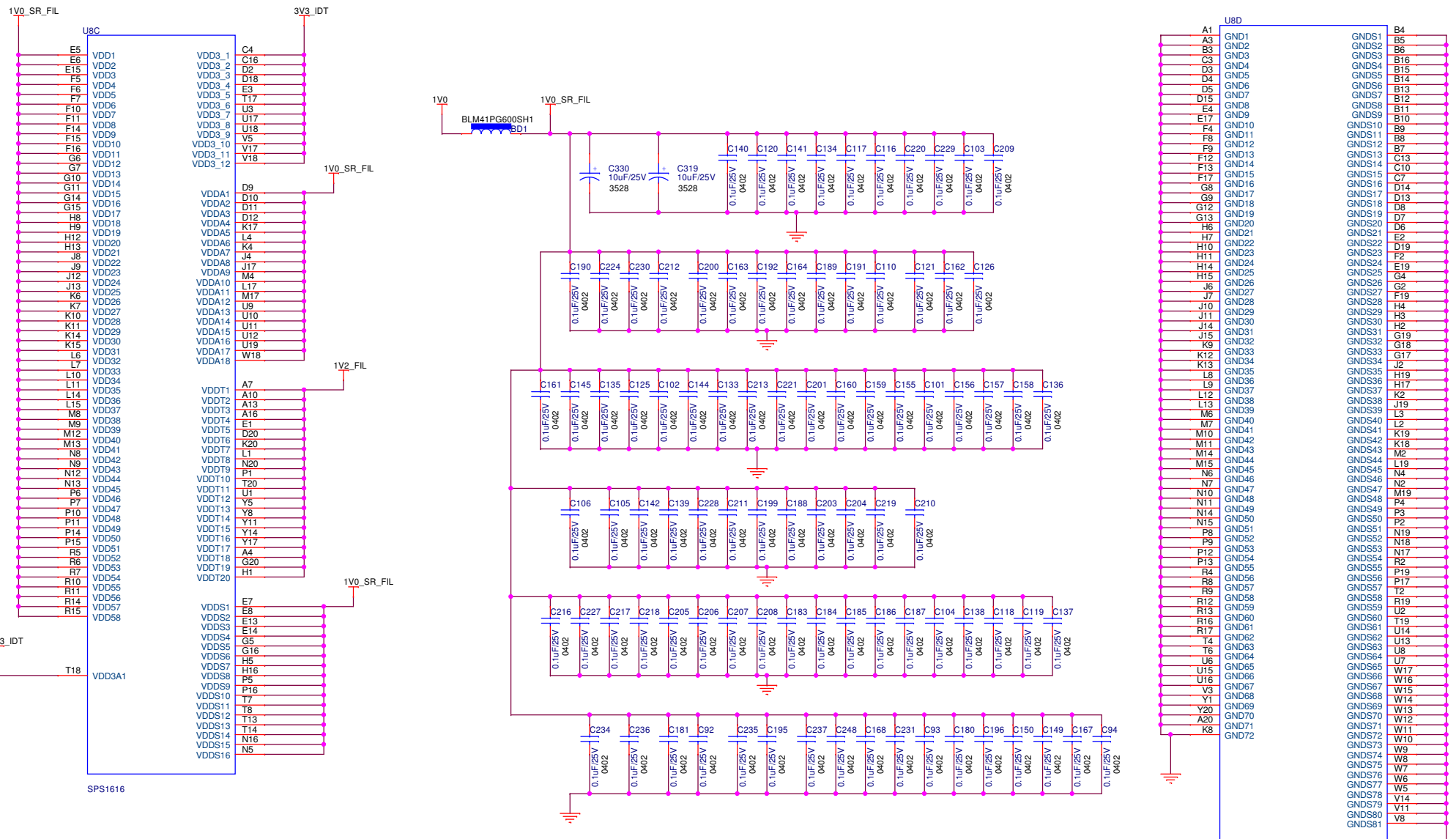


**TATA POWER SED**

**TATA**

**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	SRIO SWITCH_1
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 14 OF 40 A3 REV 1.0

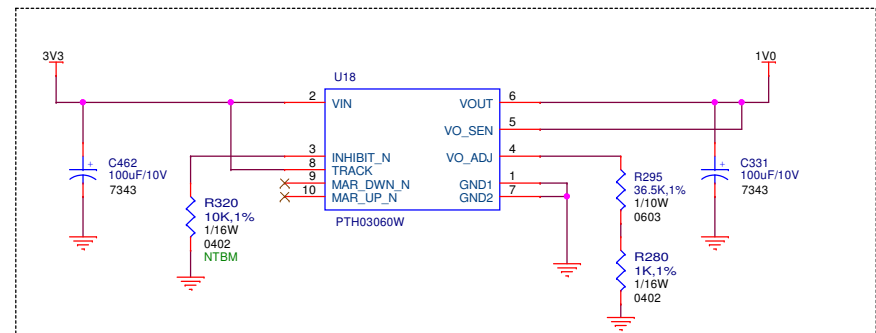
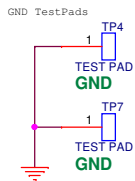
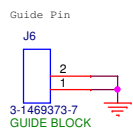
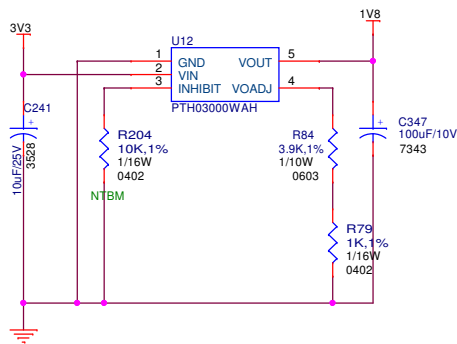
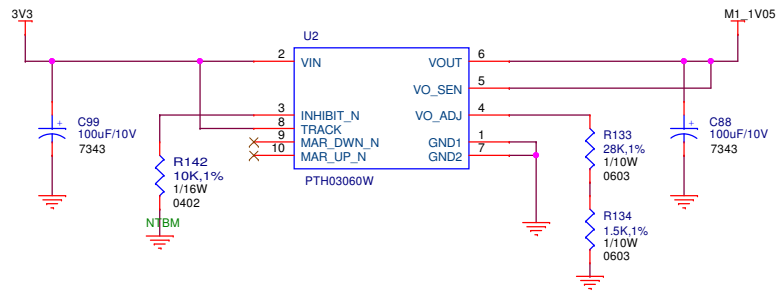
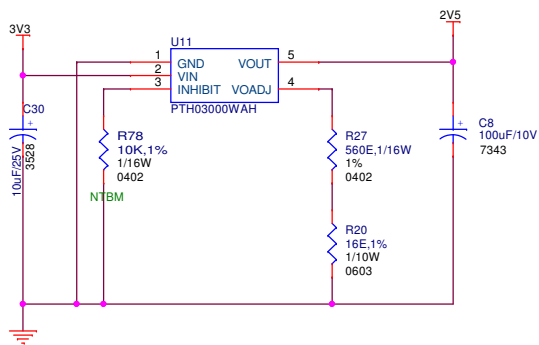


**TATA POWER SED**

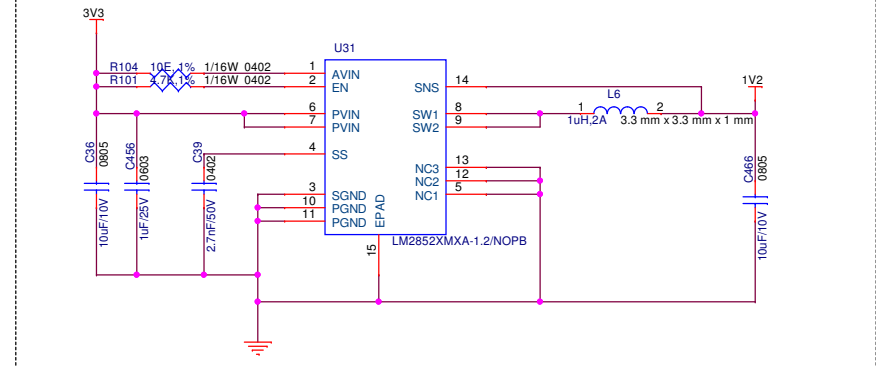
**TATA**

**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	SRIO SWITCH & GND
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 15 OF 40 A3 REV 1.0



DERIVED SUPPLY FOR SRIO SWITCH

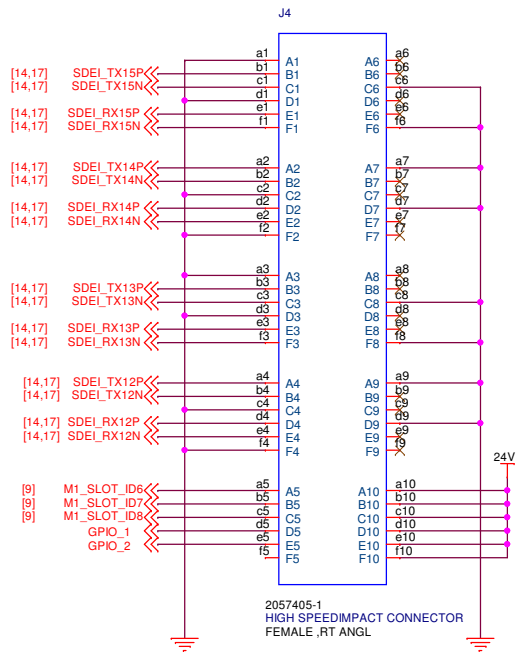
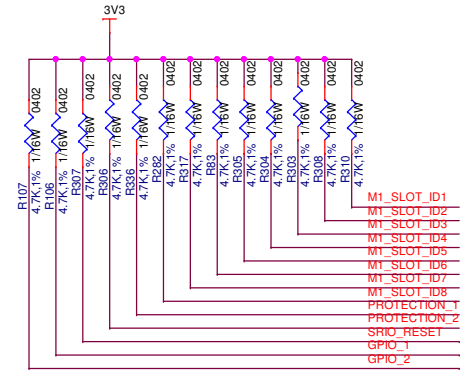
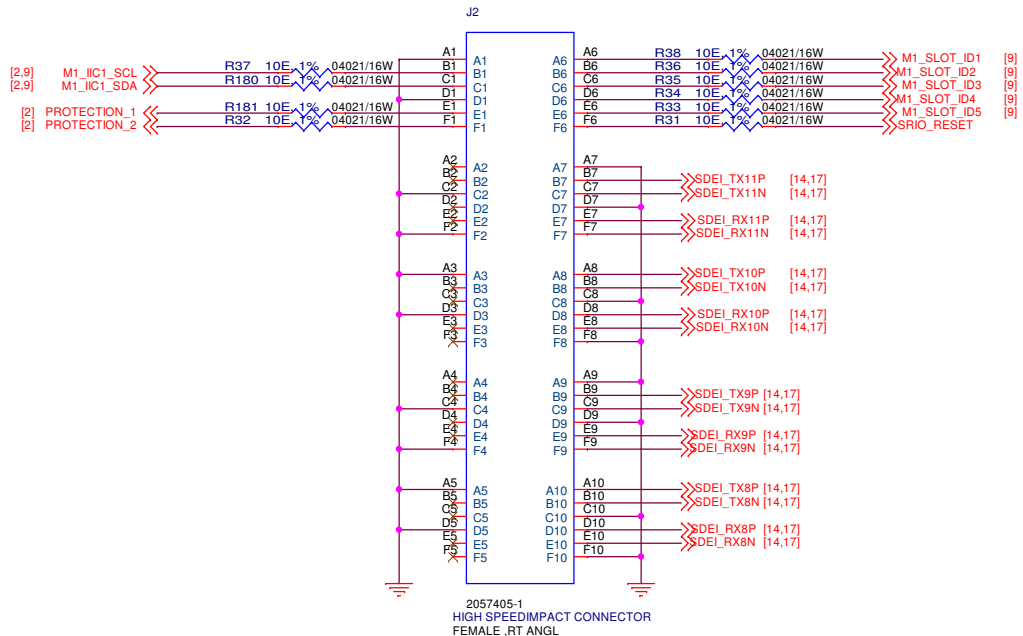


TATA POWER SED



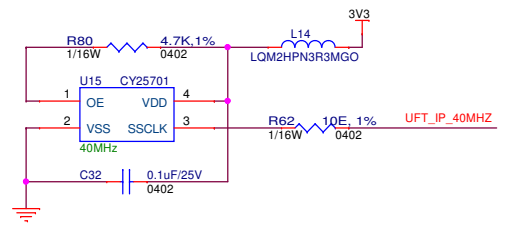
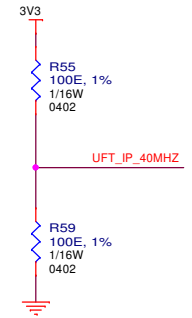
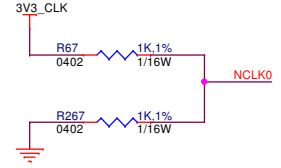
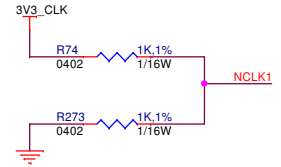
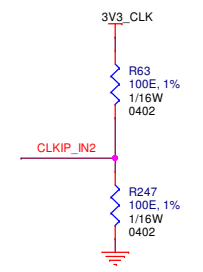
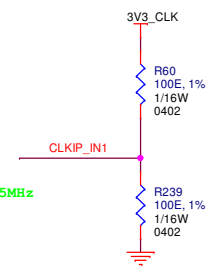
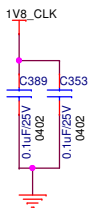
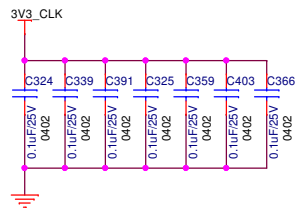
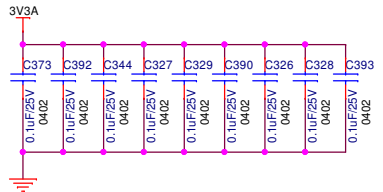
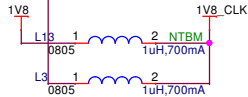
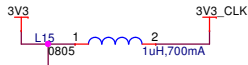
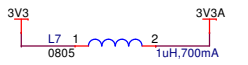
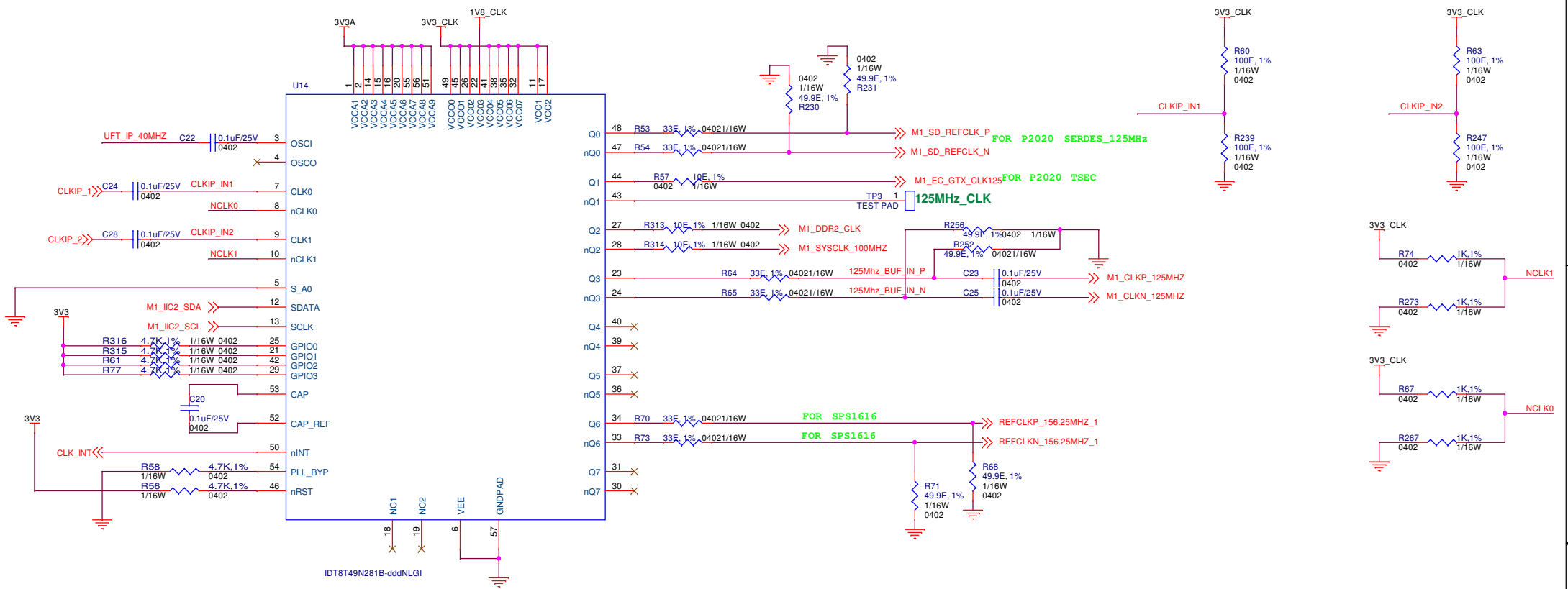
TITLE : NETWORK PROCESSOR CARD

CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	LDO'S
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 16 OF 40 A3 REV 1.0



<b>TATA POWER SED</b>									
<b>TATA</b>									
<b>TITLE : NETWORK PROCESSOR CARD</b>									
CN No.	DATE	DRN	VSO	29/01/2014	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX			
XXXX	11/02/2014	CHK	PGO	11/02/2014	CKT NUMBER	107100076112			
		APR	XXX	DD/MM/YYYY	SECTION	STACKING CONNECTOR-2			
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT	18 OF 40	A3	REV 1.0

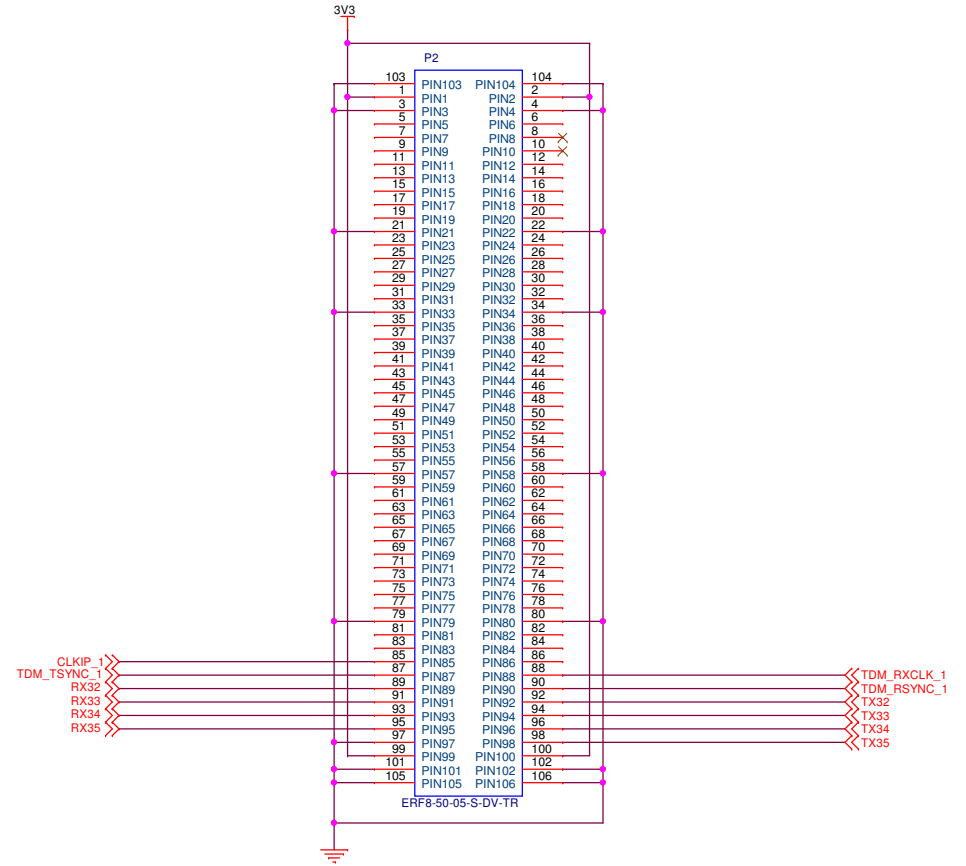
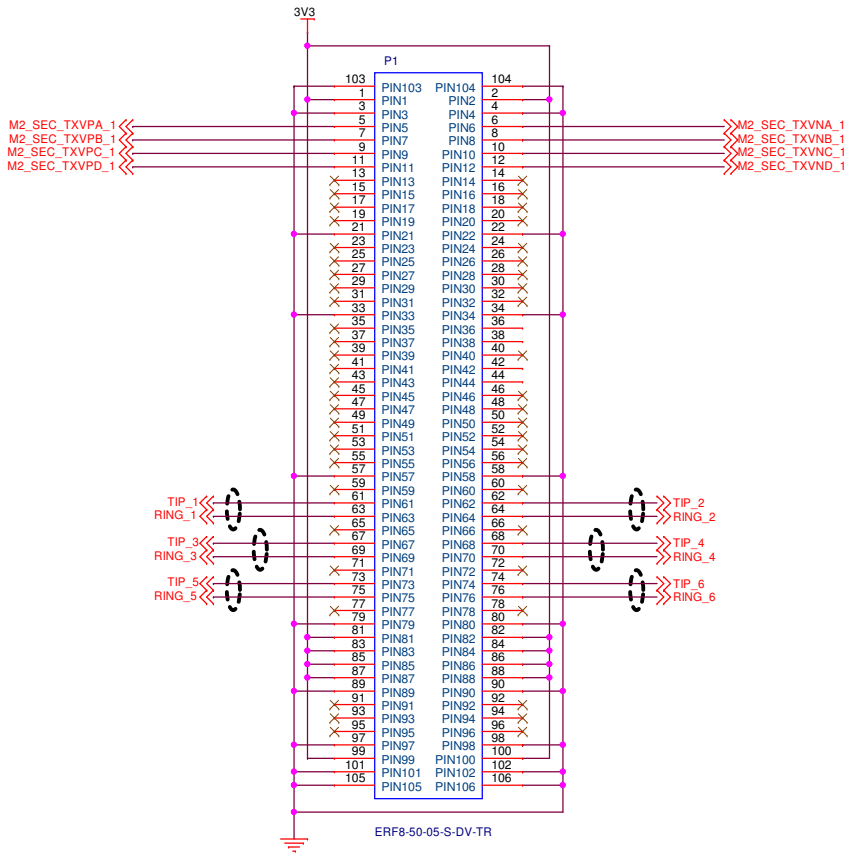





**TATA POWER SED**

**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	DD/MM/YYYY	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	DD/MM/YYYY	CHK	XXX	DD/MM/YYYY	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	XXXXXXXXXXXXXXXXXXXX
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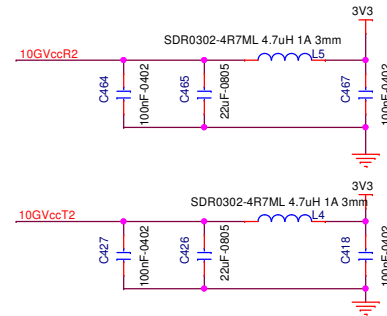
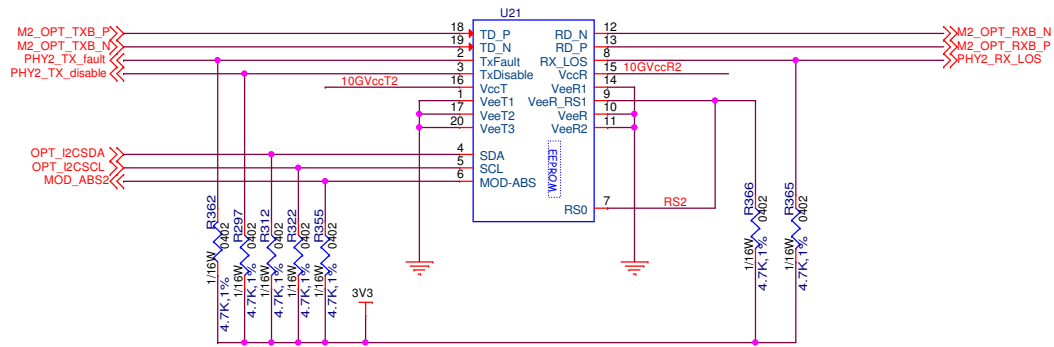




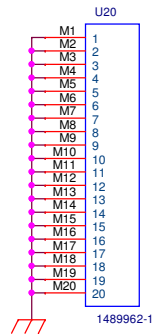
**TATA POWER**  
STRATEGIC ELECTRONICS DIVISION


**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	GK	08/04/2013	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX	
XXXX	DDMM/YYYY	CHK	SKM	08/04/2013	CKT NUMBER	107100076112	
		APR	PM	DD/MM/YYYY	SECTION	HOST BUS & POWER-Connector Interface	
		REL	DCC	DD/MM/YYYY		SHT	24 OF 40 A3 REV 1.0



**SFP Optical Cage**





**TATA POWER SED**

**TITLE : NETWORK PROCESSOR CARD**

CN No.	DATE	DRN	VSO	DD/MM/YYYY	PCB BLANK / MOD No :	010060267312 / XXXXXXXXX
XXXX	DD/MM/YYYY	CHK	XXX	DD/MM/YYYY	CKT NUMBER	107100076112
		APR	XXX	DD/MM/YYYY	SECTION	XXXXXXXXXXXXXXXXXXXX
		REL	XXX	DD/MM/YYYY	DCC-TMP11-v1.1	SHT 32 OF 40 A3 REV 1.0