T104XRDB

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Version Control

Version	Date	Modifications
V0.1	2014/10	First release of Schematics
V1.0	2014/12	Released to Manufacturing

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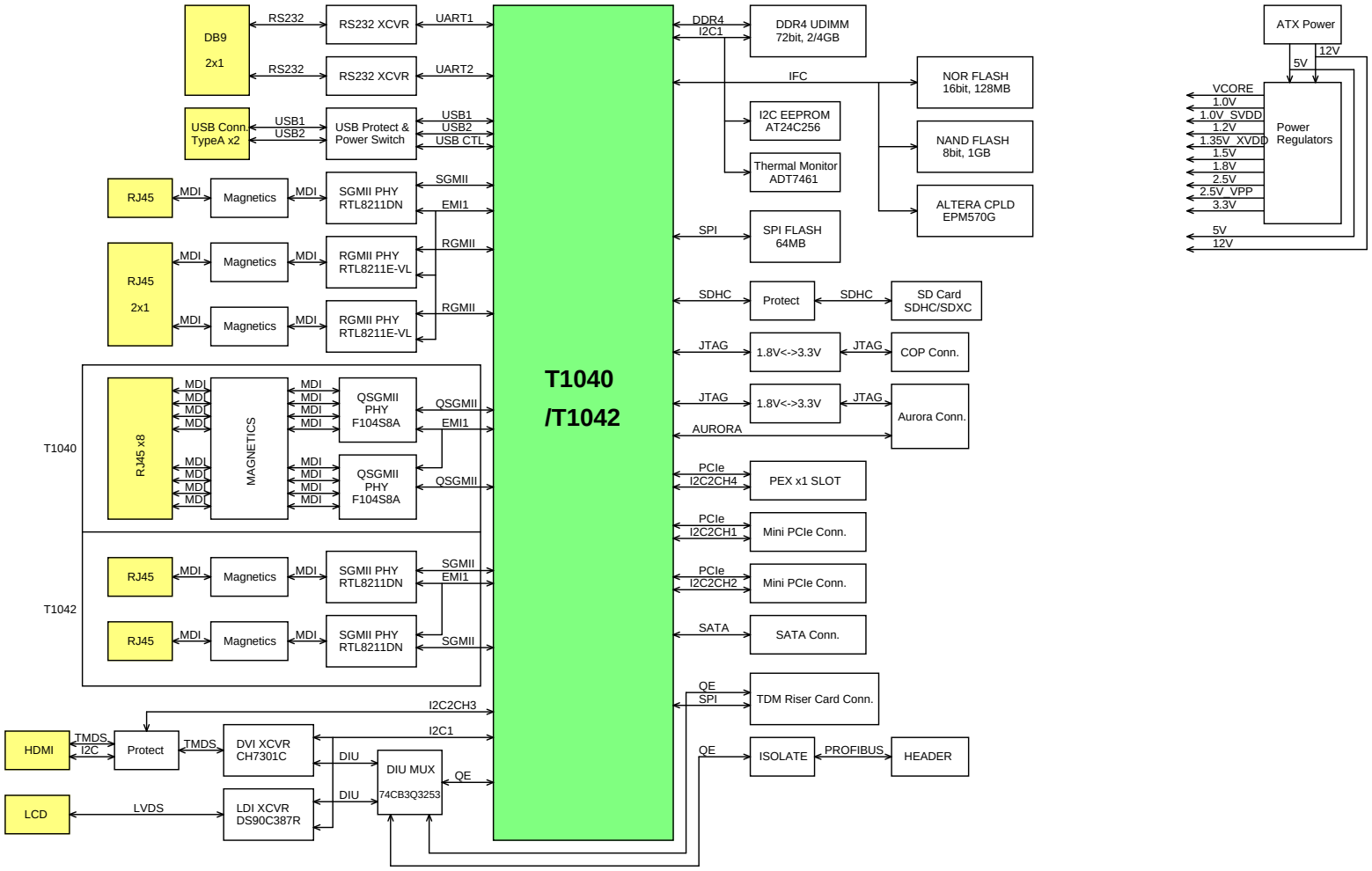
SYSTEM BLOCK DIAGRAM



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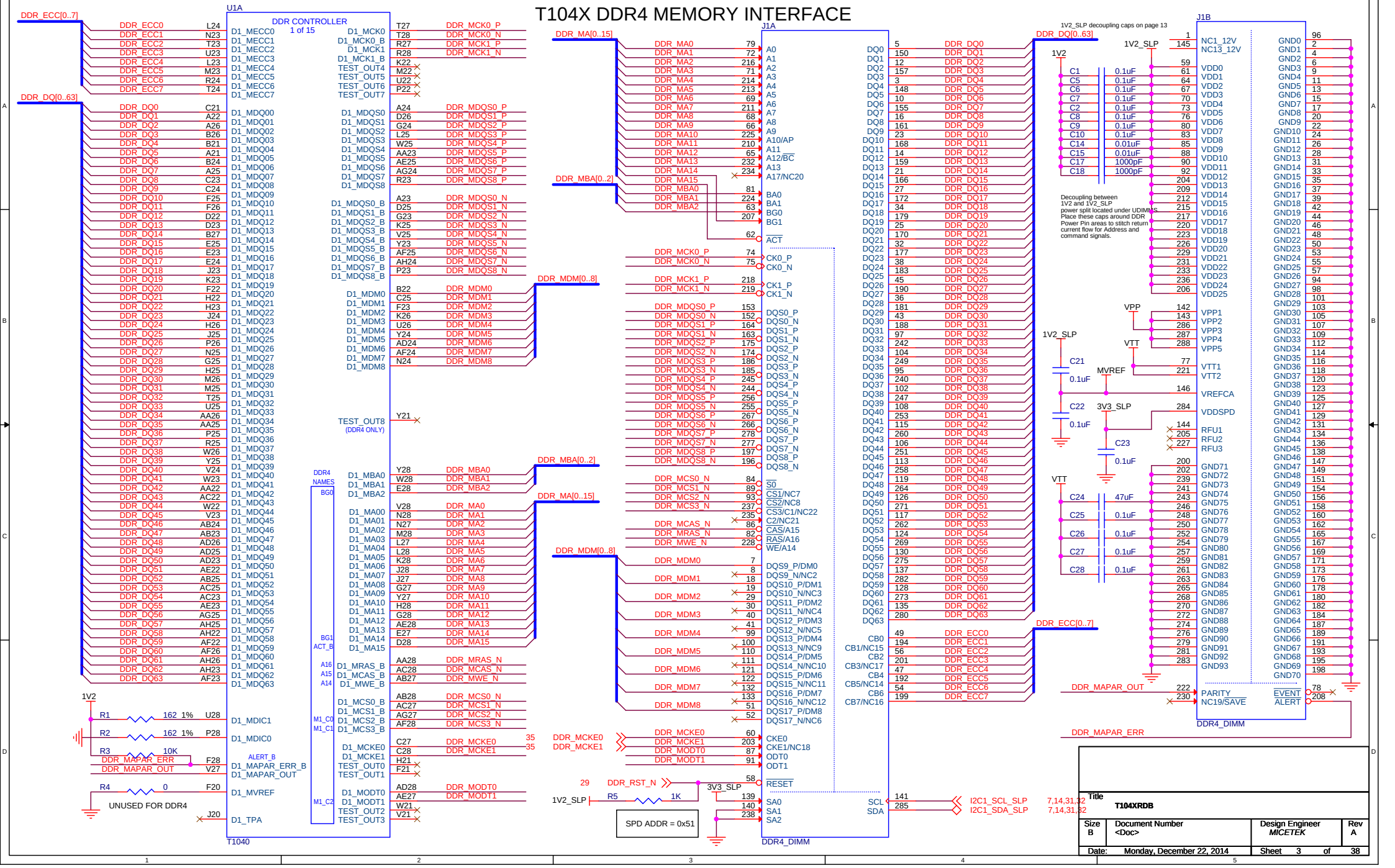
T104X DDR4 MEMORY INTERFACE



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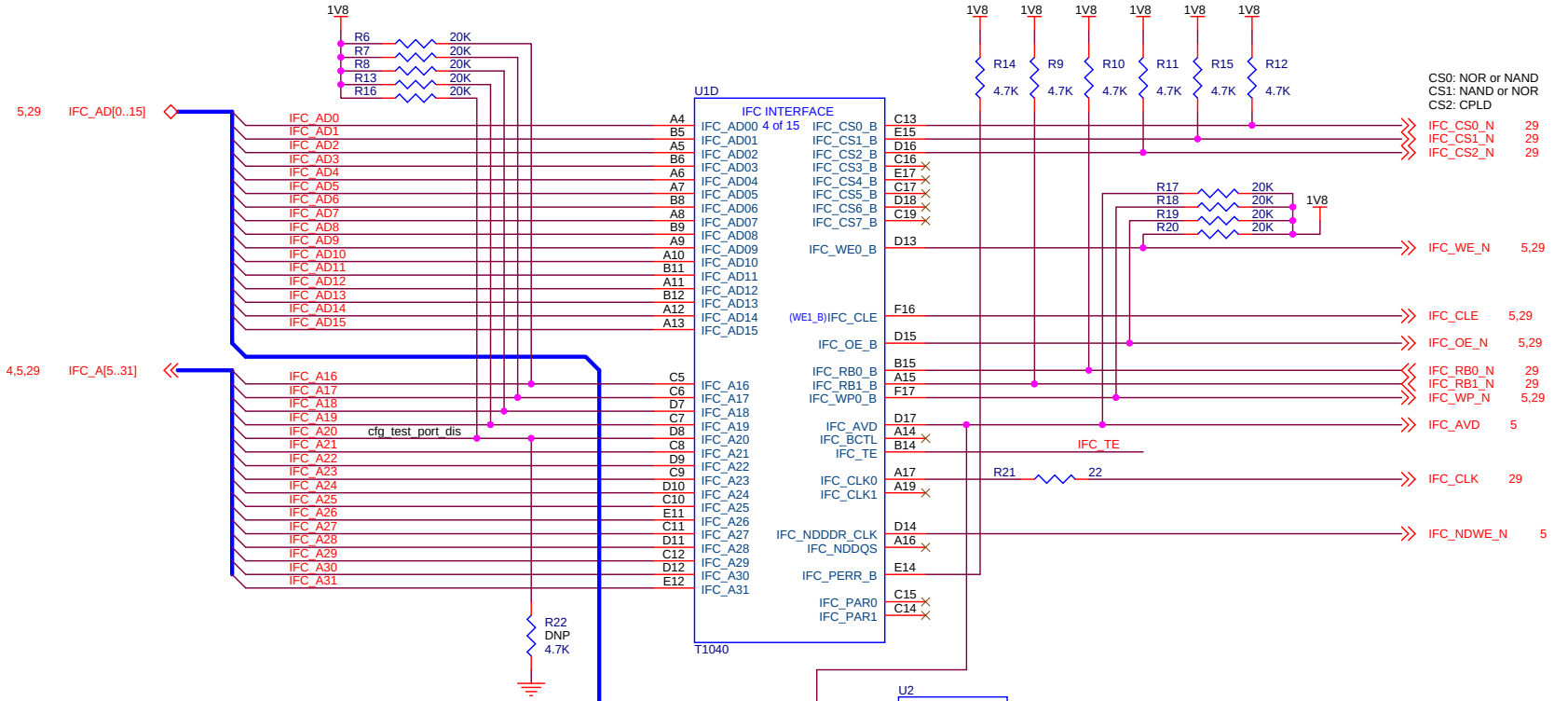
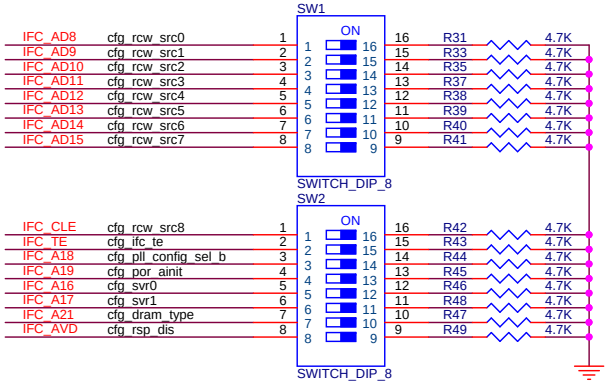
T104X IFC INTERFACE



T104X RESET CONFIGURATION

cfg_rcw_src[0:8]
0_0010_0111: NOR FLASH BOOT
0_0100_0000: SD CARD BOOT
0_0100_0101: SPI BOOT
1_0001_1001: NAND FLASH BOOT



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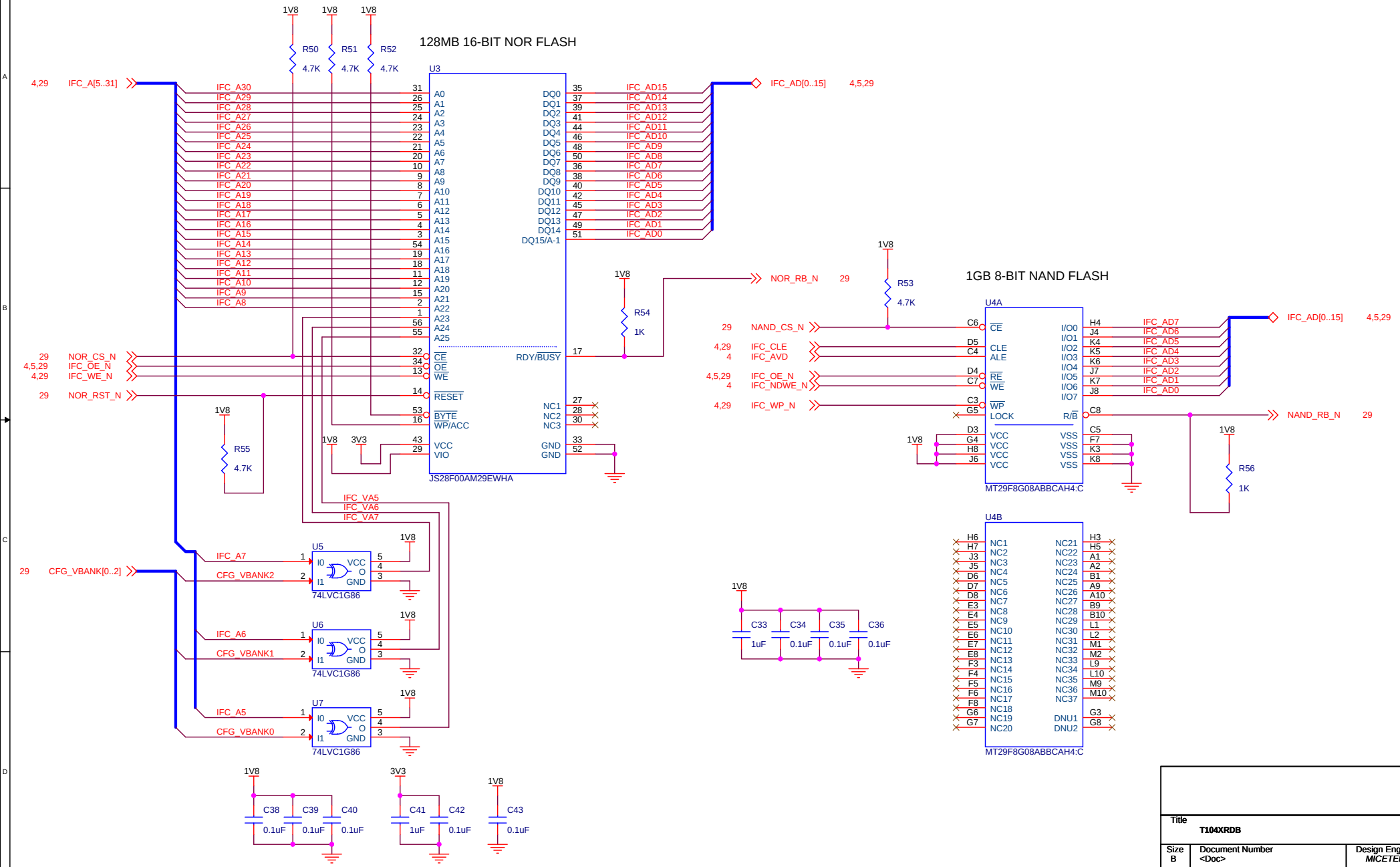
T104X NOR and NAND FLASH INTERFACE



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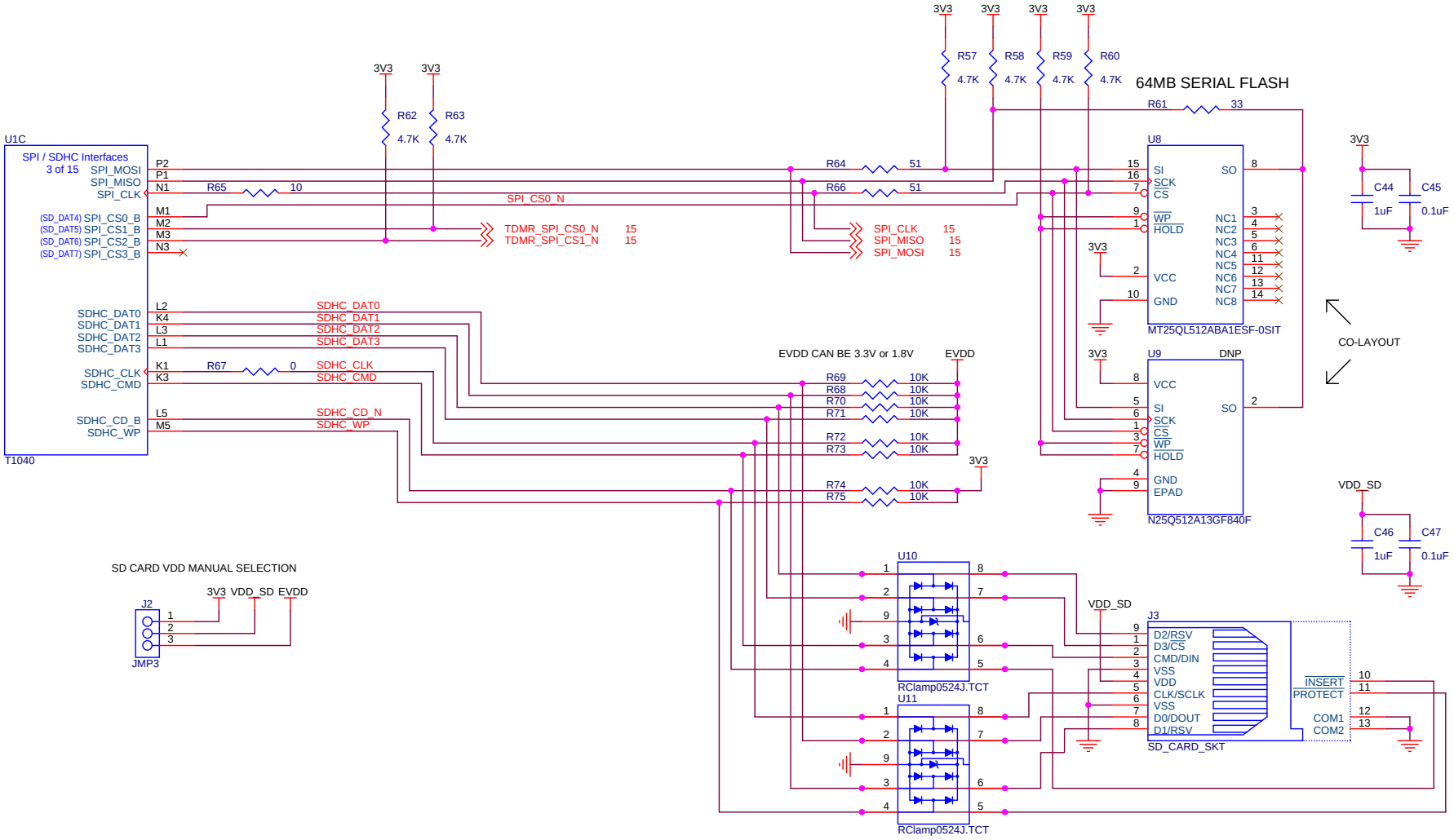
T104X SPI FLASH and SDHC INTERFACE



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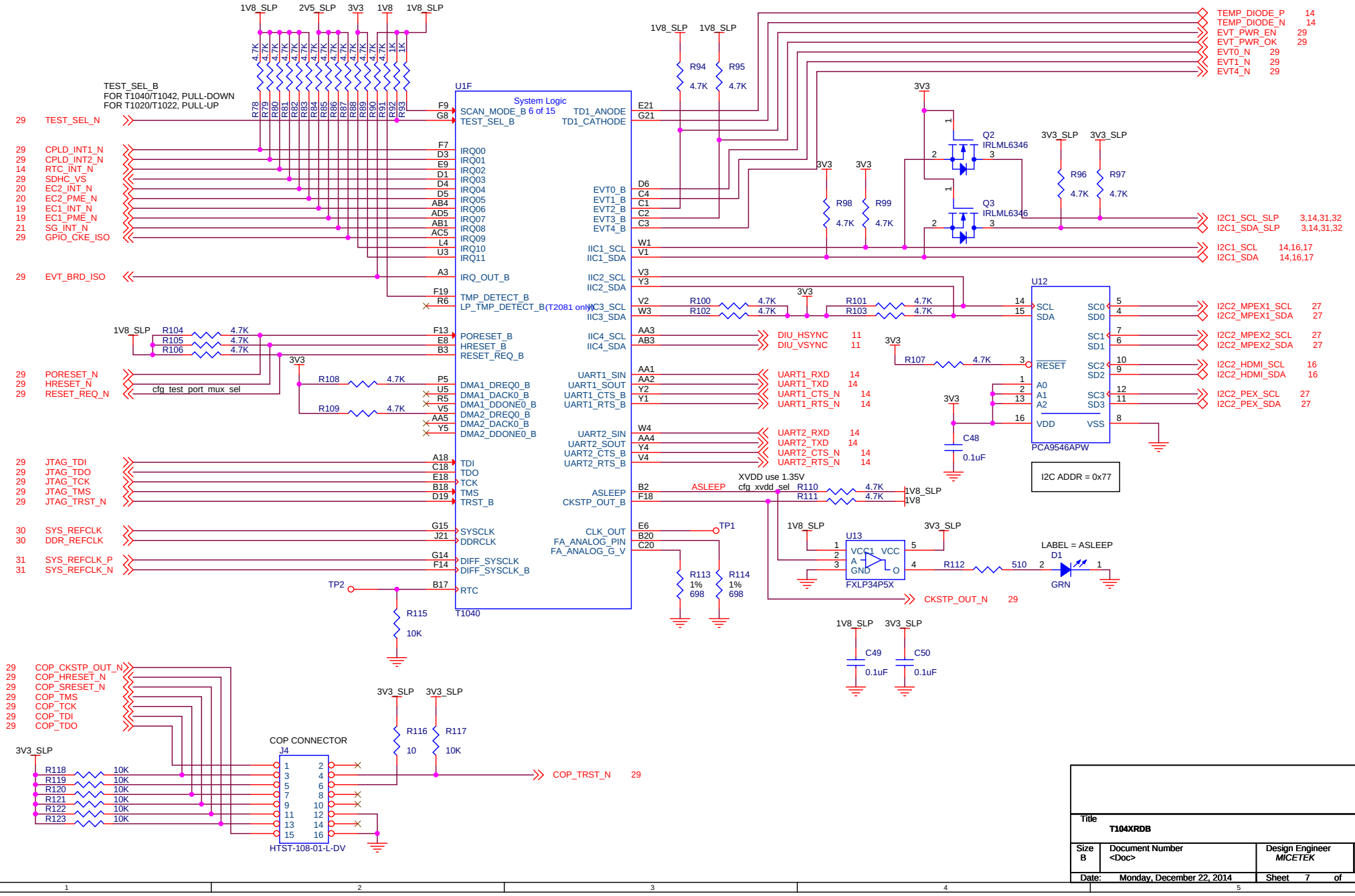
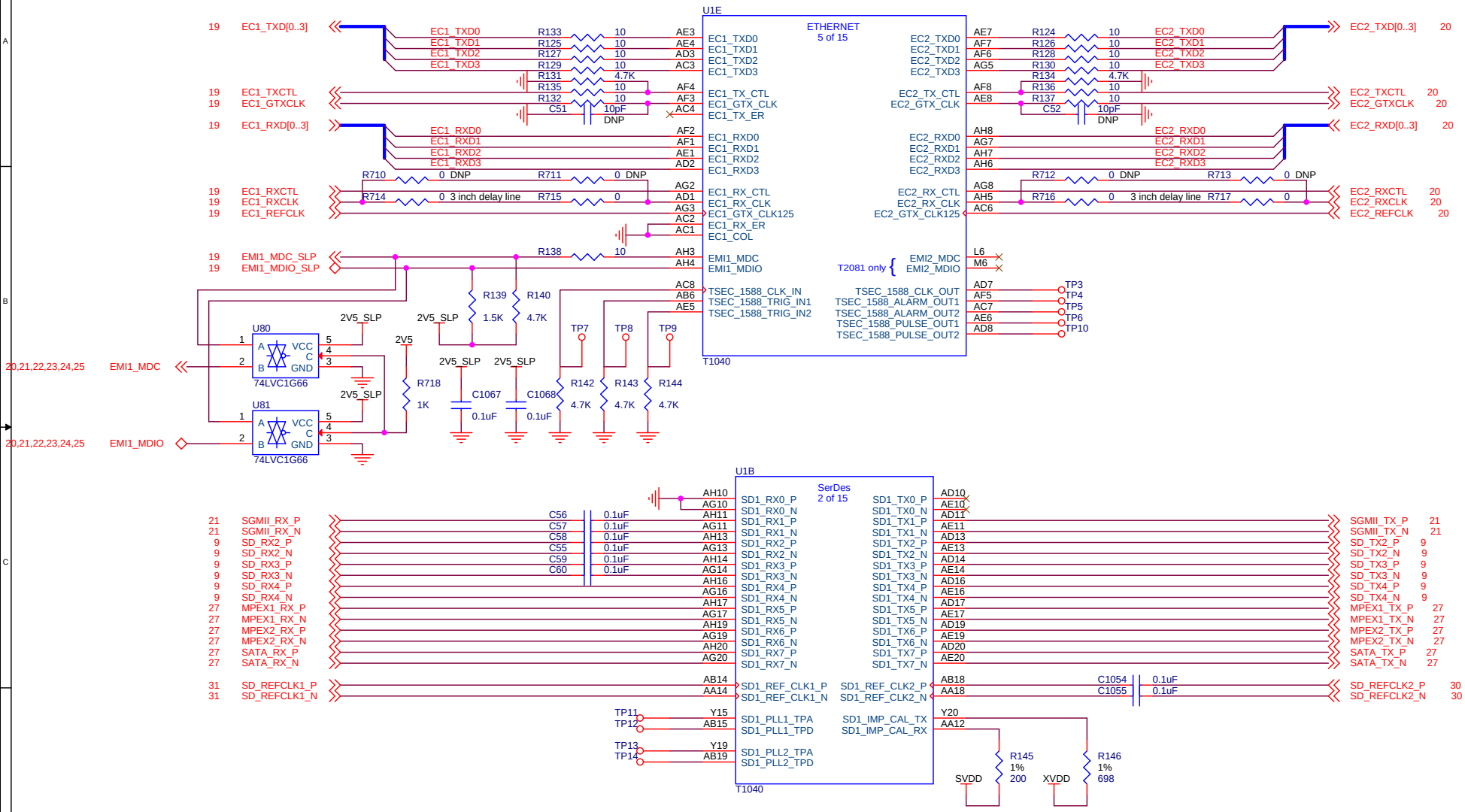
T104X SYSTEM LOGIC INTERFACE



T104X ETHERNET and SERDES INTERFACE



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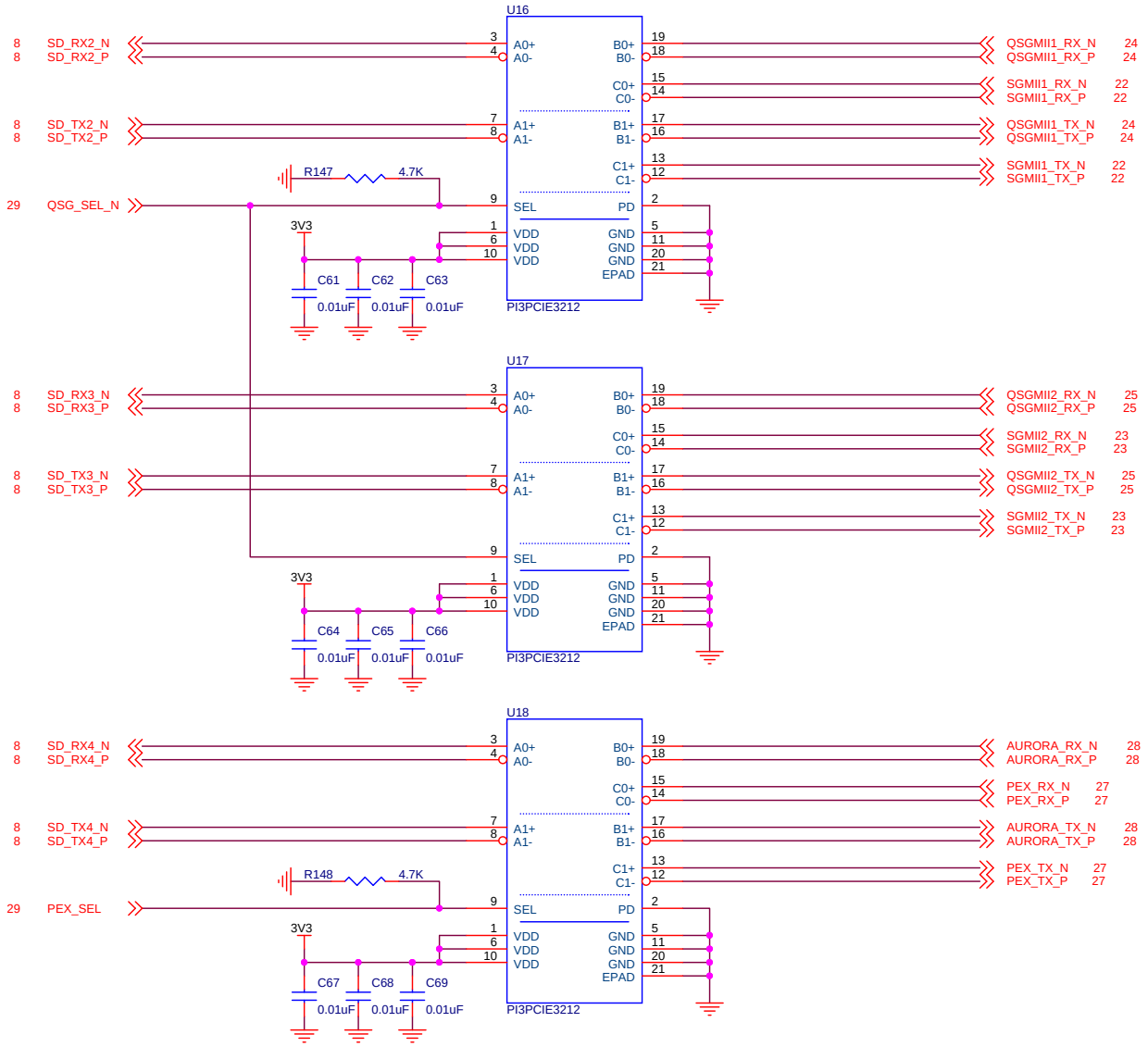
SERDES and MDIO MUX/DEMUX SWITCHs



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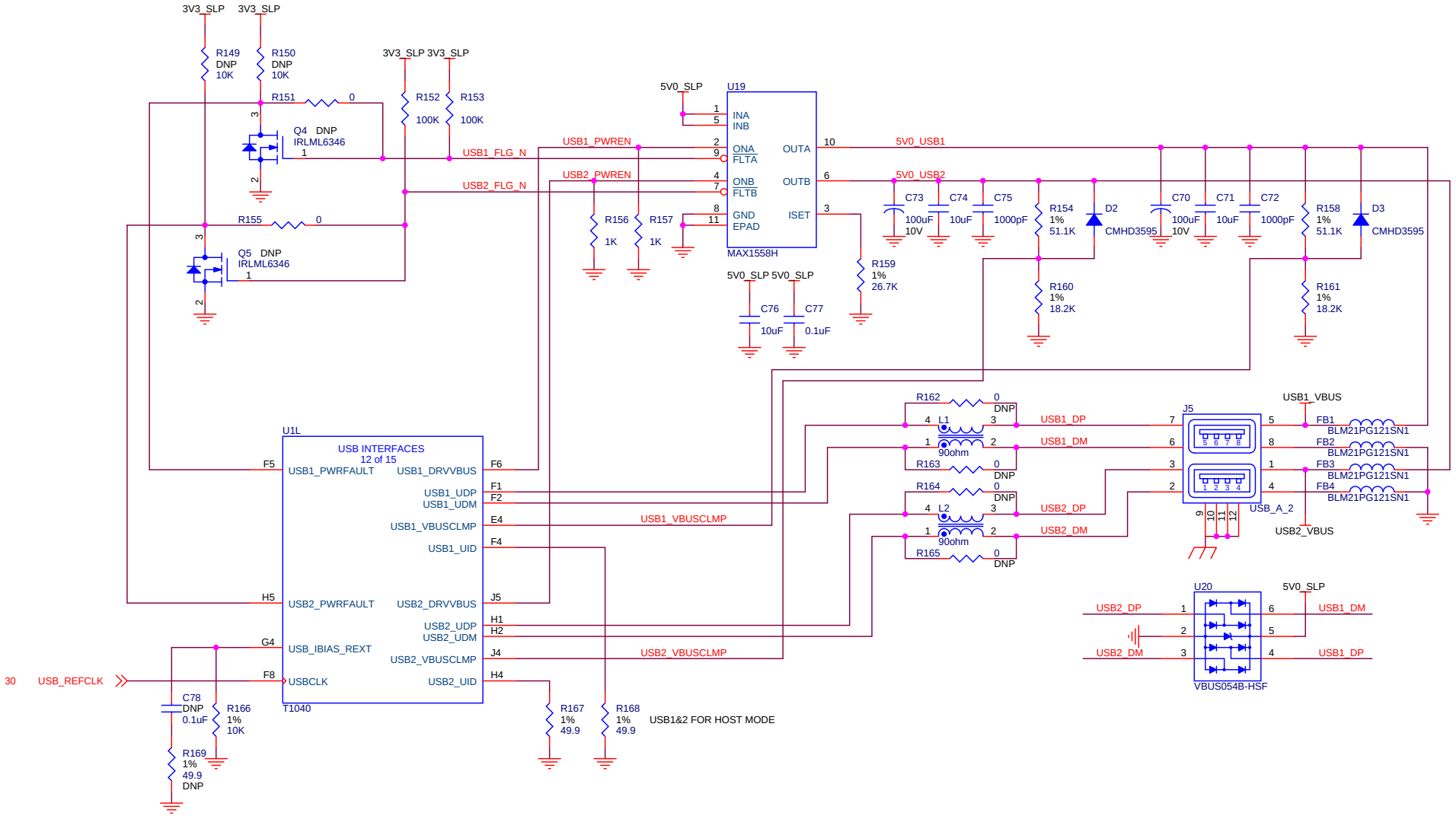
T104X USB INTERFACE



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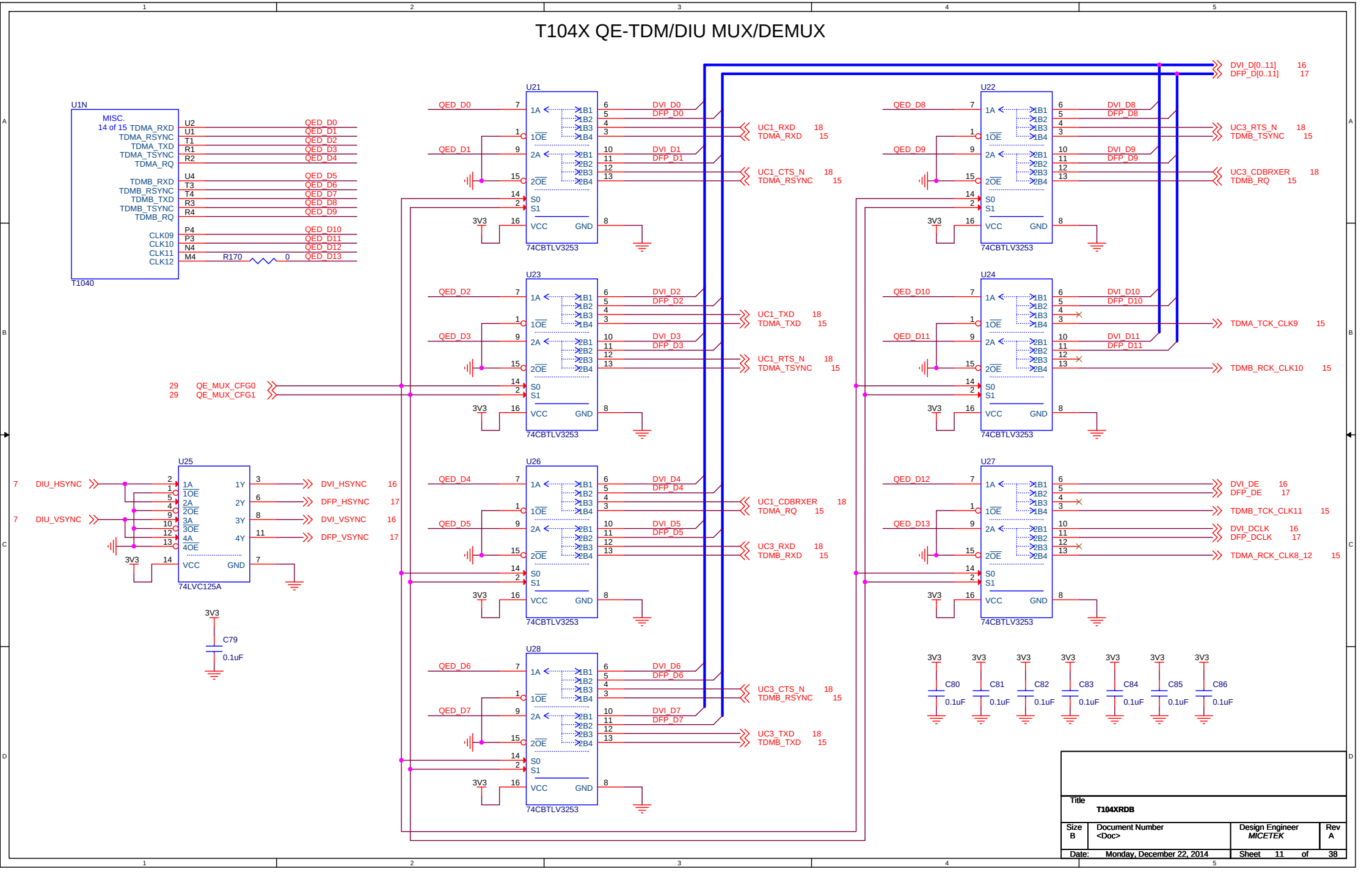
T104X QE-TDM/DIU MUX/DEMUX



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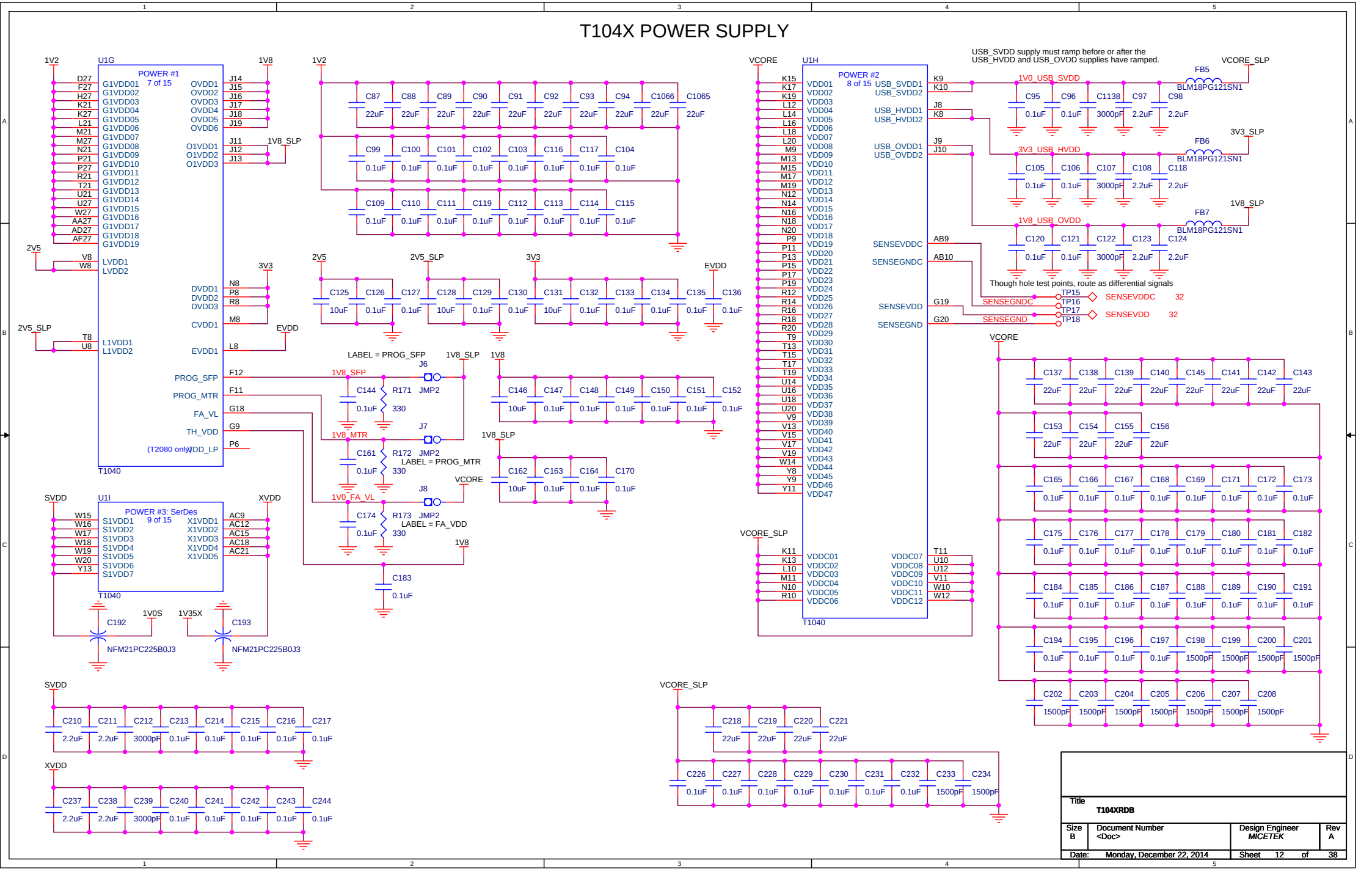
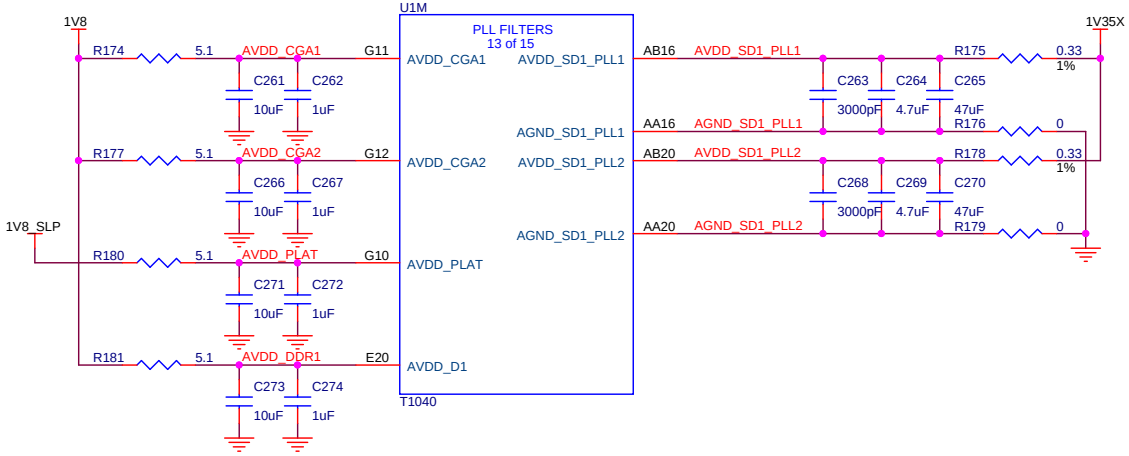
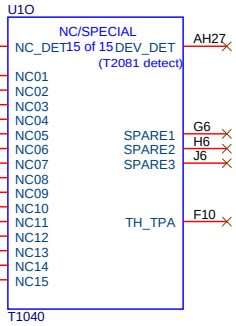
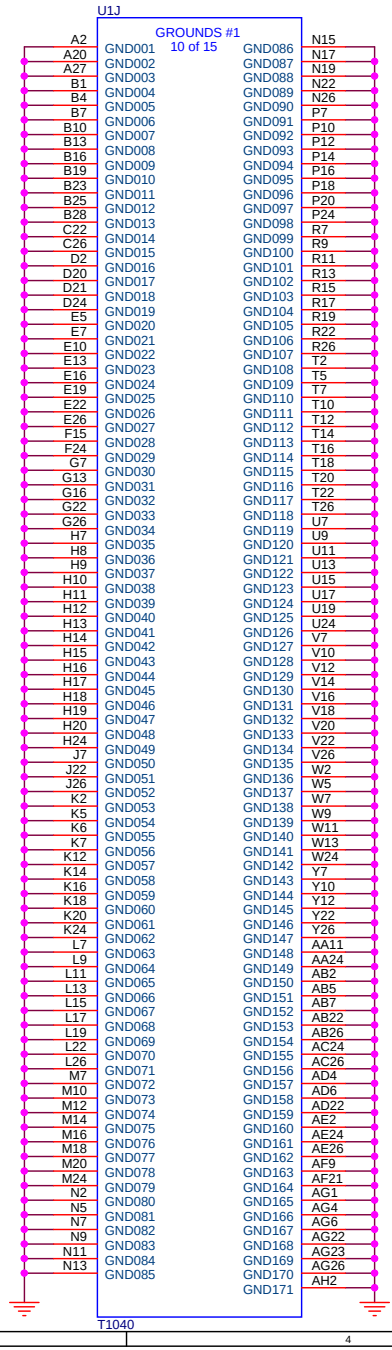
T104X POWER SUPPLY

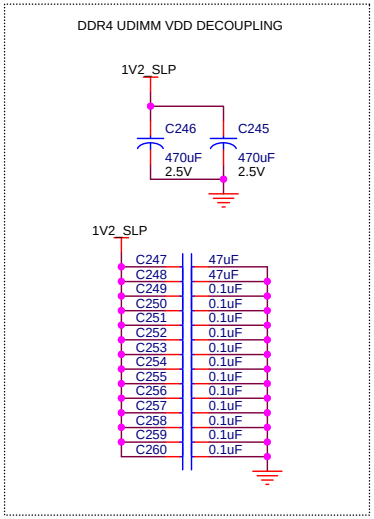


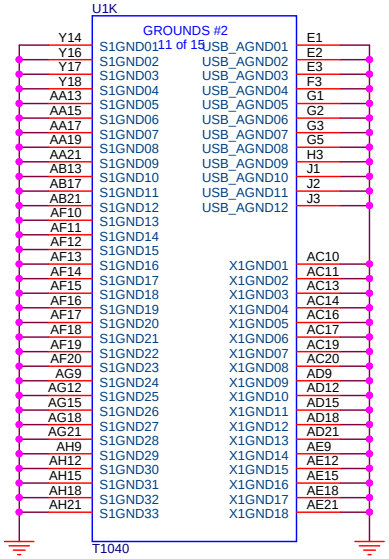
T104X PLL FILTERs and GROUND











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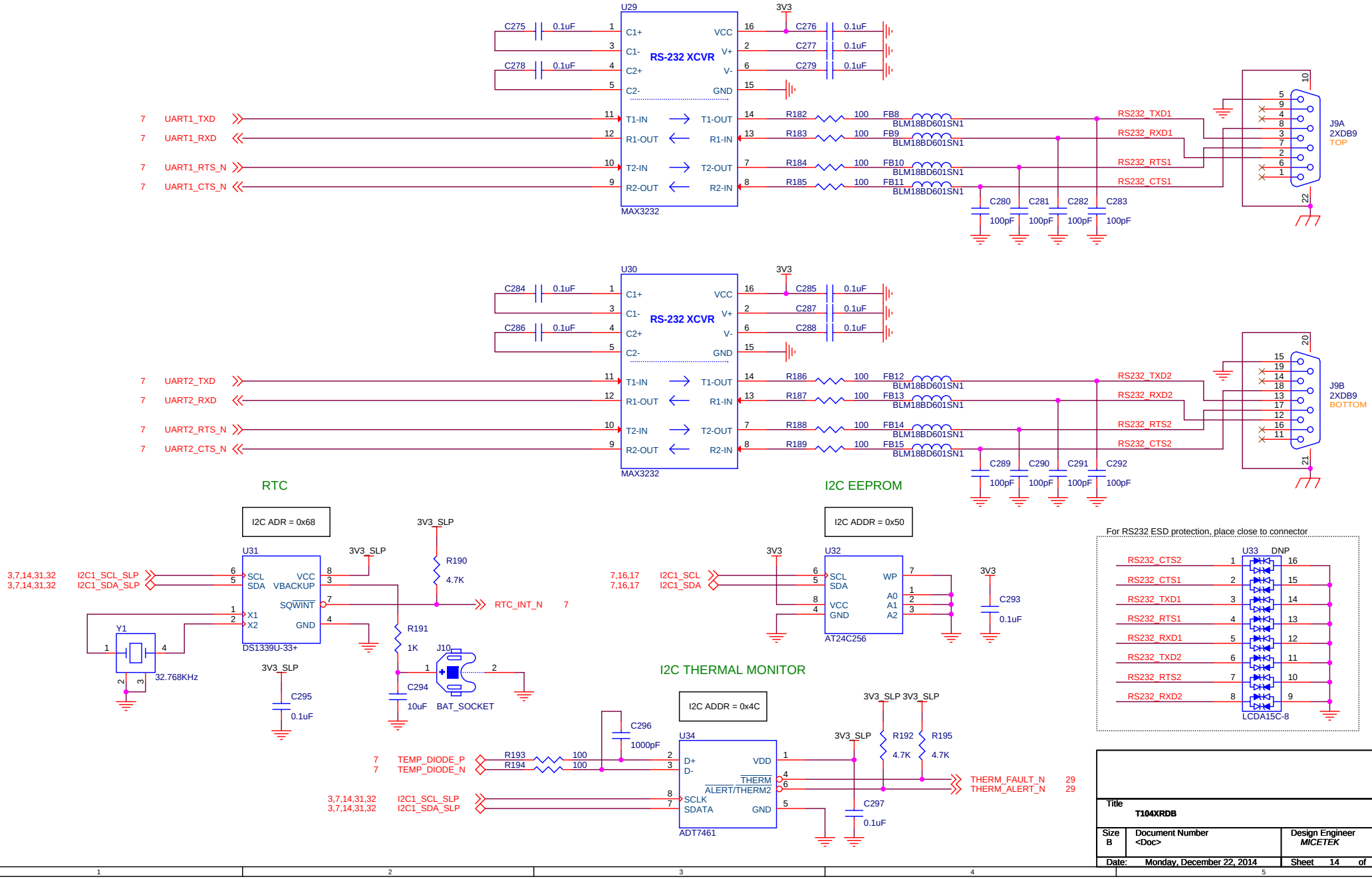
T104X DUART and I2C DEVICE INTERFACE



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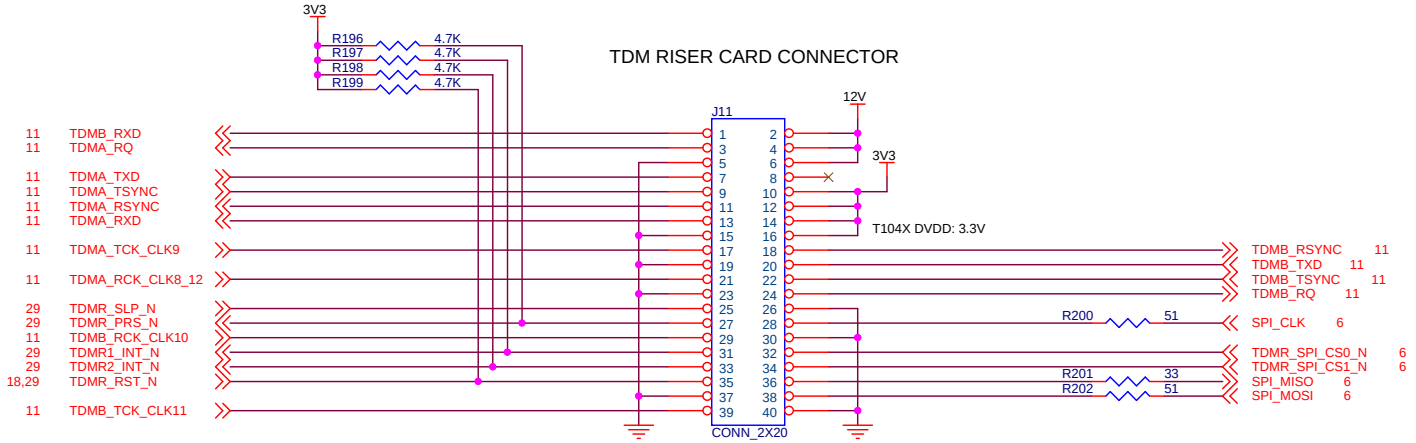
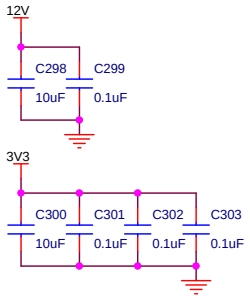
TDM RISER INTERFACE





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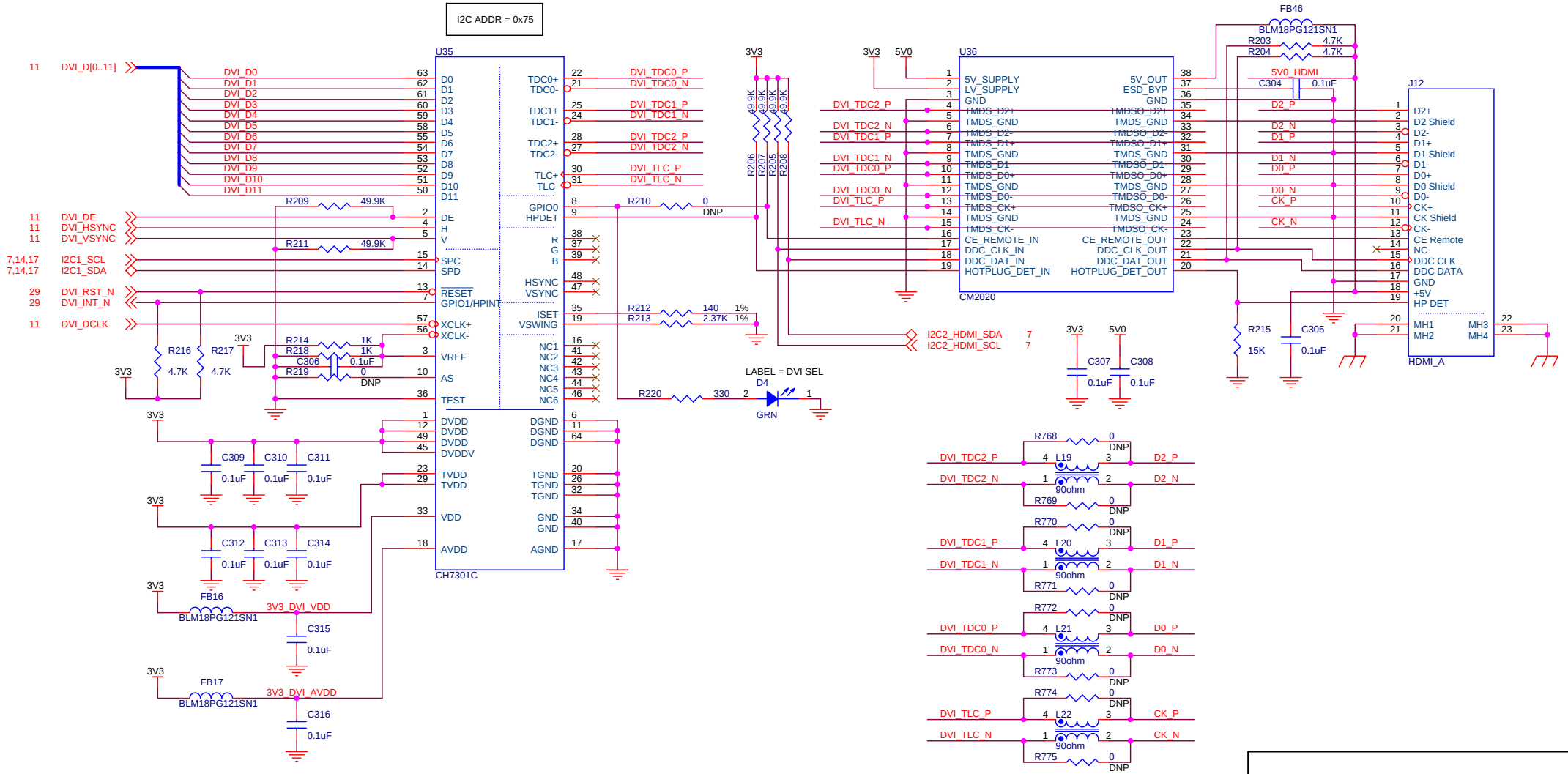
HDMI DISPLAY INTERFACE



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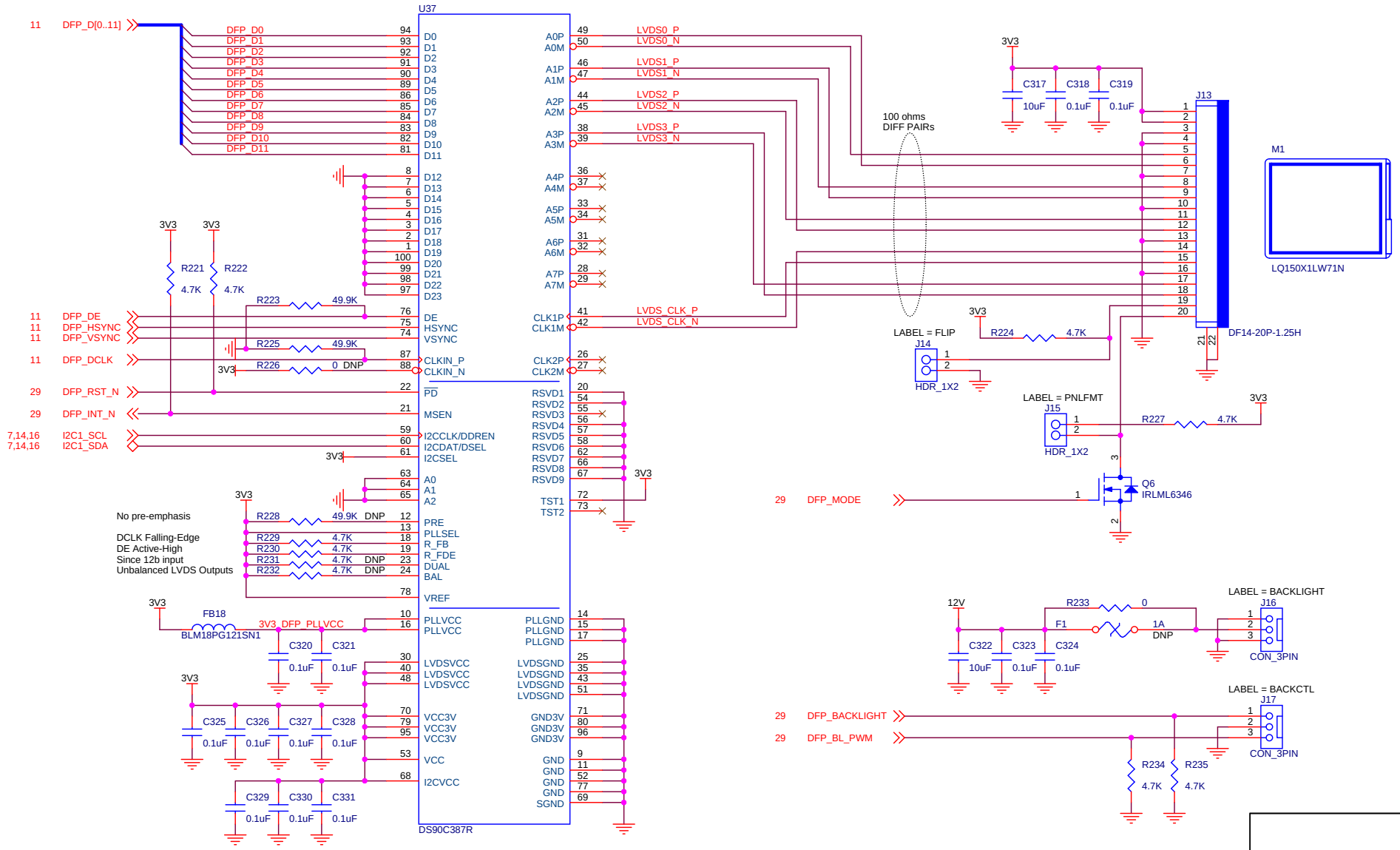
LVDS PANEL INTERFACE

I2C ADDR = 0x38



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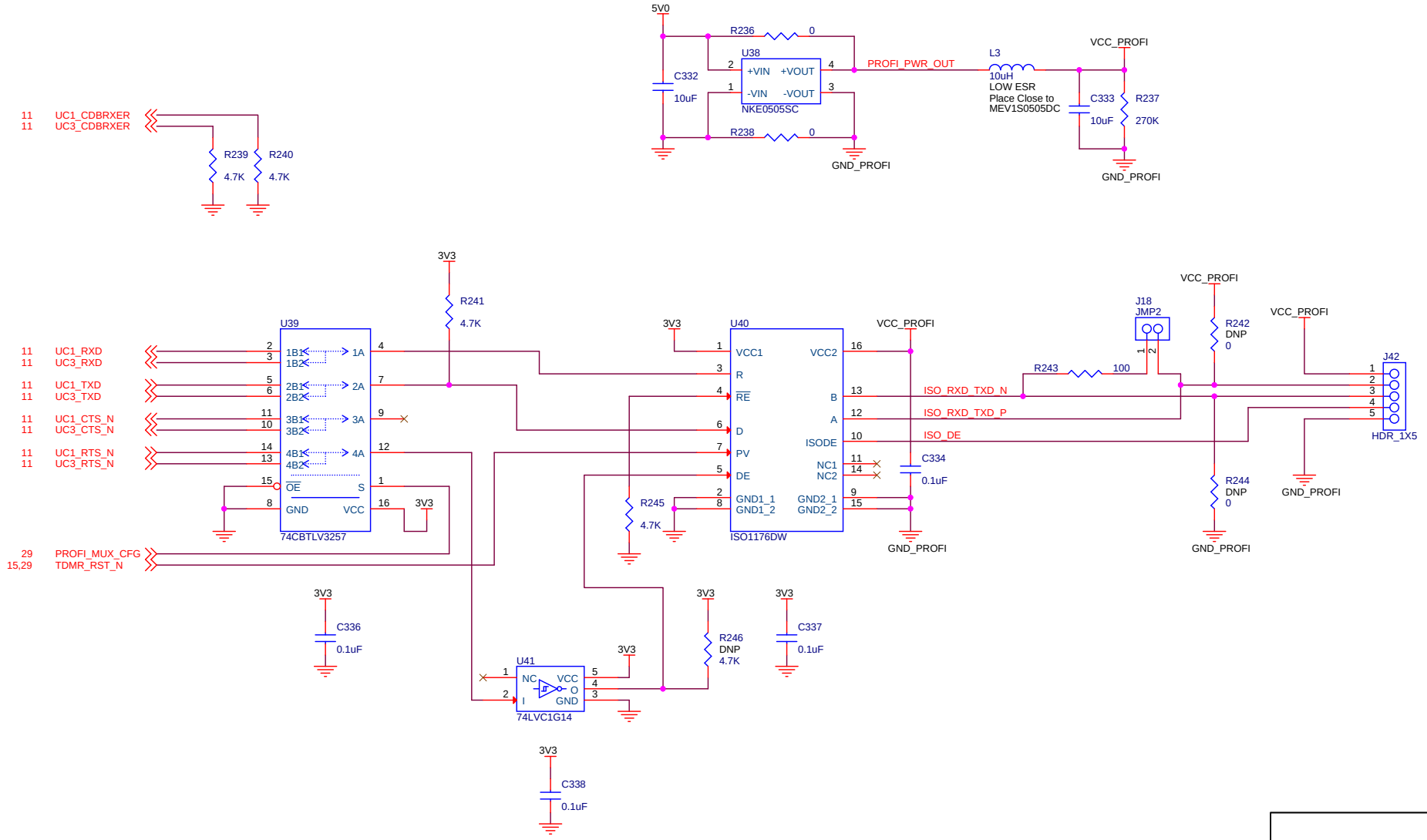
PROFIBUS INTERFACE



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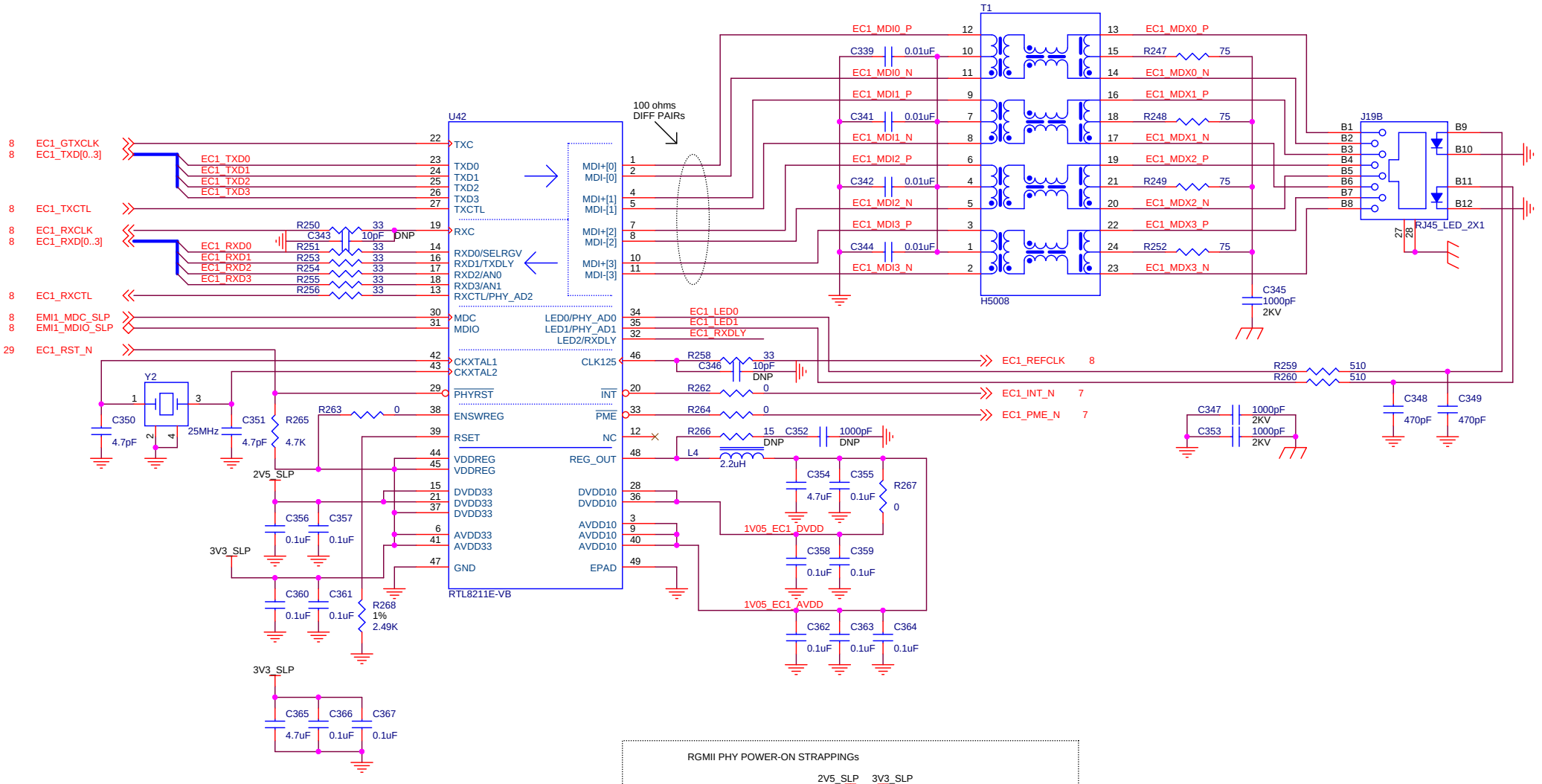
RGMII ETHERNET PORT 1



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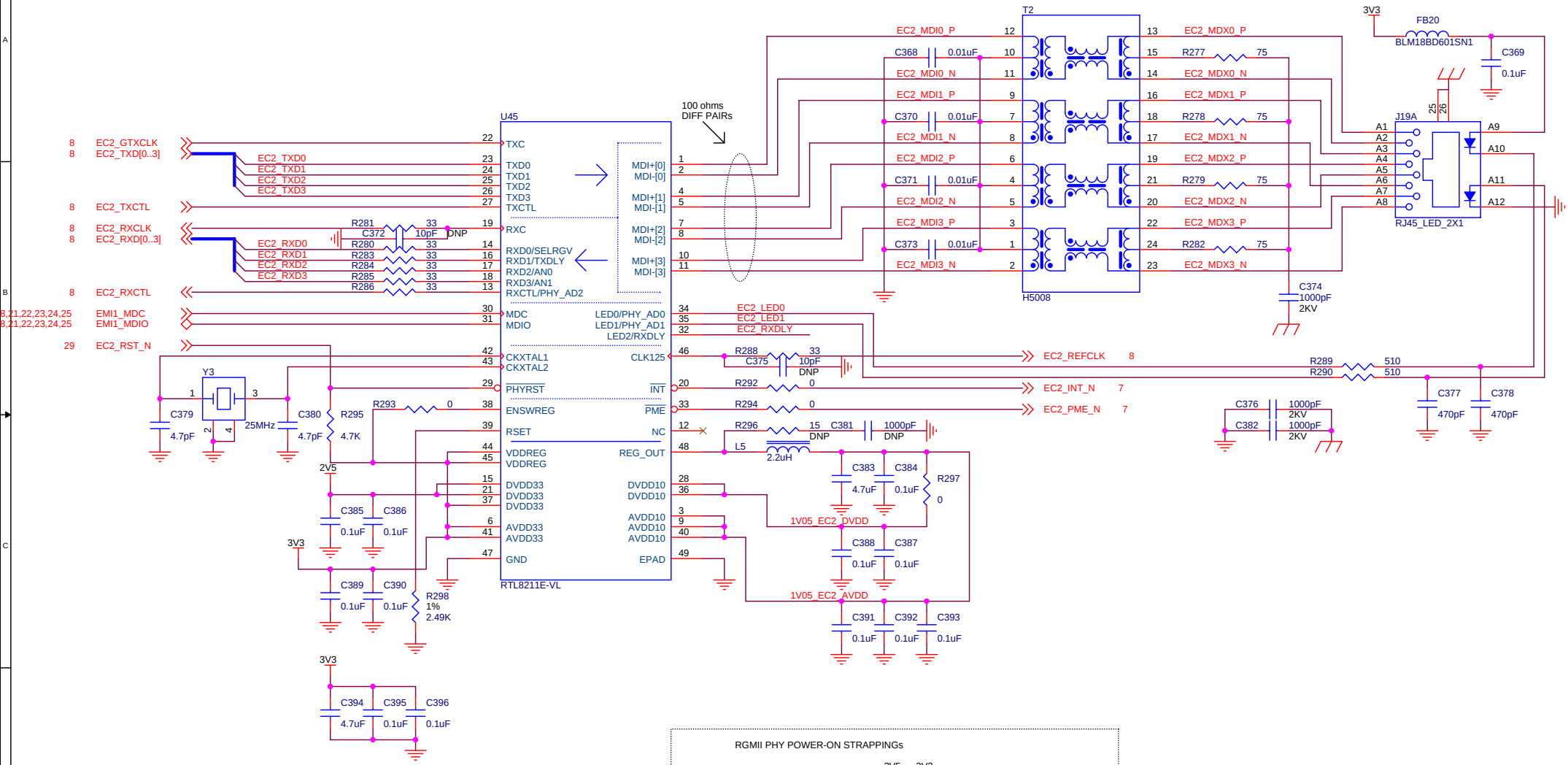
RGMII ETHERNET PORT 2



RGMII PHY POWER-ON STRAPPINGs

EC2_RXD0	R299	4.7K	SELRGV	2.5V
EC2_RXD1	R300	4.7K	TXDLY	
EC2_RXD2	R301	4.7K	AN0	NWay, advertize all capability
EC2_RXD3	R302	4.7K	AN1	
EC2_RXCTL	R303	4.7K	PHY_AD2	
EC2_LED0	R304	4.7K	PHY_AD0	PHY ADDR = 0x05
EC2_LED1	R305	4.7K	PHY_AD1	
EC2_RXDLY	R306	4.7K	RXDLY	

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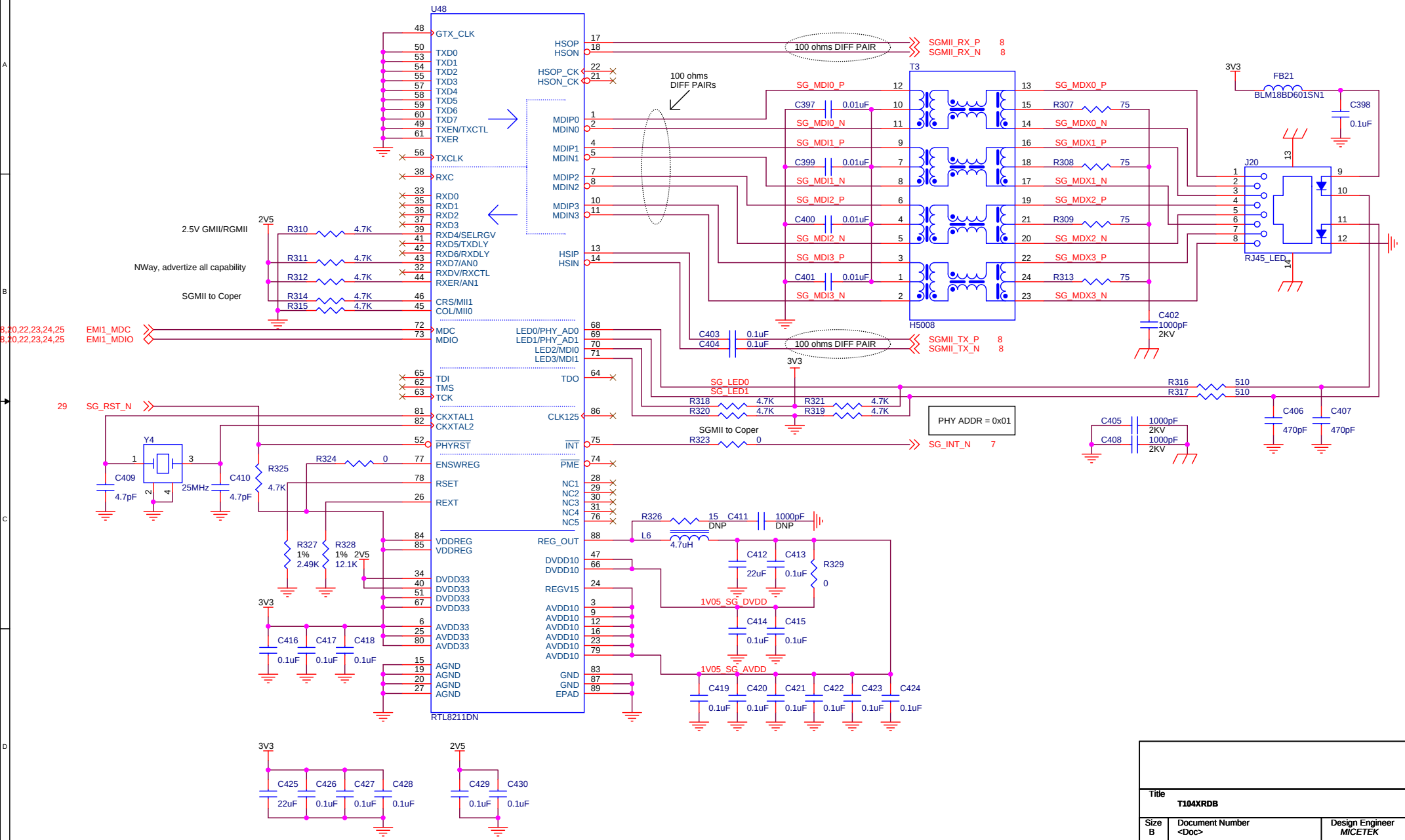
SGMII ETHERNET PORT



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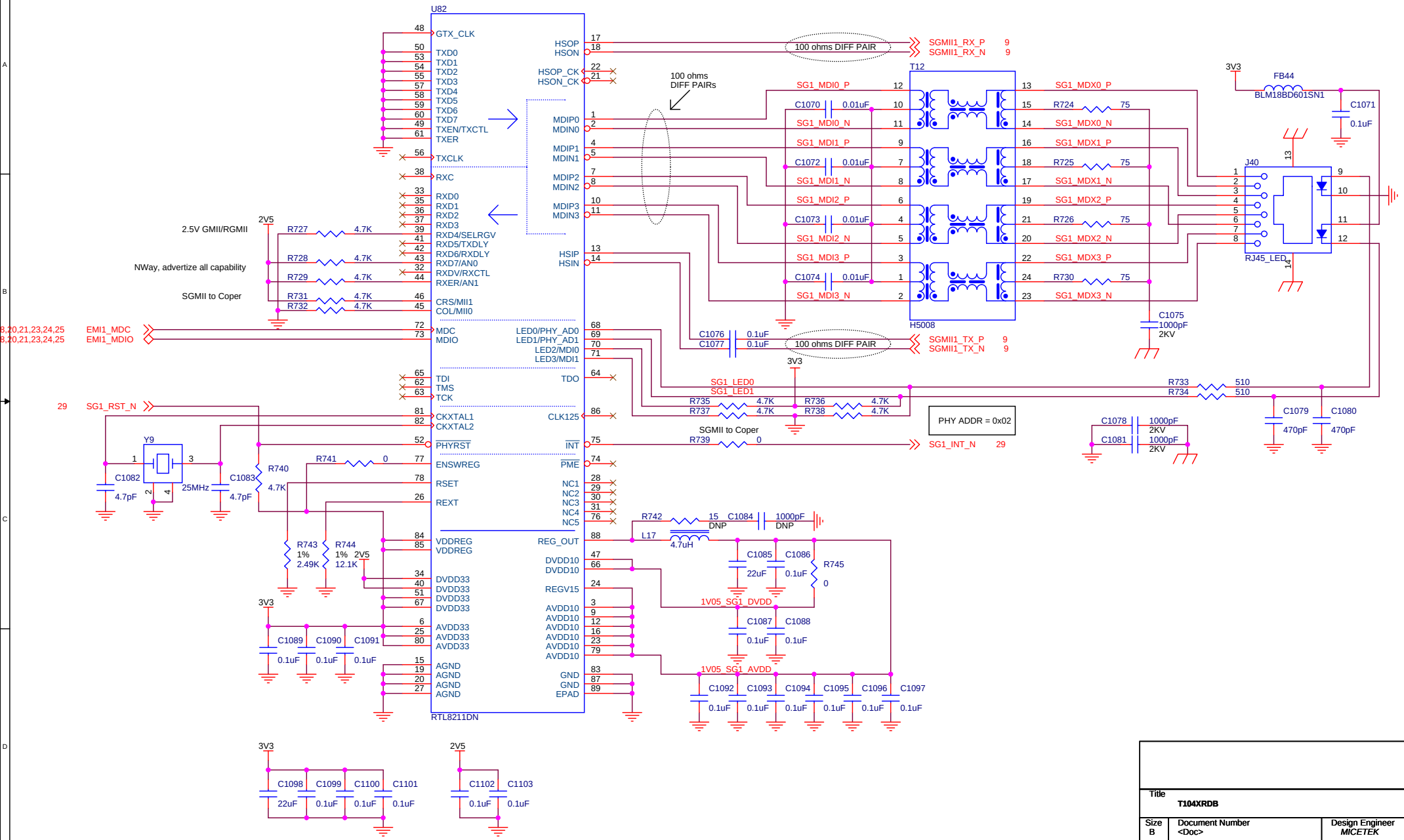
SGMII ETHERNET PORT 1



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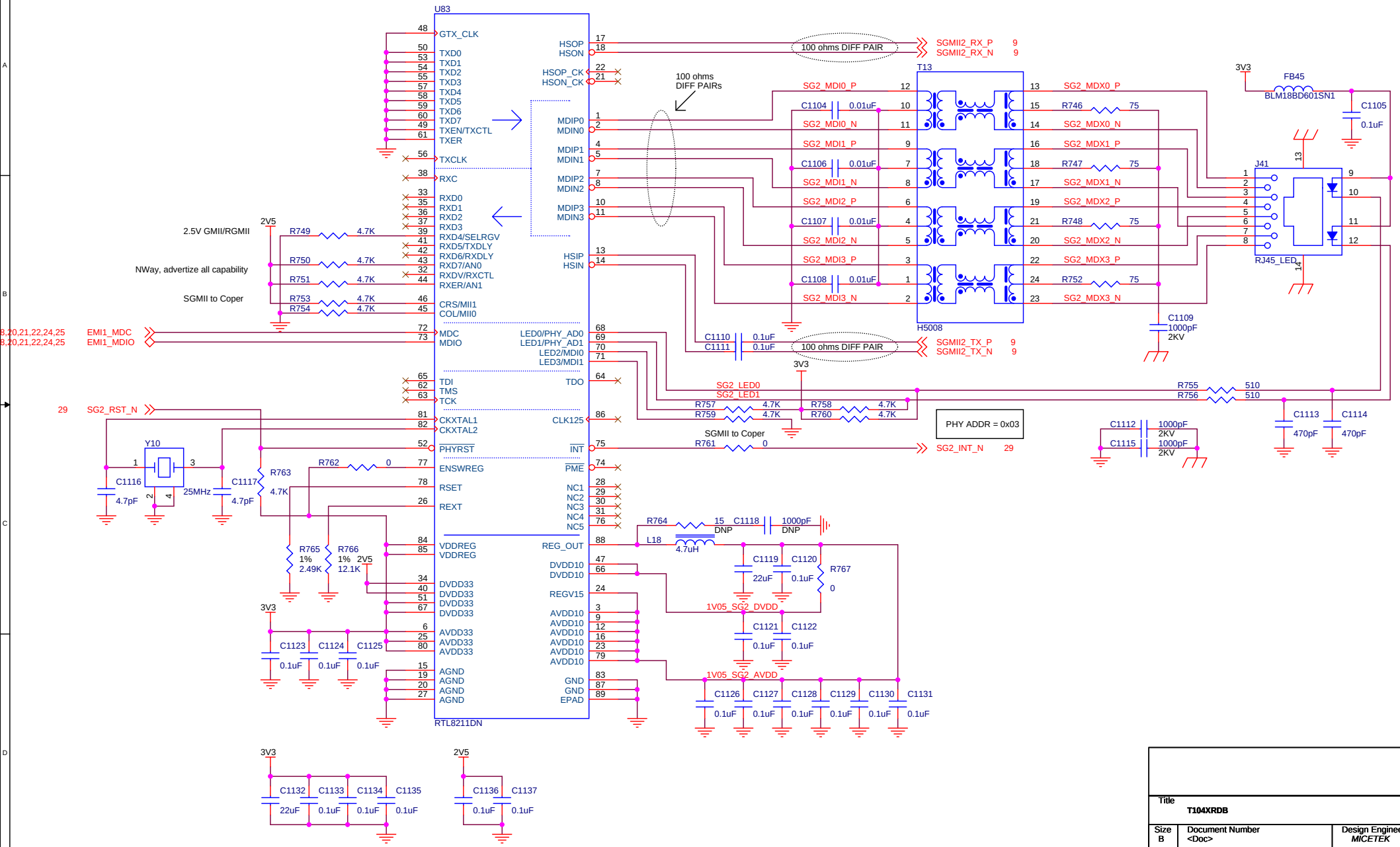
SGMII ETHERNET PORT 2



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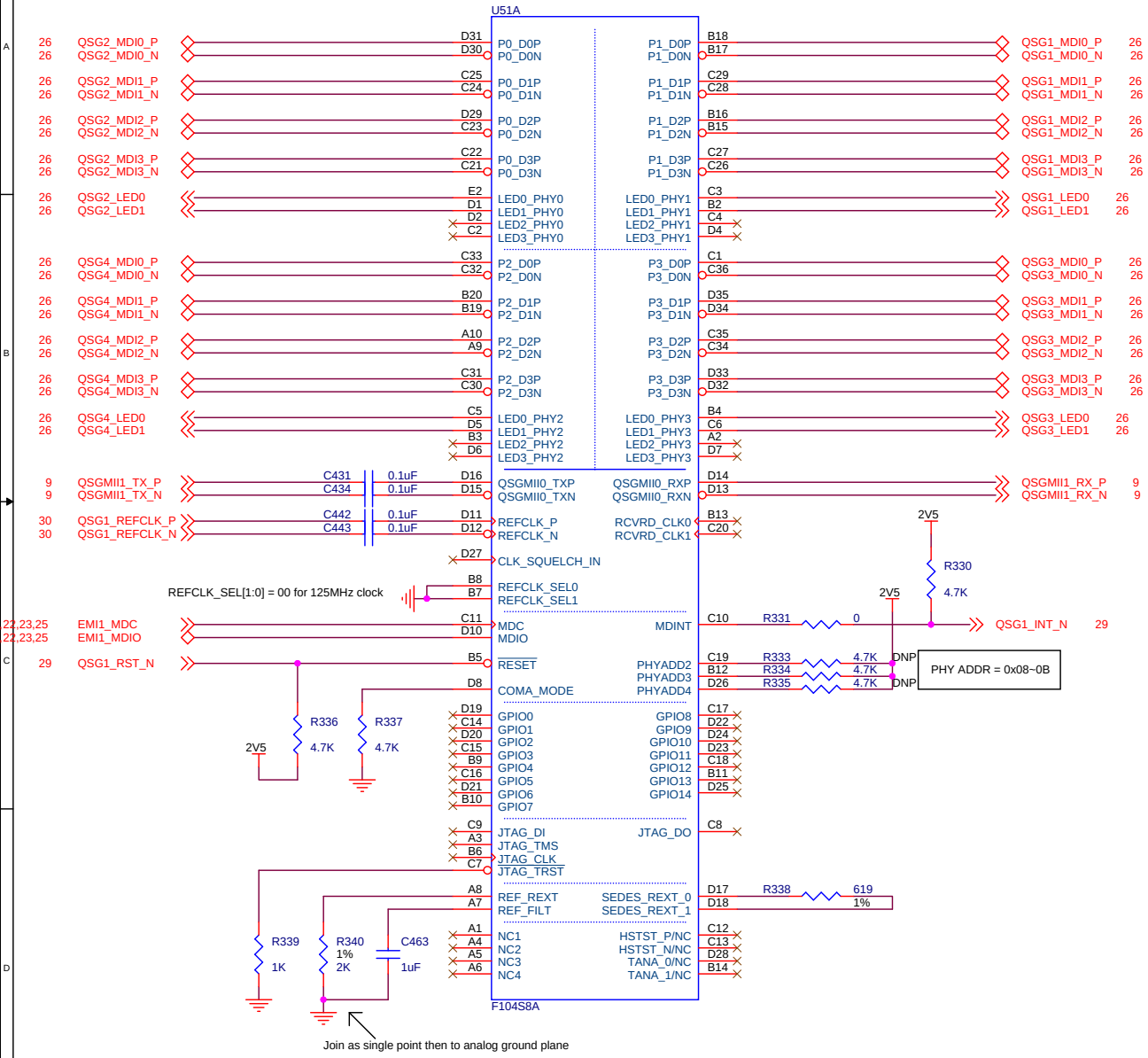
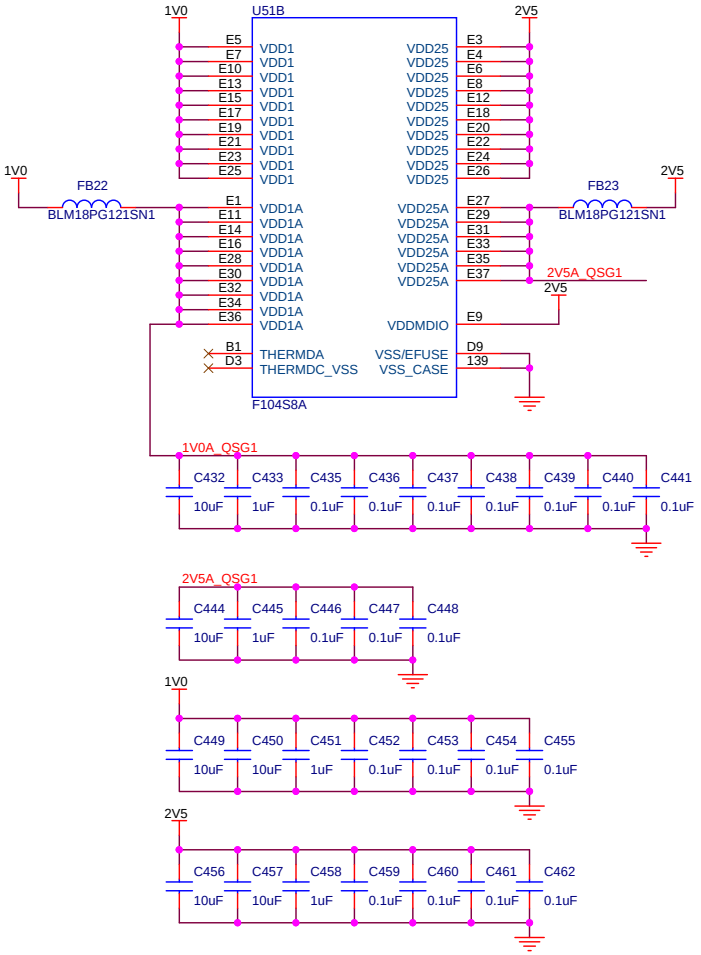
QSGMII PHY 1





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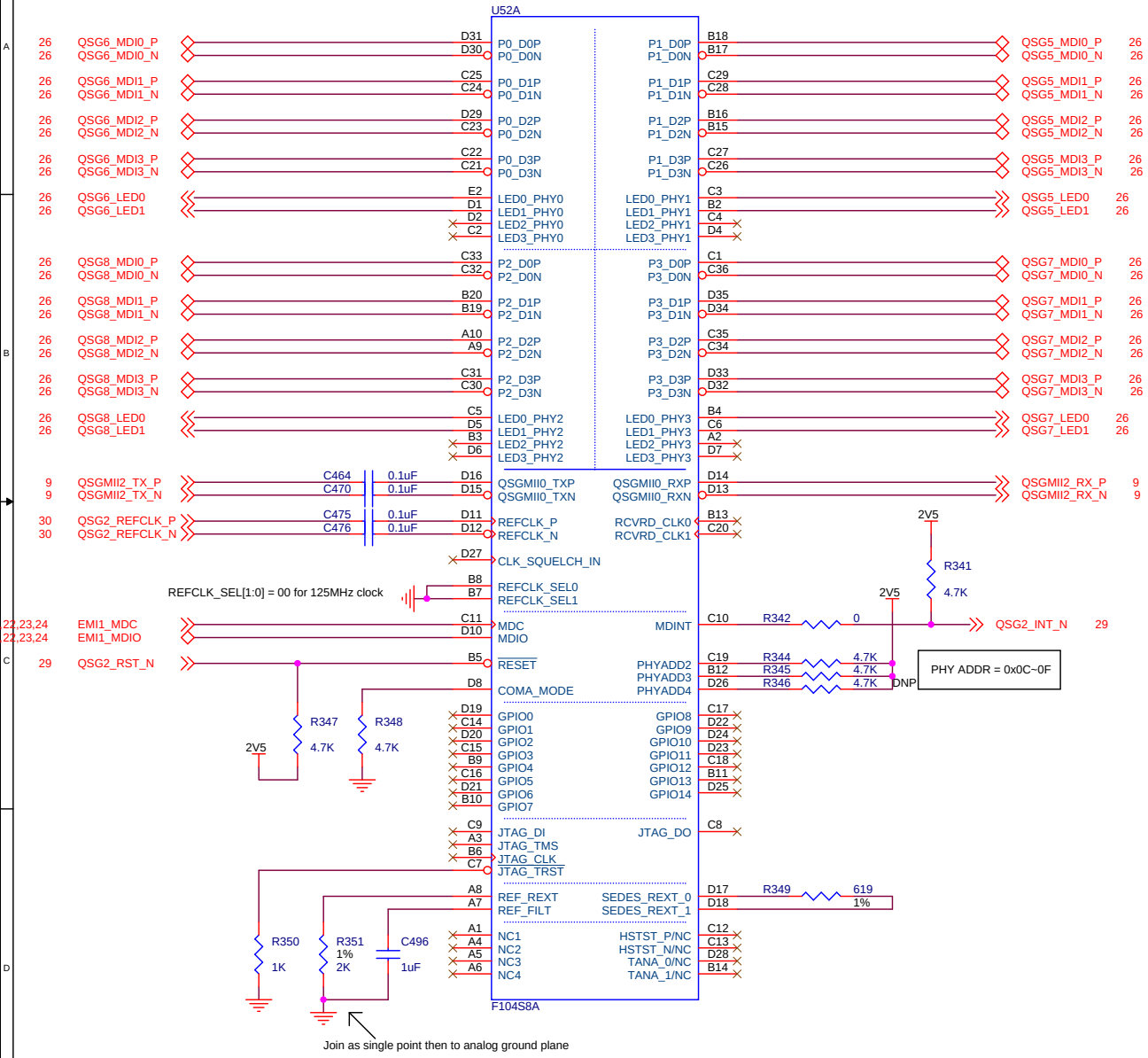
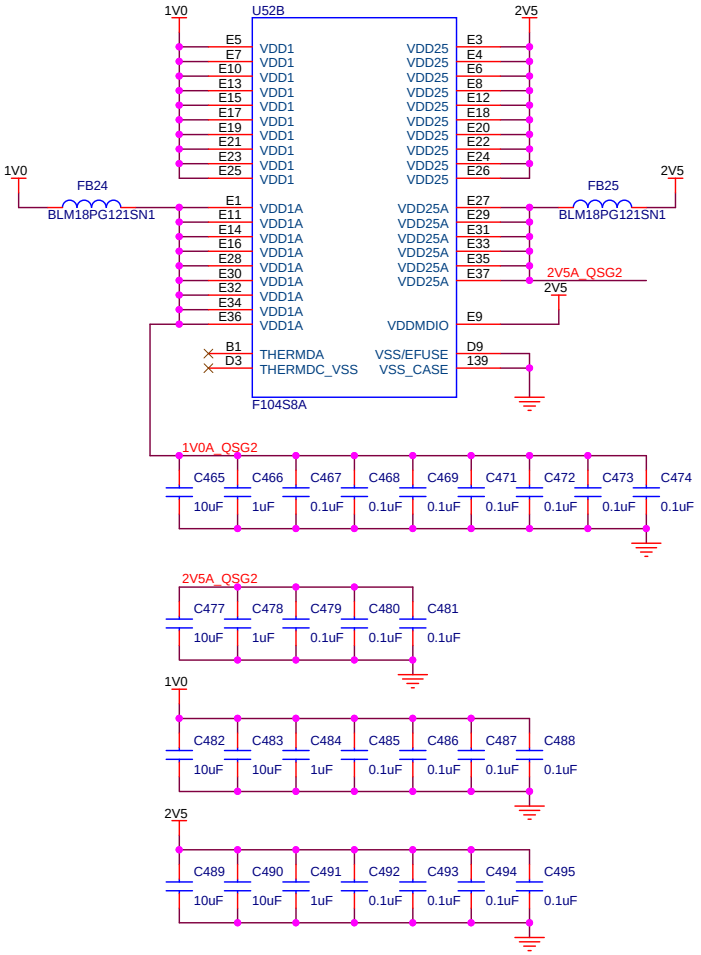
QSGMII PHY 2





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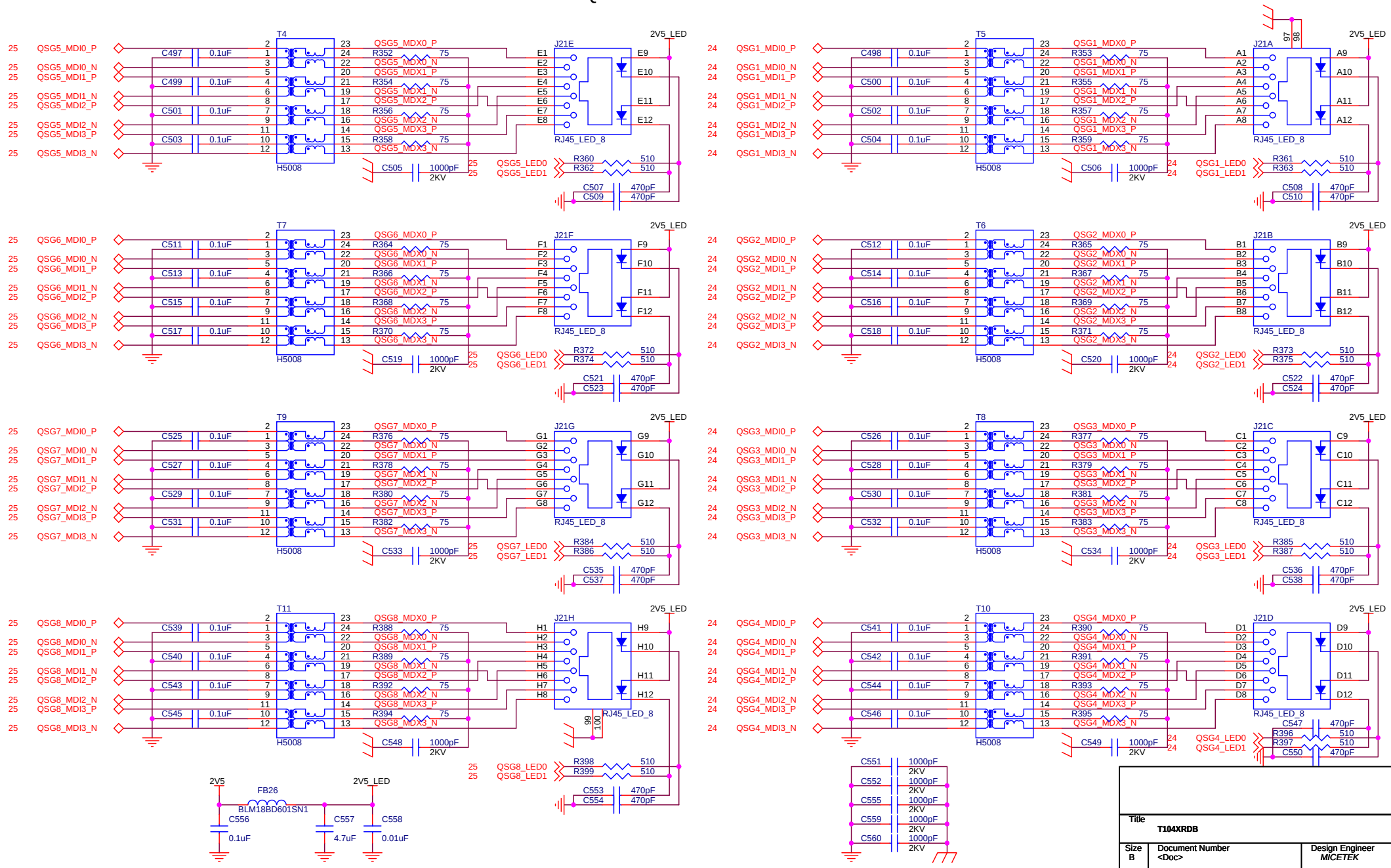
QSGMII ETHERNET PORTs



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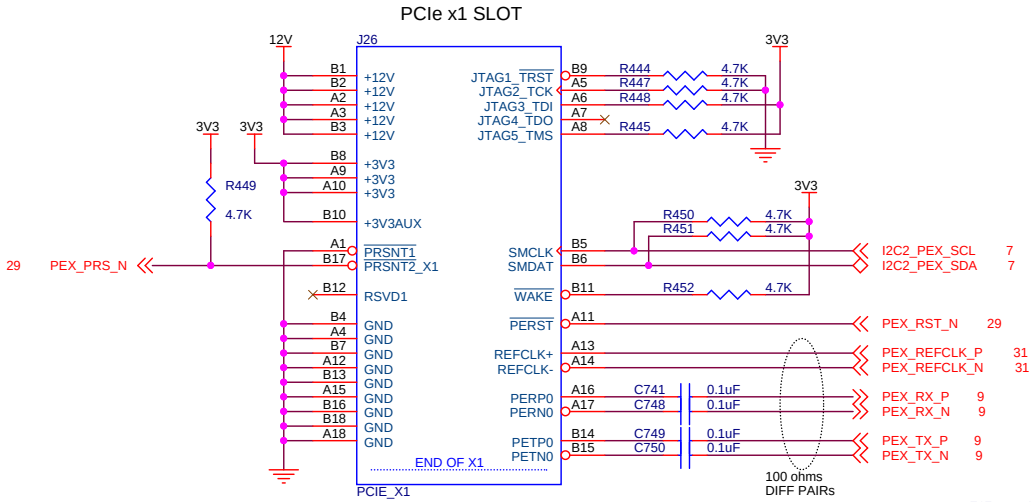
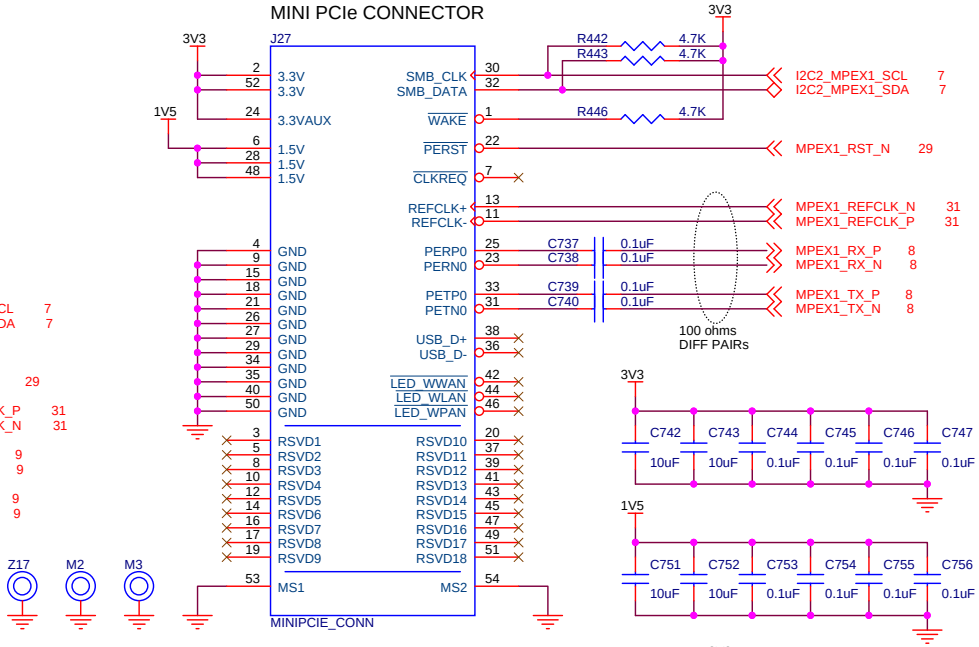
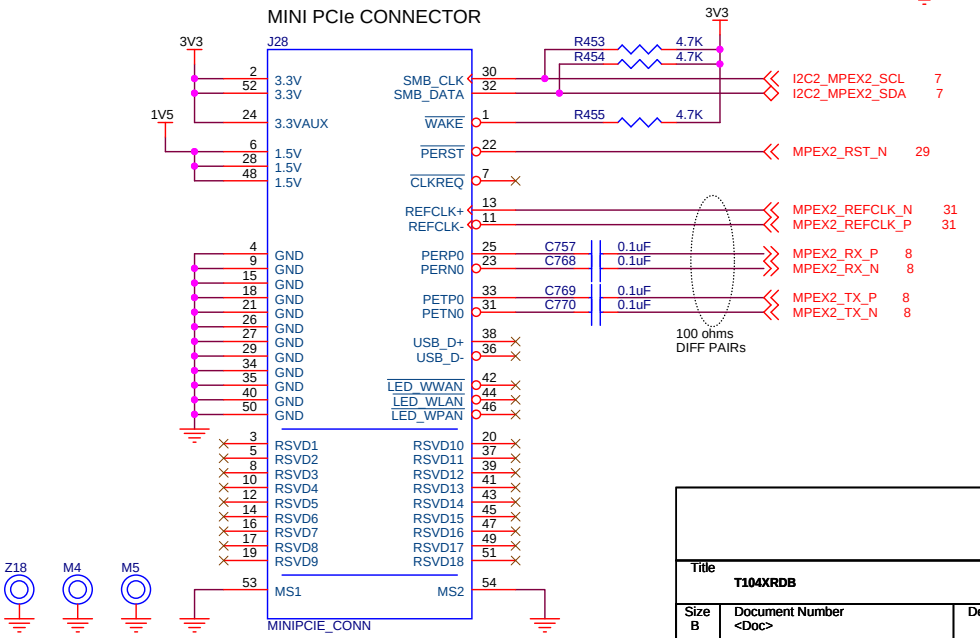
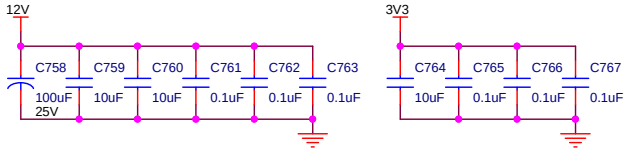
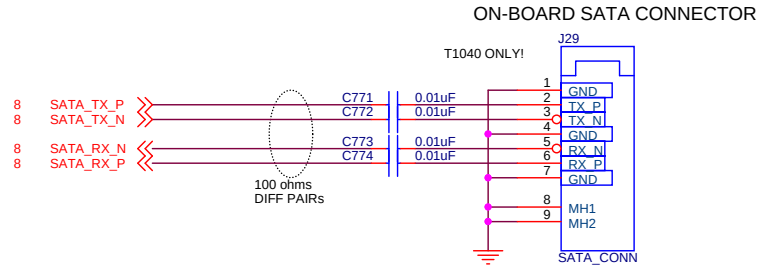
PCIe X1 SLOT, MINI PCIe and SATA CONNECTORs











Z17 M2 M3

Z18 M4 M5

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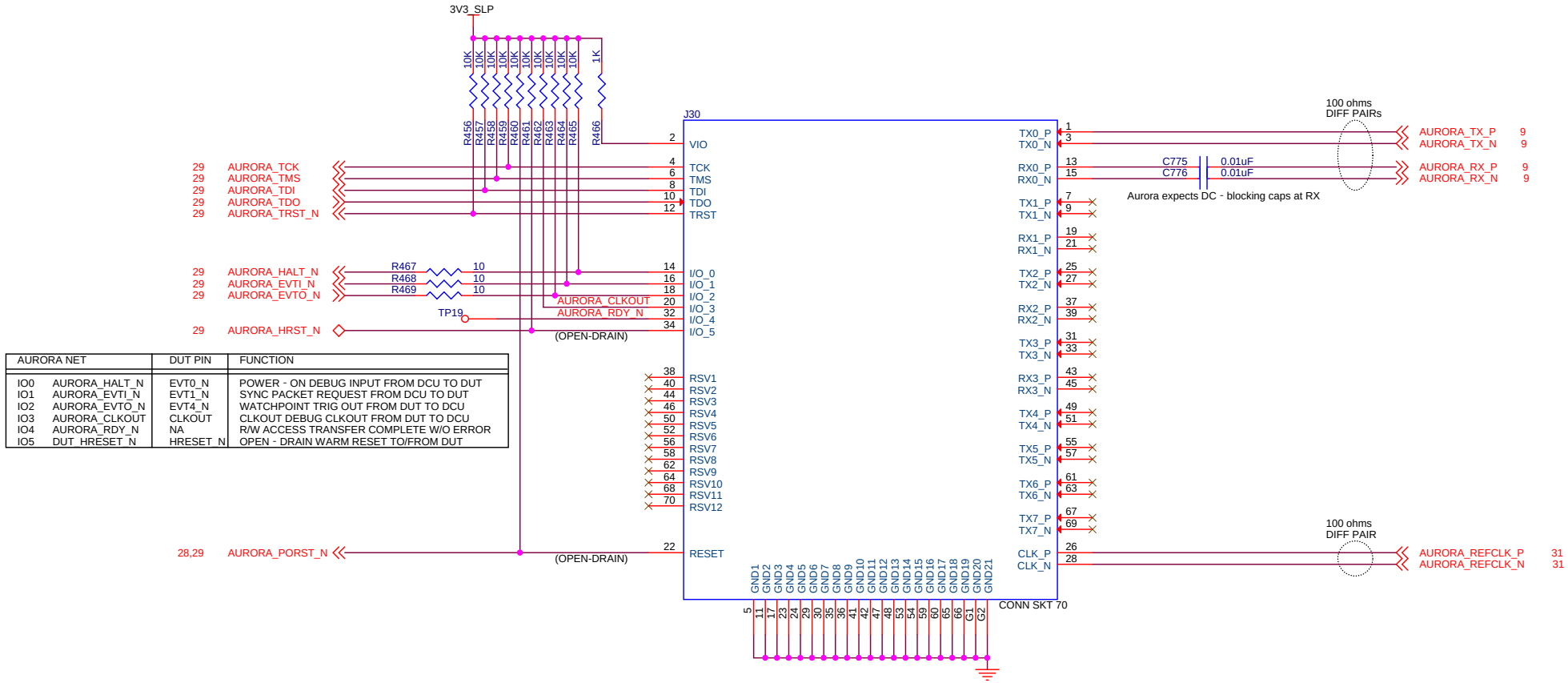
AURORA PORT



AURORA NET		DUT PIN	FUNCTION
IO0	AURORA_HALT_N	EVT0_N	POWER - ON DEBUG INPUT FROM DCU TO DUT
IO1	AURORA_EVTI_N	EVT1_N	SYNC PACKET REQUEST FROM DCU TO DUT
IO2	AURORA_EVTO_N	EVT4_N	WATCHPOINT TRIG OUT FROM DUT TO DCU
IO3	AURORA_CLKOUT	CLKOUT	CLKOUT DEBUG CLKOUT FROM DUT TO DCU
IO4	AURORA_RDY_N	NA	R/W ACCESS TRANSFER COMPLETE W/O ERROR
IO5	DUT_HRESET_N	HRESET_N	OPEN - DRAIN WARM RESET TO/FROM DUT

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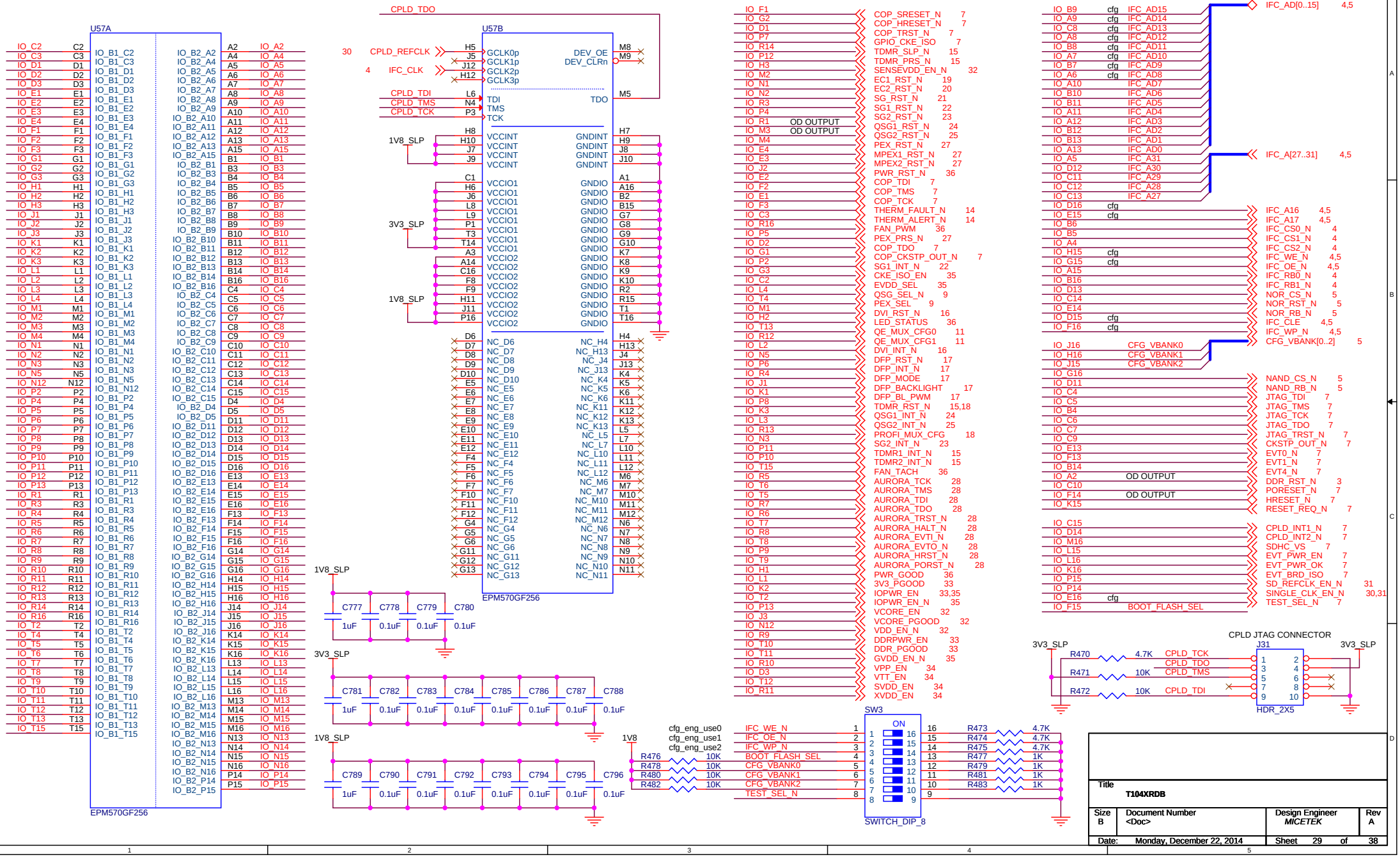
CPLD


3.3V BANK1 IO
1.8V BANK2 IO
U57A
U57B
EPM570GF256
EPM570GF256
CPLD_TDO
CPLD_REFCLK
IFC_CLK
CPLD_TDI
CPLD_TMS
CPLD_TCK
1V8_SLP
3V3_SLP
1V8_SLP
1V8_SLP
1V8
IFC_AD[0..15]
IFC_A[27..31]
CFG_VBANK[0..2]
CPLD JTAG CONNECTOR
J31
HDR_2X5
SW3
SWITCH_DIP_8
cfg_eng_use0
cfg_eng_use1
cfg_eng_use2
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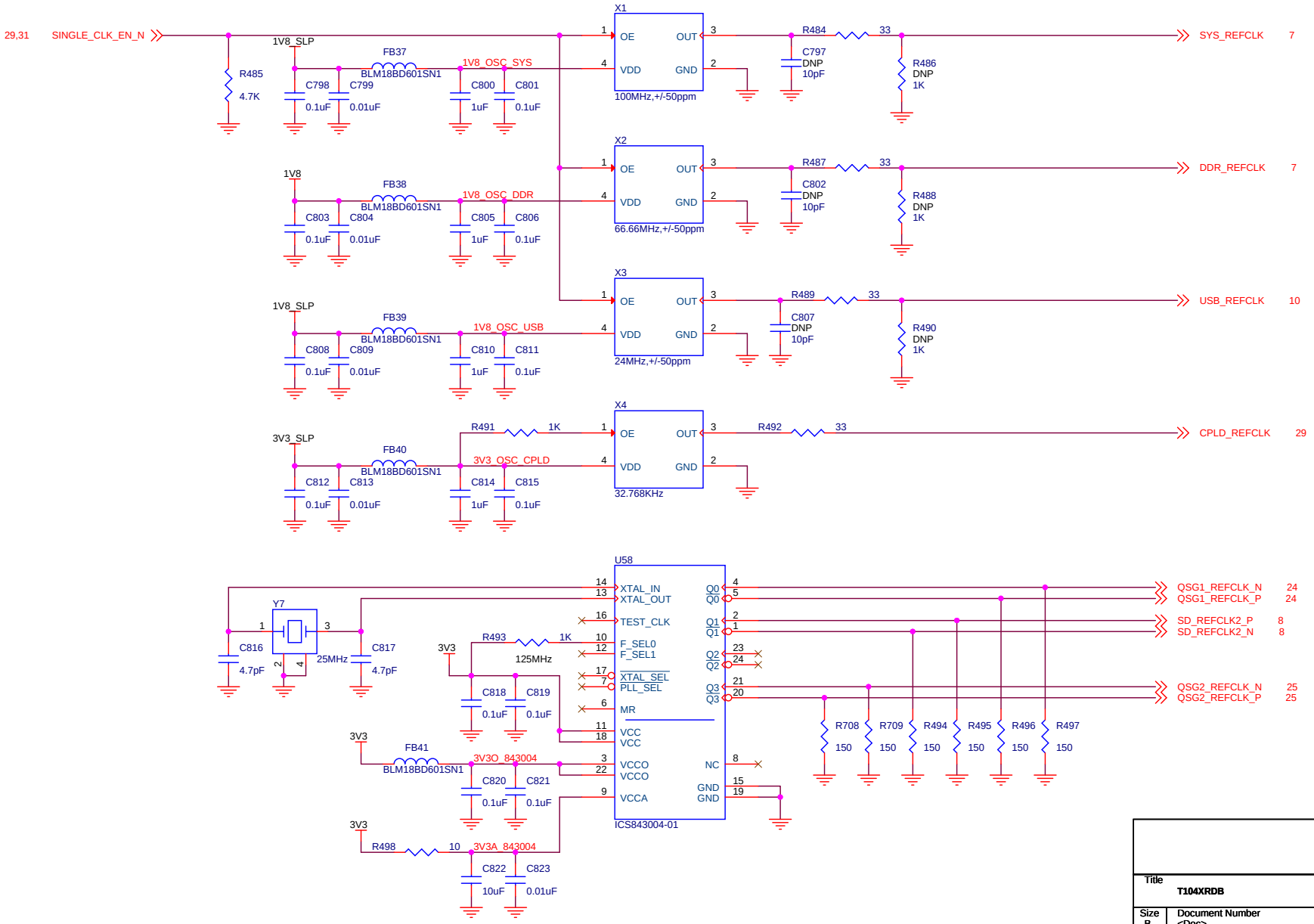
SYSTEM CLOCK GENERATORs



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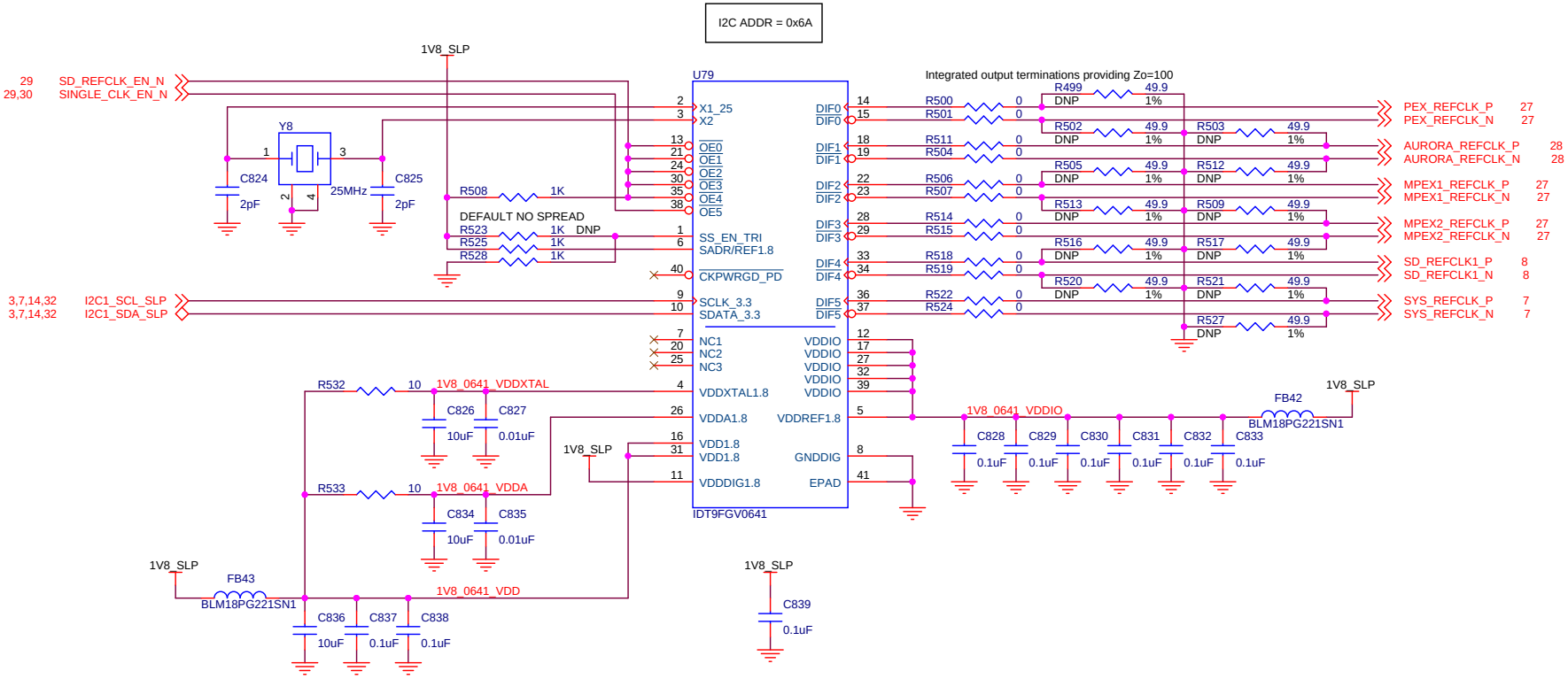
SYSTEM CLOCK GENERATORs (cont.)



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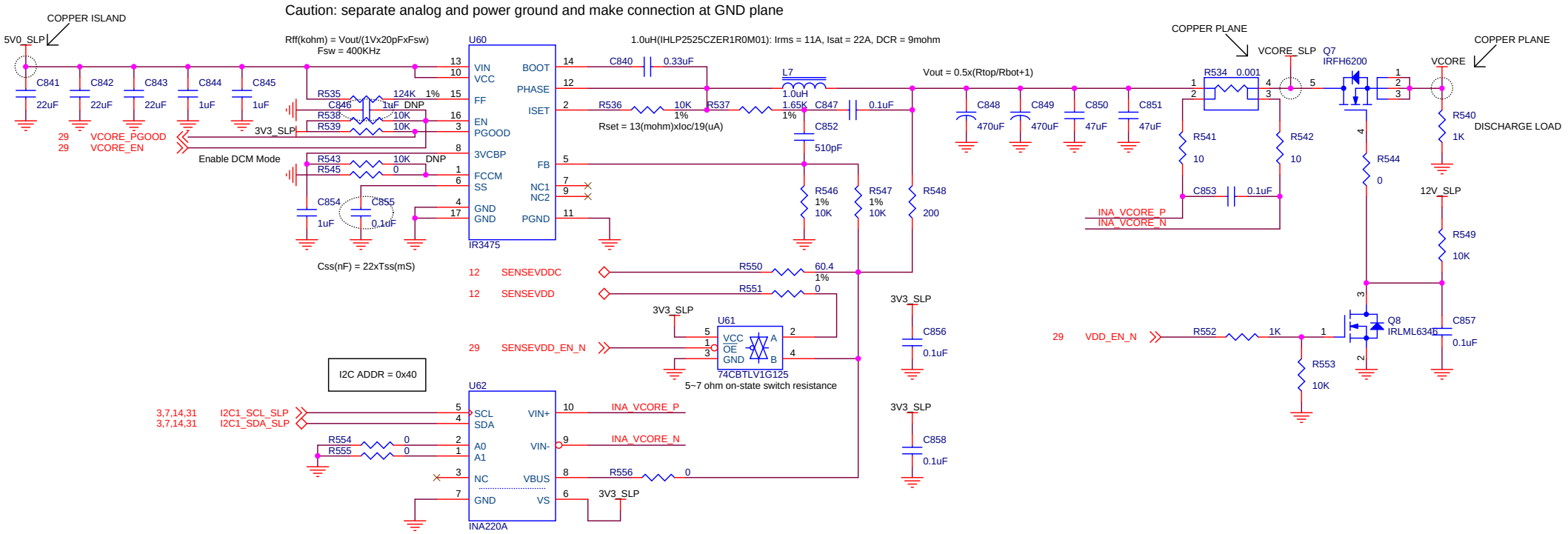
T104X CORE POWER CONVERTOR



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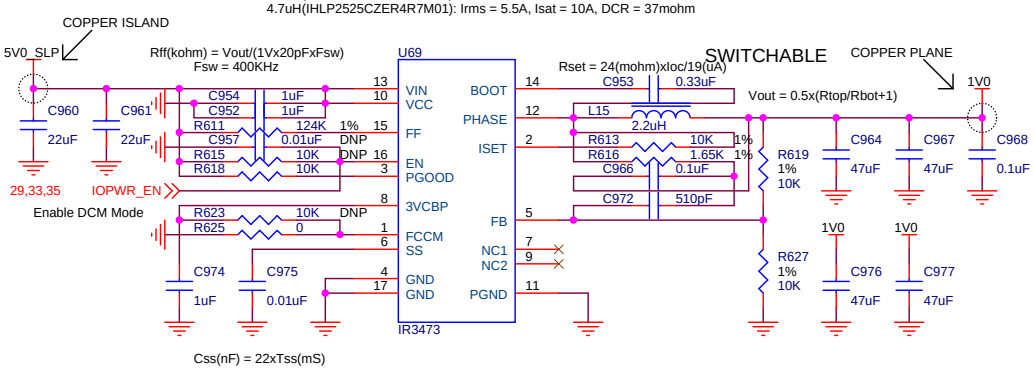
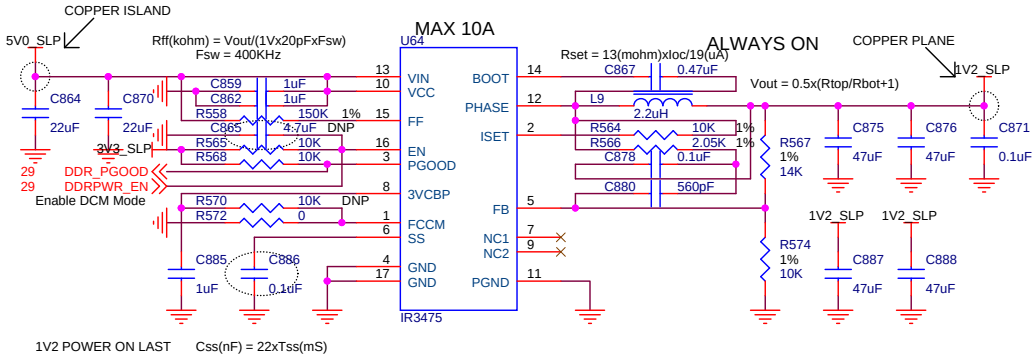
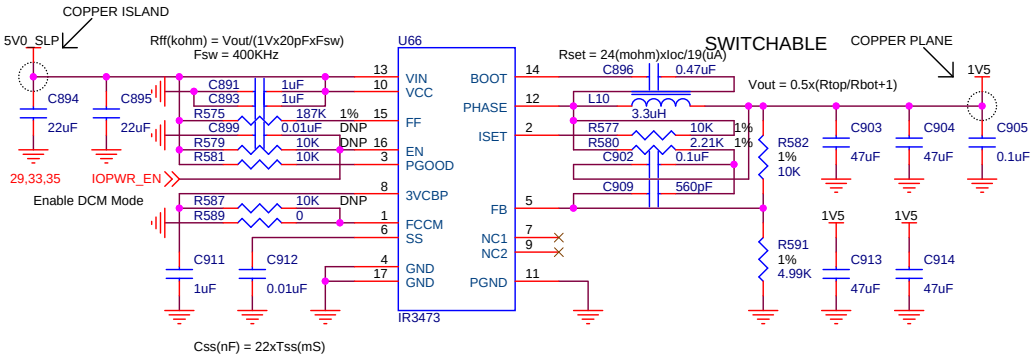
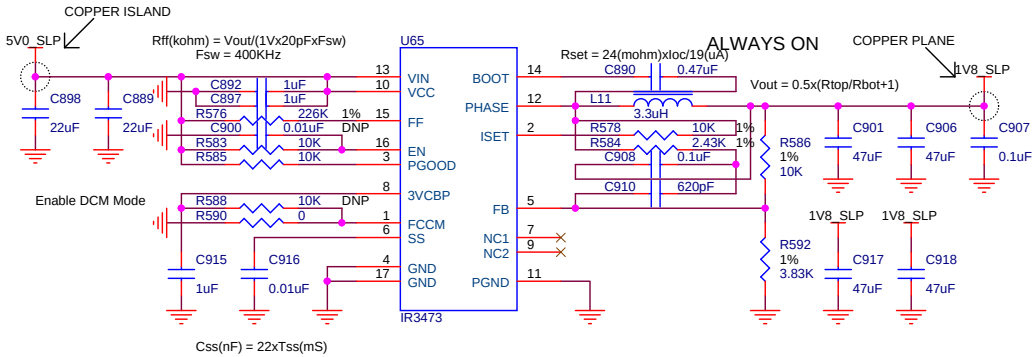
SYSTEM POWER CONVERTORS

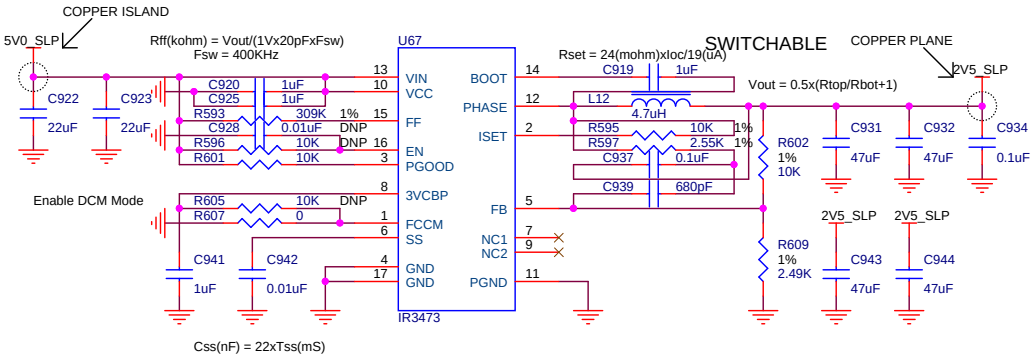
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

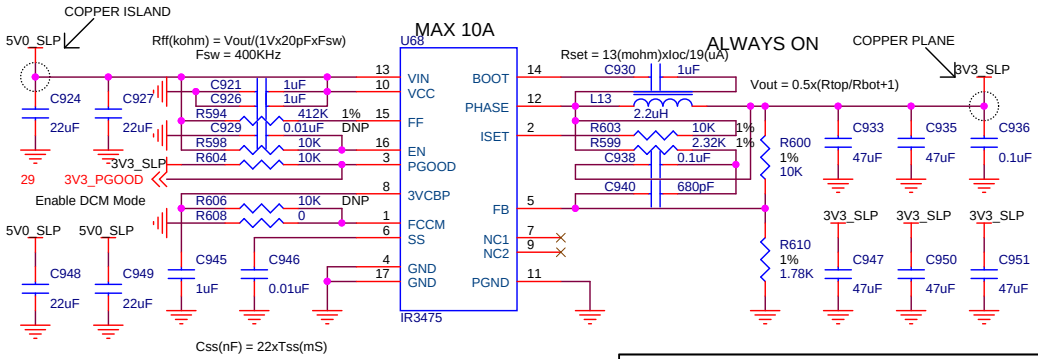












Caution: separate analog and power ground and make connection at GND plane

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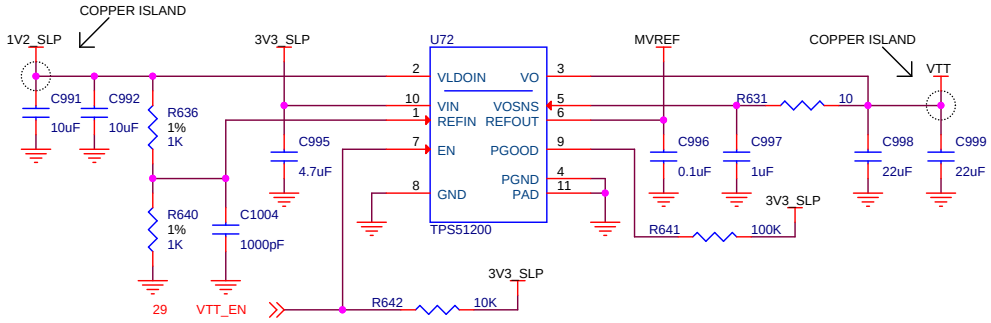
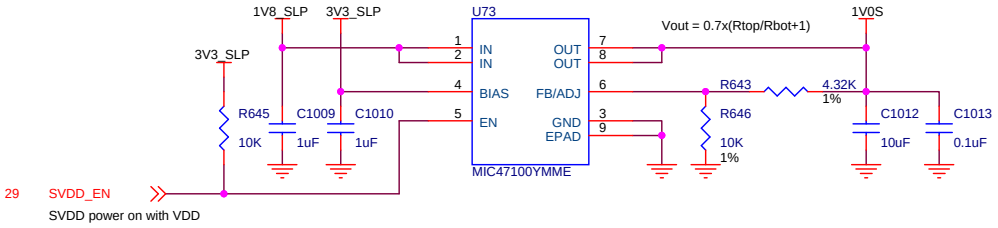
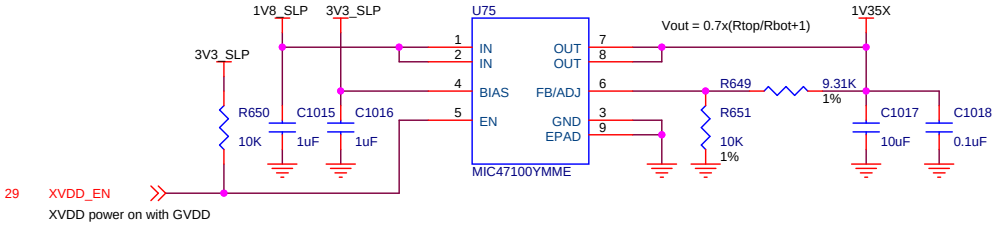
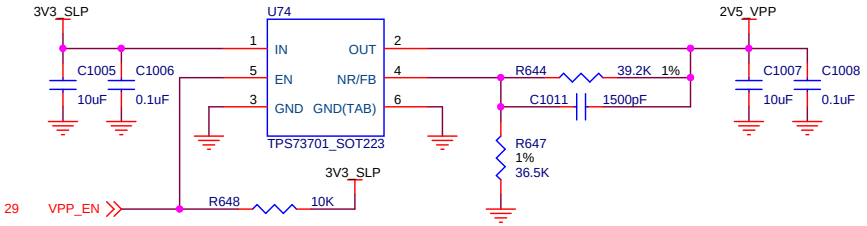
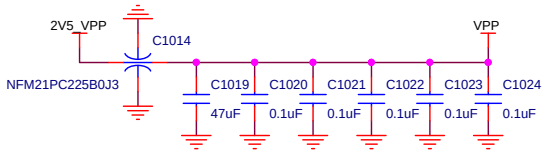
SYSTEM POWER CONVERTORs (cont.)











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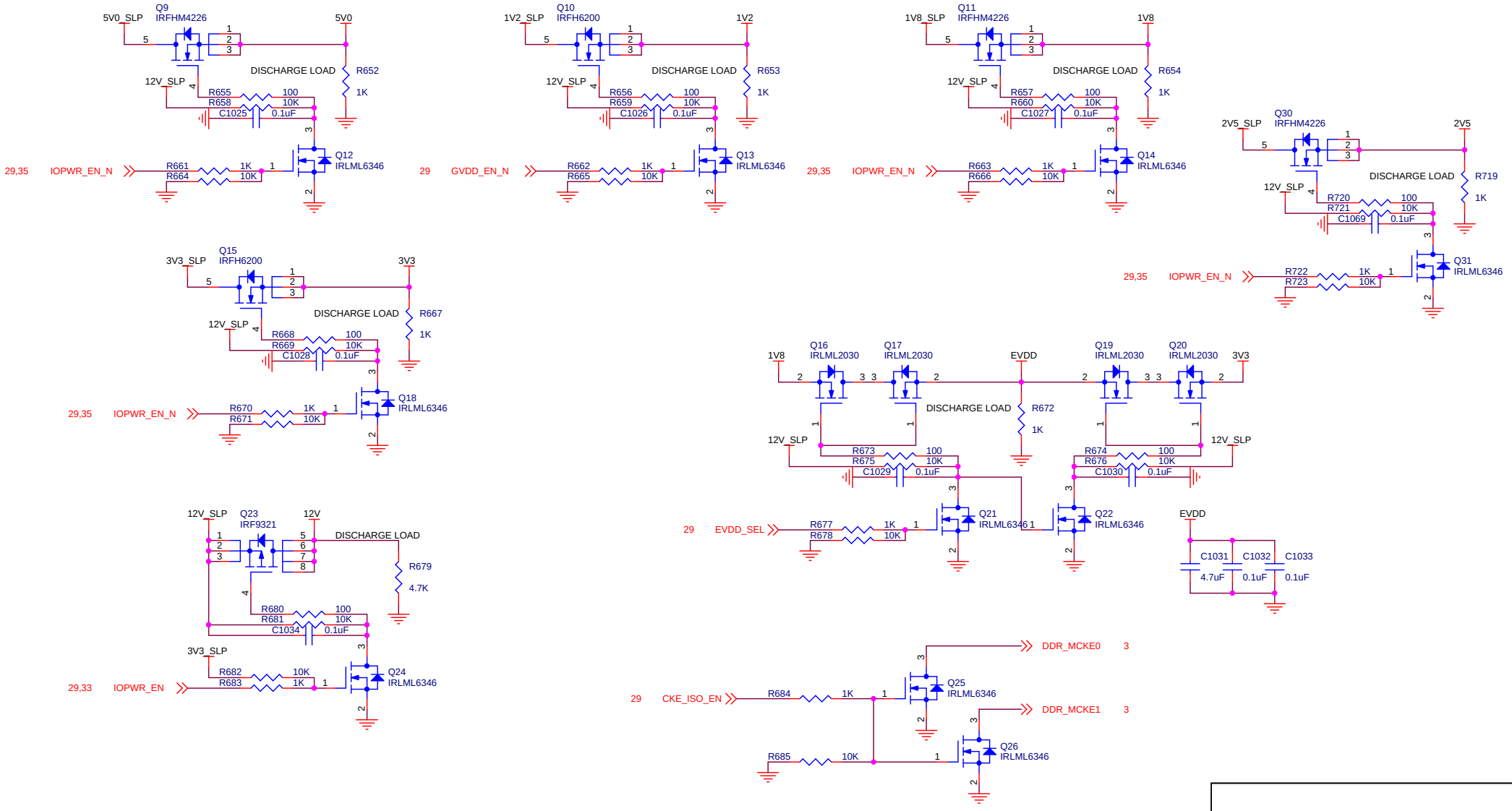
SYSTEM POWER SWITCHs



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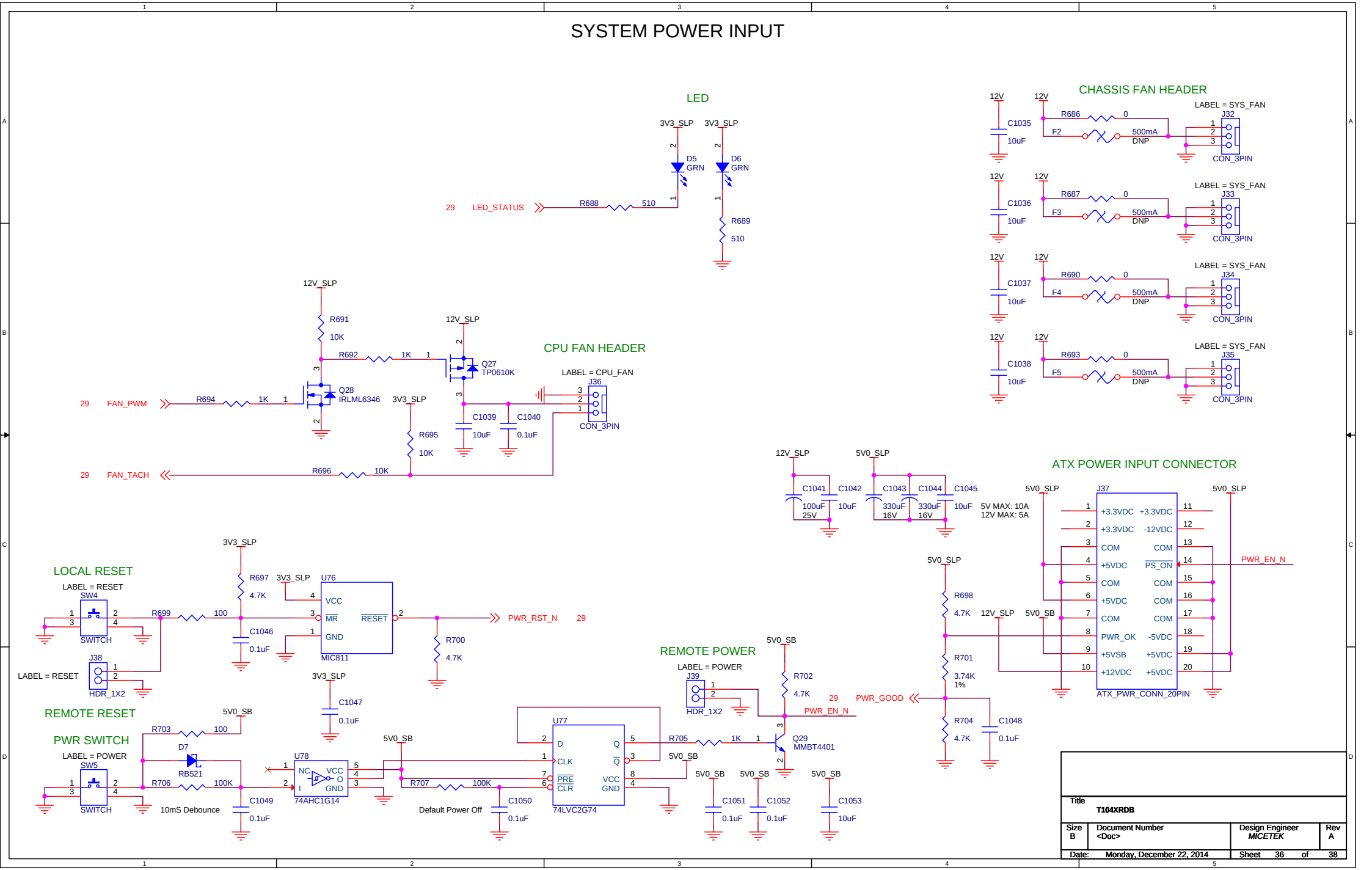
SYSTEM POWER INPUT



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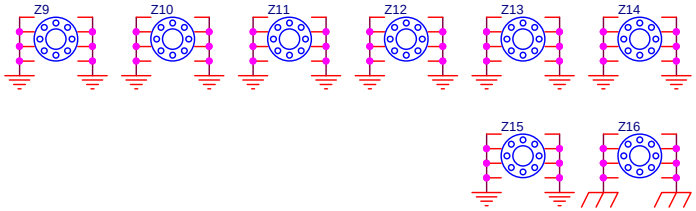
MECHANICALs

Fiducial Marks

Mouting Holes



Layer Detail

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CHANGE LIST

2014/10/28
1. Change SD_REFCLK2 to 125MHz for 2.5G SGMII
2. Add RGMII RXCLK 500ps PCB delay line for new T1040 chip requirement
3. Add MDIO mux/demux and voltage level translator

2014/11/12
1. Delete AQR105 and change to RTL8211DN
2. Change profibus DB9 to 1X5 header
3. Remove miniPCIe mounting stubs

2014/12/23
1. Add 2 mounting holes for miniPCIe connectors

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