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Rev	Date	Changes
A	18-JAN-2019	FRWYLS1046A-PA (PROTOTYPE)
B	18-MAR-2019	1) Changed R142 to 100ohm. 2) Changed logic for PROG_SFP circuit. 3) Replaced J66 with Header 210-75691. 4) Replaced J67 with Header 211-30042. 5) Added Bypass caps between DDR_VTT and GVDD power rails. 7) Replaced Micro-AB J58 with Molex 0476420001 Micro-B part. 8) Added Header for 12V CPU fan "J75". 9) DNP-> R920 and C1466. 10) Change BRD_REV[1:0]=01 for Rev B.

FRWYLS1046A-PA

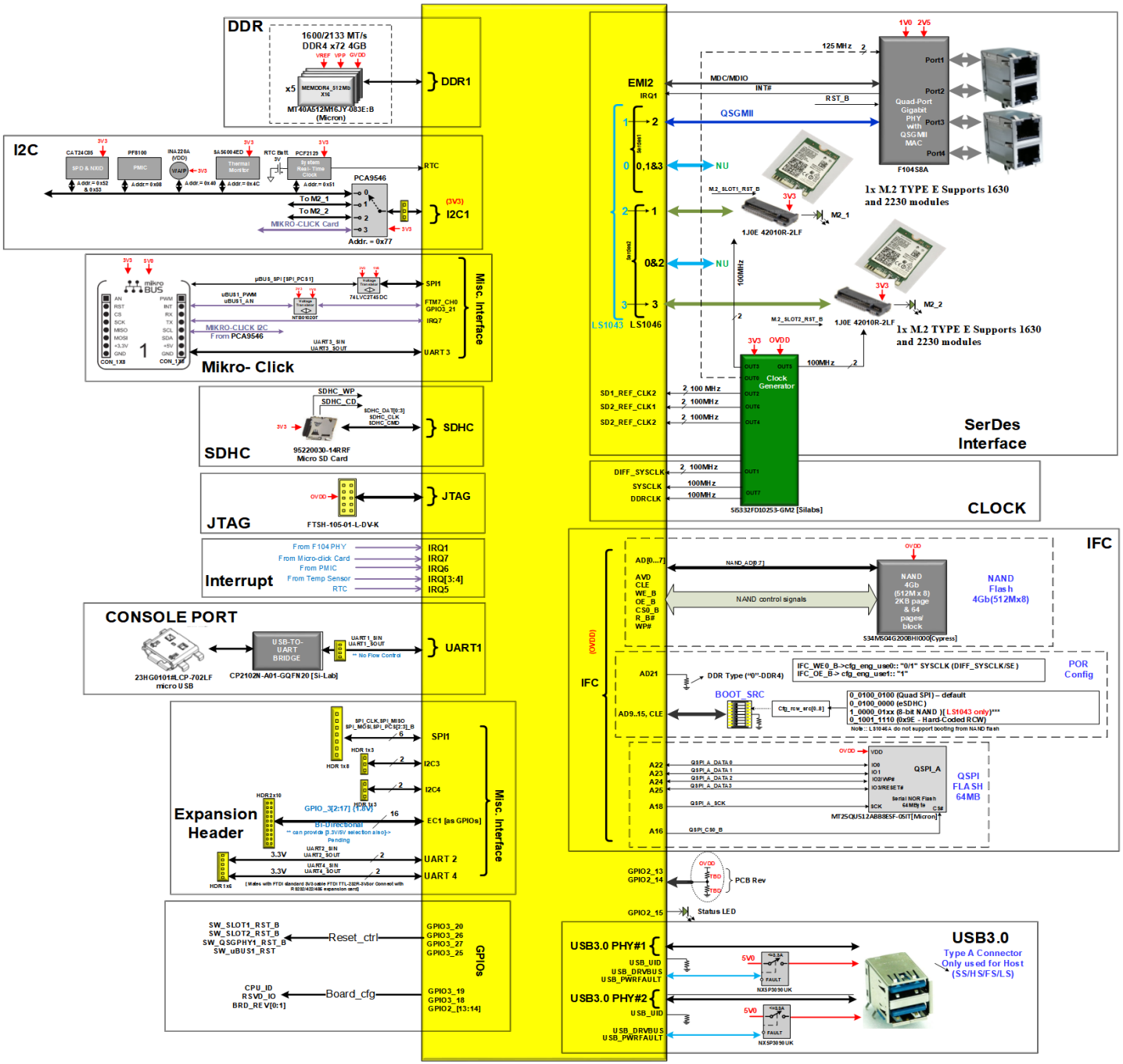
<Variant Name>

Digital Networking Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X1 PUBI:

Designer: RITURAJ ANAND	Drawing Title: FRWYLS1046A-PA		
Drawn by: RITURAJ ANAND	Page Title: TITLE		
Approved:	Size C	Document Number SCH-43607 PDF: SPF-43607	Rev B
	Date: Monday, March 18, 2019	Sheet 1 of 20	

FRWYLS1046A-PA



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ICAP Classification: CP: ___ IUO: X1 PUBI: ___

Drawing Title: **FRWYLS1046A-PA**

Page Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
C	SCH-43607 PDF: SPF-43607	B

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Layer	Info	Thickness
TOP	==========	0.5+Plating Oz
	PP IT180A 1080H	3.347 (mil)
L2	==========	1 Oz
	Core IT180A 0.076mm	2.992 (mil)
L3	==========	0.5 Oz
	PP IT180A 2116*1	4.2 (mil)
	Core(Exclude copper) IT180A 0.8mm	31.496 (mil)
	PP IT180A 2116*1	4.2 (mil)
L4	==========	0.5 Oz
	Core IT180A 0.076mm	2.992(mil)
L5	==========	1 Oz
	PP IT180A 1080H	3.347(mil)
BOT	==========	0.5+Plating Oz

Finished:	62(+6.2/-6.2) mil	1.57 (+0.16/-0.16 MM
Designed:	57.3mil	1.455 MM
Material:	IT180A	IT180A

Impedance Information:

Ctrl	Ref	Imp_type	Cust_req	Imp_req	HB_des	Imp_des	mask	H1	Er1	H2	Er2
L1	L2	Single-Ended	7	40+/-10%	8	41.84	Yes	3.347	3.8		
L1	L2	Single-Ended	6	50+/-10%	5.4	51.42	Yes	3.347	3.8		
L1	L2	Differential	4.1/7.8	100+/-10%	4.9/7.7	100.4	Yes	3.347	3.8		
L1	L2	Differential	4.3/4.5	90+/-10%	5.2/4.5	90.22	Yes	3.347	3.8		
L1	L2	Differential	4.8/5.1	80+/-10%	6.6/4.4	80.69	Yes	3.347	3.8		
L3	L2/L5	Single-Ended	7	40+/-10%	6.8	38.91		2.992	3.95	44.2	4.15
L3	L2/L5	Single-Ended	5	50+/-10%	4.2	49.66		2.992	3.95	44.2	4.15
L3	L2/L5	Differential	4.1/10.5	100+/-10%	3.7/10.9	99.85		2.992	3.95	44.2	4.15
L3	L2/L5	Differential	4.3/5.8	90+/-10%	4.1/6	89.28		2.992	3.95	44.2	4.15
L3	L2/L5	Differential	5.1/4.5	80+/-10%	4.8/4.8	80.38		2.992	3.95	44.2	4.15
L4	L2/L5	Single-Ended	5	50+/-10%	4.2	49.66		2.992	3.95	44.2	4.15
L4	L2/L5	Differential	4.1/10.5	100+/-10%	3.7/10.9	99.85		2.992	3.95	44.2	4.15
L4	L2/L5	Differential	4.3/5.8	90+/-10%	4.1/6	89.28		2.992	3.95	44.2	4.15
L4	L2/L5	Single-Ended	7	40+/-10%	6.8	38.91		2.992	3.95	44.2	4.15
L6	L5	Single-Ended	6	50+/-10%	5.4	51.42	Yes	3.347	3.8		
L6	L5	Differential	4.3/4.5	90+/-10%	5.2/4.5	90.22	Yes	3.347	3.8		
L6	L5	Differential	4.1/78	100+/-10%	4.9/7.7	100.4	Yes	3.347	3.8		

<Variant Name>

ICAP Classification: CP: ___ IUO: X1 PUBI: ___

Drawing Title: FRWYLS1046A-PA

Page Title: PCB STACKUP

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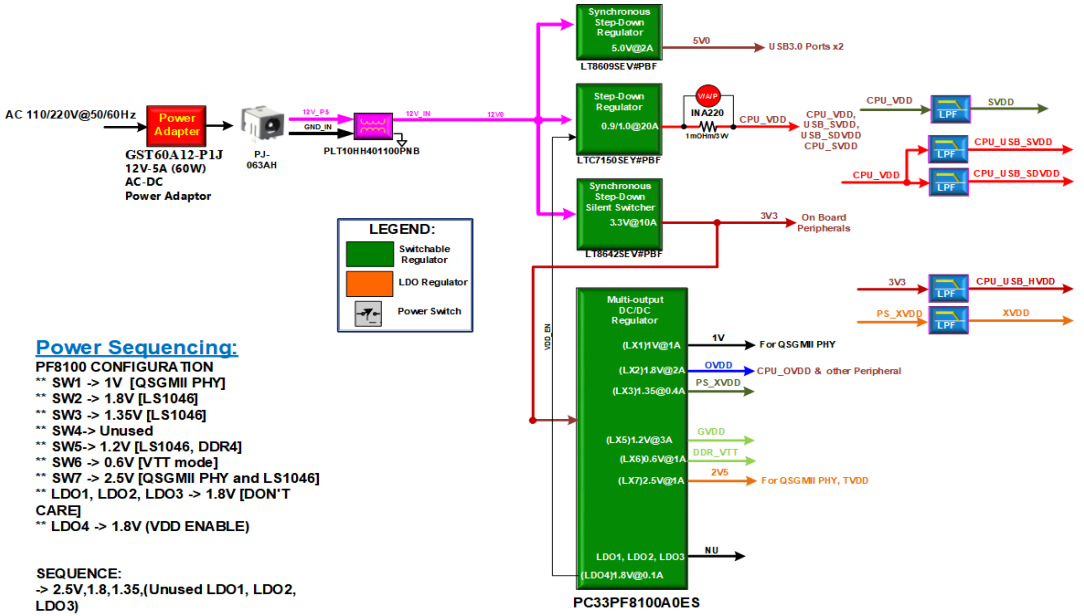
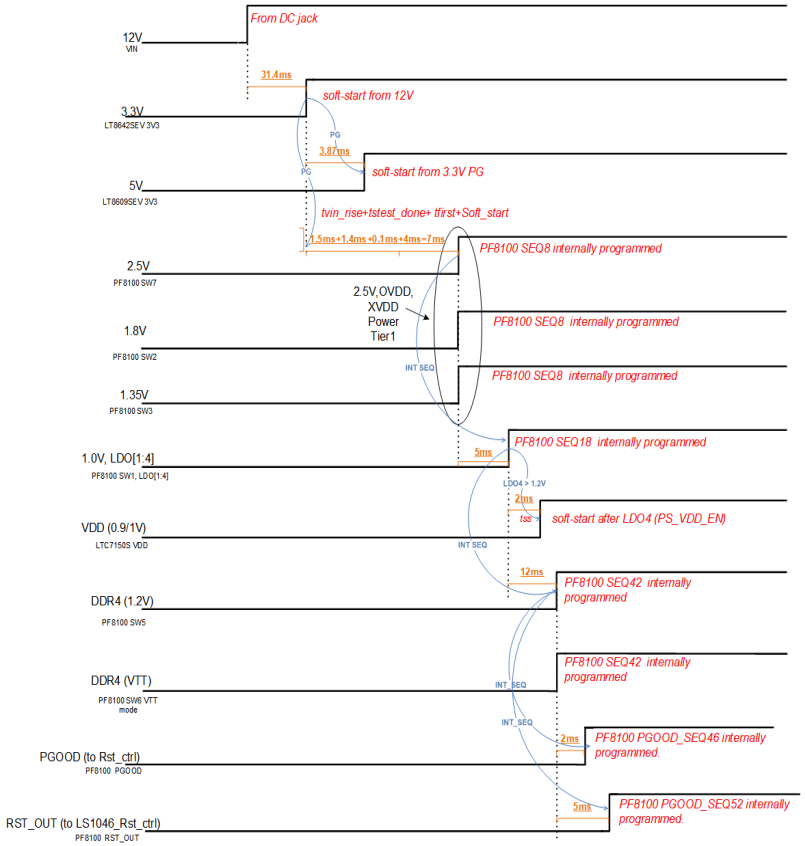


Power Sequencing:

PF8100 CONFIGURATION
** SW1 -> 1V [QSGMII PHY]
** SW2 -> 1.8V [LS1046]
** SW3 -> 1.35V [LS1046]
** SW4-> Unused
** SW5-> 1.2V [LS1046, DDR4]
** SW6 -> 0.6V [VTT mode]
** SW7 -> 2.5V [QSGMII PHY and LS1046]
** LDO1, LDO2, LDO3 -> 1.8V [DON'T CARE]
** LDO4 -> 1.8V (VDD ENABLE)

SEQUENCE:
-> 2.5V,1.8,1.35,(Unused LDO1, LDO2, LDO3)
-> 1.0, LDO4 (VDD ENABLE)
-> 1.2V and 0.6V
-> PGOOD, MCU_RESET_B



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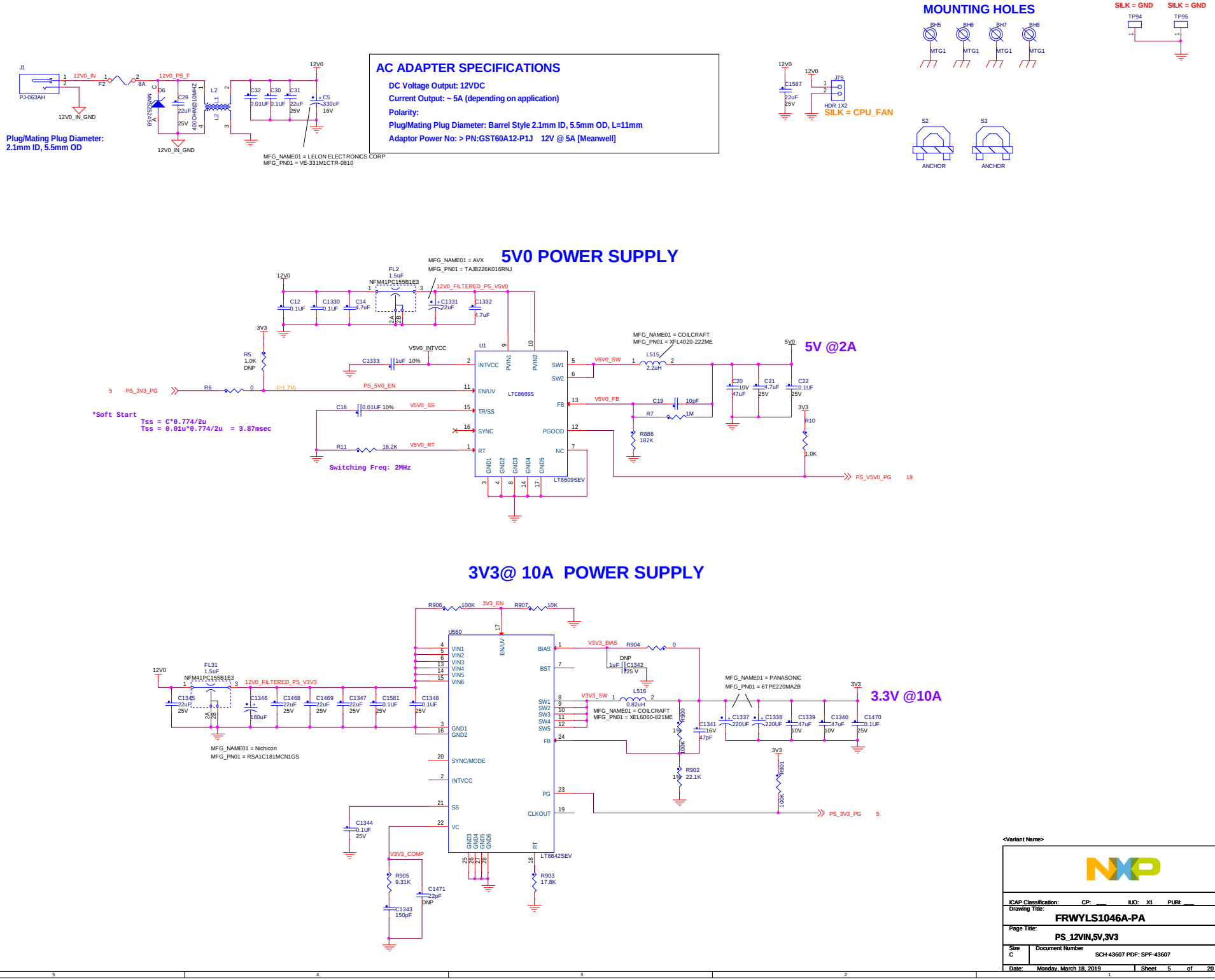
Size C | Document Number SCH-43607 PDF: SPF-43607 | Rev B
Date: Monday, March 18, 2019 | Sheet 4 of 20


MOUNTING HOLES
BH5
BH6
BH7
BH8
MTG1
SILK = GND
SILK = GND
TP94
TP95
AC ADAPTER SPECIFICATIONS
DC Voltage Output: 12VDC
Current Output: ~ 5A (depending on application)
Polarity:
Plug/Mating Plug Diameter: Barrel Style 2.1mm ID, 5.5mm OD, L=11mm
Adaptor Power No: > PN:GST60A12-P1J 12V @ 5A [Meanwell]
Plug/Mating Plug Diameter:
2.1mm ID, 5.5mm OD
J1
PJ-063AH
12V0_IN
12V0_IN_GND
F2
8A
12V0_PS_F
D6
B5819WS
C29
22uF
25V
L2
400OHM@10MHZ
L1
C32
0.01UF
C30
0.1UF
C31
22uF
25V
C5
330uF
16V
MFG_NAME01 = LELON ELECTRONICS CORP
MFG_PN01 = VE-331M1CTR-0810
C1587
22uF
25V
J75
HDR 1X2
SILK = CPU_FAN
S2
S3
ANCHOR
5V0 POWER SUPPLY
MFG_NAME01 = AVX
MFG_PN01 = TAJB226K016RNJ
FL2
1.5uF
NFM41PC155B1E3
12V0_FILTERED_PS_V5V0
C12
0.1UF
C1330
0.1UF
C14
4.7uF
C1331
22uF
C1332
4.7uF
3V3
R5
1.0K
DNP
V5V0_INTVCC
C1333
1uF 10%
U1
INTVCC
PVIN1
PVIN2
SW1
SW2
EN/UV
TR/SS
SYNC
FB
PGOOD
NC
RT
GND1
GND2
GND3
GND4
GND5
LTC8609S
LT8609SEV
R6
0
(>1.2V)
PS_3V3_PG
PS_5V0_EN
C18
0.01UF 10%
V5V0_SS
R11
18.2K
V5V0_RT
Switching Freq: 2MHz
*Soft Start
Tss = C*0.774/2u
Tss = 0.01u*0.774/2u = 3.87msec
MFG_NAME01 = COILCRAFT
MFG_PN01 = XFL4020-222ME
L515
2.2uH
V5V0_SW
V5V0_FB
C19
10pF
R7
1M
R886
182K
C20
10V
47uF
C21
4.7uF
25V
C22
0.1UF
25V
5V0
5V @2A
R10
1.0K
PS_V5V0_PG
19
3V3@ 10A POWER SUPPLY
R906
100K
3V3_EN
R907
10K
U560
ENUV
VIN1
VIN2
VIN3
VIN4
VIN5
VIN6
BIAS
BST
SW1
SW2
SW3
SW4
SW5
FB
GND1
GND2
SYNC/MODE
INTVCC
SS
VC
PG
CLKOUT
RT
GND3
GND4
GND5
GND6
LT8642SEV
V3V3_BIAS
R904
0
DNP
1uF
C1342
25 V
V3V3_SW
L516
0.82uH
MFG_NAME01 = COILCRAFT
MFG_PN01 = XEL6060-821ME
R900
100K
C1341
16V
47pF
R902
22.1K
R901
100K
MFG_NAME01 = PANASONIC
MFG_PN01 = 6TPE220MAZB
C1337
220UF
C1338
220UF
C1339
47uF
10V
C1340
47uF
10V
C1470
0.1UF
25V
3.3V @10A
FL31
1.5uF
NFM41PC155B1E3
12V0_FILTERED_PS_V3V3
C1345
22uF
25V
C1346
180uF
C1468
22uF
25V
C1469
22uF
25V
C1347
22uF
25V
C1581
0.1UF
25V
C1348
0.1UF
25V
MFG_NAME01 = Nichicon
MFG_PN01 = RSA1C181MCN1GS
C1344
0.1UF
25V
V3V3_COMP
R905
9.31K
C1471
22pF
DNP
C1343
150pF
R903
17.8K
PS_3V3_PG
5
<Variant Name>
NXP
ICAP Classification:
CP:
IUO: X1
PUBI:
Drawing Title:
FRWYLS1046A-PA
Page Title:
PS_12VIN,5V,3V3
Size
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Document Number
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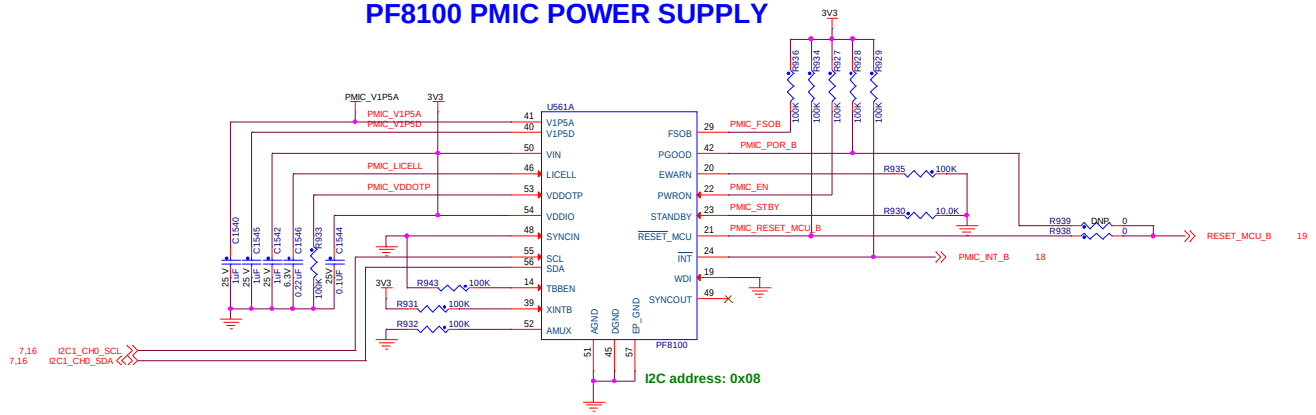
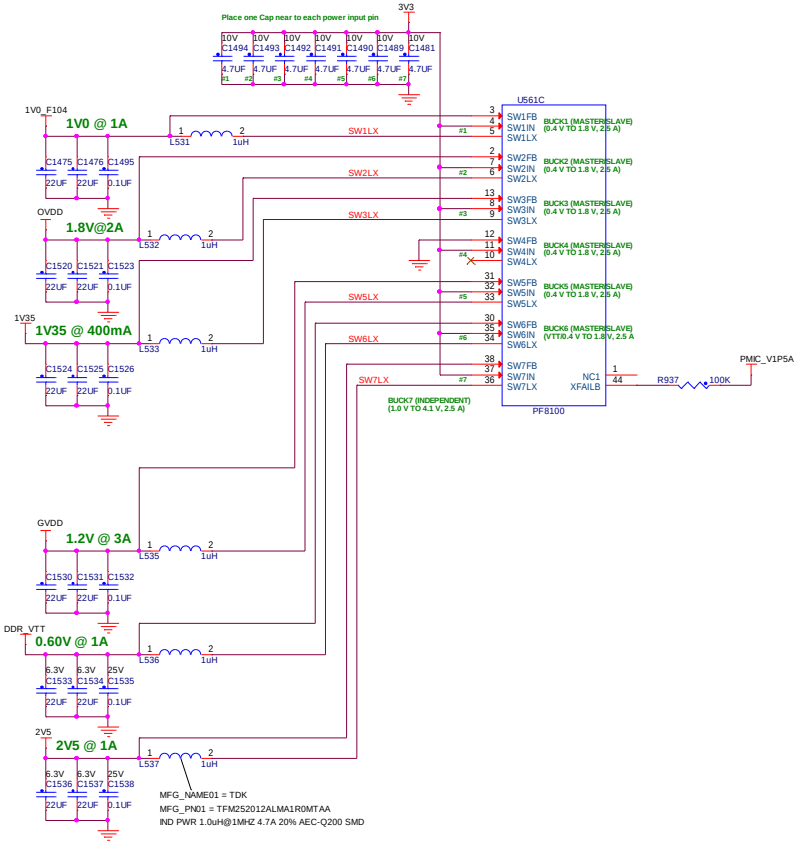
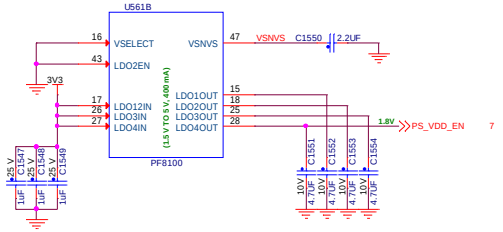
PF8100 PMIC POWER SUPPLY







PF8100 CONFIGURATION

** SW1 -> 1V [QSGMII PHY]
** SW2 -> 1.8V [LS1046]
** SW3 -> 1.35V [LS1046]
** SW4 -> Unused
** SW5-> 1.2V [LS1046, DDR4]
** SW6 -> 0.6V
** SW7 -> 2.5V [QSGMII PHY and LS1046]
** LDO1, LDO2, LDO3 -> 1.8V [DON'T CARE]
** LDO4 -> 1.8V (VDD ENABLE)

SEQUENCE:

-> 2.5V,1.8,1.35,(Unused LDO1, LDO2, LDO3)
-> 1.0, LDO4 (VDD ENABLE)
-> 1.2V and 0.6V
-> PGOOD, MCU_RESET_B

<Variant Name>

ICAP Classification: CP: ___ IUO: X1 PUBI: ___

Drawing Title: FRWYLS1046A-PA

Page Title: PS_DDR_VR5100_PMIC

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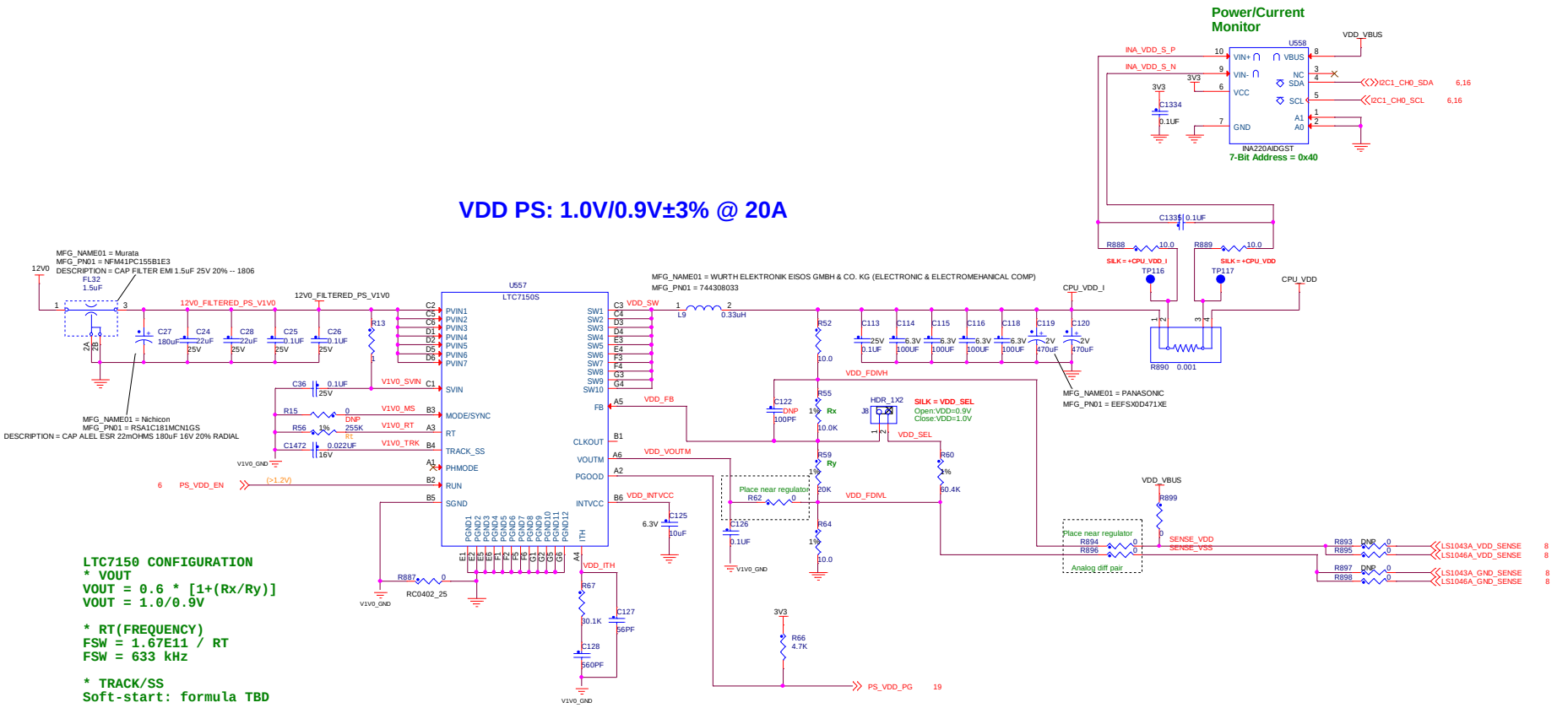
VDD PS: 1.0V/0.9V±3% @ 20A



LTC7150 CONFIGURATION

*** VOUT**
VOUT = 0.6 * [1+(Rx/Ry)]
VOUT = 1.0/0.9V

*** RT(FREQUENCY)**
FSW = 1.67E11 / RT
FSW = 633 kHz

*** TRACK/SS**
Soft-start: formula TBD

*** MODE/SYNC**
GND = discontinuous
FLOAT = forced continuous

*** PHMODE**
FLOAT = 2phase (internal)

*** ITH (LOOP COMPENSATION)**
See spec.

<variant_name>

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **FRWYLS1046A-PA**

Page Title: **PS_VDD**

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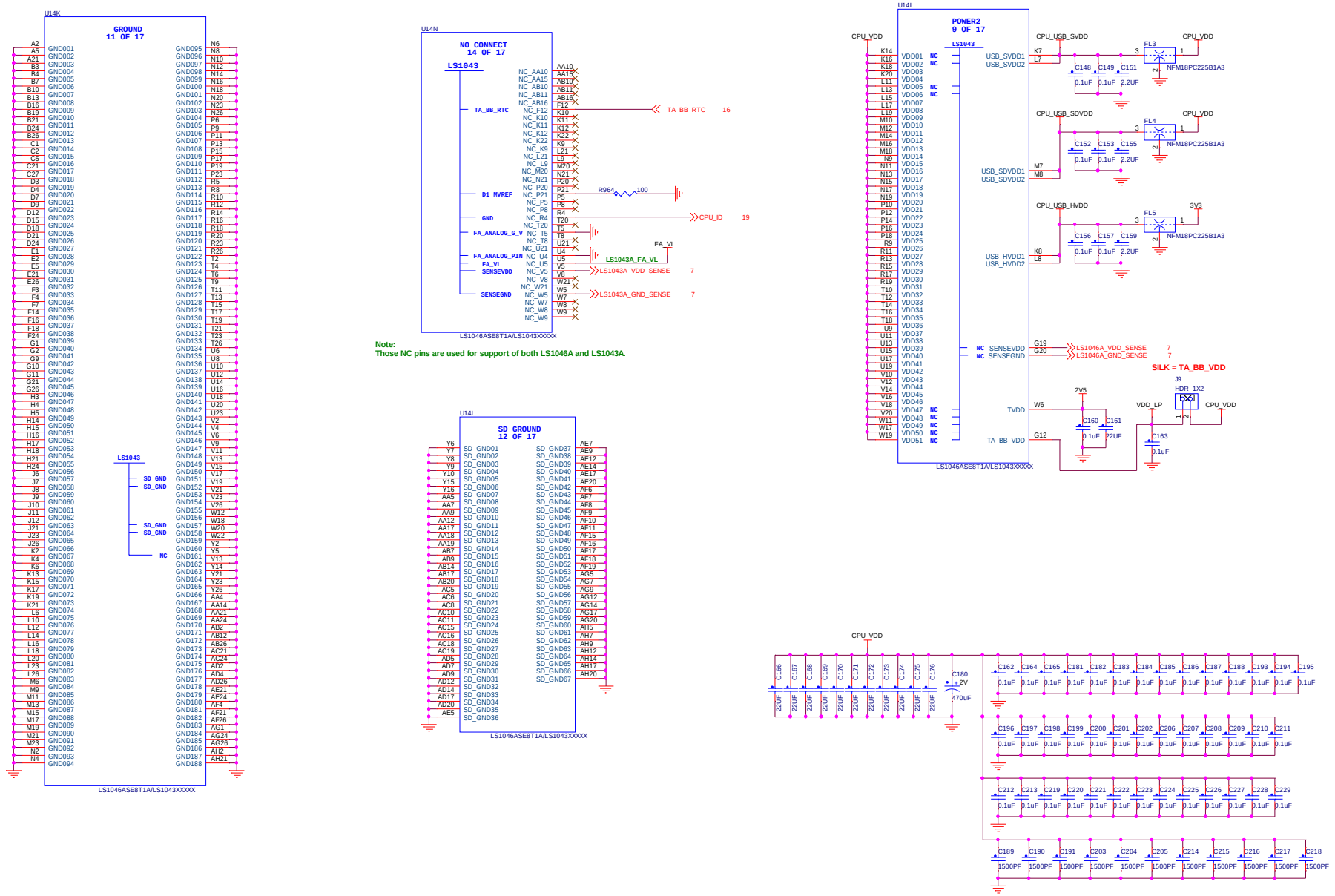

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Drawing Title: **FRWYLS1046A-PA**

Page Title: **CPU POWER1**

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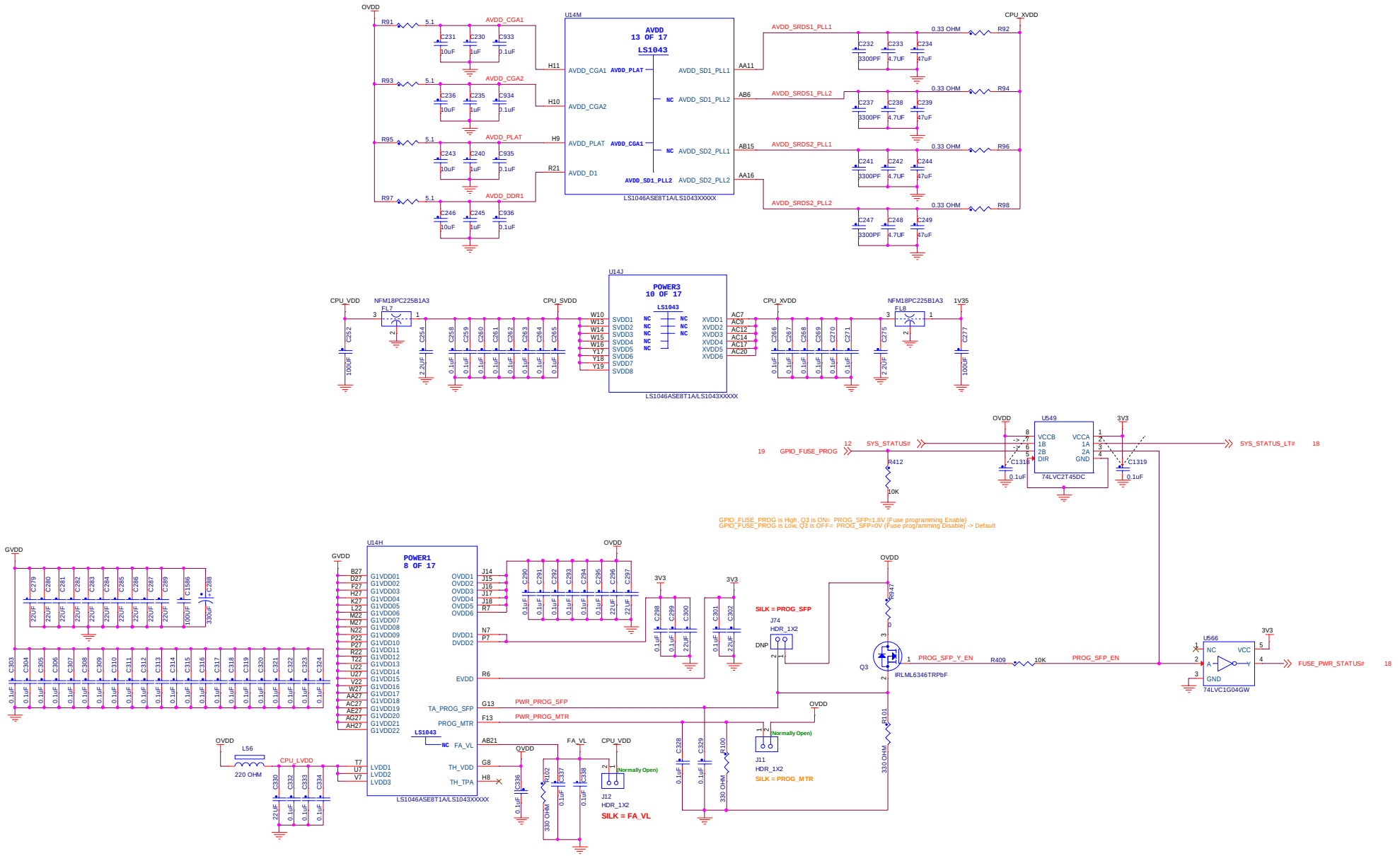

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Page Title:	CPU POWER2	
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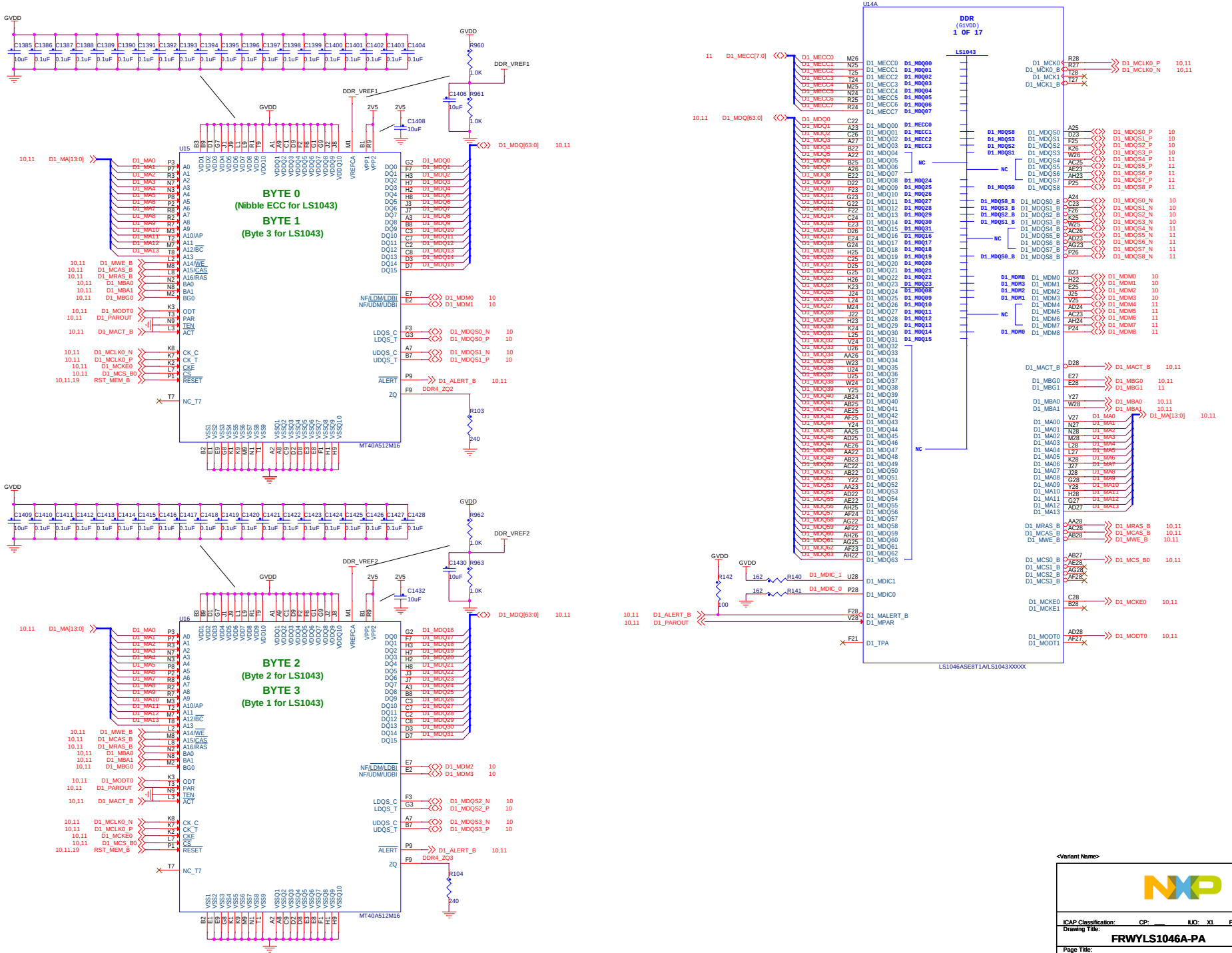

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Size: C	Document Number: SCH-43607 PDF: SPF-43607		Rev: B
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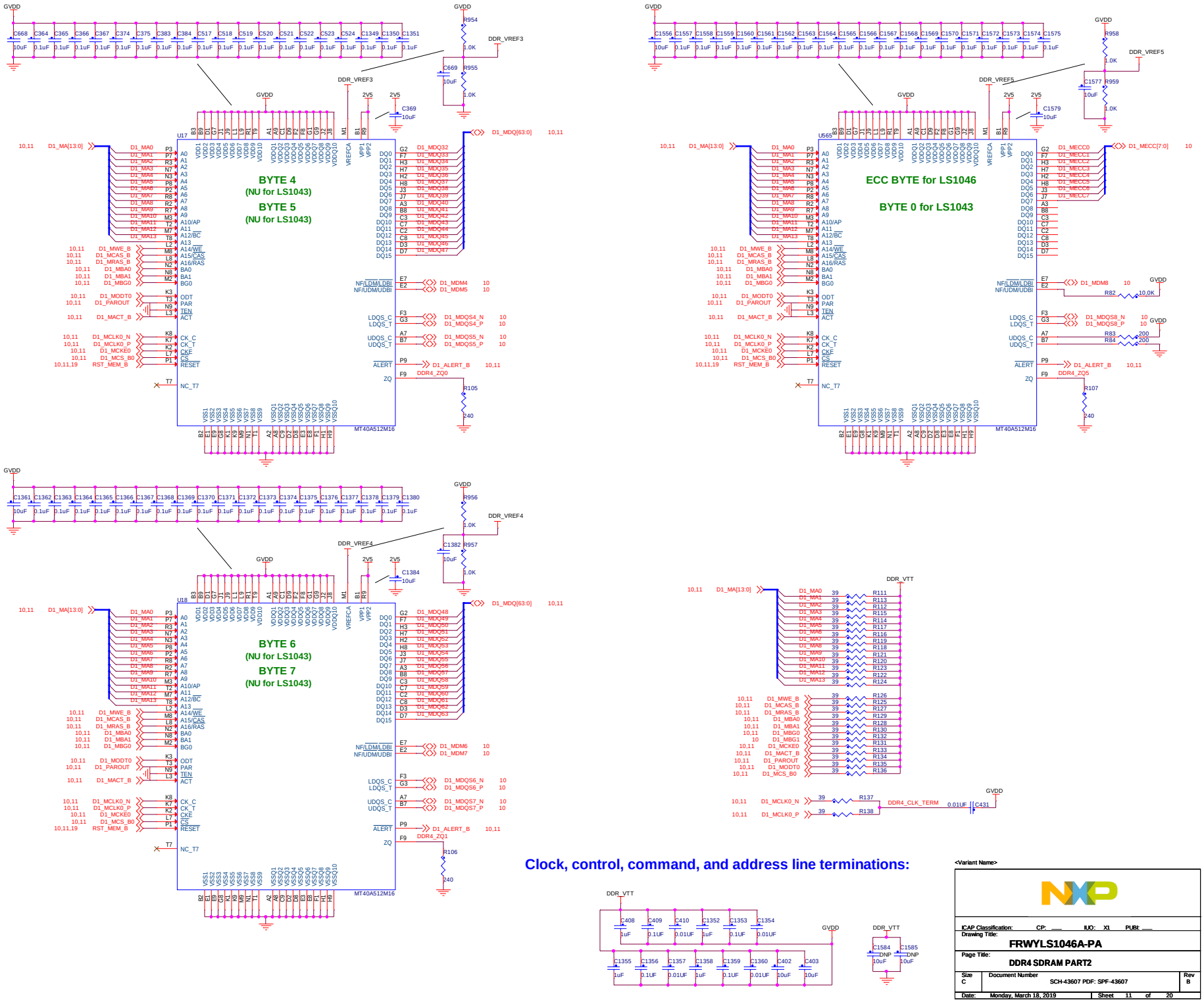

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Drawing Title:

FRWYLS1046A-PA

Page Title:

DDR4 SDRAM PART2

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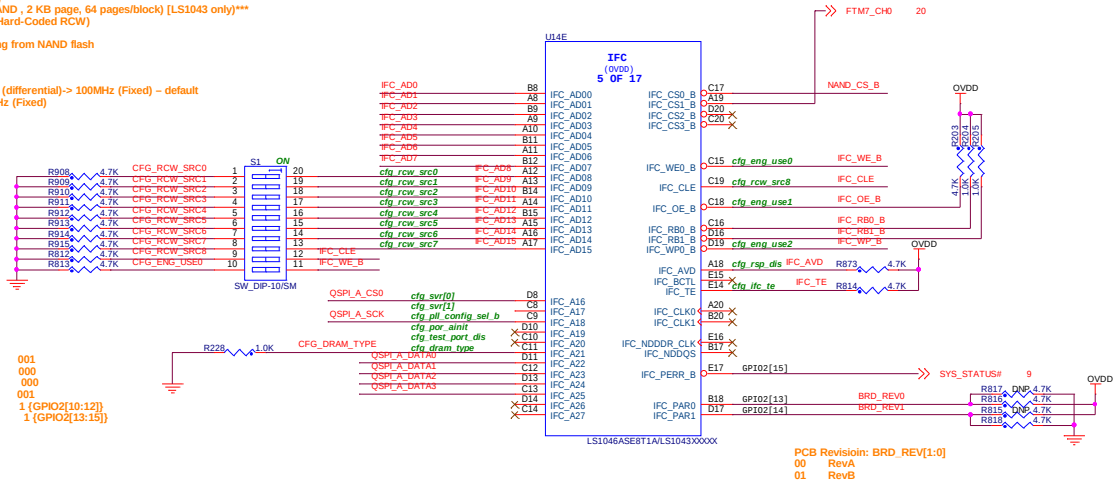
CPU BOOT SOURCE and POR CONFIG

SW1[1:9]=> CFG_RCW_SRC[0:8]
0_0100_0100 (Quad SPI) – default
0_0100_0000 (eSDHC)
1_0000_01xx (8-bit NAND , 2 KB page, 64 pages/block) [LS1043 only)***
0_1001_1110 (0x9E - Hard-Coded RCW)

Note:: LS1046A do not support booting from NAND flash

SW1[10]=> CFG_ENG_USE0
# 0 DIFF_SYSCLK/DIFF_SYSCLK_B (differential)-> 100MHz (Fixed) – default
# 1 SYSCLK (single ended)-> 100MHz (Fixed)

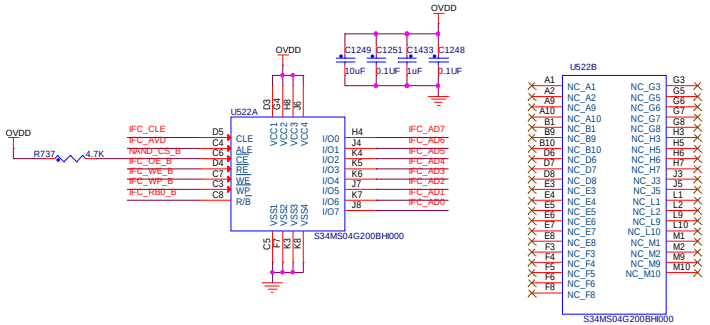


RCW Settings:

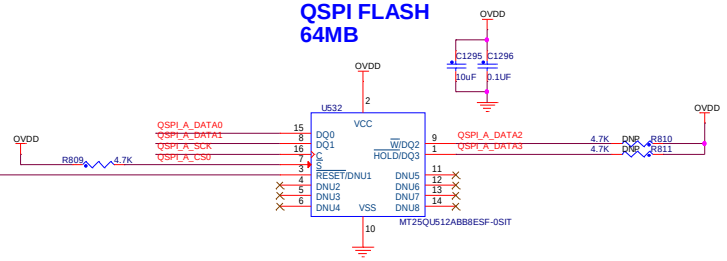
IFC_GRP_A_EXT	001
IFC_GRP_D_EXT	000
FC_GRP_E1_EXT	000
IFC_GRP_F_EXT	001
IFC_GRP_E1_BASE	1 {GPIO2[10:12]}
IFC_GRP_D_BASE	1 {GPIO2[13:15]}

PCB Revisoin: BRD_REV[1:0]
00 RevA
01 RevB

NAND Flash 4Gb(512Mx8)



QSPI FLASH 64MB



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Drawing Title: **FRWYLS1046A-PA**

Page Title: **CPU_QSPI & NAND**

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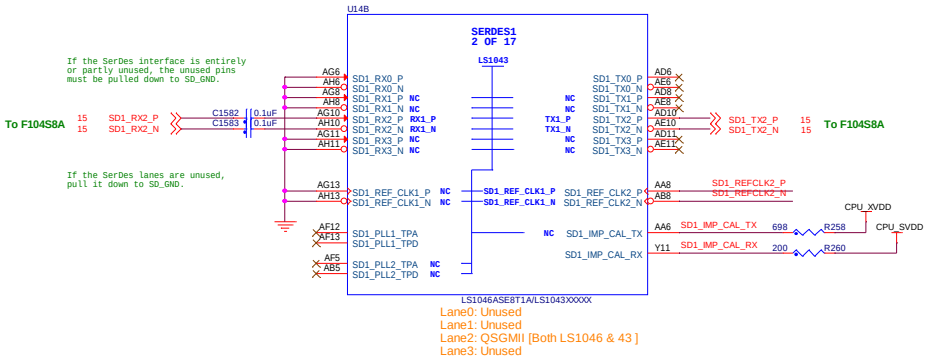
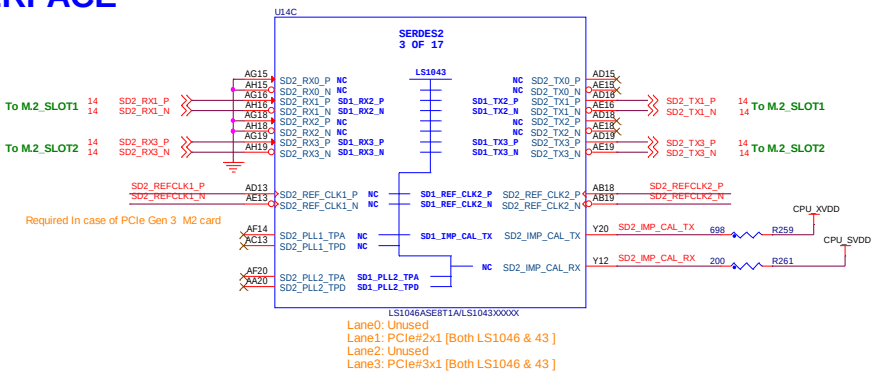
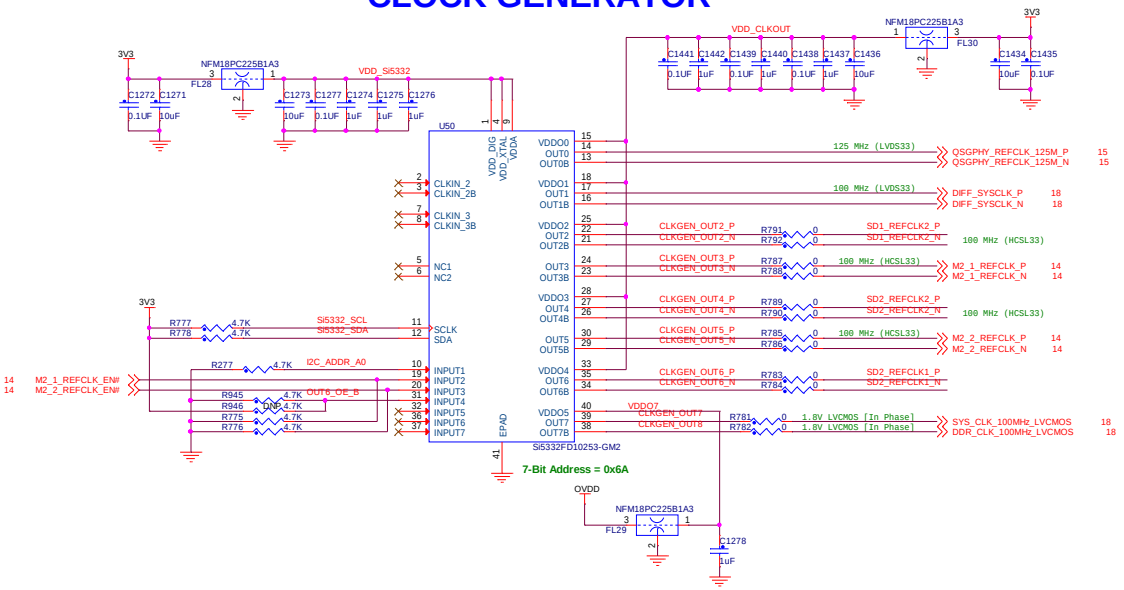
SERDES INTERFACE





CLOCK GENERATOR



Outputs:

OUT0: 125 MHz LVDS Fast 3.3 V

OUT1: 100 MHz LVDS Fast 3.3 V

OUT2: 100 MHz HCSL 3.3 V 50 Ohms - Internal Termination

OUT3: 100 MHz HCSL 3.3 V 50 Ohms - Internal Termination
OEB INPUT2 (P19)

OUT4: 100 MHz HCSL 3.3 V 50 Ohms - InternalTermination

OUT5: 100 MHz HCSL 3.3 V 50 Ohms - InternalTermination
OEB INPUT3 (P20)

OUT6: 100 MHz HCSL 3.3 V 50 Ohms - Internal Termination
OEB INPUT4 (P31)

OUT7: 100 MHz LVCMOS (in-phase) 1.8 V 50 Ohms

<Variant Name>

ICAP Classification: CP: ___ IUO: X1 PUBI: ___

Drawing Title: **FRWYLS1046A-PA**

Page Title: **CPU SERDES & CLOCKS**

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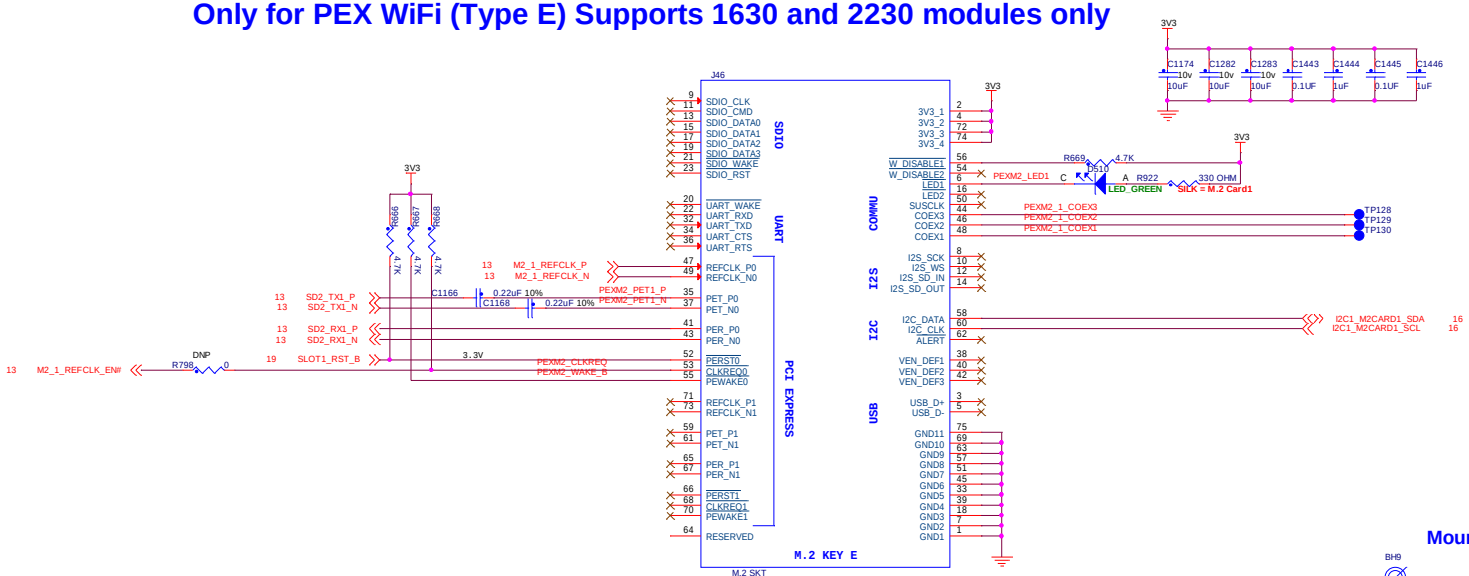
M.2 Connector (I)
Only for PEX WiFi (Type E) Supports 1630 and 2230 modules only

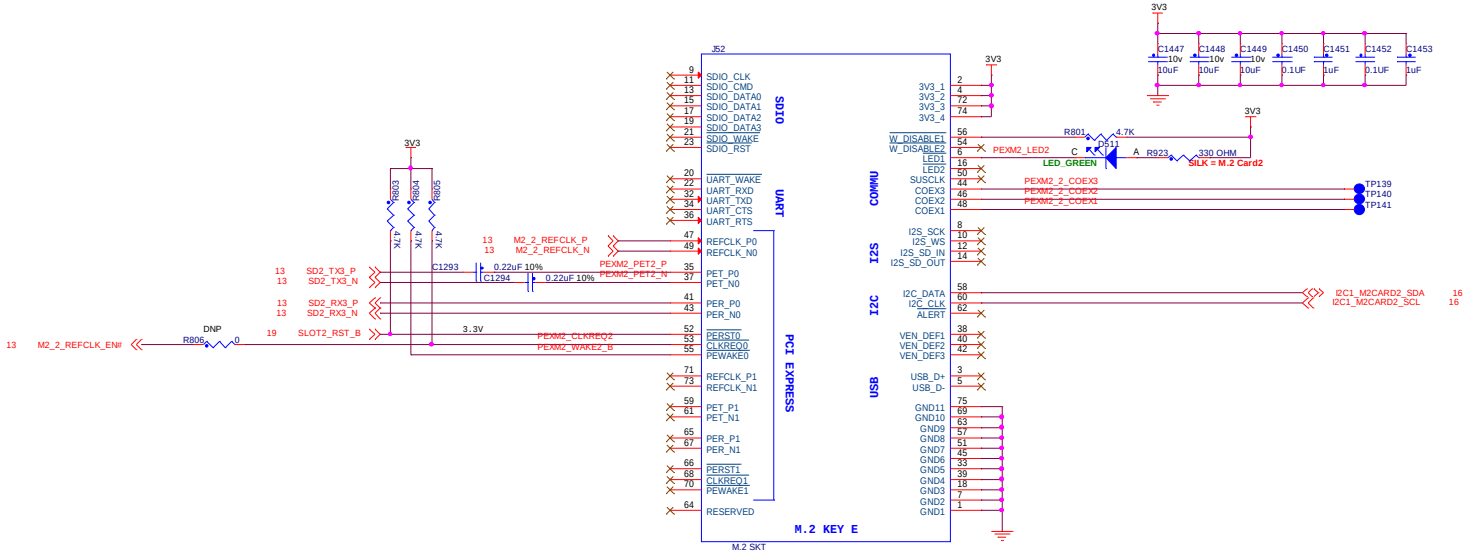


NOTE: ONLY 1630 anf 2230 Size M.2 Type E modules shal be supported.

Mounting Hole for M.2 Slots

Near J52 and J46 at 30mm
(Shouldered STANDOFF M2X0.4 SMD]

M.2 Connector (2)
Only for PEX WiFi (Type E) Supports 1630 and 2230 modules only



NOTE: ONLY 1630 anf 2230 Size M.2 Type E modules shal be supported.

<Variant Name>

ICAP Classification: CP: ___ IUO: X1 PUBL: ___

Drawing Title: **FRWYLS1046A-PA**

Page Title: **M.2_PCIe_CARD**

Size	Document Number	Rev
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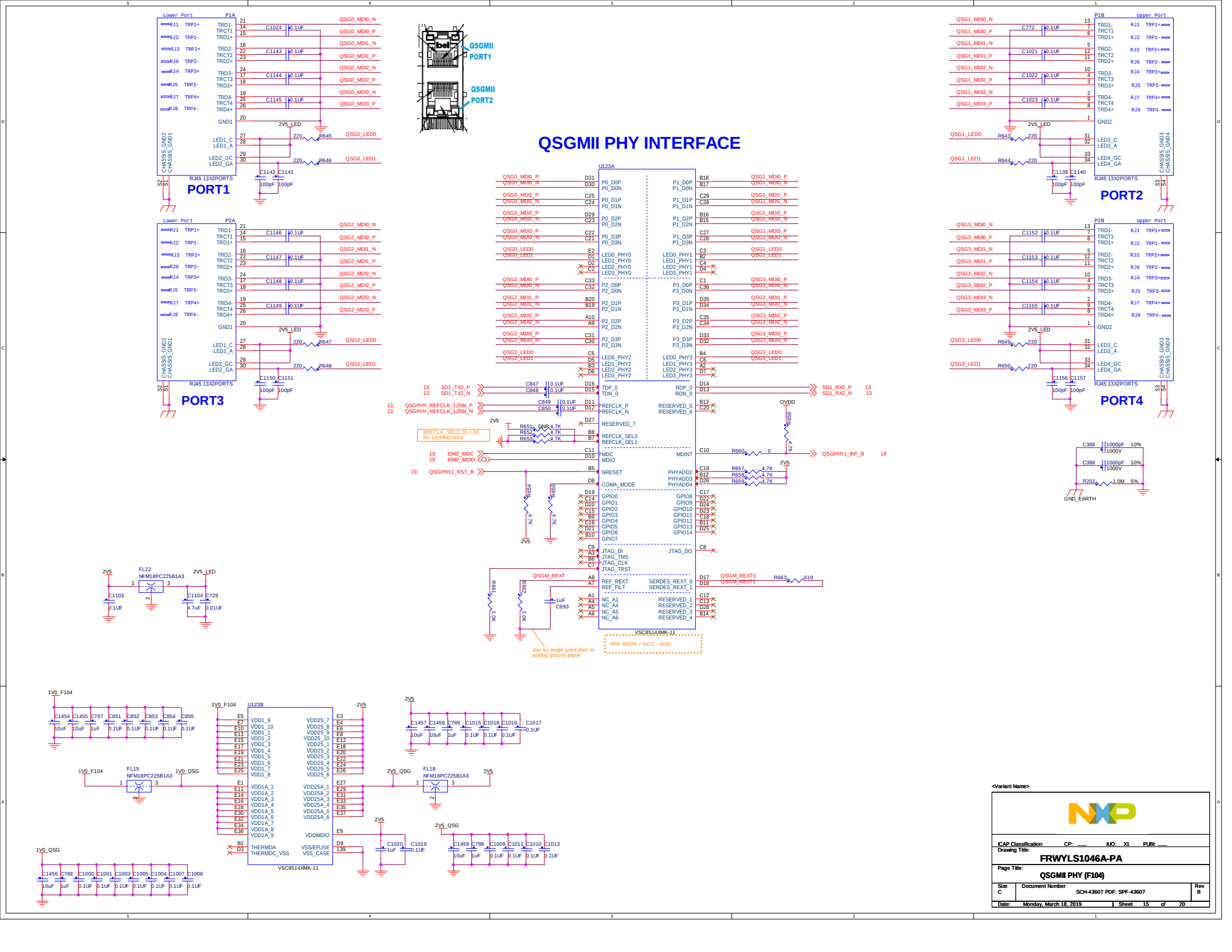
QSGMII PHY INTERFACE
PORT1
PORT2
PORT3
PORT4
QSGMII PORT1
QSGMII PORT2
U123A
U123B
VSC8514XMK-11
PHY ADDR = 0x1C - 0x1F
Join as single point then to analog ground plane
REFCLK_SEL[1:0] = 00 for 125MHz clock
RJ45 13X2PORTS
FL22 NFM18PC225B1A3
FL19 NFM18PC225B1A3
FL18 NFM18PC225B1A3
GND_EARTH
<Variant Name>
FRWYLS1046A-PA
QSGMII PHY (F104)
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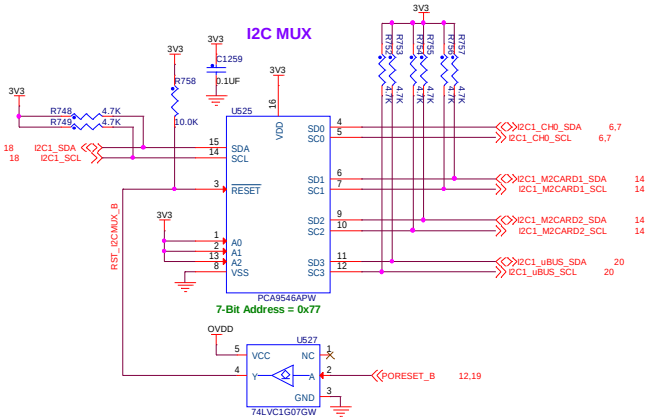
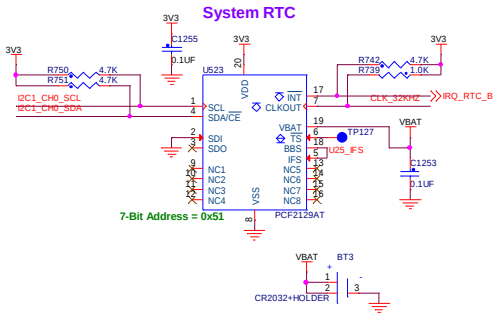
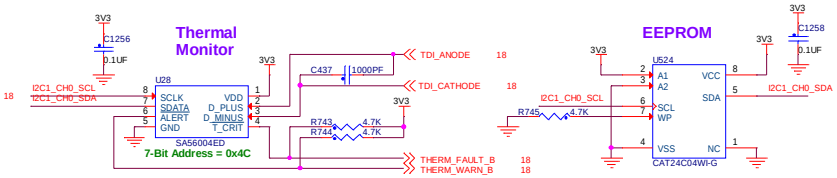
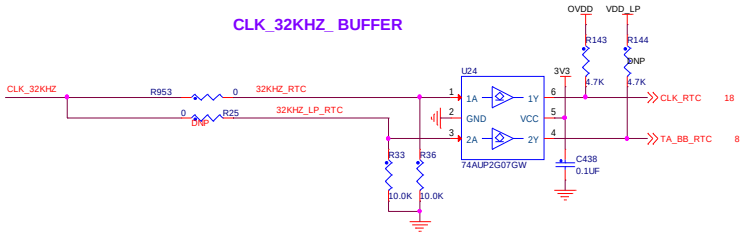
I2C INTERFACE

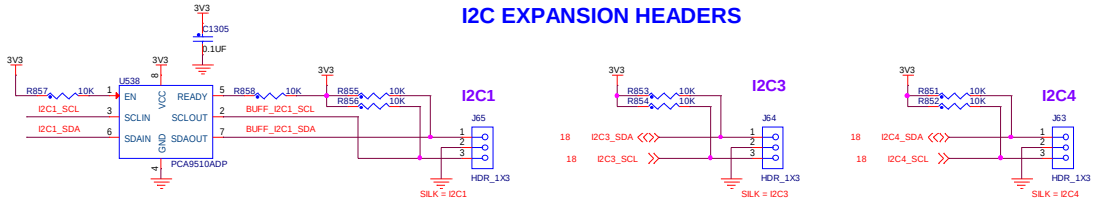








I2C EXPANSION HEADERS



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ICAP Classification:	CP: ___	IUO: X1	PUBL: ___	
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Page Title: I2C_INTERFACE				
Size C	Document Number SCH-43607 PDF: SPF-43607			Rev B
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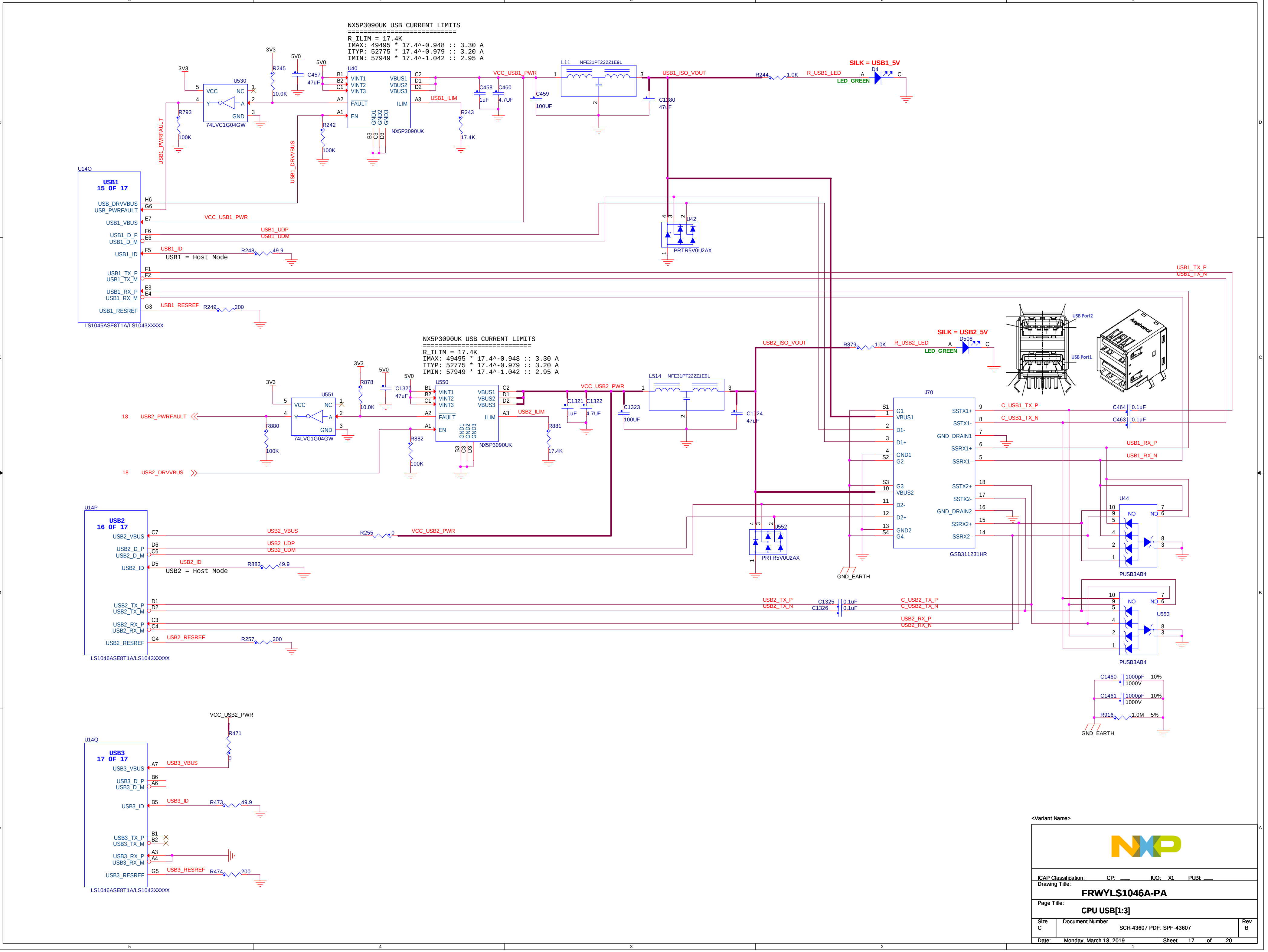
NX5P3090UK USB CURRENT LIMITS
============================
R_ILIM = 17.4K
IMAX: 49495 * 17.4^-0.948 :: 3.30 A
ITYP: 52775 * 17.4^-0.979 :: 3.20 A
IMIN: 57949 * 17.4^-1.042 :: 2.95 A
U530 74LVC1G04GW
U40 NX5P3090UK
L11 NFE31PT222Z1E9L
VCC_USB1_PWR
USB1_ISO_VOUT
SILK = USB1_5V
LED_GREEN
R_USB1_LED
USB1_ILIM
USB1_PWRFAULT
USB1_DRVVBUS
U14O
USB1
15 OF 17
USB_DRVVBUS
USB_PWRFAULT
USB1_VBUS
USB1_D_P
USB1_D_M
USB1_ID
USB1 = Host Mode
USB1_TX_P
USB1_TX_M
USB1_RX_P
USB1_RX_M
USB1_RESREF
LS1046ASE8T1A/LS1043XXXXX
U42 PRTR5V0U2AX
USB1_UDP
USB1_UDM
USB1_TX_N
SILK = USB2_5V
R_USB2_LED
USB2_ISO_VOUT
USB Port2
USB Port1
NX5P3090UK USB CURRENT LIMITS
============================
R_ILIM = 17.4K
IMAX: 49495 * 17.4^-0.948 :: 3.30 A
ITYP: 52775 * 17.4^-0.979 :: 3.20 A
IMIN: 57949 * 17.4^-1.042 :: 2.95 A
U551 74LVC1G04GW
U550 NXSP3090UK
L514 NFE31PT222Z1E9L
VCC_USB2_PWR
USB2_PWRFAULT
USB2_DRVVBUS
USB2_ILIM
J70 GSB311231HR
C_USB1_TX_P
C_USB1_TX_N
USB1_RX_N
U14P
USB2
16 OF 17
USB2_VBUS
USB2_D_P
USB2_D_M
USB2_ID
USB2 = Host Mode
USB2_TX_P
USB2_TX_M
USB2_RX_P
USB2_RX_M
USB2_RESREF
USB2_UDP
USB2_UDM
USB2_TX_N
C_USB2_TX_P
C_USB2_TX_N
USB2_RX_N
U552 PRTR5V0U2AX
GND_EARTH
U44 PUSB3AB4
U553 PUSB3AB4
C1460 1000pF 10% 1000V
C1461 1000pF 10% 1000V
R916 1.0M 5%
U14Q
USB3
17 OF 17
USB3_VBUS
USB3_D_P
USB3_D_M
USB3_ID
USB3_TX_P
USB3_TX_M
USB3_RX_P
USB3_RX_M
USB3_RESREF
<Variant Name>
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FRWYLS1046A-PA
Page Title:
CPU USB[1:3]
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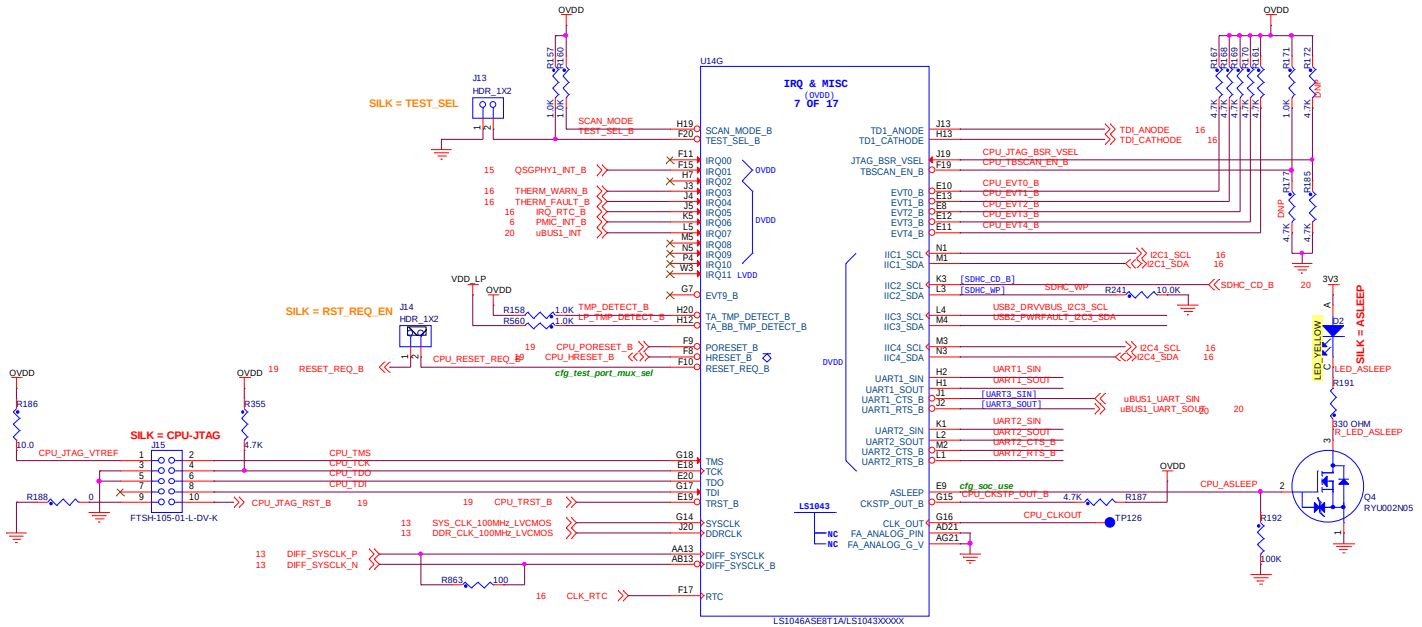
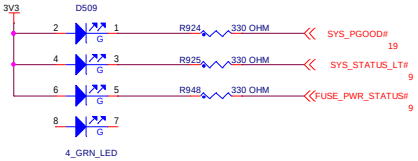
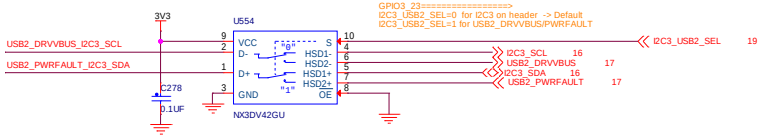
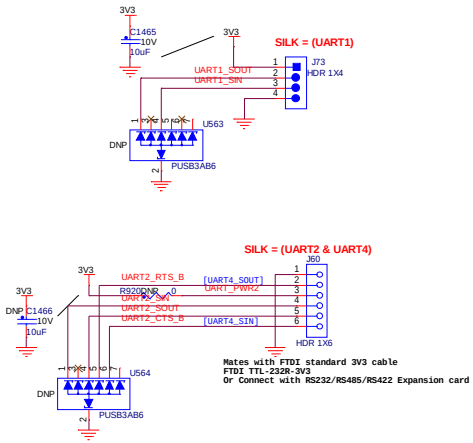


STATUS LEDS



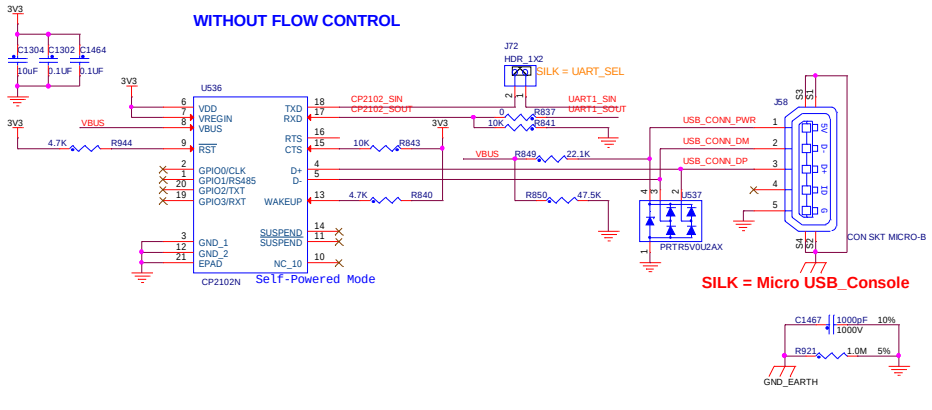


UART Expansion Header



USB-UART INTERFACE

WITHOUT FLOW CONTROL



<Variant Name>

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Page Title: CPU MISC. &UART
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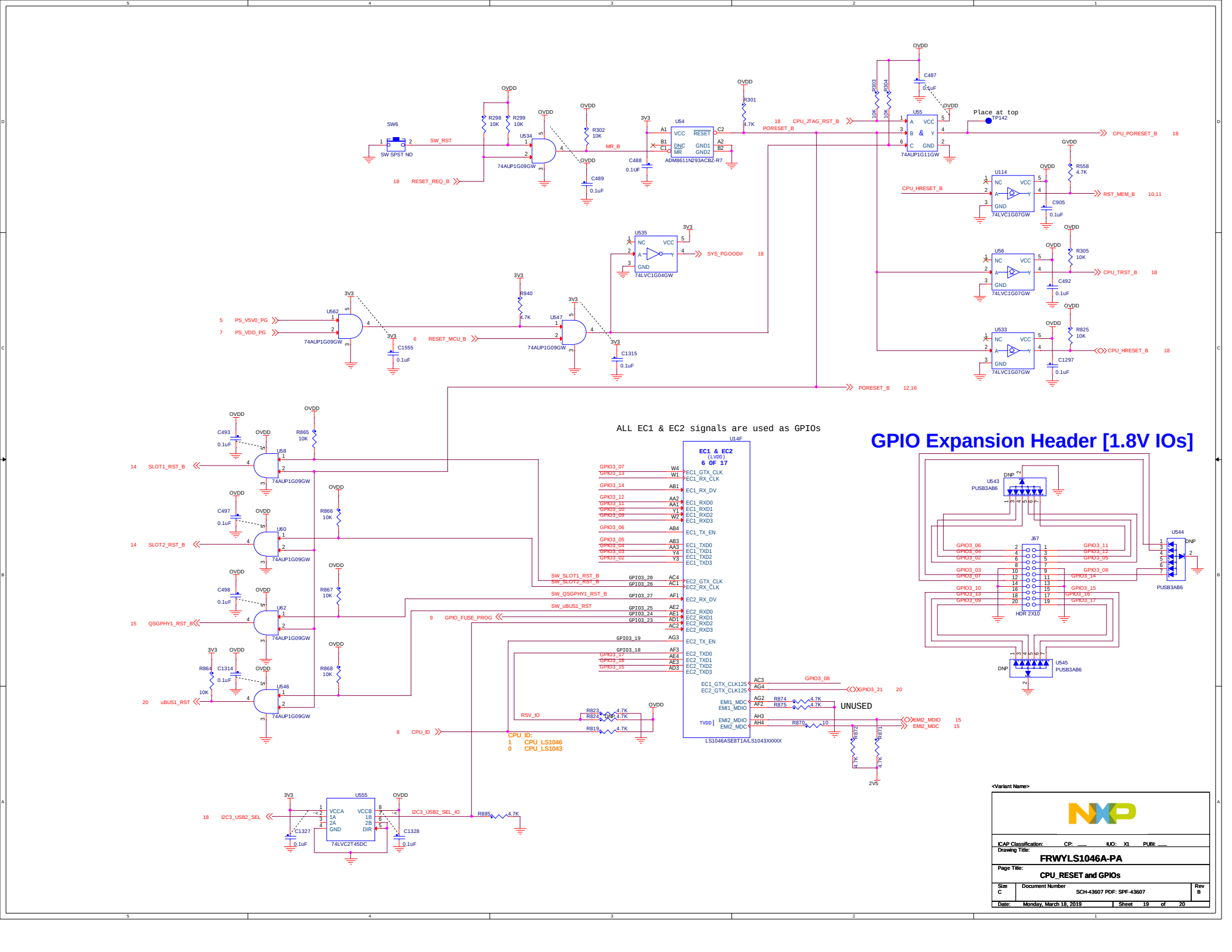
ALL EC1 & EC2 signals are used as GPIOs
GPIO Expansion Header [1.8V IOs]
SW6
SW SPST NO
SW_RST
RESET_REQ_B
MR_B
U534
74AUP1G09GW
U54
ADM8611NZ93ACBZ-R7
CPU_JTAG_RST_B
PORESET_B
U55
74AUP1G11GW
Place at top
TP142
CPU_PORESET_B
CPU_HRESET_B
RST_MEM_B
CPU_TRST_B
U114
U56
U533
74LVC1G07GW
U535
74LVC1G04GW
SYS_PGOOD#
PS_V5V0_PG
PS_VDD_PG
U562
U547
RESET_MCU_B
U14F
EC1 & EC2
(LVDD)
6 OF 17
LS1046ASE8T1A/LS1043XXXXX
SW_SLOT1_RST_B
SW_SLOT2_RST_B
SW_QSGPHY1_RST_B
SW_uBUS1_RST
GPIO_FUSE_PROG
CPU_ID
CPU_ID:
1 CPU_LS1046
0 CPU_LS1043
RSV_IO
UNUSED
U58
U60
U62
U546
74AUP1G09GW
SLOT1_RST_B
SLOT2_RST_B
QSGPHY1_RST_B
uBUS1_RST
U543
U544
U545
PUSB3AB6
J67
HDR 2X10
U555
74LVC2T45DC
I2C3_USB2_SEL
I2C3_USB2_SEL_IO
2V5
<Variant Name>
ICAP Classification:
CP:
IUO:
X1
PUBL:
Drawing Title:
FRWYLS1046A-PA
Page Title:
CPU_RESET and GPIOs
Size C
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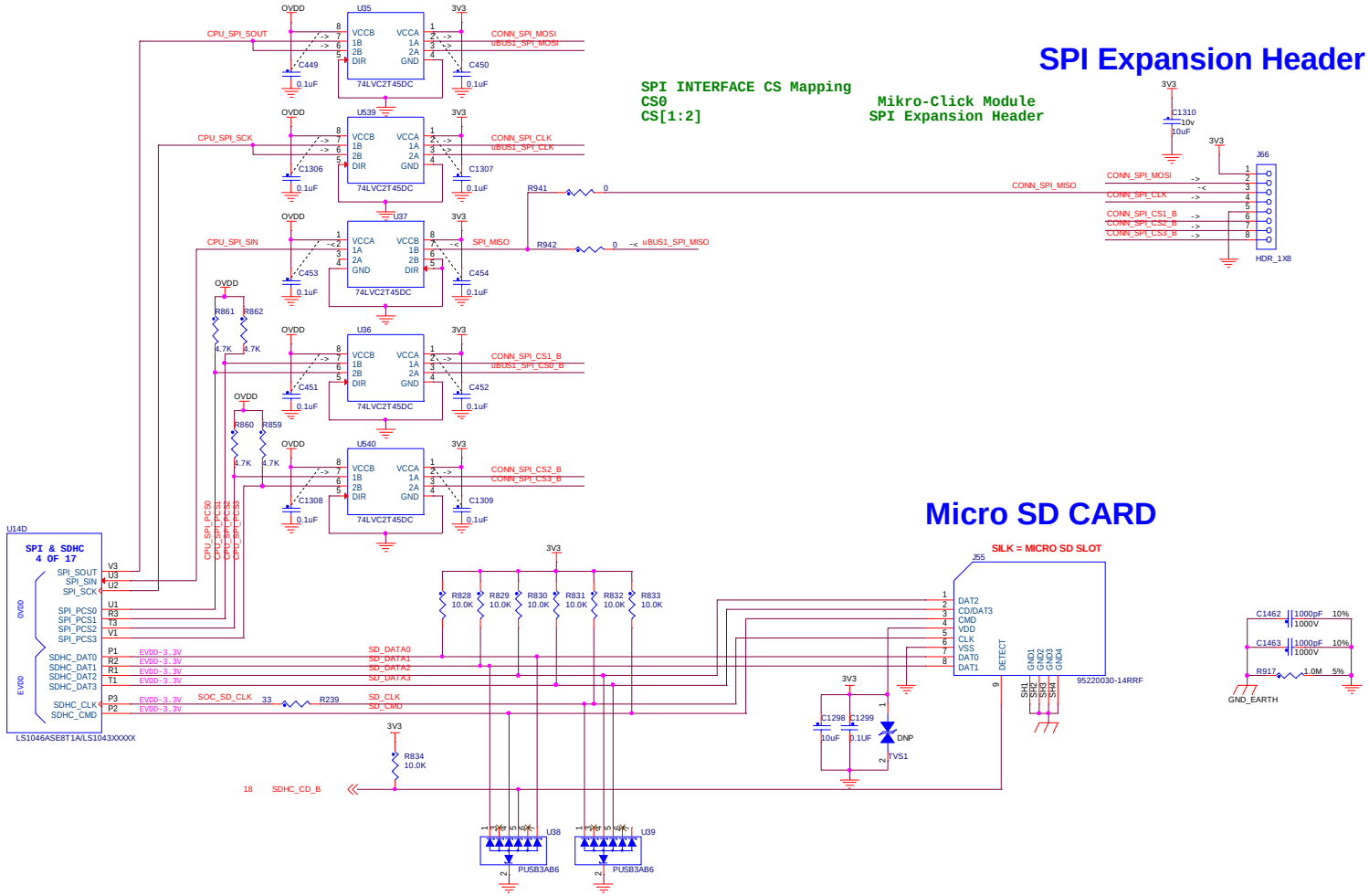
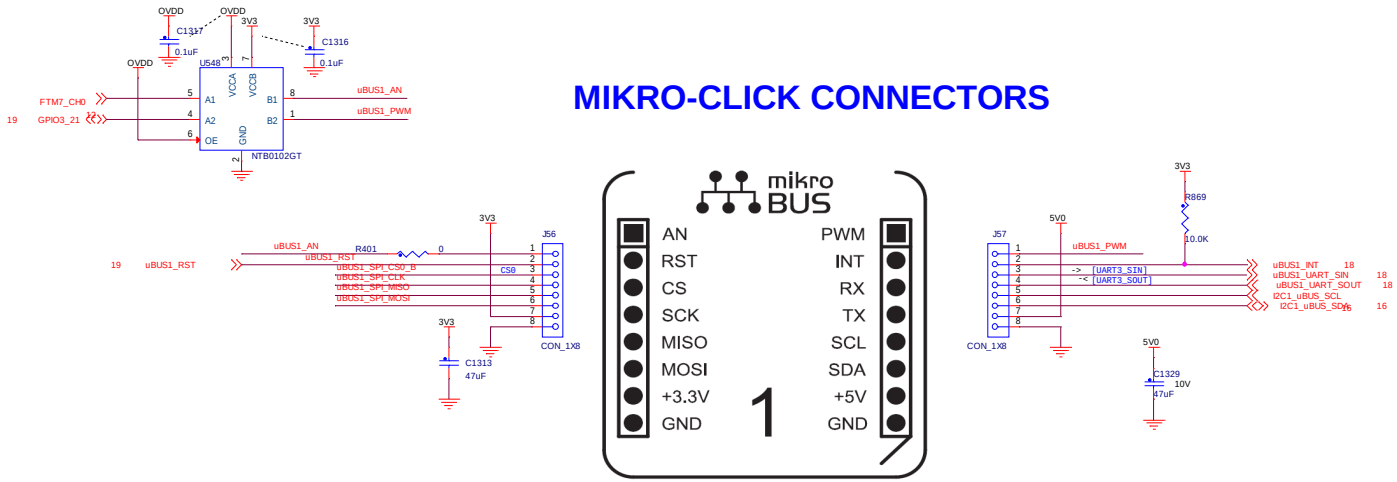
SPI Expansion Header



Micro SD CARD

MIKRO-CLICK CONNECTORS



<Variant Name>

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Drawing Title: **FRWYLS1046A-PA**

Page Title: **SD_SPI_MIKRO_CLICK**

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