Freescale Semiconductor

Rev.1 01/2015

Modify T2080 rev1.1 MEM_PLL_RAT w/ using QCVS4.1.1

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The following table provides a revision history for this document.

Table 1. Document Revision History

Revision	Date	Significant Changes
1	01/2015	• Initial release

1. AN5039

Table 2. DDR Data Rate to DDR CLK ratio

MEM_PLL_RAT				DDR Data Rate to DD REF CLK ratio (both Rev 1 and Rev 1.1)	DDR Data Rate in MT/s at DDR REF CLK frequency in MHz			
Binary value Rev 1	Binary value Rev 1.1	Decimal value Rev 1	Decimal value Rev 1.1		66.67	100	125	133.33
00_1010	00_0101	10	5	10				1333.33
00_1011		11						
00_1100	00_0110	12	6	12		1200		1600
00_1101		13				1300		
00_1110	00_0111	14	7	14				1866
00_1111		15						
00_0000	00_1000	16	8	16	1066.67	1600		
00_0001		17						
01_0010	00_1001	18	9	18	1200	1800		
01_0011		19						
01_0100	00_1010	20	10	20	1333.33			

Notes:

1. On Rev 1.1, the internal clock reference is half of what it used to be on Rev 1. This means that a Rev 1 divider of, for example 10:1, now has to be reconfigured as 5:1 on Rev 1.1. On Rev 1.1, MEM_PLL_RAT = 0.5 x DDR Data Rate/DDRCLK. Due to the change in clock reference, the divider settings for Rev 1.1 must be modified appropriately, or the DDR interface will not function.

2. Rev 1 options 11:1, 13:1, 15:1, 17:1, 19:1 are not supported on Rev 1.1.

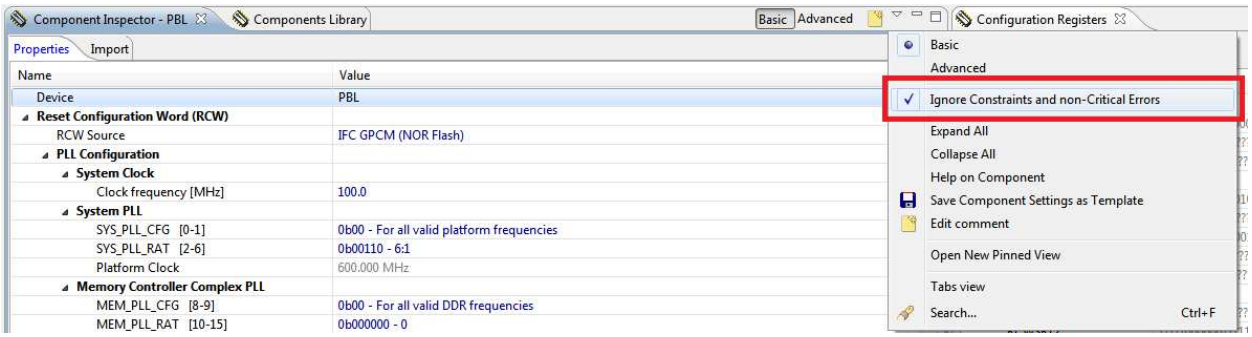
2. Procedure

   The example is according to below environment.

   DDRCLK = 133.3Mhz, DDR data rate = 1600Mbps

1) Run QCSV4.1.1 and Open a T2080 QCS project

2) Click "Ignore Constraints and non-Critical Errors"

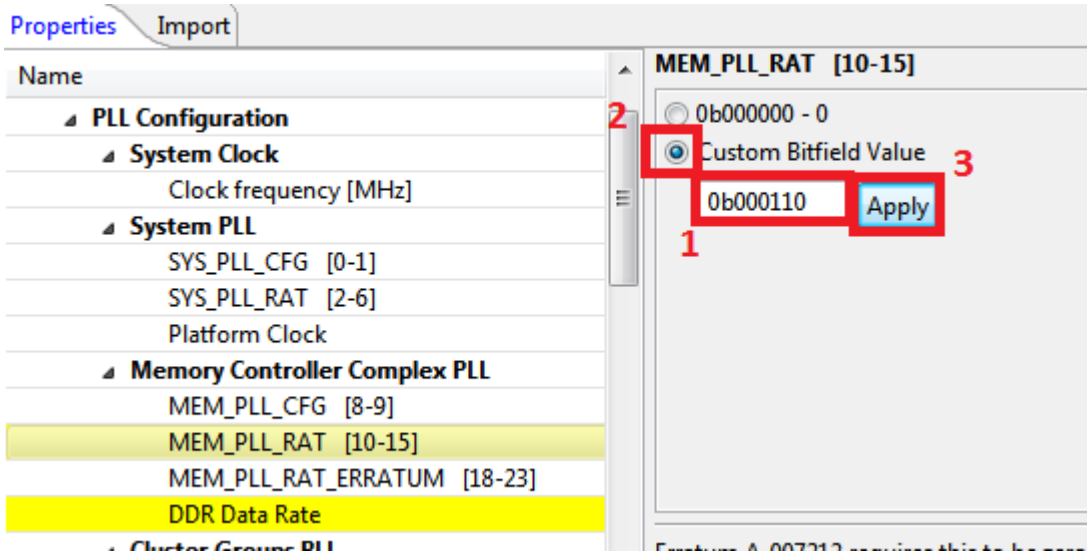


3) **Refer to AN5039, the MEM_PLL_RAT should be set to 00_0110**

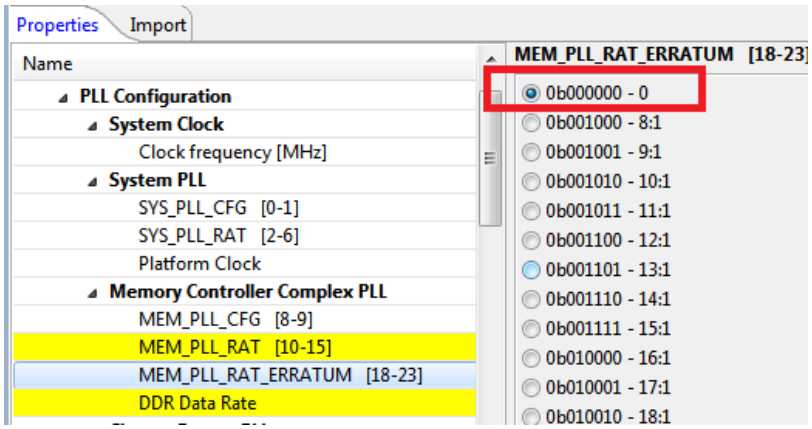
Table 2. DDR Data Rate to DDR CLK ratio

MEM_PLL_RAT				DDR Data Rate to DD REF CLK ratio (both Rev 1 and Rev 1.1)	DDR Data Rate in MT/s at DDR REF CLK frequency in MHz			
Binary value Rev 1	Binary value Rev 1.1	Decimal value Rev 1	Decimal value Rev 1.1		66.67	100	125	133.33
00_1010	00_0101	10	5	10				1333.33
00_1011		11						
00_1100	00_0110	12	6	12		1200		1600
00_1101		13				1300		
00_1110	00_0111	14	7	14				1866
00_1111		15						

4) **Select "MEM_PLL_RAT" and type "0x000110", then click "Custom Bitfield Value and "Apply"**



5) **Set "MEM_PLL_RAT_ERRATUM" to "0"**



6) **Do not care the DDR Date rate value.**