device is in the reset state. When the reset configuration words are latched inside the device, I^2C is reset until $\overline{\text{HRESET}}$ is negated. Then the device is initialized using boot sequencer mode.

Boot sequencer mode is selected at power-on reset by the BOOTSEQ field in the reset configuration word high register (RCWH). If the boot sequencer mode is selected, the I^2C module communicates with one or more EEPROM through the I^2C interface to initialize one or more configuration registers of the PowerQUICC II Pro. For the complete data format for programming the I^2C EEPROM, see *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

The boot sequencer contains a basic level of error detection. If the I^2C boot sequencer fails while loading the reset configuration words are loaded, the RSR[BSF] bit is set. If a preamble or CRC fail is detected in boot sequencer mode, there is no internal or external indication that the boot sequencer operation failed. It is recommended to set aside a GPIO pin for error signaling purpose.

5.5 $\overline{\text{HRESET}}$

The $\overline{\text{HRESET}}$ signal is not a pure input signal. It is an open-drain signal that the MPC8308 processor can drive low. The connection on the left side of this figure causes signal contention and must not be used.

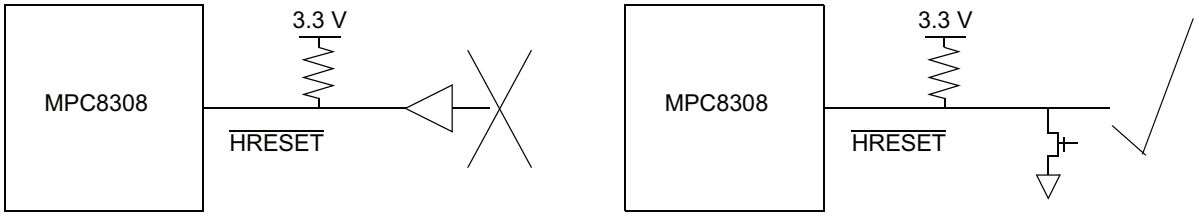

Figure 6. $\overline{\text{HRESET}}$ Connection