**Electrical Characteristics** 

## 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

**Table 3. Output Drive Capability** 

Driver Type	Programmable Output Impedance $(\Omega)$	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV <sub>DD</sub> = 3.3 V BV <sub>DD</sub> = 2.5 V	1
	45 (default) 45 (default) 125	$BV_{DD} = 3.3 \text{ V}$ $BV_{DD} = 2.5 \text{ V}$ $BV_{DD} = 1.8 \text{ V}$	
PCI signals	25	OV <sub>DD</sub> = 3.3 V	2
	42 (default)		
DDR signal	20	GV <sub>DD</sub> = 2.5 V	
DDR2 signal	16 32 (half strength mode)	GV <sub>DD</sub> = 1.8 V	
TSEC signals	42	LV <sub>DD</sub> = 2.5/3.3 V	
DUART, system control, JTAG	42	OV <sub>DD</sub> = 3.3 V	
I <sup>2</sup> C	150	OV <sub>DD</sub> = 3.3 V	
	+	!	

## Notes:

## 2.2 Power Sequencing

The device requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- 1.  $V_{DD}$ ,  $AV_{DD\_}n$ ,  $BV_{DD}$ ,  $LV_{DD}$ ,  $SV_{DD}$ ,  $OV_{DD}$ ,  $TV_{DD}$ ,  $XV_{DD}$
- $2. \text{ GV}_{DD}$

Note that all supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for  $GV_{DD}$  is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, then the sequencing for  $GV_{DD}$  is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the  $V_{DD}$  core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

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<sup>1.</sup> The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

<sup>2.</sup> The drive strength of the PCI interface is determined by the setting of the PCI\_GNT1 signal at reset.