NXP Semiconductors
Application Note

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QorIQ T1024 Family Design Checklist

1 About this document

This document provides recommendations for new designs based on the T1024, which is an advanced, multicore processor that combines two e5500 processor cores built on Power Architecture®, with high-performance datapath acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and mil/aerospace applications.

This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

NOTE

This document is also applicable to the T1023. For a list of functionality differences, see T1023 design recommendations.

Contents

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- *QorIQ T1024, T1014 Data Sheet* (T1024)
- *QorIQ T1023, T1013 Data Sheet* (T1023)

- *QorIQ T1024 Reference Manual* (T1024RM)
- *T1024 Chip Errata* (T1024CE)

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

This figure shows the major functional units within the T1024.

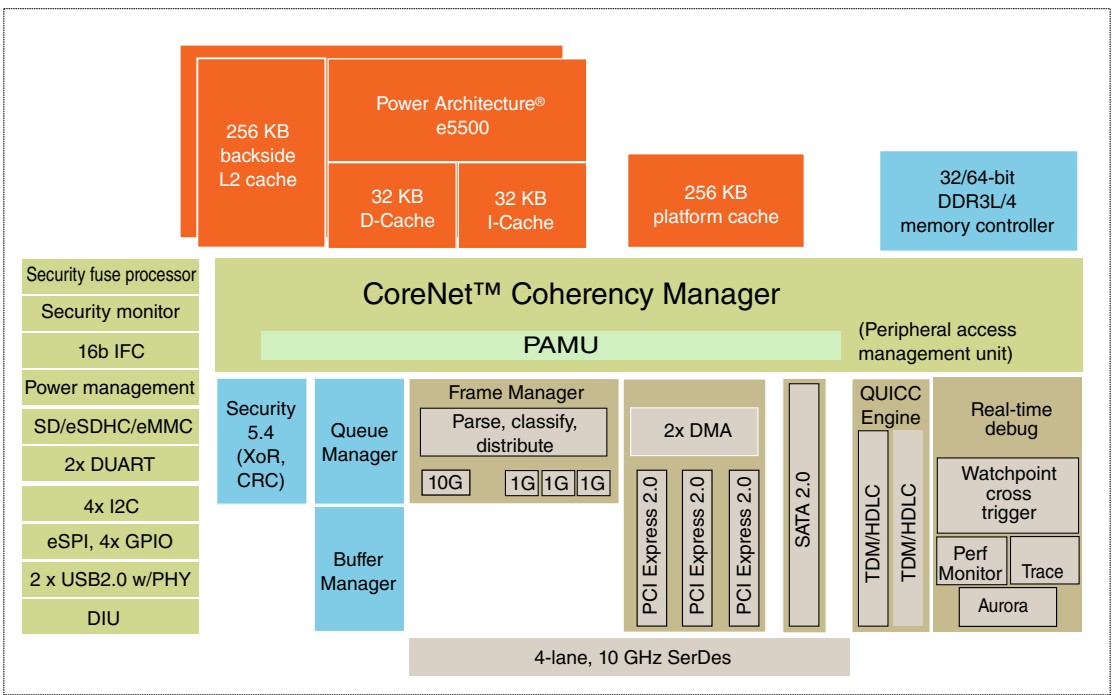

Figure 1. T1024 block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
	Related collateral	
T1024CE	*T1024 Chip Errata* **NOTE:** This document describes the latest fixes and workarounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your NXP representative

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Table 1. Helpful tools and references (continued)

ID	Name	Location
T1024	*QorIQ T1024, T1014 Data Sheet*	Contact your NXP representative
T1023	*QorIQ T1023, T1013 Data Sheet*	Contact your NXP representative
T1FAMILYFS	*T1024 Fact Sheet*	Contact your NXP representative
T1024RM	*QorIQ T1024 Reference Manual*	Contact your NXP representative
QEIWRM	*QUICC Engine Block Reference Manual with Protocol Interworking*	Contact your NXP representative
e5500RM	*e5500 Core Reference Manual*	Contact your NXP representative
AN4039	*PowerQUICC DDR3 SDRAM Controller Register Setting Considerations*	www.nxp.com
AN3939	*DDR Interleaving for PowerQUICC and QorIQ Processors*	www.nxp.com
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	www.nxp.com
AN5097	*Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces*	www.nxp.com
AN2919	*Determining the I2C Frequency Divider Ratio for SCL*	www.nxp.com
AN4311	*SerDes Reference Clock Interfacing and HSSI Measurements Recommendations*	www.nxp.com
AN2747	*Power Supply Design for Power Architecture™ Processors*	www.nxp.com
AN4375	*QorIQ eSPI Controller Register Setting Considerations and Programming Examples*	www.nxp.com
AN4829	*Common Board Design between T1024 and T1022 Processor*	Contact your NXP representative
T1024RDB	Reference design board, including schematics, bill of materials, and board errata list.	Contact your NXP representative
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board level simulations, especially for SerDes and DDR characteristics.	Contact your NXP representative
BSDL	Use the BSDL files in board verification.	Contact your NXP representative
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	Contact your NXP representative
Available training		
—	Our third-party partners are part of an extensive alliance network. More information can be found at www.nxp.com/alliances.	www.nxp.com/alliances
—	Training materials from past Smart Network Developer's Forums and NXP Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	www.nxp.com/alliances

3.2 Product revisions

This table lists the processor version register (PVR) and system version register (SVR) values for the various chip silicon derivatives.

Table 2. Revision Level to Part Marking Cross-Reference

Part	Revision	e5500 Core Revision	Processor Version Register Value	System Version Register Value	Note
T1024E	1.0	2.0	0x8024_1021	0x8548_0010	With Security
T1024	1.0	2.0	0x8024_1021	0x8540_0010	Without Security
T1014E	1.0	2.0	0x8024_1021	0x854C_0010	With Security
T1014	1.0	2.0	0x8024_1021	0x8544_0010	Without Security
T1023E	1.0	2.0	0x8024_1021	0x8549_0010	With Security
T1023	1.0	2.0	0x8024_1021	0x8541_0010	Without Security
T1013E	1.0	2.0	0x8024_1021	0x854D_0010	With Security
T1013	1.0	2.0	0x8024_1021	0x8545_0010	Without Security

4 Power design recommendations

4.1 Power pin recommendations

The T1024 has several power supplies and ground signals. When implementing deep sleep mode, the switchable supplies and the Always ON supplies need to be separated.

Table 3. Power and ground pin connection checklist

Signal name	Power Domain in Deep Sleep	Used	Not used	Completed
AV_{DD}_CGA1	Switchable	Power supply for cluster group A PLL 1 supply (1.8 V through a filter)	Must remain powered	
AV_{DD}_D1	Switchable	Power supply for DDR PLL (1.8 V through a filter)	Must remain powered	
AV_{DD}_PLAT	Always ON	Power supply for Platform PLL (1.8 V through a filter)	Must remain powered	
AV_{DD}_SD1_PLL1	Switchable	Power supply for SerDes1 PLL 1 (SerDes, filtered from $X1V_{DD}$)	Must remain powered (no need to filter from $X1V_{DD}$)	
AV_{DD}_SD1_PLL2	Switchable	Power supply for SerDes1 PLL 2 (SerDes, filtered from $X1V_{DD}$)	Must remain powered (no need to filter from $X1V_{DD}$)	
V_{DD}	Switchable	Core and platform supply voltage		

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Table 3. Power and ground pin connection checklist (continued)

Signal name	Power Domain in Deep Sleep	Used	Not used	Completed
V_{DDC}	Always ON	Core and platform supply voltage		
$S1V_{DD}$	Switchable	Core power supply for the SerDes logic and receivers (1.0 V)	Must remain powered	
DV_{DD}	Switchable	Power supply for the DUART, I^2C, MPIC, QE-TDM, DIU (3.3 V/2.5 V/1.8 V)	Must remain powered	
CV_{DD}	Switchable	Power supply for the eSPI, SDHC_WP, SDHC_CD, SDHC_DAT[4:7] (3.3 V/1.8 V)	Must remain powered	
EV_{DD}	Switchable	Power supply for eSDHC, DMA (3.3 V/1.8 V)	Must remain powered	
$G1V_{DD}$	Switchable	Power supply for the DDR3L/4 (1.35 V/1.2 V)	Must remain powered	
LV_{DD}	Switchable	Power supply for the Ethernet 2 I/O, 1588, GPIO (2.5 V/1.8 V)	Must remain powered	
$L1V_{DD}$	Always ON	Power supply for the Ethernet 1 I/O, Ethernet management interface 1 (EMI1), GPIO (2.5 V/1.8 V)	Must remain powered	
OV_{DD}	Switchable	Power supply for MPIC, GPIO, IFC, Trust, DDRCLK supply, RTC and JTAG I/O voltage (1.8 V)	Must remain powered	
$O1V_{DD}$	Always ON	Power supply for MPIC, GPIO, system control, debug, SYSCLK supply (1.8 V)	Must remain powered	
X1VDD	Switchable	Pad power supply for the SerDes transmitter (1.35 V)	Must remain powered	
PROG_SFP	Always ON	Should only be supplied 1.8 V during secure boot programming. For normal operation, this pin needs to be tied to GND.		
TH_V_{DD}	Switchable	Thermal monitor unit supply (1.8 V)	Must remain powered	
USB_HV_{DD}	Optionally Switchable or Always ON	USB PHY transceiver supply (3.3 V)	Must remain powered	
USB_OV_{DD}	Optionally switchable or Always ON	USB PHY transceiver supply (1.8 V)	Must remain powered	
USB_SV_{DD}	Optionally switchable or Always ON	USB PHY analog supply voltage (1.0 V)	Must remain powered	
SENSEVDD	Switchable	V_{DD} sense pin	No connect	
SENSEVDDC	Always ON	V_{DDC} sense pin	No connect	
SD_GND	—	SerDes core logic GND	Tie to GND	
GND	—	Ground	Tie to GND	
AGND_SD1_PLL1	—	SerDes 1 PLL 1 GND	Tie to GND	
AGND_SD1_PLL2	—	SerDes 1 PLL 2 GND	Tie to GND	
SENSEGND	—	GND sense pin	No connect	
SENSEGNDC	—	GND sense pin	No connect	
USB_AGND	—	USB PHY transceiver GND	Tie to GND	

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Table 3. Power and ground pin connection checklist (continued)

Signal name	Power Domain in Deep Sleep	Used	Not used	Completed
TVDD	Switchable	Power Supply for Ethernet management interface 2 (1.2 V)	Must remain powered to 1.2 V (TV_{DD}) or 1.8 V (OV_{DD})	

NOTE

1. All the power pins need to be tied to their corresponding voltages irrespective of whether the corresponding interfaces are used.
2. $L1V_{DD}$ and LV_{DD} should be configured at same voltage.
3. Power sequencing should be followed as per the chip data sheet.
4. All switchable supplies should be switched OFF in deep sleep mode, else it may cause irreversible damage to the device.

4.2 Power system-level recommendations

Table 4. Power design system-level checklist

Item	Completed
General	
Ensure that the ramp rate for all voltage supplies (including DV_{DD}, CV_{DD}, EV_{DD} OV_{DD}, $O1V_{DD}$, $G1V_{DD}$, LV_{DD}, $L1V_{DD}$, $S1V_{DD}$, and $X1V_{DD}$, all core and platform VDD supplies, D1_MVREF and all AV_{DD} supplies) is less than 25 V/mS. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical, because this range might falsely trigger the ESD circuitry. Required ramp rate for PROG_SFP should be less than 25 V/mS.	
Ensure that all other power supplies have a voltage tolerance no greater than 5% from the nominal value.[1]	
Ensure the power supply is selected based on MAXIMUM power dissipation.[1]	
Ensure the thermal design is based on THERMAL power dissipation.[1]	
Ensure the power-up sequence is within 75 ms.[1]	
Use large power planes to the extent possible.	
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CGA*n*, and AV_{DD}_D1.	
If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SD1_PLL*n* pins. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AV_{DD} pins. However, instead of using a filter, it needs to be connected to the $X1V_{DD}$ rail through a 0 Ω resistor.	
Ensure the PLL filter circuits are placed as close to the respective AVDD_SD1_PLL*n* pins as possible.	
Power supply decoupling	
Provide sufficiently sized power planes for the respective power rail. Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.	
Place at least one decoupling capacitor at each V_{DD}, V_{DDC}, DV_{DD}, CV_{DD}, EV_{DD}, OV_{DD}, $O1V_{DD}$, $G1V_{DD}$, LV_{DD}, $L1V_{DD}$, $S1V_{DD}$, and $X1V_{DD}$ pin of this chip.	

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Table 4. Power design system-level checklist (continued)

Item	Completed
It is recommended that the decoupling capacitors receive their power from separate V_{DD}, V_{DDC}, DV_{DD}, CV_{DD}, EV_{DD}, OV_{DD}, $O1V_{DD}$, $G1V_{DD}$, LV_{DD}, $L1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$, and GND vias in the PCB, utilizing short traces to minimize inductance.	
Capacitors may be placed directly under the chip using a standard escape pattern, and others may surround the part.	
Ensure the board has at least one 0.1 µF surface-mount technology (SMT) ceramic chip capacitor as close as possible to each supply ball of the chip (V_{DD}, V_{DDC}, DV_{DD}, CV_{DD}, EV_{DD} OV_{DD}, $O1V_{DD}$, $G1V_{DD}$, LV_{DD}, $L1V_{DD}$, $S1V_{DD}$, and $X1V_{DD}$).	
Only use ceramic SMT capacitors to minimize lead inductance, preferably 0402 or 0603.	
Distribute several bulk storage capacitors around the PCB, feeding the V_{DD} and other planes (for example, DV_{DD}, OV_{DD}, $G1V_{DD}$, LV_{DD}, SnV_{DD}, and XnV_{DD} planes) to enable quick recharging of the smaller chip capacitors.	
Ensure the bulk capacitors have a low equivalent series-resistance (ESR) rating to ensure the quick response time necessary.	
Ensure the bulk capacitors are connected to the power and ground planes through two vias to minimize inductance.	
Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements. [2] Most regulators perform best with a mix of ceramic and very low ESR tantalum type capacitors.	
As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than 1.0 V + 50 mV (negative transient undershoot should comply with specification of 1.0V - 30mV) for current steps of up to 10 A with a slew rate of 12 A/us.	
SerDes power supply decoupling	
Use only SMT capacitors to minimize inductance.	
Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.	
Ensure the board has at least one 0.1 µF SMT ceramic chip-capacitor as close as possible to each supply ball of the chip ($S1V_{DD}$ and $X1V_{DD}$).	
Where the board has blind vias, ensure these capacitors are placed directly below the chip supply and ground connections.	
Where the board does not have blind vias, ensure these capacitors are placed in a ring around the chip as close to the supply and ground connections as possible.	
For all SerDes supplies: Ensure there is a 1 µF ceramic chip capacitor on each side of the chip.	
For all SerDes supplies: Ensure there is a 10 µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100 µF, low ESR SMT tantalum chip capacitor between the device and any SerDes voltage regulator.	
PLL power supply filtering[3]	
Provide independent filter circuits per PLL power supply, as illustrated in the following figure. Where: • R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH • Low-ESL surface-mount capacitors	

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Table 4. Power design system-level checklist (continued)

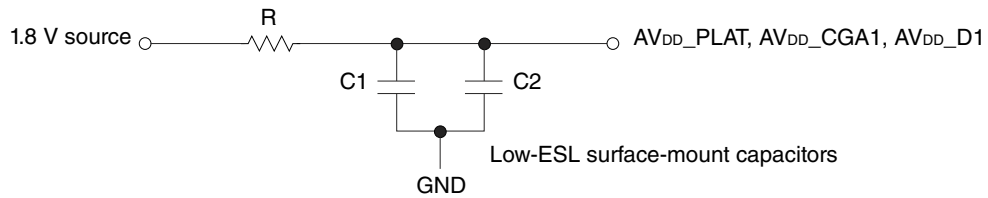
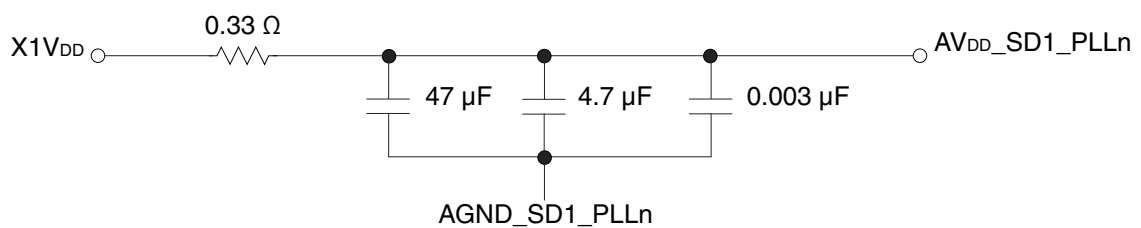
Item	Completed
NOTE: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH). **NOTE:** Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}. 	
Ensure filter circuits use surface mount capacitors with minimum effective series inductance (ESL).	
Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. **NOTE:** If done properly, it is possible to route directly from the capacitors to the AV_{DD} pins, without the added inductance of vias. **NOTE:** It is recommended that an area fill or power plane split be provided to provide a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise.	
Ensure each of the PLLs is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA*n*, AV_{DD}_D1, and AV_{DD}_SD1_PLL*n*, respectively).	
For maximum effectiveness, ensure the filter circuit is placed as close as possible to the AV_{DD}_SD1_PLL*n* ball to ensure it filters out as much noise as possible.	
Ensure the ground connection is near the AV_{DD}_SD1_PLL*n* ball. The 0.003 µF capacitor is closest to the ball, followed by a 4.7 µF capacitor and 47 µf capacitors, and finally the 0.33 Ω resistor to the board supply plane.	
To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in this figure. Note the following: • AV_{DD}_SD1_PLL*n* should be a filtered version of $X1V_{DD}$. • Signals on the SerDes interface are fed from the $X1V_{DD}$ power plane. • It is recommended that an area fill or power plane split be provided for both AV_{DD} and AGND to provide a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Voltage for AV_{DD}_SD1_PLL*n* is defined at the PLL supply filter and not the pin of AV_{DD}_SD1_PLL*n*. • A 47 µF 0805 XR5 or XR7, 4.7 µF 0603, and 0.003 µF 0402 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk. 	
Ensure the capacitors are connected from AV_{DD}_SD1_PLL*n* to the ground plane.	
Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.	

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Table 4. Power design system-level checklist (continued)

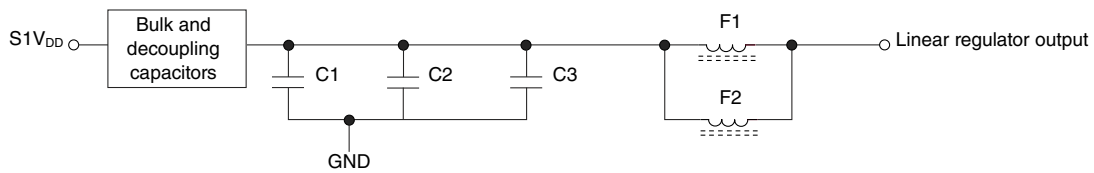
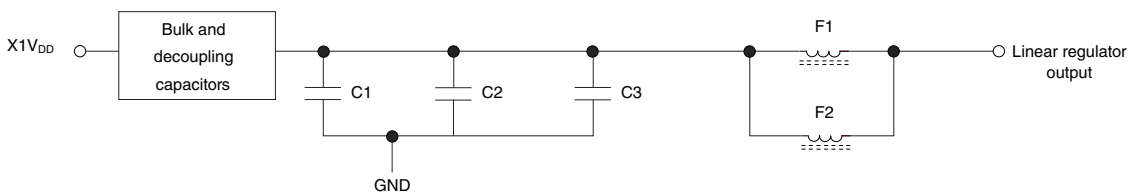
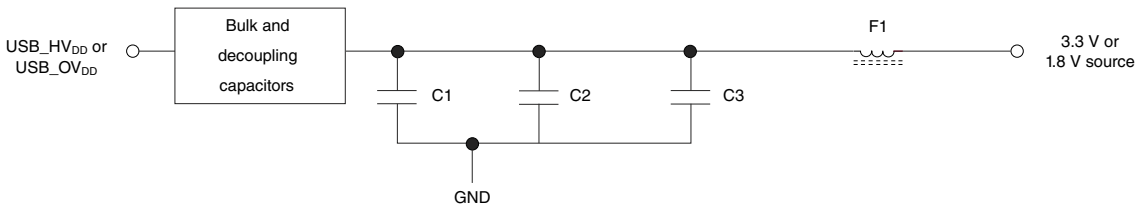
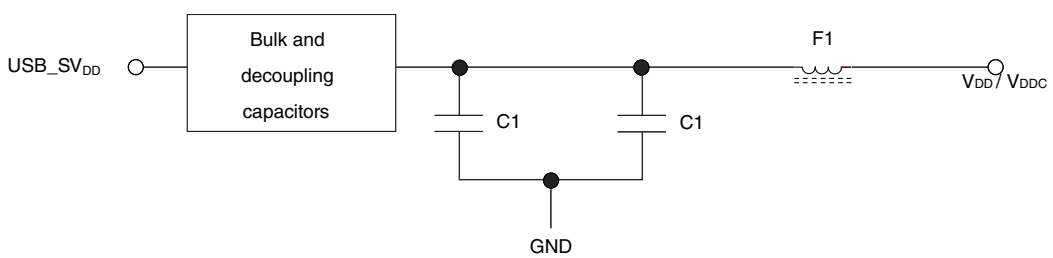
Item	Completed
Ensure AV_{DD}_SD1_PLL*n* is a filtered version of $X1V_{DD}$.	
There must be dedicated analog ground AGND_SD1_PLL*n* for each AV_{DD}_SD*n*_PLL*n* pin up to the physical locale of the filters themselves.	
$S1V_{DD}$ should be supplied by a linear regulator and needs a nominal voltage of 1.0 V. An example solution for $S1V_{DD}$ filtering, where $S1V_{DD}$ is sourced from a linear regulator, is shown in the following figure. The component values in this example filter are system dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1) • Bulk and decoupling capacitors are added, as needed, per power supply design.  **NOTE:** See section "Power-on ramp rate" in the applicable chip data sheet for maximum $S1V_{DD}$ power-up ramp rate. **NOTE:** There must be enough output capacitance or a soft-start feature to assure the ramp-rate requirement is met. **NOTE:** Besides a linear regulator, a low-noise-dedicated switching regulator can be used. 10 mVp-p, 50 kHz to 500 MHz is the noise goal.	
$X1V_{DD}$ may be supplied by a linear regulator or sourced by a filtered $G1V_{DD}$. Systems may design-in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended. An example solution for $X1V_{DD}$ filtering, where $X1V_{DD}$ is sourced from a linear regulator, is shown in the following figure. The component values in this example filter are system dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1) • Bulk and decoupling capacitors are added, as needed, per power supply design.  **NOTE:** See section "Power-on ramp rate" in the applicable chip data sheet for maximum XnV_{DD} power-up ramp rate. **NOTE:** There must be enough output capacitance or a soft-start feature to assure the ramp-rate requirement is met. **NOTE:** The ferrite beads should be placed in parallel to reduce voltage droop. **NOTE:** Besides a linear regulator, a low-noise-dedicated switching regulator can be used. 10 mVp-p, 50 kHz to 500 MHz is the noise goal.	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

Item	Completed
USB_HV_{DD} and USB_OV_{DD} must be sourced by a filtered 3.3 V and 1.8 V voltage source using a star connection. An example solution for USB_HV_{DD} and USB_OV_{DD} filtering, where USB_HV_{DD} and USB_OV_{DD} are sourced from a 3.3 V and 1.8 V voltage source, is illustrated in the following figure. The component values in this example filter are system dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1) • Bulk and decoupling capacitors are added, as needed, per power supply design. 	
USB_SV_{DD} must be sourced by a filtered V_{DD} using a star connection. An example solution for USB_SV_{DD} filtering, where USB_SV_{DD} is sourced from V_{DD}, is illustrated in the following figure. The component values in this example filter are system dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 2.2 µF ± 20%, X5R, with low ESL (for example, Panasonic ECJ0EB0J225M) • F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1) • Bulk and decoupling capacitors are added, as needed, per power supply design 	
Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.	

1. See the applicable chip data sheet for more details.
2. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).
3. The PLL power supply filter circuit filters noise in the PLLs' resonant frequency range from 500 kHz to 10 MHz.

4.3 Power-on reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted. When PORESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 5. Power-on reset system-level checklist

Item	Completed
Ensure PORESET_B is asserted for a minimum of 1 ms.	
Ensure HRESET_B is asserted for a minimum of 32 SYSCLK cycles.	
In cases where a configuration pin has no default, use a 4.7 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when HRESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of PORESET_B (PLL configuration inputs must meet a 100 µs set-up time to HRESET_B), hold their values for at least two SYSCLK cycles after the de-assertion of PORESET_B, and then release the pins to high impedance afterward for normal device operation **NOTE:** See the applicable chip data sheet for details about reset initialization timing specifications.	
Configuration settings	
Ensure the settings in Configuration signals sampled at reset are selected properly. **NOTE:** See the applicable chip reference manual for a more detailed description of each configuration option.	
Power sequencing	
The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. Power up sequence when DDR3L is used: 1. $O1V_{DD}$, OV_{DD}, DV_{DD}, CV_{DD}, EV_{DD}, $L1V_{DD}$, LV_{DD}, TH_V_{DD}, USB_HV_{DD}, USB_OV_{DD}, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1, TV_{DD}. Drive PROG_SFP = GND a. PORESET_B should be driven asserted and held during this step. 2. V_{DDC}, V_{DD}, USB_SV_{DD}, $S1V_{DD}$ a. When deep sleep is not used, it is recommended to source V_{DD} and V_{DDC} from same power supply. b. When deep sleep is used, V_{DDC} should ramp up before V_{DD}. Alternatively, V_{DD} may ramp up together with V_{DDC} provided that the relative timing between V_{DDC} and V_{DD} ramp up conforms to Figure 2. 3. $G1V_{DD}$, $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2 a. All supplies in this step may be sourced from the same supply. Power up sequence when DDR4 is used: 1. $O1V_{DD}$, OV_{DD}, DV_{DD}, CV_{DD}, EV_{DD}, $L1V_{DD}$, LV_{DD}, TH_V_{DD}, USB_HV_{DD}, USB_OV_{DD}, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1, $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2, TV_{DD}. Drive PROG_SFP = GND a. PORESET_B should be driven asserted and held during this step. 2. V_{DDC}, V_{DD}, USB_SV_{DD}, $S1V_{DD}$ a. When deep sleep is not used, it is recommended to source V_{DD} and V_{DDC} from the same power supply. b. When deep sleep is used, V_{DDC} should ramp up before V_{DD}. Alternatively, V_{DD} may ramp up together with V_{DDC} provided that the relative timing between V_{DDC} and V_{DD} ramp up conforms to Figure 2. 3. $G1V_{DD}$ Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs. All supplies must be at their stable values within 75 ms. This figure provides the V_{DDC} and V_{DD} ramp up diagram.	

Table 5. Power-on reset system-level checklist

Item	Completed

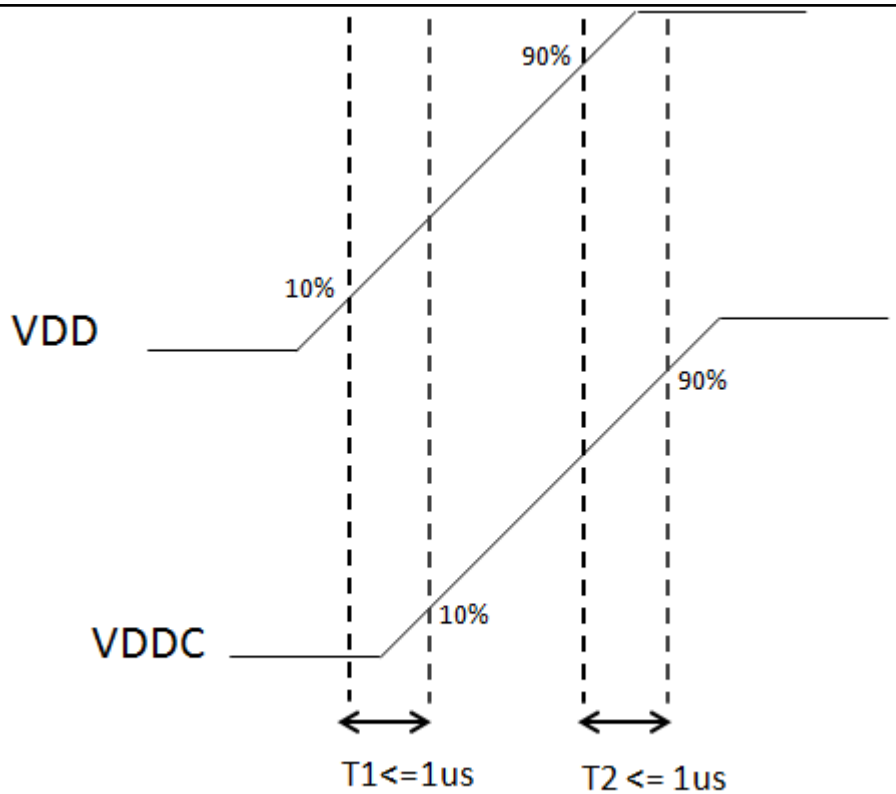


Figure 2. V_{DDC} and V_{DD} ramp up diagram

Elaborating "V_{DDC} should ramp up along with or before V_{DD} power supply":

1. Use Case 1: V_{DDC} and V_{DD} are generated using single power regulator with FET control.

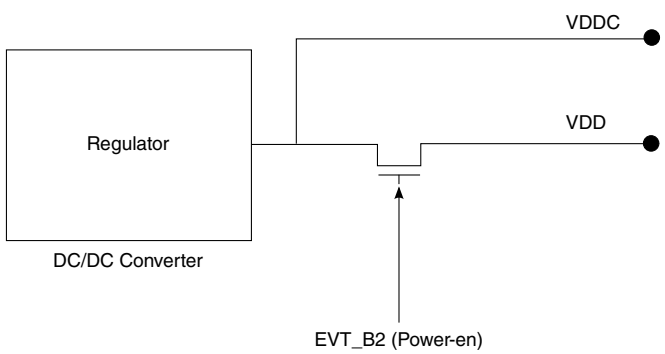
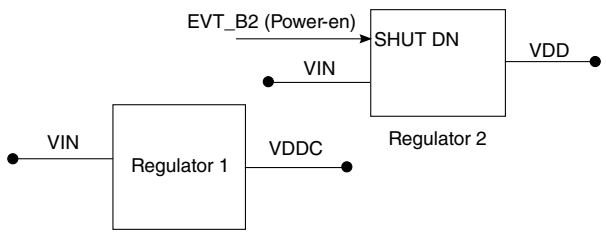


Figure 3. Single Power regulator with FET control

FET is controlled by EVT_B2 aka POWER_EN.

Due to different impedances of the two power distribution networks, it is possible that V_{DD} ramps up before V_{DDC}.

Table 5. Power-on reset system-level checklist

Item	Completed
Care should be taken to ensure that relative timing between V_{DDC} and V_{DD} conforms as per the "V_{DDC} and V_{DD} ramp up diagram" in the chip data sheet. This can be achieved using additional delay elements in the V_{DD} PDN. 2. Use Case 2: V_{DDC} and V_{DD} are generated using separate power regulators.  **Figure 4. Dual Regulator** V_{DDC} should ramp before V_{DD}. One way to achieve is to tie PGOOD of regultaor 1 to regulator 2. **NOTE:** See the chip data sheet for details of power sequencing requirments.	

4.3.1 Configuration signals sampled at reset

The signals that serve alternate functions as configuration input signals during system reset are summarized in the following table.

Reset configuration signals are sampled at the negation of PORESET_B. However, there is a setup and hold time for these signals relative to the rising edge of PORESET_B, as described in the chip data sheet.

The reset configuration signals are multiplexed with other functional signals. The values on these signals during reset are interpreted to be logic one or zero, regardless of whether the functional signal name is defined as active-low. The reset configuration signals have internal pull-up resistors so that if the signals are not driven, the default value is high (a one), as shown in the table. Some signals must be driven high or low during the reset period. For details about all the signals that require external pull-up resistors, see the chip data sheet.

Table 6. T1024 reset configuration signals

Configuration Type	Functional Pins	Comments
Reset configuration word (RCW) source inputs cfg_rcw_src[0:8]	IFC_AD[8:15] IFC_CLE	They must be set to one of the valid options. The 512 bit RCW word has all the necessary configuration information for the chip. If there is no valid RCW in the external memory, it can be programmed using CodeWarrior or other programmer. JTAG configuration files available with CodeWarrior Installation (CWInstallDir\PA\PA_Support\Initialization_Files\jtag_chains) can be used to override Reset Configuration Word (RCW) for T1024. The JTAG configuration files can be used in the following situations:

Table continues on the next page...

Table 6. T1024 reset configuration signals (continued)

Configuration Type	Functional Pins	Comments
		• Target boards that do not have RCW already programmed • New board bring-up • Recovering boards with blank or damaged flash
IFC external transceiver enable polarity select (cfg_ifc_te)	IFC_TE	Default is "1"
DRAM type select (cfg_dram_type)	IFC_A[21]	Default is "1" (DDR3L)
General-purpose input (cfg_gpinput[0:7])	IFC_AD[0:7]	Default "1111 1111", values can be application defined
"Single Oscillator Source" clock select (cfg_eng_use0)	IFC_WE0_B	Default selection is single ended SYSCLK
"Single Oscillator Source" clock configuration (cfg_eng_use1)	IFC_OE_B	Default is "1"
"Single Oscillator Source" clock configuration(cfg_eng_use2)	IFC_WP0_B	Default is "1"

NOTE

If a new board is using a blank flash and flash is the source of RCW, then all the 0xff values from flash for RCW will put the device in an unknown state. The two workarounds for this problem are:

- Put switches on cfg_rcw_src signals to choose hardcoded RCW(0x9A, 0x9E).
- Use CodeWarrior tool from NXP to override RCW.

4.4 Power Management Recommendations

The T1024 processor implements sophisticated power-saving modes for managing energy consumption in both dynamic and static power modes. These include the traditional nap, doze, sleep and packet lossless deep-sleep modes. Designers may leverage these modes to efficiently match work accomplished with the correct level of energy consumed. Refer to the QorIQ T1024 Reference Manual for details.

4.4.1 Power Management pin termination recommendations

Table 7. Power Management Control pins termination checklist

Signal Name	I/O type	Used	Not used	Completed
EVT_B[2]	I/O	EVT_B[2] serves the alternate function of POWER_EN pin (output) for deep sleep. POWER_EN is connected to external power switch device or regulator and indicates to the external power regulator to toggle the power switch to off mode during deep sleep entry.	EVT_B[2] is an output and can be left floating.	

Table continues on the next page...

Table 7. Power Management Control pins termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
		During PORESET_B assertion, EVT_B[2] is a high impedance input so there must be an external pull up on board on EVT_B[2] to ensure POWER_EN is asserted at power up. Until PORESET_B gets deasserted, EVT_B[2] (POWER_EN) should not be sampled.		
EVT_B[3]	I/O	EVT_B[3] serves the alternate function of POWER_OK pin (input) for deep sleep. Connect POWER_EN directly to external power switch device. • 0 - POWER from Regulator is not stable. • 1 - POWER from Regulator is stable. If there is no external source of POWER_OK, then the POWER_OK has to be tied to logic 1 on the board.	This pin should be pulled high through 2-10 kΩ resistors to $O1V_{DD}$ or else programmed as O/P and left floating.	
EVT_B[9]	I/O	EVT_B[9] serves the alternate function of board isolation control (output) for deep sleep mode. The functionality of this signal is determined by the IRQ_OUT field in the reset configuration word (RCW[IRQ_OUT]). • 0 - Enable board isolations • 1 - Disable board isolations During PORESET_B assertion, EVT_B[9] is a high impedance input. There must be an external pull up on board on EVT_B[9] to ensure board isolations are disabled at power up.	EVT_B[9] is an output and can be left floating.	
GPIO1[23:25]/ IRQ[3:5]	I/O	When several board isolation control signals are required, GPIO1[23:25] can be used. The functionality of these signals is determined by the RCW[373:375] field in the reset configuration word (RCW[IRQ_BASE]).	IRQ3 should be pulled high through 2-10 kΩ resistors to $L1V_{DD}$, IRQ4 should be pulled high through 2-10 kΩ resistors to CV_{DD}, IRQ5 should be pulled high through 2-10 kΩ resistors to DV_{DD}, or IRQ[3:5] pins can be programmed as output and left floating.	

4.4.2 Deep-sleep system level recommendations

In deep sleep mode, power to a large portion of the chip is turned off to save power. Dynamically turning portions of the die on or off must be coordinated between the SoC and the system. Both should know when it is safe to apply or remove power and indicate when the process is completed.

The wake up sources of the SoC are ethernet, IRQ[0:5], general purpose timer, and GPIOs. All signals of these interfaces should remain powered up during deep sleep mode. The other signals that should remain powered during deep sleep are: PORESET_B, HRESET_B, RESET_REQ_B, SYSCLK, DIFF_SYSCLK/DIFF_SYSCLK_B, ASLEEP, EVT_B[0:4], CLK_OUT, IRQ_OUT, and some test signals.

The T1024 RDB can be used as a reference design while designing a system with deep sleep mode.

Table 8. Deep-sleep system level checklist

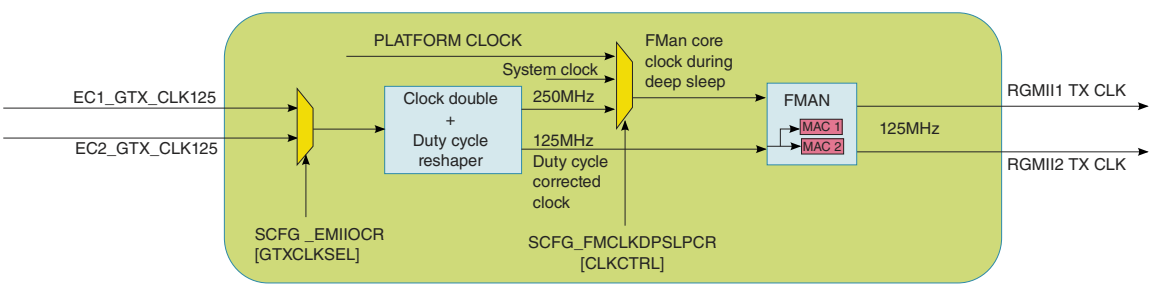
Item	Completed
For requirements of external power supply, see the QorIQ T1024 Data Sheet.	
For power sequencing in deep sleep mode, see the QorIQ T1024 Data Sheet.	
For the deep sleep entry indicative sequence and deep sleep exit indicative sequence, see the chip reference manual.	
When the I/O supplies are switched off, the corresponding I/Os should not be driven by any peripheral. It is recommended to switch off the peripheral devices connected to switched-off interfaces to avoid any damage to the device. If the peripheral device is not switched off, please ensure that the output pins of the peripheral device are driven into high impedance state or are appropriately isolated.	
All the pull up resistors should be connected to respective power supplies. See the chip data sheet for details.	
When V_{DDC} and V_{DD} are supplied by the same power source, ensure switching events do not trigger transient voltages, nor trip voltage monitors.	
Frame manager clocking in deep sleep • Frame manager is clocked with 2* 125 MHz GTX_CLK125 from PHY in RGMII mode.  	
DDR controller in deep sleep: • $G1V_{DD}$ to DDR controller is switched OFF. • GV_{DD} to SDRAM memory remains ON. • Separate power plane are required for DDR controller and SDRAM memory. • SDRAM is powered ON and in self-refresh. • MCKE should be driven low by a board level pull-down (controller cannot guarantee a low output with $G1V_{DD}$ powered down). • Deep sleep wake up requires RESET to the DDR memory to be masked.	

Figure 5. Clocking in Deep sleep mode

NOTE

1. RGMII is supported at 1.8 V to help lower the deep sleep power consumption.
2. DDR3L RDIMM are not supported in deep sleep mode.

5 Interface recommendations

5.1 DDR controller recommendations

The T1024 supports DDR3L (1.35 V) and DDR4 (1.2 V) SDRAM.

The memory interface controls main memory accesses and together supports a maximum of 32 GB of main memory.

cfg_dram_type reset configuration signal selects between GV_{DD} to be used for DDR3L and DDR4 memory controllers.

NOTE

Incorrect setting of cfg_dram_type can lead to damage of I/Os.

5.1.1 DDR controller pin termination recommendations

Table 9. DDR controller pin termination checklist

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	DDR4 Signal				
D1_MA[13:00] D1_MA[14] D1_MA[15]	D1_MA[13:00] BG1 ACT_B	O	Must be properly terminated to VTT.	These pins can be left unconnected.	
D1_MBA[0:1] D1_MBA[2]	D1_MBA[0:1] BG[0]	O	Must be properly terminated to VTT.	These pins can be left unconnected.	
D1_MCK[0:1]/D1_MCK[0:1]_B		O	These pins must be properly terminated.	These pins may be left unconnected. All unused MCK pins should be disabled via the DCFG_CCSR_DDRCLKDR register.	
D1_MCKE[0:1]		O	Must be properly terminated to VTT. These pins are actively driven during reset instead of being released to high impedance.	These pins can be left unconnected.	
D1_MCS[0:3]_B		O	Must be properly terminated to VTT.	These pins can be left unconnected.	
D1_MDIC[0:1]		I/O	• These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors. • MDIC[0] is grounded through a 162 Ω precision 1% resistor, and MDIC[1] is	These pins can be left unconnected.	

Table continues on the next page...

Table 9. DDR controller pin termination checklist (continued)

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	DDR4 Signal				
			connected to GV_{DD} through a 162 Ω precision 1% resistor. • For either full- or half-driver strength calibration of DDR I/Os, use the same MDIC resistor value of 162 Ω. • The memory controller register setting can be used to determine if automatic calibration is done to full- or half-drive strength.		
D1_MDM[0:8]	DBI_B[0:8]	O	—	These pins can be left unconnected.	
D1_MDQ[0:63]		I/O	—	These pins can be left unconnected.	
D1_MDQS[0:8]/D1_MDQS[0:8]_B		I/O	—	These pins can be left unconnected.	
D1_MECC[0:7]		I/O	—	These pins can be left unconnected.	
D1_MAPAR_ERR_B	ALERT_B	I	This pin is an open drain output from registered DIMMs. Ensure that a 2-10 kΩ pull-up to $G1V_{DD}$ is present on this pin.	This pin should be pulled up.	
D1_MAPAR_OUT	PAR	O	If the controller supports the optional MAPAR_OUT and MAPAR_ERR signals, ensure that they are hooked up as follows: • MAPAR_OUT (from the controller) => PAR_IN (at the RDIMM) • ERR_OUT (from the RDIMM) => MAPAR_ERR (at the controller)	This pin can be left unconnected.	
D1_MODT[0:1]		O	Ensure the MODT signals are connected correctly. Two dual-ranked DIMMs topology is not supported on the T1024. For a single, dual-ranked DIMM, consider the following connections: • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1)	These pins can be left unconnected.	

Table continues on the next page...

Table 9. DDR controller pin termination checklist (continued)

Signal Name[1]		I/O type	Used	Not used	Completed
DDR3L Signal	DDR4 Signal				
			For quad-ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one quad-ranked DIMM. These pins are actively driven during reset instead of being released to high impedance.		
D1_MRAS_B	A16/RAS_B	O	Must be properly terminated to VTT.	This pin can be left unconnected.	
D1_MCAS_B	A15/CAS_B	O	Must be properly terminated to VTT.	This pin can be left unconnected.	
D1_MWE_B	A14/WE_B	O	Must be properly terminated to VTT.	This pin can be left unconnected.	
D1_MVREF	DDR4 VREF is provided internally. The external VREF signal needs to be grounded when using DDR4 SDRAM.	I	DDR reference voltage: 0.49 x GV_{DD} to 0.51 x $G1V_{DD}$. D1_MVREF can be generated using a divider from $G1V_{DD}$ as MVREF. Another option is to use supplies that generate $G1V_{DD}$, VTT, and D1_MVREF voltage. These methods help reduce differences between $G1V_{DD}$ and MVREF. D1_MVREF generated from a separate regulator is not recommended, because D1_MVREF does not track $G1V_{DD}$ as closely.	This pin must be connected to GND.	

1. DDR3L signals are muxed with DDR4 signals and shown in this table

5.1.2 DDR system-level recommendations

Table 10. DDR system-level checklist

Item	Completed
General	
DDR3L /DDR4 mode selection is through por-config signal cfg_dram_type. Ensure that the pin is configured correctly as per the DDR mode. Setting DDR4 mode while applying GV_{DD} = 1.35 V can lead to damage of I/Os.	
Data Bus inversion (DBI) signals are muxed on Data Mask (D1_MDM) signals and are optional function for DDR4. Only one function can be used at a time.	
PORESET_B assertion should also reset SDRAM Memory.	
For deep sleep related recommendations, see Deep-sleep system level recommendations.	

NOTE

- Stacked memory for DDR4 are not supported.
- DDR4 RDIMM are not supported.
- For devices with 4 ECC pins, ensure to connect one of the ECC pins to the Prime DQ of ECC DRAM.

5.2 High-speed serial interfaces (HSSI) recommendations

The T1024 SerDes block provides four high-speed serial communication lanes supporting a variety of protocols, including:

- SGMII 1.25 Gbps
- SGMII 3.125 Gbps
- QSGMII 5 Gbps
- PCI Express (PEX) Gen 1 1x / 2x / 4x 2.5 Gbps
- PCI Express (PEX) Gen 2 1x / 2x 5 Gbps
- SATA 1.5 / 3 Gbps
- Aurora 2.5 / 5 Gbps
- XFI (10GbE)

5.2.1 SerDes pin termination recommendations

Table 11. SerDes pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SD1_IMP_CAL_TX	I	Tie to $X1V_{DD}$ through a 698 Ω 1% resistor.	If the SerDes interface is entirely unused, the unused pin must be left unconnected	
SD1_IMP_CAL_RX	I	Tie to $S1V_{DD}$ through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, the unused pin must be left unconnected	
SD1_PLLn_TPA	O	Provide a test point if possible. These pins can be left floating.		
SD1_PLLn_TPD	O	Provide a test point if possible. These pins can be left floating.		
SD1_TX[3:0]_P	O	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD1_TX[3:0]_N	O			
SD1_RX[3:0]_P	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to SD_GND.	
SD1_RX[3:0]_N	I	Ensure pins are correctly terminated for the interface type used.		
SD1_REF_CLK1_P/ SD1_REF_CLK1_N	I	Ensure clocks are driven from an appropriate clock source. See the chip reference manual for RCW and PLL configuration settings.	If the clock is not used in the system, these pin must be connected to SD_GND.	
SD1_REF_CLK2_P/ SD1_REF_CLK2_N	I	Ensure clocks are driven from an appropriate clock source. See the chip reference manual for RCW and PLL configuration settings.	If the clock is not used in the system, these pin must be connected to SD_GND.	

NOTE

1. In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. The SerDes module is disabled when both its PLLs are turned off.
2. After POR, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDS*x*PLL*l*RSTCTL).
3. Unused lanes must be powered down by clearing the RRST and TRST fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDS*x*LN*m*G0).
4. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed protocol, such as SATA, SGMII, SGMII 2.5G, QSGMII, 1000Base-KX, is used concurrently on the same SerDes PLL, spread-spectrum clocking is not permitted.
5. RCW[SRDS_PRTCL_S1] selection should be strictly according to product personality.

5.2.2 SerDes system-level recommendations

For the high-speed protocols below, test both receive equalization boost settings of 1b (enabled - default) or 0b (disabled) to determine which setting yields better signal integrity for the customer's system, in which signal integrity can vary due to board design, layout, and fabrication.

To disable the receive equalization boost setting:

- For 10GBase-KR, perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit LNaRECR0[RXEQ_BST] to 0b.
- For XFI 10.3125 Gbaud, perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit LNaRECR0[RXEQ_BST] to 0b.

5.3 Integrated flash controller (IFC)

The integrated flash controller (IFC) shares signals with GPIO1 and GPIO2. The functionality of these signals is determined by the IFC_GRP_[a]_BASE fields in the reset configuration word.

The T1024 IFC supports 32-bit addressing and 8- or 16-bit data widths for a variety of devices.

5.3.1 IFC pin termination recommendations

Table 12. IFC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
IFC_A[16:20]	O	These pins must not be pulled down during power-on reset. They may be pulled up, driven high, or, if there are no externally connected devices, left in tristate. If these pins are connected to a device that pulls down during reset, an external pull-up is required to drive these pins to a safe state during reset.		
IFC_A[21]	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor.		

Table continues on the next page...

Table 12. IFC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
		However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_A[22:31]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_AD[0:15]	I/O	These pins are a reset configuration pins. They have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The pull-ups are designed such that they can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_PAR[0:1]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_CS[0:7]_B	O	Recommend weak pull-up resistors (2–10 kΩ) be placed on these pins to OV_{DD}.	These pins can be left unconnected.	
IFC_WE[0]_B	O	These pins are reset configuration pins. They have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The internal pull-ups are designed such that they can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_OE_B	O			
IFC_WP[0]_B	O			
IFC_WP[1:3]_B	O	Connect as needed.	This pin can be left unconnected.	
IFC_BCTL	O	Connect as needed.	This pin can be left unconnected.	
IFC_TE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_NDDQS	I/O	Connect as needed.	This pin can be left unconnected.	
IFC_AVD	O	This pin must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_CLE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_RB[0:1]_B	I	These pins should be pulled high through a 1 kΩ resistor to OV_{DD}.	These pins should be pulled high through a 1 kΩ resistor.	
IFC_RB[2:4]_B	I	These pins should be pulled high through a 1 kΩ resistor to OV_{DD}.	These pins can be left floating if left as default function of IFC_AD[29:31] or if configured as outputs via the GPIO_GPDIR register.	
IFC_PERR_B	I	These pins should be pulled high through a 2-10 kΩ resistor to OV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.		

Table continues on the next page...

Table 12. IFC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
IFC_CLK[0:1]	O	Connect as needed.	All unused IFC_CLK pins should be disabled via the DCFG_CCSR_IFCCLKDR register.	
IFC_NDDDR_CLK	O	Connect as needed	This pin can be left unconnected.	

NOTE

IFC interface is on OV_{DD} power domain, which is 1.8 V only.

For functional connection diagram, see the chip reference manual.

5.4 QUICC Engine recommendations

The QUICC Engine block on the T1024 supports two TDM/UART interfaces.

The QUICC Engine shares signals with GPIO4 and DIU. The functionality of these signals is determined by the QE-TDMA and QE-TDMB fields in the reset configuration word, and the functionality of the clock signals is determined by the SCFG[QEIOCLKCR] register.

QUICC Engine supports 3.3 V and 2.5 V operation only.

5.4.1 QUICC Engine pin termination recommendations

Table 13. QUICC Engine pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
QE Clock Signals				
BRGO[1:4]	O	The functionality of this signal is determined by the SCFG[QEIOCLKCR] register bit fields.	If clocks are not used, pins can be programmed GPIOs and output.	
CLK[9:12]	I			
UCC1 signals				
UC1_CDB_RXER	I	The functionality of these signals is determined by the QE-TDMA field in the reset configuration word.	If UCC1 is not used, all the pins can be programmed as GPIOs and outputs.	
UC1_CTSB_RXDV	I			
UC1_RXD7	I			
UC1_TXD7	O			
UC1_RTSB_TXEN	O			
UCC3 signals				
UC3_CDB_RXER	I	The functionality of these signals is determined by the QE-TDMB field in the reset configuration word.	If UCC3 is not used, all the pins can be programmed as GPIOs and outputs.	
UC3_CTSB_RXDV	I			
UC3_RXD7	I			
UC3_TXD7	O			
UC3_RTSB_TXEN	O			

Table continues on the next page...

Table 13. QUICC Engine pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
TDMA signals				
TDMA_TXD	O	The functionality of these signals is determined by the QE-TDMA field in the reset configuration word.	If TDMA is not used, all the pins can be programmed as GPIOs and outputs.	
TDMA_TSYNC	I			
TDMA_RQ	O			
TDMA_RSYNC	I			
TDMA_RXD	I			
TDMB signals				
TDMB_TXD	O	The functionality of these signals is determined by the QE-TDMB field in the reset configuration word.	If TDMB is not used, all the pins can be programmed as GPIOs and outputs.	
TDMB_TSYNC	I			
TDMB_RQ	O			
TDMB_RSYNC	I			
TDMB_RXD	I			

5.5 Display Unit Interface recommendations

The T1024 has an internal display interface unit (DIU) that is suitable for driving video at resolution up to 1280 x 1024 (single-plane), or any resolution up to 1024 x 768 (three multiple planes).

DIU signals are muxed with QUICC Engine signals; therefore, when DIU is selected, QUICC Engine cannot be used.

DIU is supported at 3.3 V only. DIU usage requires DV_{DD} at 3.3 V; otherwise, board-level converters may be required.

General guidelines for interfacing the DIU controller can be referenced from *MPC5121e Hardware Design Guide* (MPC5121EQRUG), available on www.nxp.com

5.5.1 Display Interface Unit pin termination recommendations

Table 14. DIU pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
DIU_CLK_OUT	O	The functionality of these signals is determined by the RCW[QE_TDMA] and RCW[QE_TDMB] fields in the reset configuration word.	If DIU is not used, pins can be programmed as GPIOs and outputs.	
DIU_D[0:11]	O			
DIU_DE	O			
DIU_HSYNC	O	The functionality of this signal is determined by the I2C4 field in the reset configuration word (RCW[I2C4]).		
DIU_VSYNC	O			

NOTE

1. The DIU on the T1024 is similar to the T1040 from NXP.
2. See the chip reference manual for pixel data mapping details.

5.6 DMA recommendations

DMA shares pins with SDHC and GPIO2. The functionality of these signals is determined by the RCW[SDHC_BASE], RCW[SDHC], and RCW[SDHC_EXT] fields.

5.6.1 DMA pin termination recommendations

Table 15. DMA pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
DMA1_DREQ0_B	I	The functionality of this signal is determined by the DMA1 field in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC] and RCW[SDHC_EXT]).	This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
DMA1_DACK0_B	O		This pin can be left unconnected.	
DMA1_DDONE0_B	O		This pin can be left unconnected.	
DMA2_DREQ0_B	I	The functionality of these signals is determined by the DMA2 field in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC] and RCW[SDHC_EXT]).	This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
DMA2_DACK0_B	O		This pin can be left unconnected.	
DMA2_DDONE0_B	O		This pin can be left unconnected.	

5.7 Multicore programmable interrupt controller (MPIC) recommendations

The MPIC pins on the T1024 are distributed over several voltage domains. Some MPIC signals can be used to generate interrupt for wake up from deep sleep mode.

5.7.1 MPIC pin termination recommendations

Table 16. MPIC pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
IRQ[0:2]	I	Ensure these pins are driven in the non-asserted state.	IRQ[0:1] should be tied high through a 2-10 kΩ resistor to $O1V_{DD}$. IRQ[2] should be tied high through a 2-10 kΩ resistor to $L1V_{DD}$.	
IRQ[3:5]	I	The functionality of these signals is determined by the IRQ_BASE field in the reset configuration word (RCW[IRQ_BASE]).	IRQ3 should be pulled high through 2-10 kΩ resistors to $L1V_{DD}$, IRQ4 should be pulled high through 2-10 kΩ resistors to CV_{DD},	

Table continues on the next page...

Table 16. MPIC pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
			IRQ5 should be pulled high through 2-10 kΩ resistors to DV_{DD}, or IRQ[3:5] pins can be programmed as output and left floating.	
IRQ_OUT_B	O	The functionality of this signal is determined by the IRQ_OUT field in the reset configuration word (RCW[IRQ_OUT]). Tie this open-drain signal high through a weak pull-up resistor (2-10 kΩ) to $O1V_{DD}$.	If unused, this pin can be left floating.	

5.8 IEEE1588 recommendations

5.8.1 IEEE 1588 pin termination recommendations

Table 17. IEEE 1588 pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
TSEC_1588_CLK_IN	I	Connect to external high-precision timer reference input. The functionality of these signals is determined by the 1588 field in the reset configuration word (RCW[1588]).	Program as GPIOs and output.	
TSEC_1588_TRIG_IN[1:2]	I	The functionality of these signals is determined by the 1588 field in the reset configuration word (RCW[1588]).		
TSEC_1588_ALARM_OUT[1:2]	O			
TSEC_1588_CLK_OUT	O			
TSEC_1588_PULSE_OUT[1:2]	O			

NOTE

1. All IEEE 1588 pins are referenced to LV_{DD}.

5.9 Ethernet management recommendations

The T1024 supports two Ethernet Management Interfaces (EMIs).

5.9.1 Ethernet management pin termination recommendations

Table 18. Ethernet management pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
MDIO and MDC in $L1V_{DD}$ voltage domain mapped on AH4 and AH3 balls, respectively				
EMI1_MDC	O	—	This pin can be left unconnected.	
EMI1_MDIO	I/O	This pin should be pulled high through a 2-10 kΩ resistor to $L1V_{DD}$.	This pin should be tied low through a 2-10 kΩ resistor to GND.	
MDIO and MDC in TV_{DD} voltage domain				
EMI2_MDC	O	These pins must be pulled up to 1.2 V through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.	This pin can be left unconnected.	
EMI2_MDIO	I/O		This pin should be tied high through a 2-10 kΩ resistor to TV_{DD} or OV_{DD}.	

5.10 Ethernet controller recommendations

The T1024 supports two Ethernet controllers (EC), which can connect to the Ethernet PHYs RGMII protocol.

The EC1 interface is powered by $L1V_{DD}$ supply and supports 2.5 V and 1.8 V operation for RGMII mode. The EC2 interface is powered by L_{VDD} supply and supports 2.5 V and 1.8 V operation for RGMII mode.

NOTE

$L1_{VDD}$ and L_{VDD} should always be configured at the same voltage.

5.10.1 Ethernet controller pin termination recommendations

Table 19. Ethernet controller pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1 in RGMII mode				
EC1_TXD[0:3]	O	The functionality of these signals is determined by the EC1 field in the reset configuration word (RCW[EC1]).	These pins may be left unconnected.	
EC1_TX_CTL [1]	O			
EC1_GTX_CLK125 [2]	O			
EC1_RXD[0:3]	I	FMAN-MAC4 is connected to the EC1 interface when RGMII is selected through the RCW[EC1] field.	These pins can be configured as GPIOs and outputs.	
EC1_RX_CTL	I			
EC1_RX_CLK	I			
EC1_GTX_CLK125	I			
EC2 in RGMII mode				
EC2_TXD[0:3]	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	These pins may be left unconnected.	
EC2_TX_CTL [1]	O			
EC2_GTX_CLK	I			
EC2_RXD[0:3]	I		These pins can be configured as GPIOs and outputs.	
EC2_RX_CTL	I			

Table continues on the next page...

Table 19. Ethernet controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
EC2_RX_CLK	I	FMAN-MAC3 is connected to the EC2 interface when RGMII is selected through the RCW[EC2] field.		
EC2_GTX_CLK125 [2]	O		When EC2 is unused, this pin can be configured as GPIO and output. When EC2 is used and EC1_GTX_CLK125 is used to clock the EC2 interface, then pull high or low through a 2-10 kΩ resistor to LV_{DD} or GND.	

1. This pin requires an external 1 kΩ pull-down resistor to prevent the PHY from seeing a valid transmit enable before it is actively driven.
2. Either of the EC1_GTX_CLK125 or EC2_GTX_CLK125 can be used to clock both of the EC interfaces in RGMII mode. The selection is through SCFG_EMIIOCR[GTXCLKSEL].

NOTE

1. RGMII interface has t_{SKEW} Rx (t_{SKRGT_RX}) in the range of 1.6 ns to 2.6 ns. Therefore, it's necessary to add a delay of 2.1 ns on board + PHY.
2. RGMII interface has t_{SKEW} Tx (t_{SKRGT_TX}) in the range of -0.6 ns to 0.5 ns. Therefore, it's necessary to add a delay of 2.0 ns on board + PHY.

5.11 UART recommendations

The T1024 supports two DUART interfaces.

5.11.1 UART pin termination recommendations

Table 20. UART pin termination checklist

Signal name	I/O type	Used	Not used	Completed
UART1_SOUT	O	The functionality of these signals is determined by the UART_BASE field in the reset configuration word (RCW[UART_BASE]).	These pins can be left unconnected.	
UART1_RTS_B	O			
UART1_SIN	I		If unused, pins can be programmed as GPIOs and output.	
UART1_CTS_B	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART2_SOUT	O		This pin can be left unconnected.	
UART2_RTS_B	O			
UART2_SIN	I		If unused, pins can be programmed as GPIOs and output.	
UART2_CTS_B	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART3_SOUT	O		This pin can be left unconnected.	

Table continues on the next page...

Table 20. UART pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
UART3_SIN	I		This pin can be programmed as GPIO and output.	
UART4_SOUT	O		This pin can be left unconnected.	
UART4_SIN	I		This pin can be programmed as GPIO and output.	

5.12 I2C recommendations

The T1024 supports up to four I^2C interfaces.

5.12.1 I2C pin termination recommendations

Table 21. I2C pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
IIC1_SDA	I/O	Tie these open-drain signals high through a nominal 1 kΩ resistor to DV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD}.	
IIC1_SCL	I/O			
IIC2_SDA	I/O			
IIC2_SCL	I/O			
IIC3_SDA	I/O	The functionality of this signal is determined by the I2C3 field in the reset configuration word (RCW[I2C3]). Tie these open-drain signals high through a nominal 1 kΩ resistor to DV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If I2C3 is not used, all pins can be programmed as GPIOs and output.	
IIC3_SCL	I/O			
IIC4_SDA	I/O	The functionality of this signal is determined by the I2C4 field in the reset configuration word (RCW[I2C4]). Tie these open-drain signals high through a nominal 1 kΩ resistor to DV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	If I2C4 is not used, all pins can be programmed as GPIOs and output.	
IIC4_SCL	I/O			

5.13 eSDHC recommendations

The T1024 eSDHC interface supports a large variety of devices:

- SDXC cards up to 2 TB of space with UHS-I speed grade
- UHS-I (ultra high speed grade) SDR12, SDR25, SDR50, SDR104, and DDR50

- UHS-I cards work on 1.8 V signaling
- On-board dual voltage regulators are needed to support UHS-I cards because card initialization happens at 3.3 V and regular operations happen at 1.8 V. The SD controller provides a signal to control the voltage regulator, which is controlled via the SDHC_VS bit.

- eMMC 4.5 (HS200, DDR)

eMMC DDR at 3.3 V is not supported.

Table 22. Supported SD card modes

Mode	1 bit support		4 bit support		8 bit support
	T1024	SD (3.0)	T1024	SD (3.0)	
Default Speed (DS)	Yes	Yes	Yes	Yes	Not supported by SD standards or by the T1024
High Speed (HS)	Yes	Yes	Yes	Yes	
SDR12	No	No	Yes	Yes	
SDR25	No	No	Yes	Yes	
SDR50	No	No	Yes	Yes	
SDR104	No	No	Yes	Yes	
DDR50	No	No	Yes	Yes	

Table 23. Supported MMC/eMMC modes

Mode	1 bit support		4 bit support		8 bit support	
	T1024	eMMC (4.5)	T1024	eMMC (4.5)	T1024	eMMC (4.5)
Default Speed (DS)	Yes	Yes	Yes	Yes	Yes	Yes
High Speed (HS)	Yes	Yes	Yes	Yes	Yes	Yes
HS200	No	No	Yes	Yes	Yes	Yes
DDR (1.8 V)	No	No	Yes	Yes	No	Yes

5.13.1 eSDHC pin termination recommendations

Table 24. eSDHC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SDHC_CMD	I/O	This pin should be pulled high through a 10-100 kΩ resistor to EV_{DD}. The functionality is determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).	Program as GPIO and output.	
SDHC_CLK	O	The functionality is determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).		
SDHC_DAT[0]	I/O	These pins should be pulled high through 10-100 kΩ resistors to EV_{DD}.	Program as GPIO and output.	

Table continues on the next page...

Table 24. eSDHC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
SDHC_DAT[1:3]	I/O	The functionality is determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).	Unused pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}.	
SDHC_DAT[4:7]	I/O	These pins should be pulled high through 10-100 kΩ resistors to CV_{DD}. The functionality is determined by the SPI_BASE field in the reset configuration word (RCW[SPI_BASE]).	Program as GPIOs and output.	
SDHC_CD_B	I	These pins should be pulled high through 10-100 kΩ resistors to CV_{DD}. The functionality is determined by the SDHC field in the reset configuration word (RCW[SDHC]).	These pins should be pulled high through a 10-100 kΩ resistor to CV_{DD} or program as GPIOs and output.	
SDHC_WP	I			
SDHC_CMD_DIR	O	These pins should be pulled high through 10-100 kΩ resistors to CV_{DD}. The functionality is determined by the SPI_BASE field in the reset configuration word (RCW[SPI_BASE]). **NOTE:** DIR signals are used as direction controls of external voltage translator.	Pins can be programmed for other functions or as GPIO and output.	
SDHC_DAT0_DIR	O			
SDHC_DAT123_DIR	O			
SDHC_VS	O	These pins should be pulled high through 10-100 kΩ resistors to $O1V_{DD}$. The functionality is determined by the IRQ_BASE and IRQ_EXT field in the reset configuration word (RCW[IRQ_BASE] and RCW[IRQ_EXT]). **NOTE:** External voltage select, to change voltage of external regulator.	Can be left floating or programmed for other function.	
SDHC_CLK_SYNC_IN	I	The functionality is determined by the IRQ_BASE and IRQ_EXT field in the reset configuration word (RCW[IRQ_BASE] and RCW[IRQ_EXT]).	If signal is not used, pin can be programmed for other functions or pulled down using a weak resistor.	
SDHC_CLK_SYNC_OUT	O	The functionality is determined by the SPI_BASE field and SPI_EXT field in the reset configuration word (RCW[SPI_BASE] and RCW[SPI_EXT]).	Can be left floating or programmed for other function.	

NOTE

1. Separate DIR signals are implemented to support card interrupt on DAT1 in single bit mode.

2. SDHC_CLK_SYNC_OUT to SDHC_CLK_SYNC_IN connection is required in SDR50 and DDR50 mode only.
3. In SDR50 and DDR50 mode, all the input signals are sampled with respect to SDHC_CLK_SYNC_IN.
4. SDHC_CLK_SYNC_OUT and SDHC_CLK_SYNC_IN should be routed as close as possible to card with minimum skew, with respect to SD_CLK.
5. When using 8-bit MMC/eMMC configuration, EV_{DD} and CV_{DD} should be set at the same voltage.

5.13.2 eSDHC system-level recommendations

Table 25. eSDHC system-level checklist

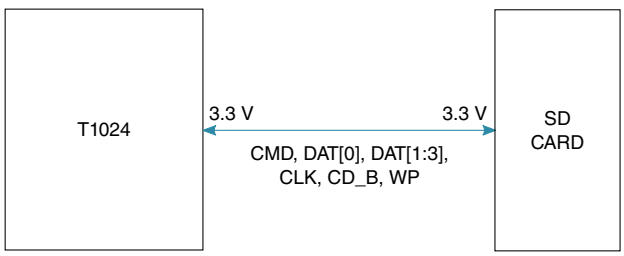
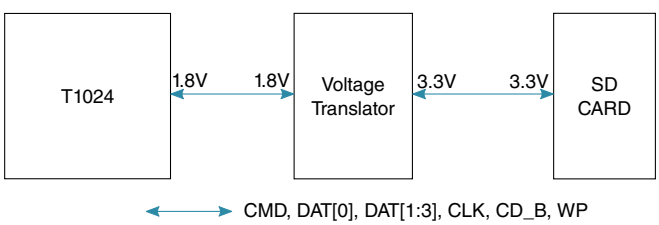
Item	Completed
SD card interfacing (8 bit is not supported)	
SD card connections (DS and HS mode) EV_{DD} is configured for 3.3 V.  **Figure 6. DS and HS modes**	
SD card connections (DS and HS modes with voltage translator) EV_{DD} is configured for 1.8 V.  **Figure 7. DS and HS modes**	
SD card connections (SDR12, 25, 50, 104 and DDR50 modes without voltage translator) UHS-I modes work on 1.8 V signalling. SYNC_OUT and SYNC_IN connections are required in SDR50 and DDR50 modes only. **NOTE:** Resistor R = 10 K is needed when RCW loading is required to be done from SD card.	

Table continues on the next page...

Table 25. eSDHC system-level checklist (continued)

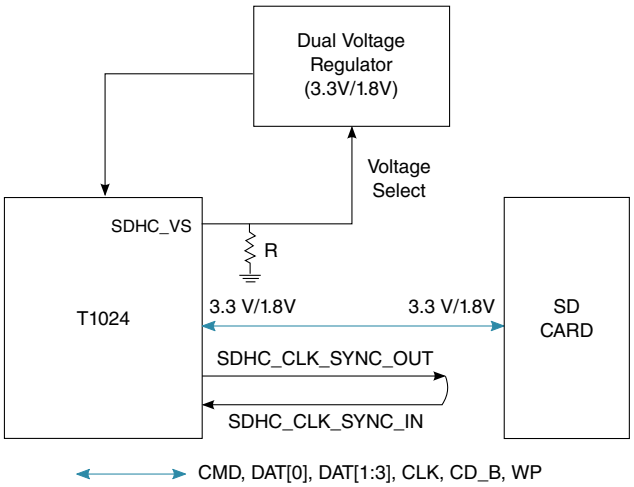
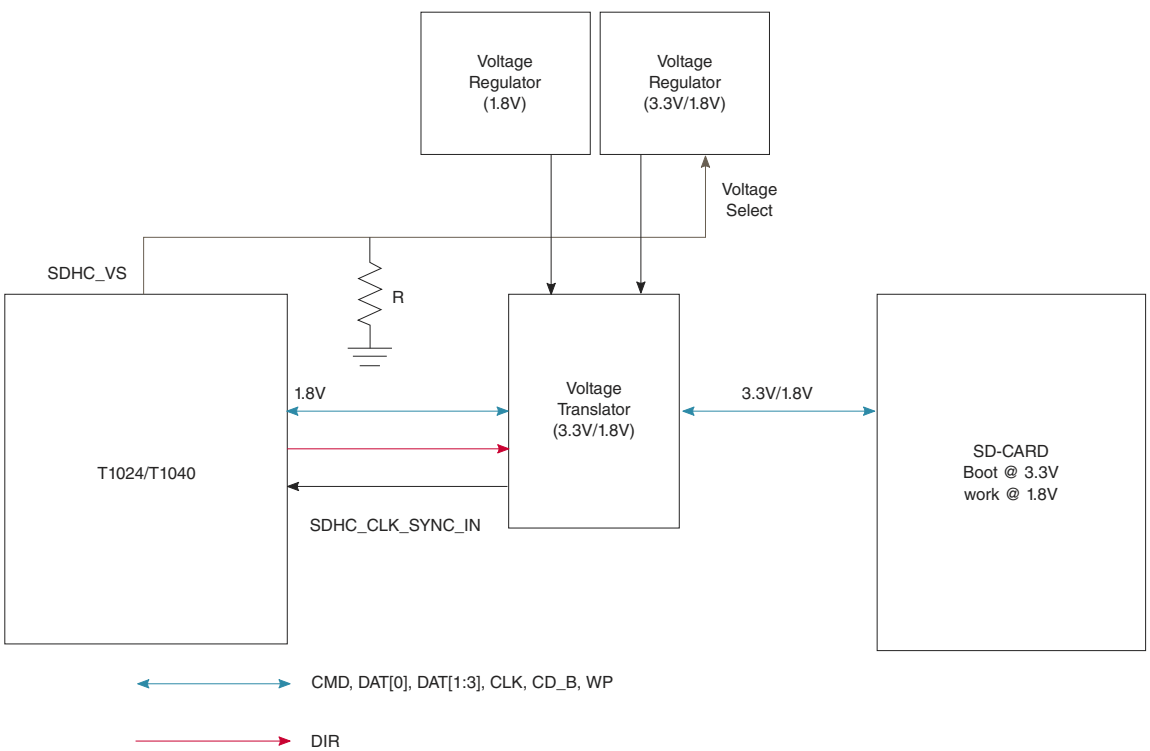
Item	Completed
 **Figure 8. SDR12, 25, 50, 104 and DDR50 modes**	
SD card connections (SDR12, 25, 50, 104 and DDR50 modes with voltage translator) UHS-I modes work on 1.8 V signalling. SYNC_IN connections are required in SDR50 and DDR50 modes only. **NOTE:** Resistor R = 10 K is needed when RCW loading is required to be done from SD card.  **Figure 9. SDR12, 25, 50, 104 and DDR50 modes**	
MMC Interfacing	

Table continues on the next page...

Table 25. eSDHC system-level checklist (continued)

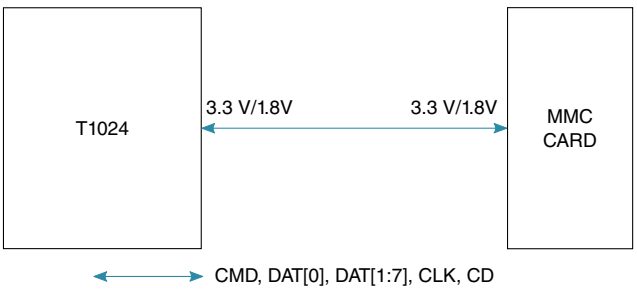
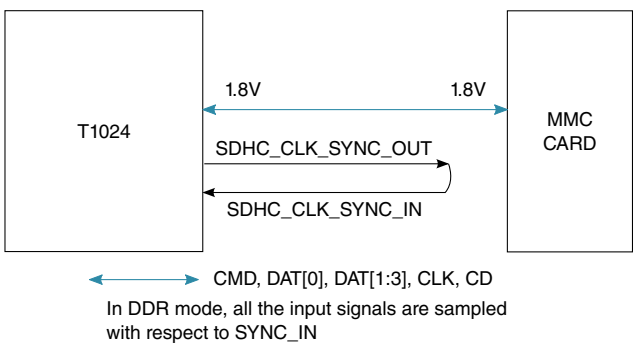
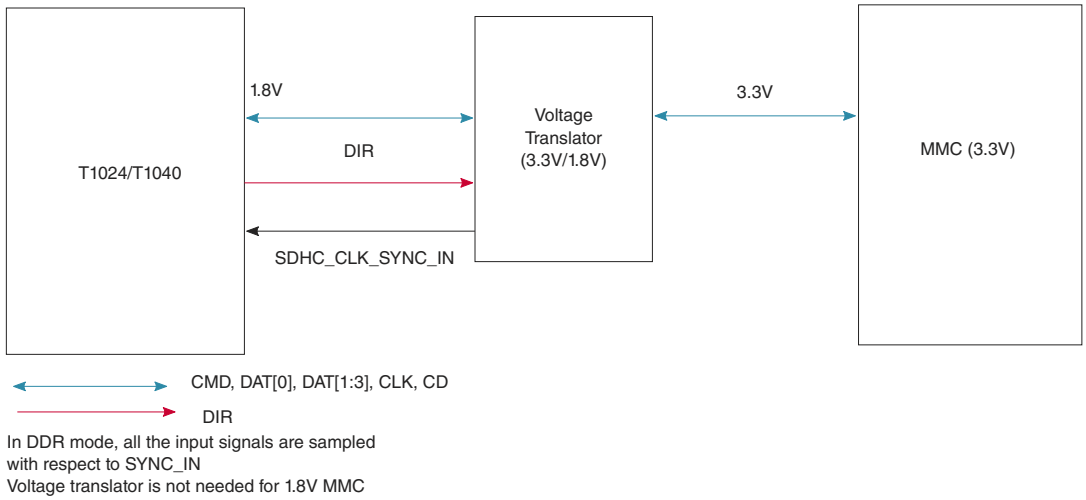
Item	Completed
MMC card connections (DS, HS, HS200 modes) 8-bit MMC requires EVDD and CVDD configured at the same voltage because DAT[0:3] are on EVDD and DAT[4:7] are on CVDD.  **Figure 10. DS, HS, HS200 modes for MMC** **NOTE:** Voltage translator requirement depends upon the chosen MMC/eMMC voltage and CV_{DD}/EV_{DD} voltage configuration. The HS200 modes operates at 1.8 V.	
MMC card connection in DDR mode 8-bit operation cannot be supported due to pin multiplexing constraints.  **Figure 11. DDR mode without voltage translator**	

Table 25. eSDHC system-level checklist

Item	Completed
 **Figure 12. DDR mode with voltage translator**	

5.14 eSPI recommendations

The T1024 serial peripheral interface (SPI) pins are powered from CV_{DD} supply, which supports 1.8 V and 3.3 V.

5.14.1 eSPI pin termination recommendations

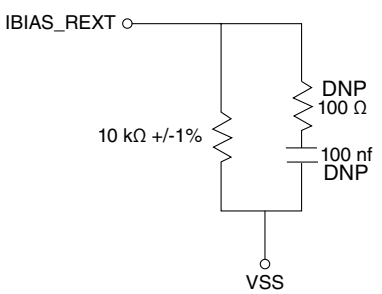
Table 26. eSPI pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SPI_MISO	I	—	This pin should be pulled high through a 2-10 kΩ resistor to CV_{DD}.	
SPI_MOSI	I/O	—	This pin should be pulled high through a 2-10 kΩ resistor to CV_{DD}.	
SPI_CLK	O	—	This pin may be left unconnected.	
SPI_CS[0:3]_B	O	The functionality of this signal is determined by the SPI_BASE field in the reset configuration (RCW[SPI_BASE]).	These pins may be left unconnected.	

5.15 USB recommendations

5.15.1 USB pin termination recommendations

Table 27. USB pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
USB1_UDP	I/O	—	This pin may be left unconnected.	
USB1_UDM	I/O	—	This pin may be left unconnected.	
USB1_VBUSCLMP	I	A divider network is required on this signal. See USB divider network.	This pin should be pulled low through a 1 kΩ resistor to GND.	
USB1_UID	I	—	This pin should be pulled low through a 1 kΩ resistor to GND.	
USB1_DRVVBUS	O	A divider network is required on this signal. See USB divider network.	This pin may be left unconnected.	
USB1_PWR_FAULT	I	—	This pin should be pulled low through a 1 kΩ resistor to GND.	
USB2_UDP	I/O	—	This pin may be left unconnected.	
USB2_UDM	I/O	—	This pin may be left unconnected.	
USB2_VBUSCLMP	I	A divider network is required on this signal. See USB divider network.	This pin should be pulled low through a 1 kΩ resistor to GND.	
USB2_UID	I	—	This pin should be pulled low through a 1 kΩ resistor to GND.	
USB2_DRVVBUS	O	A divider network is required on this signal. See USB divider network.	This pin may be left unconnected.	
USB2_PWR_FAULT	I	—	This pin should be pulled low through a 1 kΩ resistor to GND.	
USB_IBIAS_REXT	I/O	Connect as shown in following figure. Keep filter components close to the SoC pin as much as possible. 	This pin may be left unconnected.	
USBCLK[1]	I	Connect to 24 MHz clock oscillator. USBCLK is on $O1V_{DD}$ power domain (1.8 V). Spread spectrum clocking is not supported.	This pin should be pulled low through a 2-10 kΩ resistor to GND.	

1. USB PHY can optionally be provided reference clock generated internally from system clock. In that case, USBCLK is unused and must be pulled low through a 2-10 kΩ resistor to GND.

5.15.2 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are:

- Both resistors require 1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5–5.25 V.
- The 0.6 V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8 V. If the USB PHY does not support OTG mode, this diode can be removed from the schematic or made a DNP component.

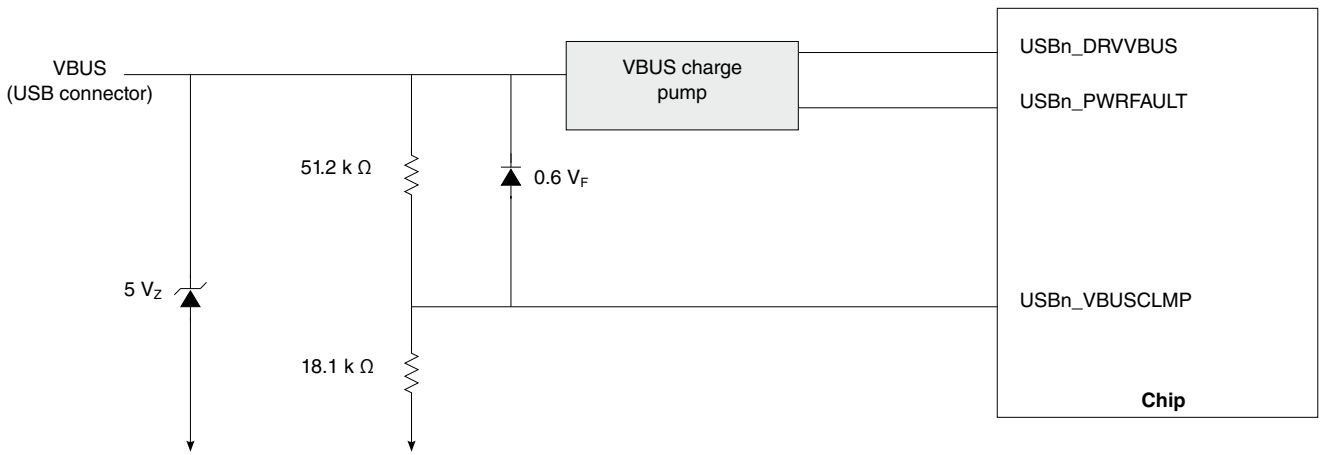


Figure 13. Divider network at VBUS

5.16 GPIO recommendations

5.16.1 GPIO pin termination recommendations

Table 28. GPIO pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
GPIO1[9:12]	I/O	The functionality of these signals is determined by the IFC_GRP_[a]_BASE fields in the reset configuration word (RCW).	These pins should be pulled high through 2-10 kΩ resistors to OV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO1[13]	O	The functionality of this signal is determined by the ASLEEP field in the reset configuration word (RCW[ASLEEP]).	This pin should be pulled high through a 2-10 kΩ resistor to $O1V_{DD}$ or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO1[14]	I/O	The functionality of this signal is determined by the RTC field in the reset configuration word (RCW[RTC]).	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	

Table continues on the next page...

Table 28. GPIO pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
GPIO1[15:22]	I/O	The functionality of these signals is determined by the UART_BASE field in the reset configuration word (RCW[UART_BASE]).	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO1[23:31]	I/O	The functionality of these signals is determined by the IRQ_BASE field in the reset configuration word (RCW[IRQ_BASE]).	GPIO1[23:31] can be pulled high through a 2-10 kΩ resistor to their respective power supply domain or can be left floating if configured as outputs via the GPIO_GPDIR register. For pin power supply domain, refer to pinout list table of QorIQ T1024 datasheet.	
GPIO2[0:3]	I/O	The functionality of these signals is determined by the SPI_BASE field in the reset configuration word (RCW[SPI_BASE]).	These pins should be pulled high through 2-10 kΩ resistors to CV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO2[4:9]	I/O	The functionality of these signals are determined by the SDHC_BASE field in the reset configuration word (RCW[SDHC_BASE]).	These pins should be pulled high through 2-10 kΩ resistors to EV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO2[10:15], GPIO2[25:31]	I/O	The functionality of these signals is determined by the IFC_GRP_[a]_BASE fields in the reset configuration word.	These pins should be pulled high through 2-10 kΩ resistors to OV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO3[0:7]	I/O	The functionality of these signals is determined by the 1588 field in the reset configuration word (RCW[1588]).	These pins should be pulled high through 2-10kΩ resistors to LV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO3[8:23]	I/O	The functionality of these signals is determined by the EC1 field in the reset configuration word (RCW[EC1]).	These pins should be pulled high through 2-10 kΩ resistors to $L1V_{DD}$ or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO3[24:31]	I/O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	These pins should be pulled high through 2-10 kΩ resistors to LV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO4[0:1]	I/O	The functionality of these signals is determined by the I2C3 field in the reset configuration word (RCW[I2C3]).	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO4[2:3]	I/O	The functionality of these signals is determined by the I2C4 field in the reset configuration word (RCW[I2C4]).	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO4[4:6]	I/O	The functionality of these signals is determined by the DMA1 field in the reset configuration word (RCW[DMA1]).	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
GPIO4[7:9]	I/O	The functionality of these signals is determined by the DMA2 field in the reset configuration word (RCW[DMA2]).	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	

5.17 Debug and reserved pin recommendations

5.17.1 Debug and reserved pin termination recommendations

Table 29. Debug and test pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
ASLEEP	O	The functionality of this signal is determined by the ASLEEP field in the reset configuration word (RCW[ASLEEP]).		
SCAN_MODE_B	I	This is a test signal for factory use only and must be pulled up (100 Ω to 1 kΩ) to $O1V_{DD}$ for normal device operation.		
TEST_SEL_B	I	This pin must be pulled to $O1V_{DD}$ through a 100 Ω to 1 kΩ resistor for a two-core T1024 and tied to ground for a single-core T1014 device.		
EVT_B[0:4]	I/O	Debug event. 1. EVT_B[2]: Functions as POWER_EN output in deep sleep. See Power Management pin termination recommendations. 2. EVT_B[3]: Functions as POWER_OK pin input in deep sleep. See Power Management pin termination recommendations.	These pins should be pulled high through 2-10 kΩ resistors to $O1V_{DD}$.	
EVT_B[5:6]	I/O	The functionality of these signals is determined by the I2C4 field in the reset configuration word (RCW[I2C4]). [1]	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD}.	
EVT_B[7:8]	I/O	The functionality of these signals is determined by the DMA2 field in the reset configuration word (RCW[DMA2]).	These pins should be pulled high through 2-10 kΩ resistors to DV_{DD}.	
EVT_B[9]	I/O	The functionality of this signal is determined by the IRQ_OUT field in the reset configuration word (RCW[IRQ_OUT]). EVT_B[9] functions as isolation enable output during deep sleep. For details, see Power Management pin termination recommendations.	This pin should be pulled high through 2-10 kΩ resistors to $O1V_{DD}$.	
CKSTP_OUT_B	O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to OV_{DD}.		
FA_VL	—	Reserved. This pin must be pulled to ground (GND).		
PROG_MTR	—	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_G_V	—	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_PIN	—	Reserved. This pin must be pulled to ground (GND).		
TH_TPA	—	Do not connect. This pin should be left floating.		
TD1_ANODE	—	Connect as required.	Tie to GND if not used.	

Table continues on the next page...

Table 29. Debug and test pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
TD1_CATHODE	—	Connect as required.	Tie to GND if not used.	

1. The direction of EVT[5:7] is controlled by EPEVTCR8 instead of EPEVTCR[5:7].

5.18 Platform trust recommendations

5.18.1 Platform trust pin termination recommendations

Table 30. Trust pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (1.8 V) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}.	

5.19 Clock recommendations

5.19.1 Clock pin termination recommendations

Table 31. Clock pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1_GTX_CLK125	I	For gigabit operation, connect to a 125 MHz clock source or connect to PHY. T1024 has a duty cycle reshaper built in the RGMII block. This allows the clock from RGMII PHY to be used.	If EC1 is not used, this pin can be programmed as GPIO and output.	
EC2_GTX_CLK125	I	For gigabit operation, connect to a 125 MHz clock source or connect to PHY. T1024 has a duty cycle reshaper inbuilt in RGMII block which allows clock from RGMII PHY to be used.	If EC2 is not used, this pin can be programmed as GPIO and output.	
CLK_OUT	O	CLK_OUT is for monitoring purposes only. Connect to test point to aid debug.	This pin may be left unconnected.	
RTC	I	Alternative time-base clock to the platform clock. For more details, see the *e5500 Core Reference Manual*.	This pin can be programmed as GPIO and output.	

Table continues on the next page...

Table 31. Clock pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
		The functionality of this signal is determined by the RTC field in the reset configuration word (RCW[RTC]).		
SYSCLK	I	This is the single ended primary clock input to the chip and supports a 64-133.3 MHz clock range. 64 MHz SYSCLK reference frequency support is specifically for Profibus support on QUICC Engine.	This pin should be pulled low through a 2-10 kΩ resistor to GND.[1]	
DDRCLK	I	Reference clock for DDR controller, supports 64-133.3 MHz input clock range.	This pin should be pulled low through a 2-10 kΩ resistor to GND.[2]	
DIFF_SYSCLK/ DIFF_SYSCLK_B	I	These pins are the differential primary clock input to the chip and support 100 MHz only. When used, these pins should be connected to a 100 MHz differential clock generator.	These pins should be pulled low through 2-10 kΩ resistors to GND or they can be left floating.[3]	
USBCLK	I	This pin should be connected to a 24 MHz clock source.	This pin should be pulled low through a 2-10 kΩ resistor to GND.[4]	

1. In the "Single Oscillator Source" Reference Clock Mode supported by T1024, DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs are used as primary clock input and SYSCLK is unused. Power-on-config signal *cfg_eng_use0* selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs.
2. In the "Single Oscillator Source" Reference Clock mode, DIFF_SYSCLK/DIFF_SYSCLK_B clock inputs can be selected to feed the DDR PLL. RCW bits [DDR_REFCLK_SEL] are used for this selection and DDRCLK is unused.
3. When SYSCLK is chosen as the primary clock input to the chip, these pins are unused.
4. Control bits in USB PHY registers can be programmed to select USB reference clock generated internally from system clock. A divide by 5 logic is used to obtain 20 MHz reference to USB PHY. This requires system clock to be 100 MHz. USBCLK is unused.

5.19.2 Clocking system-level recommendations

Table 32. Clocking system-level checklist

Item	Completed
"Single Oscillator Source" Reference Clock Mode	
• In this clocking mode, DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs are used as primary clock input and SYSCLK is unused. Power-on-config signal *cfg_eng_use0* selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs. • DIFF_SYSCLK/DIFF_SYSCLK_B clock inputs can be selected to feed the DDR PLL and DDRCLK is unused. RCW bits RCW[DDR_REFCLK_SEL] are used for this selection. • USB PHY is provided reference clock generated internally from system clock. A divide by 5 logic is used to generate 20MHz reference clock for USB PHY in this mode. Control bits for programmable divider are specified in USB registers. • RCW[DDR_REFCLK_SEL] bit is used to select clock input (DIFF_SYSCLK or DDRCLK) to the DDR PLL.	

Table continues on the next page...

Table 32. Clocking system-level checklist (continued)

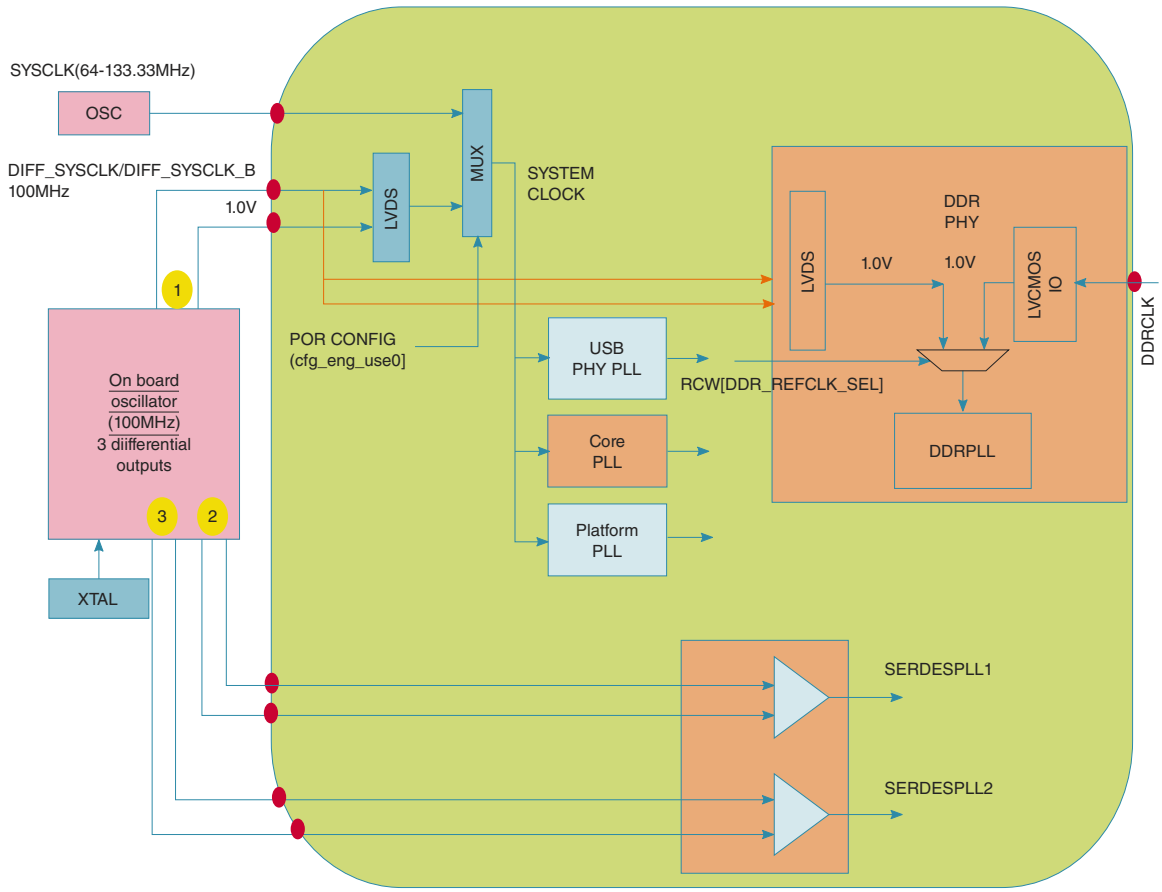
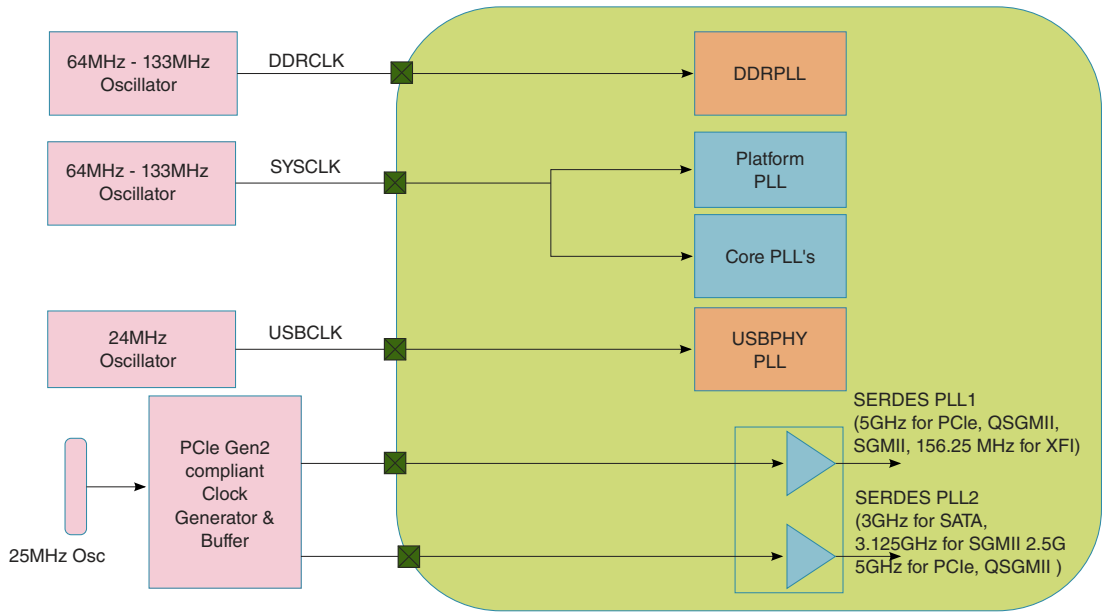
Item	Completed
 **Figure 14. Single Oscillator Source clocking** **NOTE:** Spread spectrum is not supported on Differential SYSCLK clock inputs.	
Multiple Reference Clock Mode (legacy mode)	
• In this clocking mode, SYSCLK (single ended) clock input is used as primary clock input. Power-on-config signal *cfg_eng_use0* selects between SYSCLK (single ended) and DIFF_SYSCLK/ DIFF_SYSCLK_B (differential) clock inputs. • DDRCLK clocks the DDRPLL. RCW bits RCW[DDR_REFCLK_SEL] are used for this selection. • USB PHY is clocked by USBCLK clock input or can be provided reference clock generated internally from system clock. A divide by 5 logic is used to generate 20MHz reference clock for USB PHY in this mode. Control bits for programmable divider are specified in USB registers.	

Table 32. Clocking system-level checklist

Item	Completed
 **Figure 15. Multiple Reference Clocking**	

5.19.2.1 DIFF_SYSCLK/DIFF_SYSCLK_B system-level recommendations

Table 33. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist

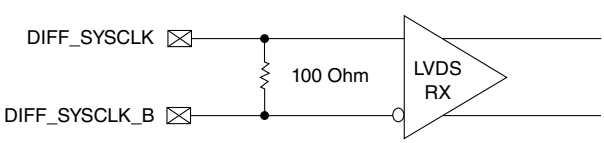
Item	Completed
DIFF_SYSCLK/DIFF_SYSCLK_B can be selected to provide primary clock to the chip. Although it is a Low Voltage Differential Signaling (LVDS) type clock driver, it has AC/DC characteristics identical to the SerDes reference clock inputs, which are High-Speed Current Steering Logic (HCSL) compatible. This eases system design because the same clock driver can be used to provide the various differential clock inputs required by the chip.  **Figure 16. LVDS receiver**	
Interfacing DIFF_SYSCLK/DIFF_SYSCLK_B with other Differential Signalling levels	
Connection with HCSL clock driver	

Table continues on the next page...

Table 33. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

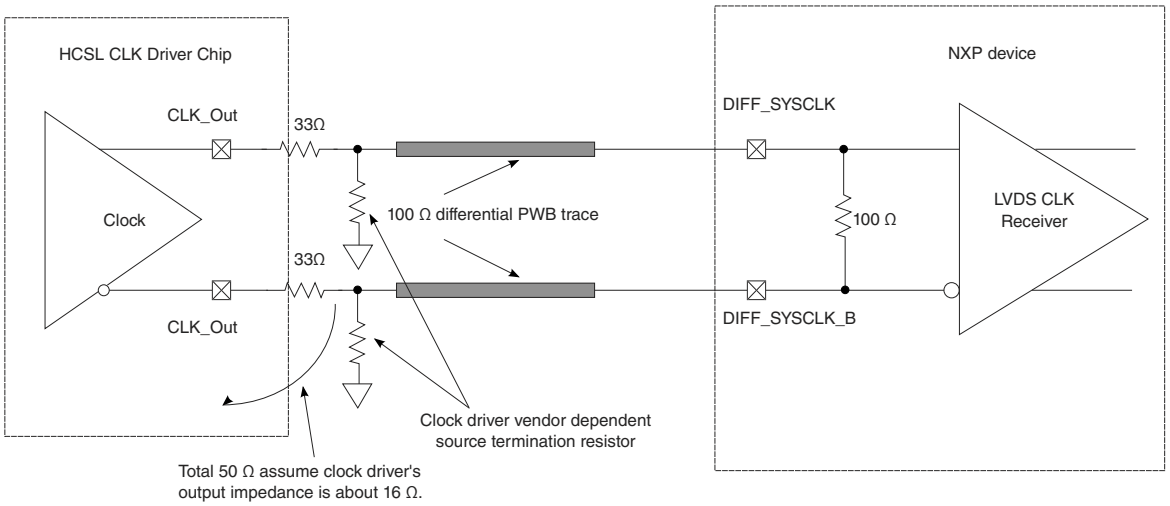
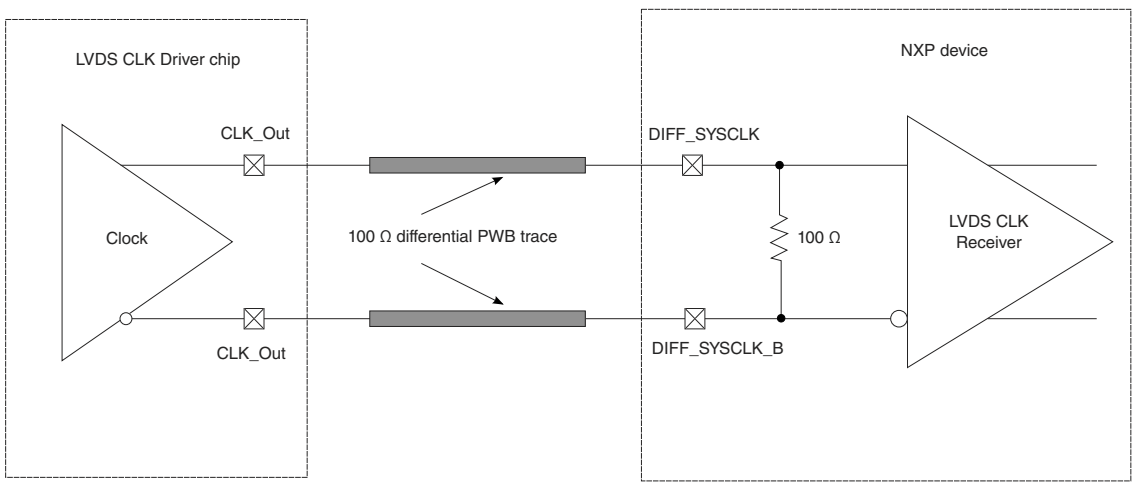
Item	Completed
 **Figure 17. Interfacing with HCSL clock driver (Reference only)**	
Connection with LVDS clock driver  **Figure 18. Interfacing with LVDS clock driver (Reference only)**	
Connection with LVPECL clock driver	

Table continues on the next page...

Table 33. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

Item	Completed

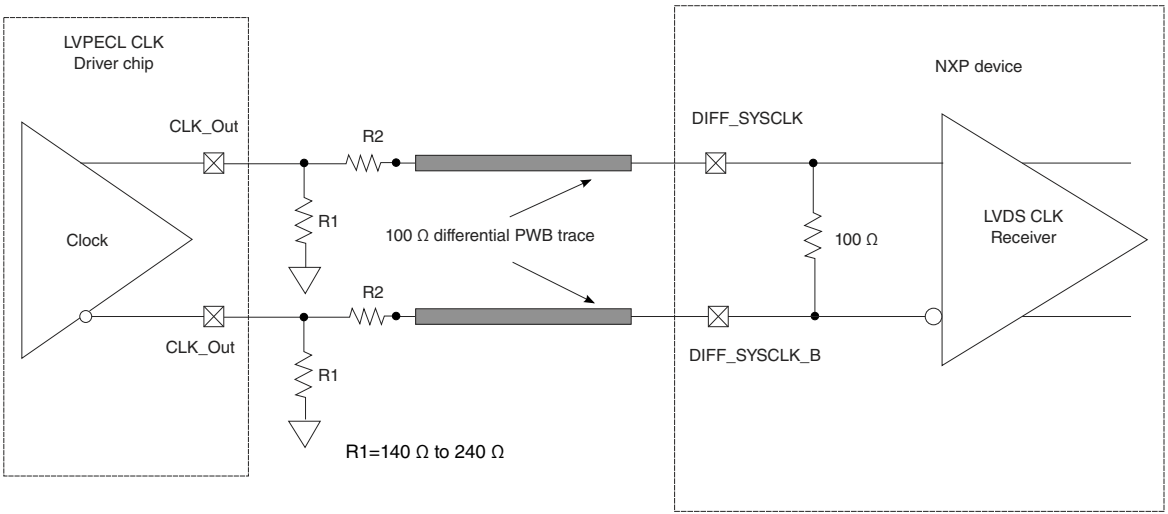
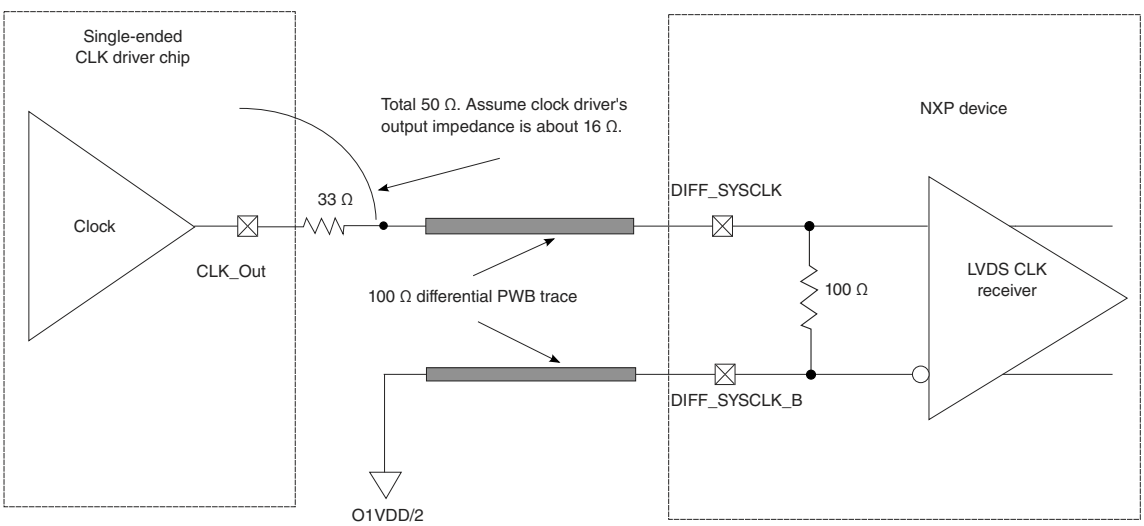



Figure 19. Interfacing with LVPECL clock driver (Reference only)	
Single-ended connection with clock driver The DIFF_SYSCLK_B should be terminated to O1VDD/2. 	
Figure 20. Single ended connection (Reference only)	

5.19.3 System clocking

This section describes the PLL configuration of the chip.

5.19.3.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There is a core cluster PLL that generates a clock for each core cluster from the externally supplied SYSCLK input.
  - Core cluster Group A PLL
  - The frequency ratio between the core cluster PLL and SYSCLK is selected using the configuration bits as described in Core cluster to SYSCLK PLL ratio. The frequency for each core cluster is selected using the configuration bits as described in Table 38.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- Cluster group A generates an asynchronous clock for eSDHC SDR mode from CGA PLL, described in eSDHC SDR mode clock select.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input. The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in DDR controller PLL ratios.
- SerDes block has two PLLs that generate a core clock from their respective externally supplied SD1_REF_CLK*n*_P/ SD1_REF_CLK*n*_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in SerDes PLL ratio.
- When using Single Oscillator Source clocking mode, a single onboard oscillator can provide the reference clock (100 MHz) to all the PLLs (that is, Platform PLL, Core Cluster PLLs, DDR PLL, USB PLL and SerDes PLLs).

5.19.3.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 34. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1000 MHz		1200 MHz		1400 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	1000	1400	MHz	1, 2
Core cluster frequency	500	1000	500	1200	500	1400	MHz	2
Platform clock frequency	256	400	256	400	256	400	MHz	1, 6
Memory bus clock frequency (DDR3L)	500	800	500	800	500	800	MHz	1, 3, 4
Memory bus clock frequency (DDR4)	625	800	625	800	625	800	MHz	1, 3, 4
IFC clock frequency	—	100	—	100	—	100	MHz	5
FMAN	500	500	500	600	500	700	MHz	—

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies

2. The core cluster runs at cluster group A PLL. The core cluster group A PLL minimum frequency is 1000 MHz. With a minimum cluster group PLL frequency of 1000 MHz, this results in a minimum allowable core cluster frequency of 500 MHz. Frequency provided to the e5500 cluster after any dividers must always be greater than or equal to the platform frequency. For the case of the platform frequency = 400 MHz, the minimum core cluster frequency is 500 MHz.

Table 34. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1000 MHz		1200 MHz		1400 MHz			
	Min	Max	Min	Max	Min	Max		
3. The memory bus clock speed is half the DDR3L/DDR4 data rate. 4. The memory bus clock speed is dictated by its own PLL. 5. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information. 6. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces. 7. "Single Oscillator Source" Reference clock mode supports differential reference clock pair frequency of 100 MHz.								

5.19.3.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 35. Memory bus clocking specifications

Characteristic		Min	Max	Unit	Notes
Memory bus clock frequency	DDR3L	500	800	MHz	1, 2, 3, 4
	DDR4	625	800		
Notes: 1. **Caution:** The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios for ratio settings. 2. The memory bus clock refers to the chip's memory controllers' D1_MCK[0:1] and D1_MCK[0:1]_B output clocks, running at half of the DDR data rate. 3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios. 4. The minimum frequency supported by DDR4 is 1250 MT/s.					

5.19.3.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 36. Platform to SYSCLK PLL ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1

Table continues on the next page...

Table 36. Platform to SYSCLK PLL ratios (continued)

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
All Others	Reserved

5.19.3.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CGA_PLLn_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CGA_PLLn_CFG = 0b00.

This table lists the supported asynchronous core cluster to SYSCLK ratios.

Table 37. Core cluster PLL to SYSCLK ratios

Binary value of CGA_PLLn_RAT(n=1 or 2)	Core cluster:SYSCLK Ratio
00_0110	6:1
00_0111	7:1
00_1000	8:1
00_1001	9:1
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1
00_1111	15:1
01_0000	16:1
01_0010	18:1
01_0100	20:1
01_0110	22:1
01_1001	25:1
01_1010	26:1
01_1011	27:1
All others	Reserved

5.19.3.5 Core complex PLL select

The clock frequency of each core cluster is determined by the binary value of the RCW Configuration field Cn_PLL_SEL. These tables describe the selections available to each core cluster, where each individual core cluster can select a frequency from their respective tables.

NOTE

There is a restriction that requires that the frequency provided to the e5500 core cluster after any dividers must always be greater than half of the platform frequency. Special care must be used when selecting the /2 outputs of a cluster PLL in which this restriction is observed.

Table 38. Core cluster PLL select

Binary Value of Cn_PLL_SEL for n=1-4	Core cluster ratio
0000	CGA PLL1 /1
0001	CGA PLL1 /2
All Others	Reserved

5.19.3.6 DDR controller PLL ratios

The DDR memory controller operates asynchronous to the platform.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 39. DDR clock ratio

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
00_1000	8:1	1066
00_1010	10:1	1333
00_1011	11:1	1465
00_1100	12:1	1600
00_1101	13:1	1300
00_1110	14:1	1400
00_1111	15:1	1500
01_0000	16:1	1600
1_0100	20:1	1333
1_1000	24:1	1600
All Others	Reserved	—

5.19.3.7 SerDes PLL ratio

The clock ratio between each of the two SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/ SD1_REF_CLKn_N inputs is determined by a set of RCW Configuration fields (SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_*_S1), as shown in this table.

Table 40. Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S1	Legal setting for SRDS_PLL_REF_CLK_SEL_S1	Legal setting for SRDS_DIV_*_S1	Notes
High-speed serial interfaces					
PCI Express 2.5 Gbps	100 MHz	Any PCIe	0b0: 100 MHz	2b10: 2.5 G	1
(doesn't negotiate upwards)	125 MHz		0b1: 125 MHz		1
PCI Express 5 Gbps	100 MHz	Any PCIe	0b0: 100 MHz	2b01: 5.0 G	1
(can negotiate up to 5 Gbps)	125 MHz		0b1: 125 MHz		1
SATA (1.5 or 3 Gbps)	100 MHz	SATA	0b0: 100 MHz	Don't care	2
	125 MHz		0b1: 125 MHz		
Debug (2.5 Gbps)	100 MHz	Aurora @ 2.5 or 5 Gbps	0b0: 100 MHz	0b1: 2.5 G	-
	125 MHz		0b1: 125 MHz		-
Debug (5 Gbps)	100 MHz	Aurora @ 2.5 or 5 Gbps	0b0: 100 MHz	0b0: 5.0 G	-
	125 MHz		0b1: 125 MHz		-
Networking interfaces					
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0b0: 100 MHz	Don't care	-
	125 MHz	1000Base-KX @ 1.25 Gbps	0b1: 125 MHz		-
QSGMII (5.0 Gbps)	100 MHz	Any QSGMII	0b0: 100 MHz	0b0: 5.0 G	-
	125 MHz		0b1: 125 MHz		-
2.5G SGMII (3.125 Gbps)	125 MHz	SGMII @ 3.125 Gbps	0b0: 125 MHz	Don't care	-
XFI (10.3125 Gbps)	156.25 MHz	XFI @ 10.3125 Gbps	0b0: 156.25 MHz	Don't care	-

1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface, such as SATA, SGMII, QSGMII, 1000Base-KX, or Aurora is used concurrently on the same SerDes PLL, spread-spectrum clocking is not permitted.

2. SerDes lanes configured as SATA initially operate at 3.0 Gbps. A 1.5 Gbps operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rate.

5.19.3.8 eSDHC SDR mode clock select

The eSDHC SDR mode is asynchronous to the platform.

This table describes the clocking options that may be applied to the eSDHC SDR mode. The clock selection is determined by the binary value of the RCW Clocking Configuration field HWA_CGA_M1_CLK_SEL.

Table 41. eSDHC SDR mode clock select

Binary value of HWA_CGA_M1_CLK_SEL	eSDHC SDR mode frequency[1]
0b000	Reserved
0b001	Cluster group A PLL 1/1
0b010	Cluster group A PLL 1/2
0b011	Cluster group A PLL 1/3
0b100	Cluster group A PLL 1/4

Table continues on the next page...

Table 41. eSDHC SDR mode clock select (continued)

Binary value of HWA_CGA_M1_CLK_SEL	eSDHC SDR mode frequency[1]
0b101	Reserved

Notes:

1. For asynchronous mode max frequency, see the "Processor clocking specifications" table in the chip reference manual.
2. For SDR104 and HS200 modes, CGA1 PLL should be set to provide a minimum of 1200 MHz.
3. For SDR50 mode, cluster PLL should be set to provide a minimum of 600 MHz.

5.19.3.9 Frequency options

This section discusses interface frequency options.

5.19.3.9.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 42. SYSCLK and core cluster frequency options

Core cluster: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Core cluster Frequency (MHz)[1]				
6:1					
7:1					
8:1				1000	1067
9:1				1125	1200
10:1			1000	1250	1333
11:1			1100	1375	
12:1			1200		
13:1			1300		
14:1			1400		
15:1		1000			
16:1	1024	1067			
18:1	1152	1200			
20:1	1280	1333			
21:1	1344	1400			

Notes:

1. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. When using single source clocking, only 100 MHz input is available.

5.19.3.9.2 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 43. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Platform Frequency (MHz)[1]				
3:1			300	375	400
4:1	256	267	400		
5:1	320	333			
6:1	384	400			
7:1					
8:1					
9:1					

Notes:

1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).
2. When using single source clocking, only 100 MHz options are valid.

5.19.3.9.3 DDRCLK and DDR data rate frequency options

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 44. DDRCLK and DDR data rate frequency options

DDR data rate: DDRCLK Ratio	DDRCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	DDR Data Rate (MT/s)[1]				
8:1				1000	1066
10:1			1000	1250	1333
11:1			1100	1375	1465
12:1			1200	1500	1600
13:1			1300		
14:1			1400		
15:1		1000	1500		
16:1	1024	1067	1600		
20:1	1280	1333			
24:1	1536	1600			

Notes:

1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. When using single source clocking, only 100 MHz options are available.
3. The minimum frequency supported by DDR4 is 1250 MT/s.

5.19.3.9.4 SYSCLK and eSDHC high speed modes frequency options

These table shows the expected frequency options for SYSCLK and eSDHC high speed modes.

Table 45. SYSCLK and eSDHC high speed mode frequency options (clocked by CGA PLL1 / 1)

Core cluster: SYSCLK ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Resultant frequency (MHz)[1]				
9:1					1200
12:1			1200		
18:1	1152	1200			

Notes:

1. Resultant frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. For low speed operation, eSDHC is clocked from platform PLL and does not use CGA PLL.

5.19.3.9.5 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below:

1. The platform clock frequency must be equal to 400 MHz for PCI Express Gen 2.
2. For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 21. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 22. Gen 2 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

5.20 System control recommendations

5.20.1 System control pin termination recommendations

Table 46. System Control pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
PORESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power-up and power-down. It is an input-only pin and must be asserted to sample power-on configuration pins.		

Table continues on the next page...

Table 46. System Control pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
HRESET_B	I/O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to $O1V_{DD}$.		
RESET_REQ_B	O	Must not be pulled down during power-on reset.	This pin should be pulled high through a 2-10 kΩ resistor to $O1V_{DD}$ and must not be pulled down during power-on reset.	

NOTE

1. If on-board programming of NOR boot flash, NAND boot flash, SPI boot flash, or SD card is needed. Then an option should be kept (may be via a jumper) to keep PORESET_B and RESET_REQ_B disconnected from each other. Booting from a blank NOR, NAND, or SPI flash causes a pre-boot error, which causes assertion of RESET_REQ_B. When RESET_REQ_B is connected with PORESET_B, then the device goes into a recurring reset loop and does not provide enough time for JTAG to take control of the device and perform any operation.
2. For RCW override, RESET_REQ_B should be disconnected from PORESET_B or HRESET_B. An option on board is required.
3. HRESET_B from COP connector should be connected to PORESET_B of the chip as recommended in the JTAG connection diagram.
4. PORESET_B should be asserted zero during the JTAG boundary scan operation and is required to be controllable on board.
5. Use of PORESET_B is recommended. HRESET_B should be used for debug purposes only.
6. HRESET_B input must not be asserted during deep sleep mode.

5.21 JTAG recommendations

5.21.1 JTAG pin termination recommendations

Table 47. JTAG pin termination checklist

Signal name	I/O type	Used	Not used	Completed
TCK	I	Connect to pin 7 of the COP connector. This pin requires a 2-10 kΩ resistor to OV_{DD}.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}. This prevents TCK changing states and clocking data into the chip.	
TDI	I	This pin has a weak internal pull-up P-FET that is always enabled. Connect to pin 3 of the COP connector.	This pin may be left unconnected.	
TDO	O	Connect to pin 1 of the COP connector.	This pin may be left unconnected.	
TMS	I	This pin has a weak internal pull-up P-FET that is always enabled. Connect to pin 9 of the COP connector.	This pin may be left unconnected.	
TRST_B	I	Connect as shown in Figure 23.	TRST_B should be tied to PORESET_B through a 0 Ω resistor.	

5.21.2 JTAG system-level recommendations

Table 48. JTAG system-level checklist

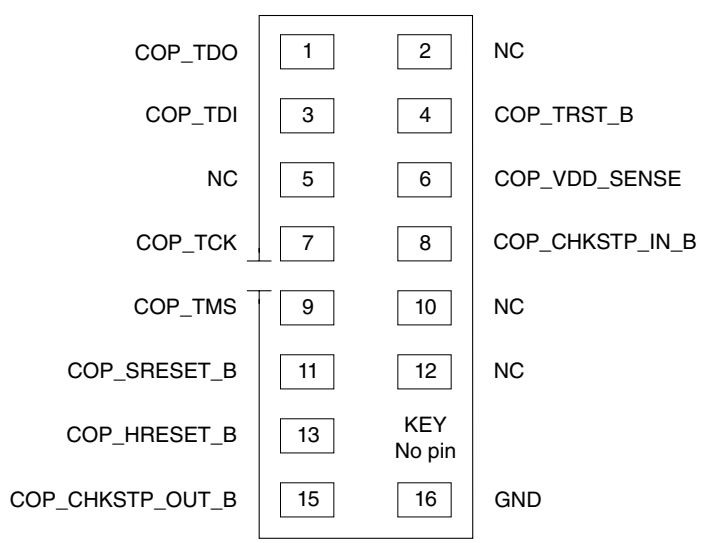
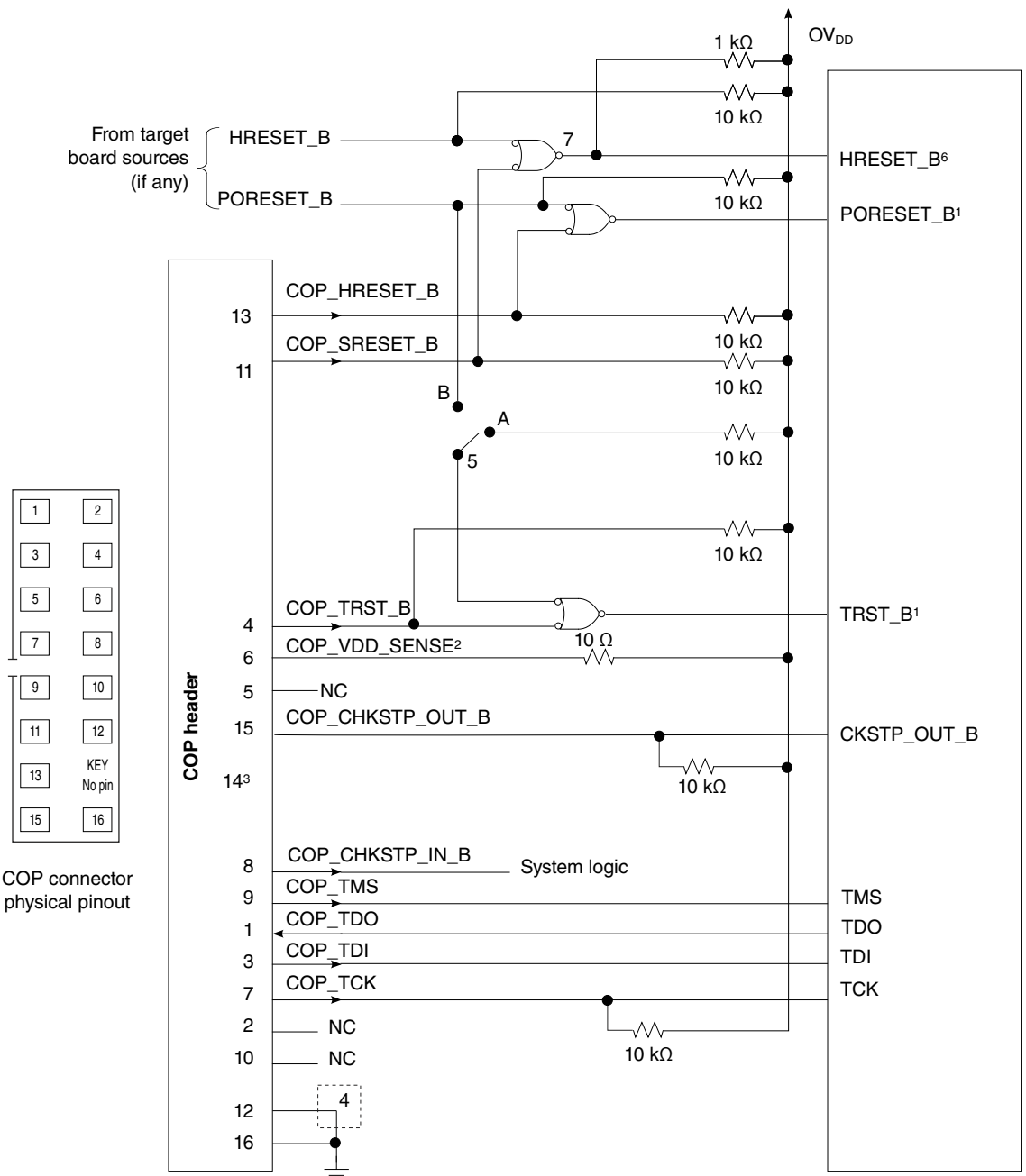
Item	Completed
COP signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 23. **NOTE:** These pins must be maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. **NOTE:** While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.	
Follow the arrangement shown in Figure 23 to allow the COP port to assert PORESET_B or TRST_B independently while ensuring that the target can drive PORESET_B, as well.	
The COP interface has a standard header, shown in the following figure, for connection to the target system and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key. There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in this figure is common to all known emulators.  	

Table 48. JTAG system-level checklist

Item	Completed
NOTE: The COP header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the COP header unpopulated until needed.	

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 23. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Notes:

1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.

3. The KEY location (pin 14) is not physically present on the COP header.

4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

6. Asserting HRESET_B causes a hard reset on the device

7. This is an open-drain output gate.

Figure 23. JTAG interface connection

6 Thermal recommendations

6.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

6.2 Thermal system-level recommendations

Proper thermal control design is primarily dependent on the system level design-the heat sink, airflow and thermal interface material.

Table 49. Thermal system-level checklist

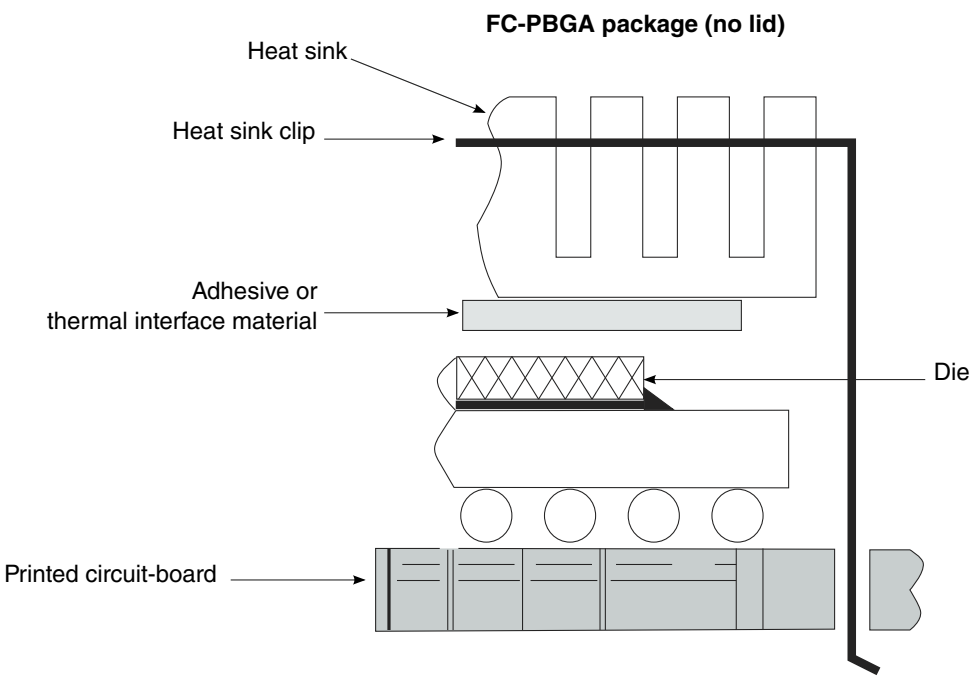
Item	Completed
Use the recommended thermal model. Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.	
Use this recommended board attachment method to the heat sink.[1] The processor heat sink must be connected to GND at one point for EMC performance. GND here specifies processor ground **FC-PBGA package (no lid)**  	
Ensure the heat sink is attached to the printed-circuit board with the spring force centered over the package.[2]	
Ensure the spring force does not exceed 15 pounds force (65 Newtons).	
A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance.[3]	

Table continues on the next page...

Table 49. Thermal system-level checklist (continued)

Item	Completed
Ensure the method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.	
A thermal simulation is required to determine the performance in the application.[4]	

1. The system board designer can choose among several types of commercially available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly and cost.
2. The performance of the thermal interface materials improves with increased contact pressure; the thermal interface vendor generally provides a performance characteristic to guide improved performance.
3. The system board designer can choose among several types of commercially available thermal interface materials.
4. A Flotherm model of the part is available.

6.3 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

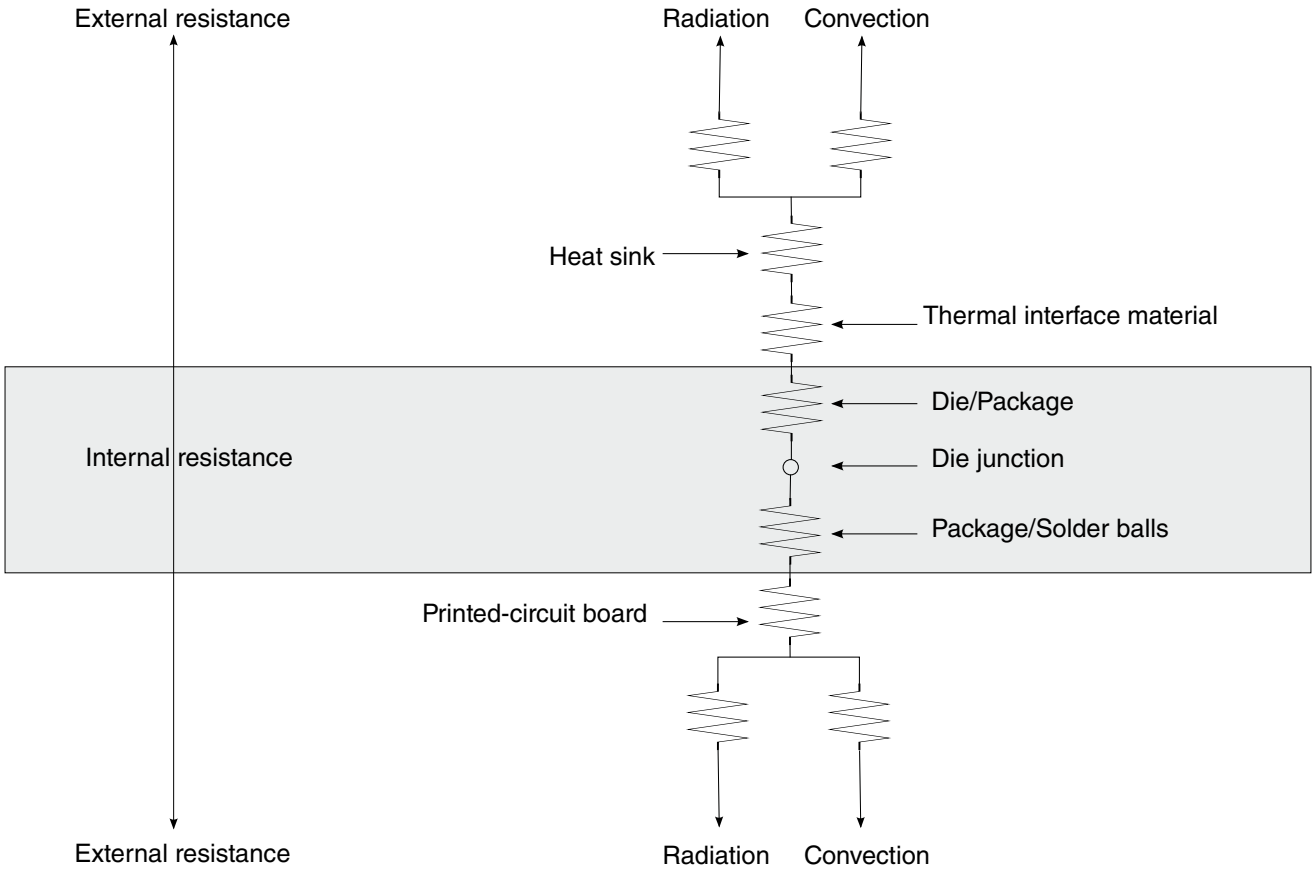


Figure 24. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

7 T1023 design recommendations

If you are using the T1023, the following sections provide necessary feature and other differences.

7.1 Introduction

The QorIQ T1023 advanced, multicore processor combines two, e5500 Power Architecture® processor cores with high-performance datapath acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and mil/aerospace applications.

This figure shows the major functional units within the T1023.

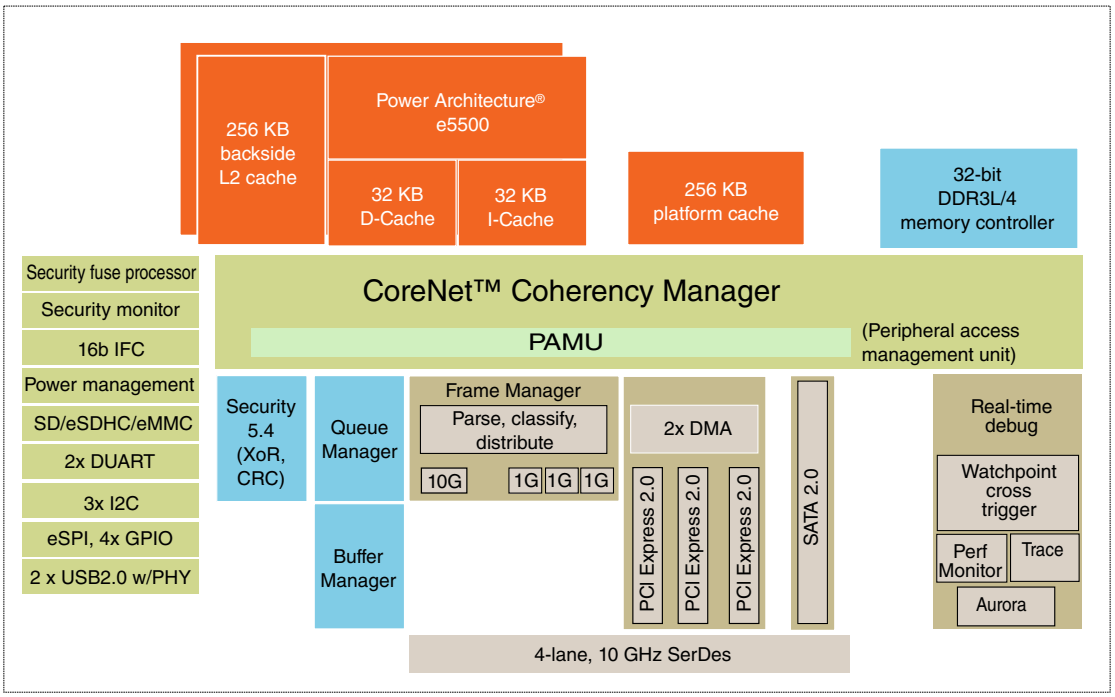


Figure 25. T1023 block diagram

This figure shows the major functional units within the T1013, which is a single core personality of the T1023.

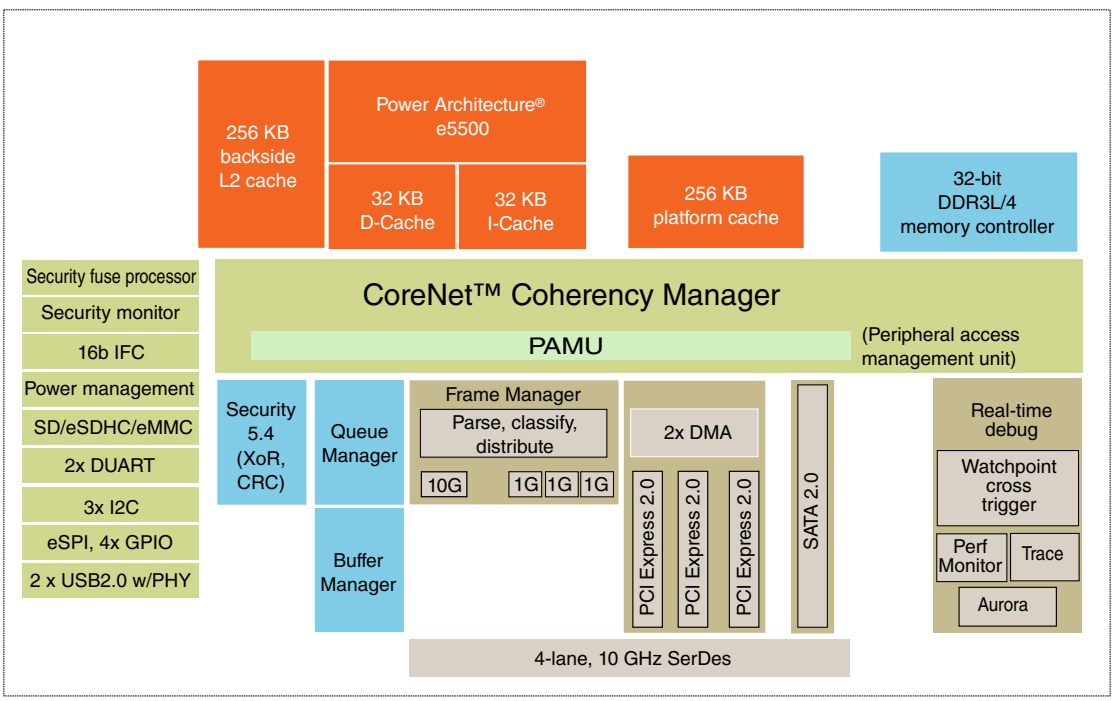


Figure 26. T1013 block diagram

This figure shows the major functional units within the T1014, which is single core personality of the T1024.

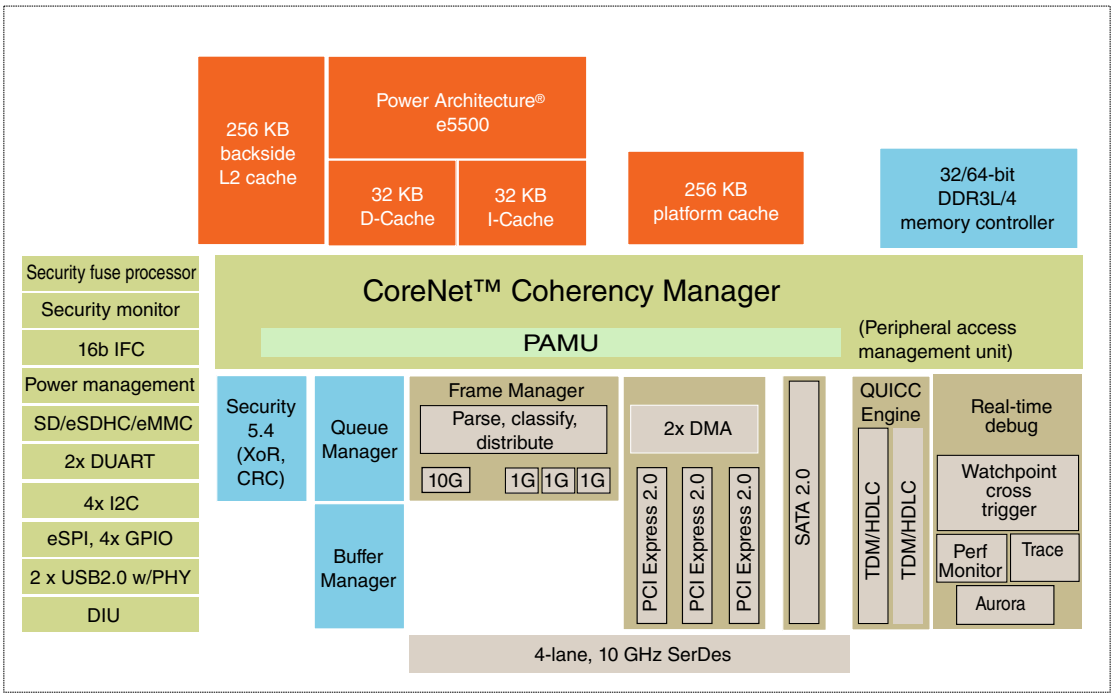


Figure 27. T1014 block diagram

7.2 Overview of differences

Table 50. Comparison between T1024, T1014, T1023 and T1013

Feature	T1024	T1014	T1023	T1013
Peripherals				
CPU	2 x e5500	1 x e5500	2 x e5500	1 x e5500
Ethernet interface options	1× 5 Gbps QSGMII 3x 2.5 Gbps SGMII 3x 1 Gbps SGMII 2x RGMII 1x XFI (10 GbE)	1× 5 Gbps QSGMII 3x 2.5 Gbps SGMII 3x 1 Gbps SGMII 2x RGMII 1x XFI (10 GbE)	1× 5 Gbps QSGMII 3x 2.5 Gbps SGMII 3x 1 Gbps SGMII 2x RGMII 1x XFI (10 GbE)	1× 5 Gbps QSGMII 3x 2.5 Gbps SGMII 3x 1 Gbps SGMII 2x RGMII 1x XFI (10 GbE)
DDR3L/DDR4	32-/64-bit, ECC[0:7]	32-/64-bit, ECC[0:7]	32-bit, ECC[0:3]	32-bit, ECC[0:3]
IFC	32-bit address bus	32-bit address bus	28-bit address bus GPCM mode is not supported.	28-bit address bus GPCM mode is not supported.
QE-TDM/HDLC	Supported	Supported	Not supported	Not supported
I^2C	4x I2C	4x I2C	3x I2C	3x I2C
DIU	Supported	Supported	Not supported	Not supported
Deep sleep	Supported	Supported	Not supported	Not supported
Package	23mm X 23mm, 0.8mm pitch, 780 pin FC-PBGA	23mm X 23mm, 0.8mm pitch, 780 pin FC-PBGA	19mm X 19mm, 0.8mm pitch, 525 pin FC-PBGA	19mm X 19mm, 0.8mm pitch, 525 pin FC-PBGA

NOTE

T1023 and T1013 IFC supports 28-bit address bus. For IFC connection, see the chip reference manual and erratum A-009138 in *T1024 Chip Errata*.

7.3 Pin termination differences

TEST_SEL_B needs to be differently terminated between 2 core and 1 core personalities. Please note that T1024 and T1023 are different personalities.

TEST_SEL_B	Termination
T1024/T1023	Pulled to $O1V_{DD}$ through a 100 Ω to 1 kΩ resistor
T1014/T1013	Terminate to GND

8 Revision history

This table summarizes changes to this document.

Table 52. Revision history

Revision	Date	Change

3	04/2018	• In Table 4, updated positive transient power as 1 V + 50 mv.
		• In Configuration signals sampled at reset , updated the note for hardcoded RCW values as RCW(0x9A, 0x9E).
		• In Table 19 :
		  • Updated the EC1 connection to FMAN-MAC4.
		  • Updated the EC2 connection to FMAN-MAC3.
		• In Table 25 :
		  • Updated Figure 8.
		  • Updated the voltage translator requirement for MMC card connections.
		  • Updated Figure 11.

2	12/2016	• In Table 3, removed the signal X1GND. • In Table 4, updated positive transient power as 1 V + 30 mv. • In Table 18, removed V6 and U6 balls reference and OVDD supply reference from TVDD voltage domain. • In Table 27, updated resistor value for USB_IBIAS_REXT as 10 kΩ +/-1%. • Added new section, SerDes system-level recommendations. • In Table 34, updated the core cluster group PLL minimum frequency as 1000 MHz and the minimum allowable core cluster frequency as 500 MHz. • In Table 42, updated the core cluster frequency options. • Template updated for NXP. • Replaced all "Freescale" instances to "NXP" in the content.
1	11/2015	• In the section Configuration signals sampled at reset , added note about the work around in case a new board is using a blank flash and flash is the source of RCW. • In DDR system-level recommendations, added the checklist item: Connect one of the ECC pins to the Prime DQ of ECC DRAM • In IFC pin termination recommendations corrected the bit listing of the IFC-A signal.
0	07/2015	Initial public release

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