ETHERNET–

MDIO Accesses Including Internal SGMII TBI, SGMII PCS, QSGMII PCS, and XFI PCS

For QorIQ Product Families – P-series, T-series, and LS-Series

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SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- Overview
- MII Management (Internal & External Support)
  - Internal: TBI (eTSEC/dTSEC)
  - Internal: PCS (mEMAC)
  - External (1st MAC or Dedicated)
- LS1043ARDB Example – Clause 22
  - Internal (QSGMII PCS, Port 0)
  - External (RGMII PHY, QSGMII PHY)
- LS1043ARDB Example – Clause 45
  - Internal (XFI PCS)
  - External (Aquantia AQRate PHY – AQR105)
- Request: SDK Support For Internal PCS Registers
- Summary / Conclusion

Overview – Ethernet Data Controllers

The NXP QorIQ product families support the Ethernet protocol with a variety of controllers for the data path and the PCS/PHY management path. Parallel data interfaces are MII, RMII, GMII, and RGMII. Serial data interfaces are SGMII, QSGMII, XAUI, and XFI.

For the P-series, the main Ethernet controllers are eTSEC 1.x/2.x, DPAA1-FMAN-dTSEC, and DPAA1-FMAN-10GEC.

For the T-series, the main Ethernet controller is DPAA1-FMAN-mEMAC.

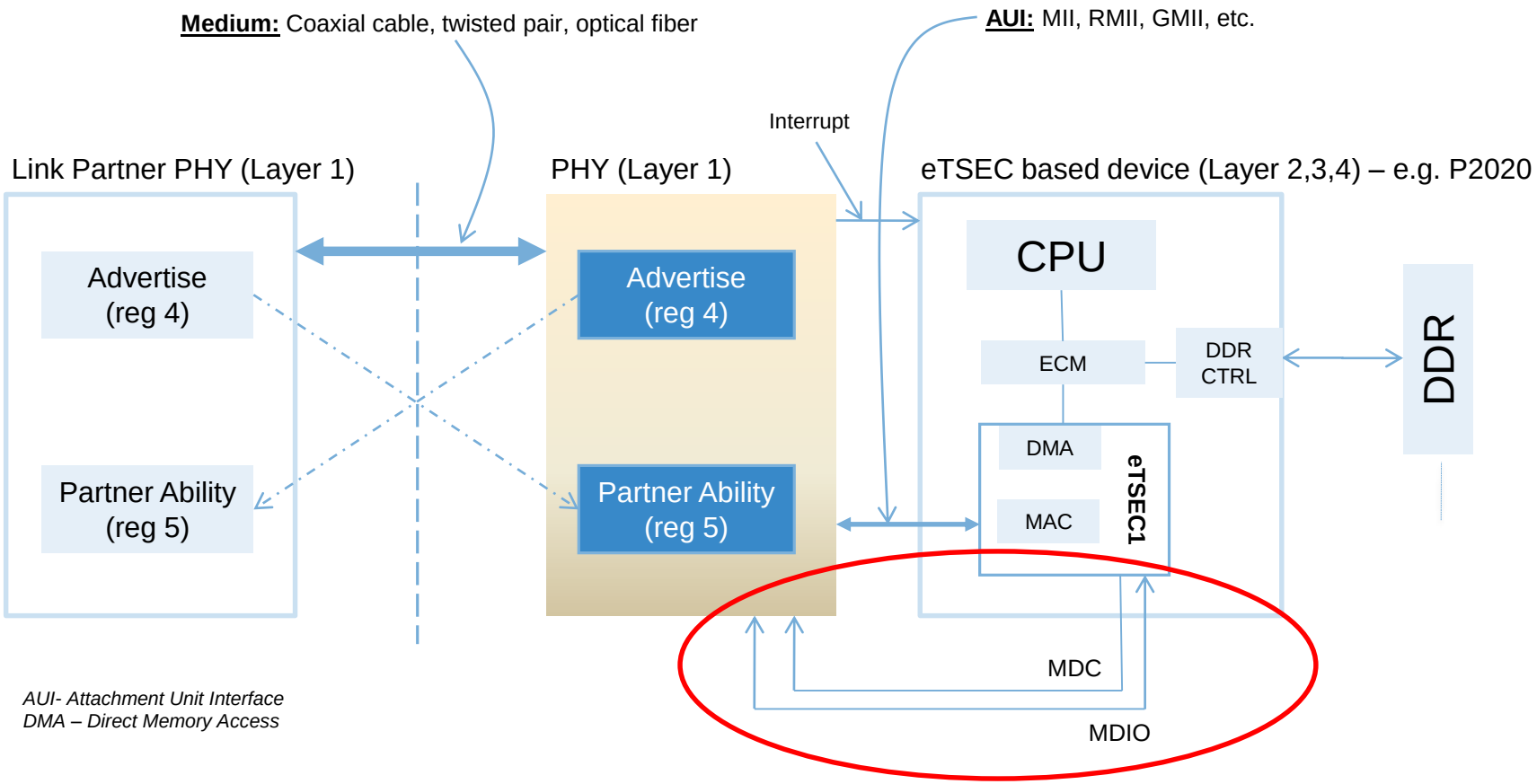
For the LS-series, the main Ethernet controllers are eTSEC 2.x, PPFE, DPAA1-FMAN-mEMAC, and DPAA2-WRIOP-mEMAC.

Overview – Ethernet Management Controllers

Ethernet management controllers support IEEE 802.3 Clause 22 and Clause 45. External PHY registers are accessed via eTSEC1, EMI1 and EMI2. Internal TBI and PCS registers are accessed via registers in the associated Ethernet Data Controller.

Clause 22 has been associated with 10/100/1000Mbps PHYs and Clause 45 with 10GBps PHYs but this is not a hard restriction. The Aquantia PHYs support 10G/5G/2.5G/1G/100M and use the Clause 45 MDIO register set. Our 4-Port Gigabit Ethernet Copper PHY [*F104S8A*] supports Clause 45 for the Energy Efficient Ethernet (EEE) registers but Clause 22 for all other registers.

Overview - MDC/MDIO Bus



MII Management –

Supported Serial Interfaces with Internal MII Mgmt Registers (1 of 2)

- **SGMII TBI (*DPAA Reference Manual*)**
  - Clause 22
  - MAC: eTSEC/dTSEC
  - TBIPA defines the PHY address for Clause 22 accesses
  - MIIMCOM, MIIMADD, MIIMCON, MIIMSTAT used to perform read/writes
  - e.g., TBICON is at register address 0x11

- **SGMII PCS**
  - Clause 22; Clause 45 for 1000Base-KX mode (device address = 0x03)
  - MAC: mEMAC
  - SGMIInCR1[MDEV_PORT] defines the PHY address for Clause 22 accesses and the PORT address for Clause 45 accesses. (***SoC Reference Manual***)
  - MDIO_CTL & MDIO_DATA used to perform reads/writes (***DPAA Reference Manual***)
  - e.g., MDIO_SGMII_SR is at register address 0x1; MDIO_SGMII_SR is at register 0x8001 for 1000Base-KX

MII Management –

Supported Serial Interfaces with Internal MII Mgmt Registers (2 of 2)

- **QSGMII PCS**
  - Clause 22
  - QSGMIInCR1[MDEV_PORT] defines the internal PHY address (upper 3 bits of MDIO_CTL[PHY addr]) and the QSGMII port address (lower 2 bits of MDIO_CTL[PHY addr]) for Clause 22 accesses to each of the four QSGMII ports. (***SoC Reference Manual***)
  - MDIO_CTL & MDIO_DATA used to perform reads/writes (***DPAA Reference Manual***)
  - e.g., QSGMII_SR is at register address 0x1 (ports 0,1,2,3)

- **XFI PCS**
  - Clause 45 (including 10GBASE-KR)
  - XFInCR1[MDEV_PORT] defines the PORT address for Clause 45 accesses. (***SoC Reference Manual***)
  - MDIO_CTL & MDIO_DATA used to perform reads/writes (***DPAA Reference Manual***)
  - e.g., MDIO_XFI_PCS_SR1 is at register address 0x1 (device address = 0x3); MDIO_XFI_10GKR_PMD_SR is at register address 0x97 (device address =0x1)

MII Management –

Interfaces by Controller (*Internal* and External)

TBI / *PCS* / EMI1 (Clause 22)

- Typically 3.3v, 2.5v or 1.8v
- PHY addr & REG addr
- eTSEC
  - Internal: TBI per MAC
  - External: Normally 1st MAC pins are routed externally
- DPAA1-FMAN-dTSEC/mEMAC
  - Internal: TBI or PCS per MAC
  - External: Dedicated (not MAC dependent)
- DPAA2-WRIOP-mEMAC
  - Internal: PCS per MAC
  - External: Dedicated (not MAC dependent)

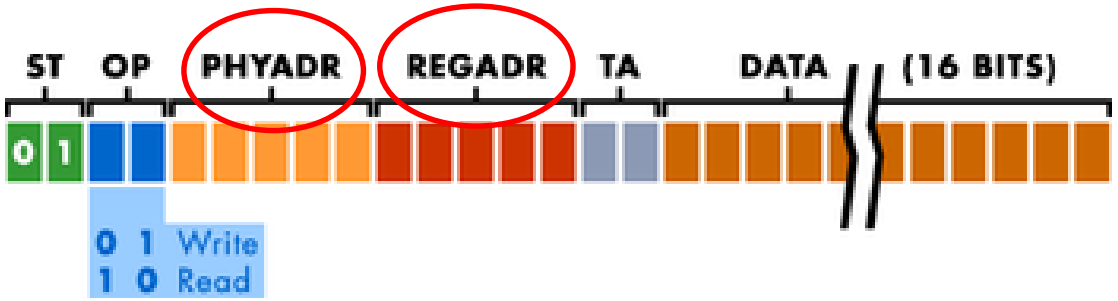
PCS / EMI2 (Clause 45)

- Typically 1.2v or 1.8v
- PORT addr, DEV addr, & REG addr
- DPAA1-FMAN-10GEC/mEMAC
  - Internal: PCS per MAC
  - External: Dedicated (not MAC dependent)
- DPAA2-WRIOP-mEMAC
  - Internal: PCS per MAC
  - External: Dedicated (not MAC dependent)

MII Management - Clause 22

Clause 22 defines the MDIO communication basic frame format which is composed of the following elements:

The frame format only allows a 5-bit number for both the PHY address and the register address, which limits the number of MMDs that the STA can interface. Additionally, Clause 22 MDIO only supports 5V tolerant devices and does not have a low voltage option.



ST	2 bits	Start of Frame (01 for Clause 22)
OP	2 bits	OP Code
PHYADR	5 bits	PHY Address
REGADR	5 bits	Register Address
TA	2 bits	Turnaround time to change bus ownership from STA to MMD if required
DATA	16 bits	Data Driven by STA during write Driven by MMD during read

MII Management - Clause 22 Internal PCS Register Set

MDIO memory map

Offset address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	SGMII Control (MDIO_SGMII_CR)	16	R/W	1140h	31.5.4.1/ 1822
1	SGMII Status (MDIO_SGMII_SR)	16	R	0009h	31.5.4.2/ 1824
2	SGMII PHY Identifier Upper (MDIO_SGMII_PHY_ID_H)	16	R	0083h	31.5.4.3/ 1825
3	SGMII PHY Identifier Lower (MDIO_SGMII_PHY_ID_L)	16	R	E400h	31.5.4.4/ 1826
4	SGMII Device Ability for SGMII (MDIO_SGMII_DEV_ABIL_SGMII)	16	R/W	01A0h	31.5.4.5/ 1826
5	SGMII Partner Ability for SGMII (MDIO_SGMII_LP_DEV_ABIL_SGMII)	16	R	0000h	31.5.4.6/ 1827
6	SGMII AN Expansion (MDIO_SGMII_AN_EXP)	16	R	0004h	31.5.4.7/ 1828
7	SGMII Next Page Transmit (MDIO_SGMII_NP_TX)	16	R/W	0000h	31.5.4.8/ 1829
8	SGMII LP Next Page Receive (MDIO_SGMII_NP_RX)	16	R	0000h	31.5.4.9/ 1830
F	SGMII Extended Status (MDIO_SGMII_XTND_STAT)	16	R	0000h	31.5.4.10/ 1831
10	SGMII Scratch (MDIO_SGMII_SCRATCH)	16	R/W	0000h	31.5.4.11/ 1831
11	SGMII Design Revision (MDIO_SGMII_REV)	16	R	0001h	31.5.4.12/ 1832
12	SGMII Link Timer Lower (MDIO_SGMII_LINK_TMR_L)	16	R/W	12D0h	31.5.4.13/ 1832
13	SGMII Link Timer Upper (MDIO_SGMII_LINK_TMR_H)	16	R/W	0013h	31.5.4.14/ 1833
14	SGMII IF Mode (MDIO_SGMII_IF_MODE)	16	R/W	0000h	31.5.4.15/ 1833

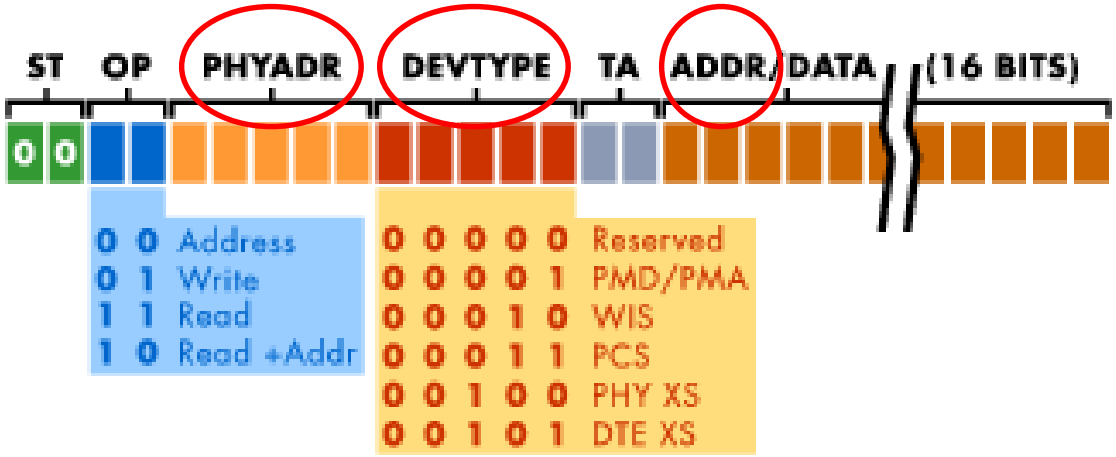
MII Management – PCS Link Status (register 0x1)

32.6.14.3 Diagram

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ST_100BASET4	FD_100BASEX	HD_100BASEX	FD_10MBPS	HD_10MBPS	FD_100BASET2	HD_100BASET2	EXT_STAT			AN_COMP	REM_FAULT	AN_ABIL	LINK_STAT	JAB_DET	EXT_CAP
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

MII Management - Clause 45

In order to address the deficiencies of Clause 22, Clause 45 was added to the 802.3 specification. Clause 45 added support for low voltage devices down to 1.2V and extended the frame format to provide access to many more devices and registers. Some of the elements of the extended frame are similar to the basic data frame:



ST	2 bits	Start of Frame (00 for Clause 45)
OP	2 bits	OP Code
PHYADR	5 bits	PHY Address
DEVTYPE	5 bits	Device Type
TA	2 bits	Turnaround time to change bus ownership from STA to MMD if required
ADDR/DATA	16 bits	Address or Data Driven by STA for address Driven by STA during write Driven by MMD during read Driven by MMD during read-increment-address

MII Management - Clause 45 Internal PCS Register Set

19.5.2 XFI PCS MDIO Memory Map/Register Definition

The XFI PCS register space is selected when the associated XFInCR1[MDEV_PORT] matches the Ethernet MAC port address (MDIO_CTL[PORT_ADDR]) and the device address (MDIO_CTL[DEV_ADDR]) is 03h.

MDIO memory map

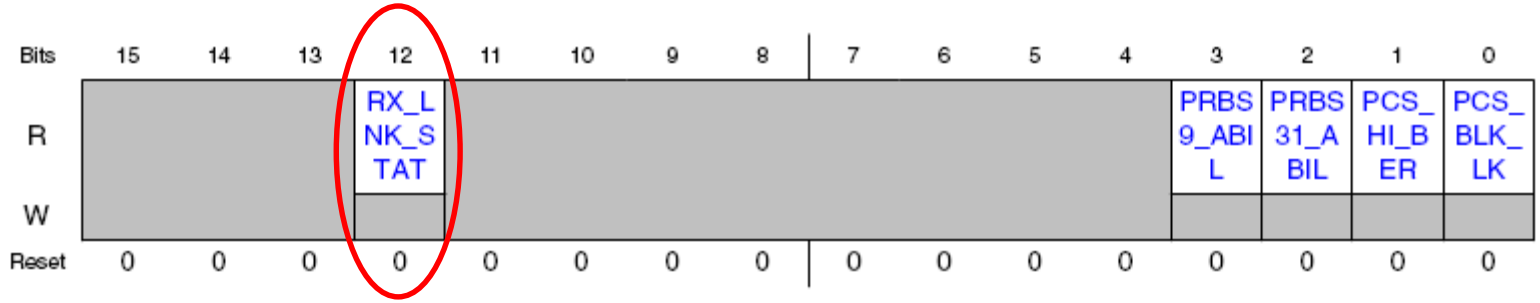
Offset address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	XFI PCS Control 1 (MDIO_XFI_PCS_CR1)	16	R/W	2000h	19.5.2.1/ 1323
1	XFI PCS Status 1 (MDIO_XFI_PCS_SR1)	16	R	0002h	19.5.2.2/ 1324
2	XFI PCS Device Identifier Upper (MDIO_XFI_PCS_DEV_ID_H)	16	R	0083h	19.5.2.3/ 1326
3	XFI PCS Device Identifier Lower (MDIO_XFI_PCS_DEV_ID_L)	16	R	E400h	19.5.2.4/ 1326
4	XFI PCS Speed Ability (MDIO_XFI_PCS_SPEED_ABIL)	16	R	0001h	19.5.2.5/ 1327
5	XFI PCS Devices In Package 0 (MDIO_XFI_PCS_DEV_PRES0)	16	R	008Ah	19.5.2.6/ 1328
6	XFI PCS Devices in Package 1 (MDIO_XFI_PCS_DEV_PRES1)	16	R	0000h	19.5.2.7/ 1329
7	XFI 10G PCS Control 2 (MDIO_XFI_PCS_CR2)	16	R	000Bh	19.5.2.8/ 1330
8	XFI 10G PCS Status 2 (MDIO_XFI_PCS_SR2)	16	R	8001h	19.5.2.9/ 1330
E	XFI PCS Package Identifier Upper (MDIO_XFI_PCS_PKG_ID_H)	16	R	0083h	19.5.2.10/ 1331

MII Management – PCS link Status (register 0x3.0x20)

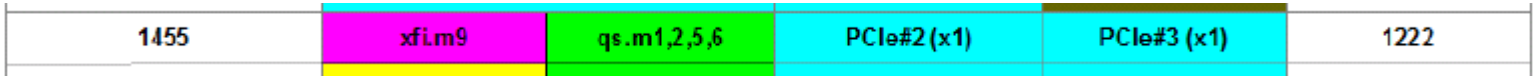
32.6.104.2 Function

The XFI 10GBASE-R PCS Status 1 Register contains 10GBase-R PCS status.

32.6.104.3 Diagram



Examples: LS1043ARDB - Using SERDES1 Protocol: 5205 (0x1455)



- Check what PHYs are recognized by the external MDIO controllers from the u-boot prompt

⇒*mdio list*

FSL_MDIO0:

1 - RealTek RTL8211F <--> FM1@DTSEC3 **RGMII, MAC3*

2 - RealTek RTL8211F <--> FM1@DTSEC4

4 - Vitesse VSC8514 <--> FM1@DTSEC1 **QSGMII, Port 0, MAC1, lane B*

5 - Vitesse VSC8514 <--> FM1@DTSEC2

6 - Vitesse VSC8514 <--> FM1@DTSEC5

7 - Vitesse VSC8514 <--> FM1@DTSEC6

FM_TGEC_MDIO:

1 - Aquantia AQR105 <--> FM1@TGEC1 **AQRate PHY, XFI, MAC9, lane A *

Examples: LS1043ARDB - Using SERDES1 Protocol: 5205 (0x1455) [external]

- FSL_MDIO0 equates to EMI1, Clause 22 bus-RGMII PHY

=> mdio read FM1@DTSEC3 1

Reading from bus FSL_MDIO0

PHY at address 1:

*1 - 0x79a**d***

=> mdio read 1 1

1 is not a known ethernet

Reading from bus FSL_MDIO0

PHY at address 1:

*1 - 0x79a**d***

- FM_TGEC_MDIO equates to EMI2, Clause 45 bus-AQ PHY

=> mdio read FM1@TGEC1 0x1e.0x20

Reading from bus FM_TGEC_MDIO

PHY at address 1:

30.32 - 0x200

=> mdio read FM1@TGEC1 0x1e.0xc885

Reading from bus FM_TGEC_MDIO

PHY at address 1:

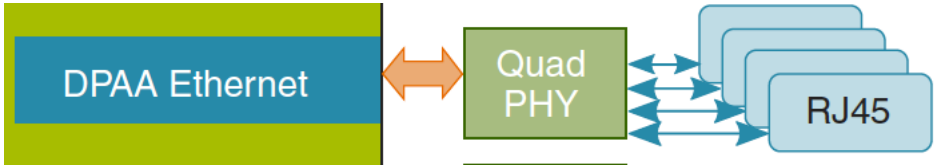
30.51333 - 0xb9

Examples: LS1043ARDB - Using SERDES1 Protocol: 5205 (0x1455) [external]

- FSL_MDIO0 equates to EMI1, Clause 22 bus-QSGMII PHY

=> mdio read FM1@DTSEC1 1
Reading from bus FSL_MDIO0
PHY at address 4:
*1 - 0x796**d***

=> mdio read 4 1
4 is not a known ethernet
Reading from bus FSL_MDIO0
PHY at address 4:
*1 - 0x796**d***



Examples: LS1043ARDB - Using SERDES1 Protocol: 5205 (0x1455) [internal]

- **QSGMII PCS-P0 = FM1.MAC1**
- QSGMII PCS-P1 = FM1.MAC2
- QSGMII PCS-P2 = FM1.MAC5
- QSGMII PCS-P3 = FM1.MAC6

Check PCS Link status (register 1)
FMAN offset = 0x0_01A0_0000
MDIO-1 offset in FMAN = 0xE_1000
(little endian)

=> mm 01ae1034
01ae1034: 00000000 ? 01800000
01ae1038: 29000000 ? x
=> mm 01ae1034
01ae1034: 01000000 ? 01800000
*01ae1038: **2d**000000 ? x*

- **XFI PCS = FM1.MAC9**

Check PCS Link Status (register 0x3.0x20)
FMAN offset = 0x0_01A0_0000
MDIO-9 offset in FMAN = 0xF_1000
(little endian)

=> mm 01af103c
*01af103c: 40200000 ? **20**000000*
01af1040: 00000000 ? x
=> mm 01af1034
*01af1034: 03000000 ? **0380**0000*
*01af1038: 01**1**00000 ? x*

Summary / Conclusion

- **Clause 22 reads and writes require two parameters: PHY ADDR & REG ADDR**
- **Clause 45 reads and writes require three parameters: PHY ADDR, DEV ADDR, and REG ADDR**
- In U-boot, ‘mdio’ command supports using EMI1 and EMI2 to communicate with external PHYs
- Ethernet Data Controller IP determines MDIO Controller used
  - *Internal* and External connections
    - eTSEC (*TBI* – Clause 22)
    - DPAA1-FMAN-dTSEC (*TBI* – Clause22)
    - DPAA1-FMAN-10GEC (external only Clause 45)
    - DPAA1-FMAN-mEMAC (*Q/SGMII PCS*-Clause 22; *XFI PCS*-Clause 45)
    - DPAA2-WRIOP-mEMAC (*Q/SGMII PCS*-Clause 22; *XFI PCS*-Clause 45)

Summary / Conclusion (cont.)

- mEMAC based devices added link info registers for RGMII interface
  - e.g., See IF_MODE and IF_STATUS in T2080 DPAA RM
- Consult Datasheet/Bring-Up Guide/Design Checklist to confirm if pins are open-drain
- Consult Bring-Up Guide for unused pin termination recommendations
- Some connected devices (e.g., SFP modules) also support the I2C bus in addition to (or in lieu of) the MDIO bus
- Internal PCS Link Status should follow the live link (reception of valid symbols should set link status bit)
  - e.g., unplug cable or power down lane ***should*** clear link bit

MDIO timings can be tweaked on mEMAC based devices with MDIO_CFG. See DPAA RM.

6.4.3.4.1 MDIO Configuration Register (MDIO_CFG)

MDIO interrupt is enabled by bit 2.

Offset 0x030 Access: Mixed

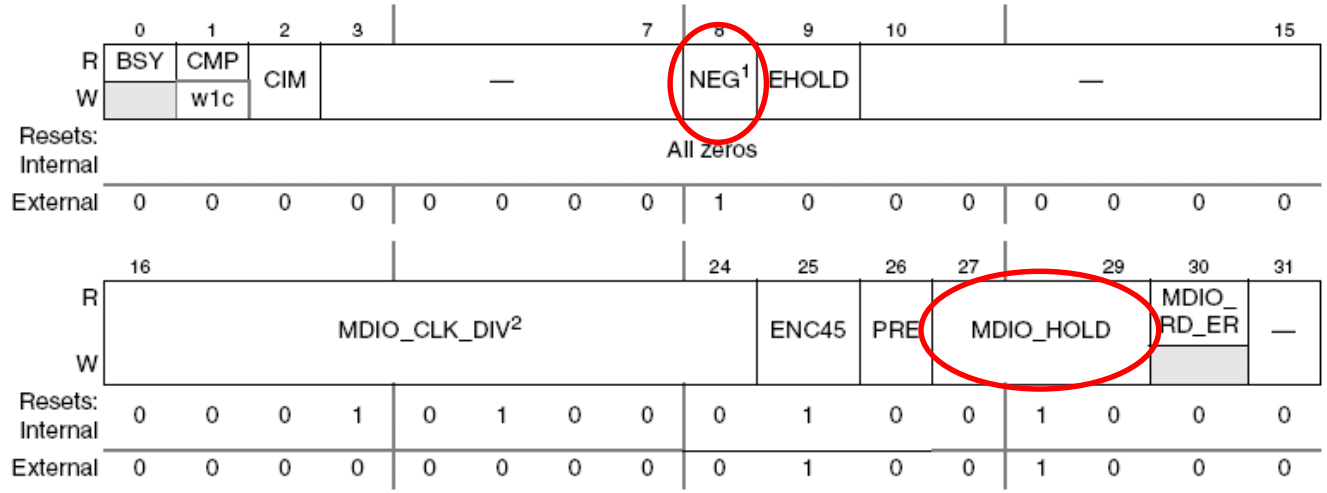


Figure 6-92. MDIO_CFG Register Definition

1 Reset value of NEG for external MDIOs is 1

2 Reset value of MDIO_CLK_DIV for external MDIOs is 9'b0

XAUI does not have accessible MII registers.

bit #1 (ALG) - Lane Alignment Status. Asserted to indicate that the lanes are correctly synchronized, negated when the lane synchronization is lost or not acquired.

For the first 10GEC, the offset is CCSRBAR+0xE_A250
For the second 10GEC, the offset is CCSRBAR+0xE_A260 (for devices like P4080).

The last nibble should be 0xF. A bit for each lane to reflect if the sync status.
bit #28 for first XAUI lane...bit #31 for last XAUI lane.

If for any reason bit #1 and bits #28-31 are not set, then the XAUI lane is not synchronized.

Currently Switching between 1G SGMII and 2.5G SGMII on the same SerDes lane requires a RCW change and device reboot

The Aquantia AQRate PHYs with XFI interface is a simpler solution because our MAC only needs to enable Flow Control. The PHY sends PAUSE control fames to the MAC to regulate the data rate.

GLOSSARY

RDB –	Reference Design Board
SDK –	Software Development Kit
PHY –	Physical Transceiver
PCS –	Physical Coding Sublayer
TBI –	Ten Bit Interface
MDIO –	Management Data Input/Output
EMI –	Ethernet management Interface
eTSEC –	Enhanced Three Speed Ethernet Controller
mEMAC –	Multirate Ethernet MAC
FMAN –	Frame Manager
WRIOP –	Wire Rate I/O Processor
DPAA –	Data Path Acceleration Architecture
MII –	Media-Independent Interface
RGMII –	Reduced Gigabit MII
SGMII –	Serial Gigabit MII (x1 @1.25Gbps/3.125Gbps)
QSGMII –	Quad SGMII (x1 @ 5Gbps)
XAUI (8b/10b) –	“Zowie”, X=10, AUI=Attachment Unit Interface
	IEEE 802.3, 10G (x4 lanes @ 3.125Gbps ea.)
XFI (64b/66b) –	“Ziffy” or “X.F.I.”, XFP module interface
	XFP MSA Group, 10G (x1 @ 10.3125Gbps)

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