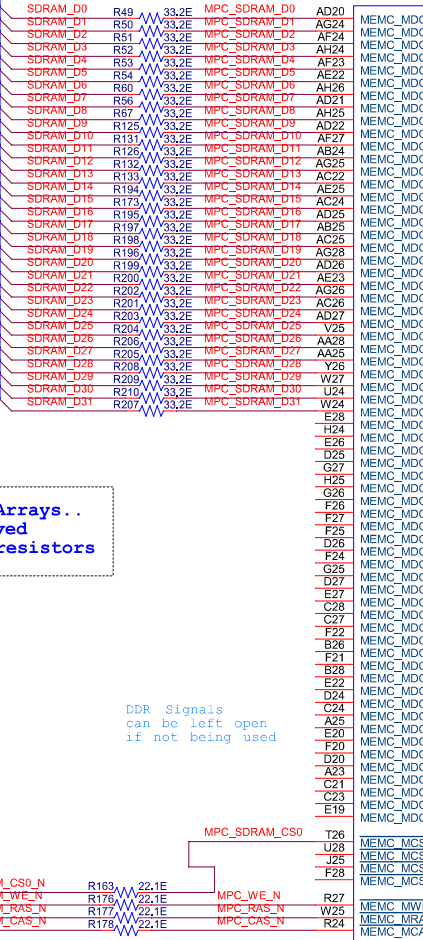


[14] SDRAM_D[31:0]

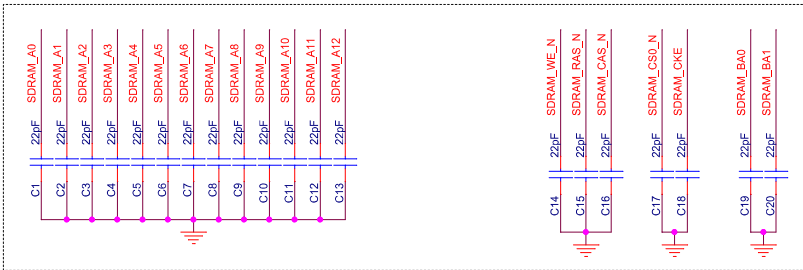
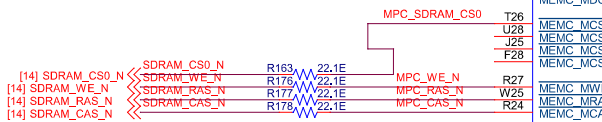


DDR SDRAM MEMORY CONTROLLER

Changed in Rev 4.0

Series termination provided through Resistor Arrays.. namely...RN17 to RN25, RN28 to RN30 are removed & termination is provided through individual resistors

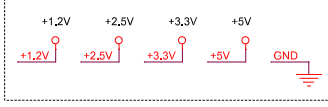
DDR Signals can be left open if not being used



22.1E series termination added to the CLK_P & CLK_N outputs from the Processor

Changed in Rev 4.0

Only for DDR 2 can be left open if config as DDR 1



Designed By		CSKB, ATS
Checked By		KPL, ATS
Verified By		CSS, ATS
		AM, ADE
Approved By		SKS, ADE
		JKK, CEMILAC
	SIGN	DATE
		NAME

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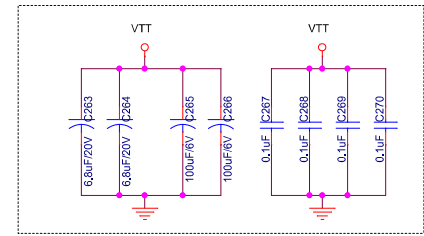
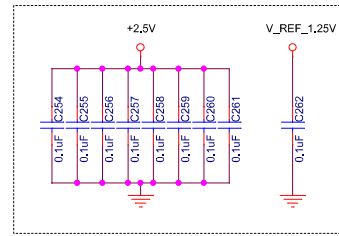
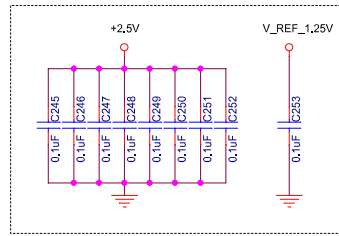
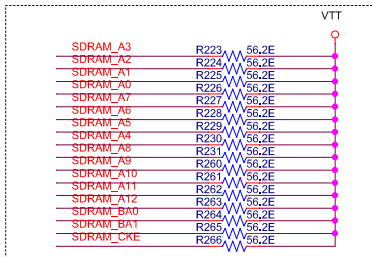
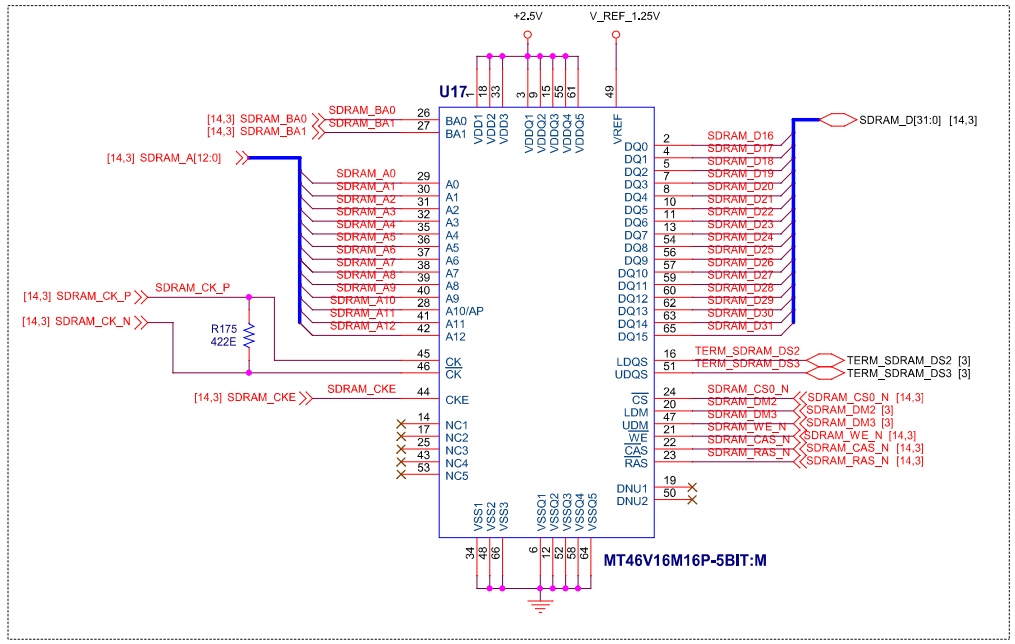
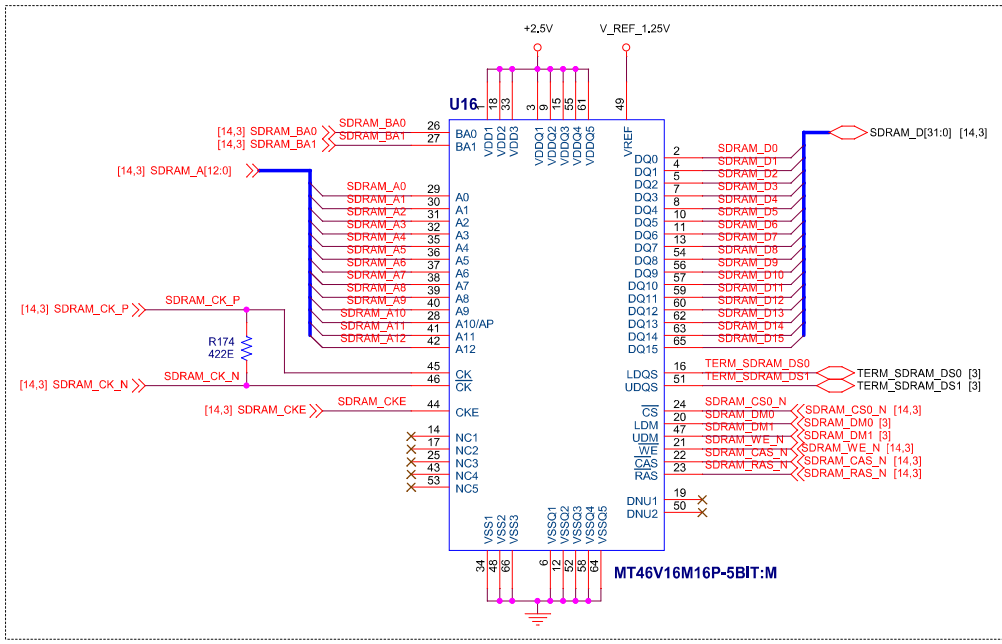
RII - AED PROCESSOR CARD_MPC8358 DDR MEMORY

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ATS-AED-PROC SCH-001

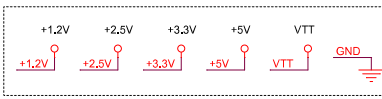
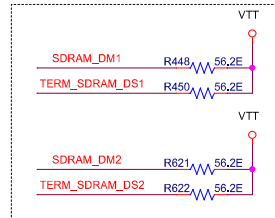
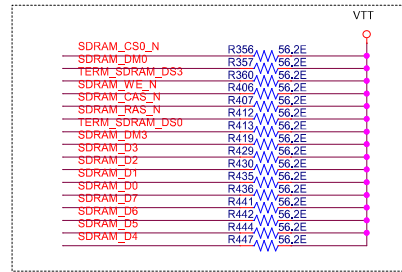
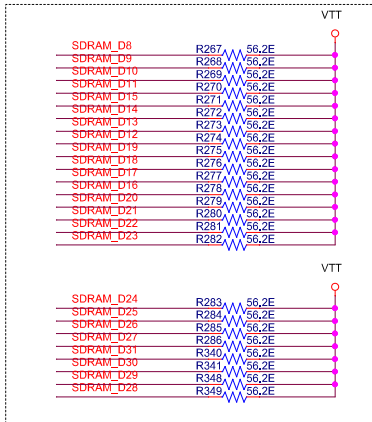
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Rev 4.0



Changed in Rev 4.0

Series termination provided through Resistor Arrays.. namely.. RN31 to RN44 are removed & termination is provided through individual resistors



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		SKS, ADE
		JKK, CEMILAC
	SIGN	DATE
		NAME

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R11 - AED PROCESSOR CARD_SDRAM INTERFACE
 Size A3 Document Number **ATS-AED-PROC SCH-001** Rev 4.0
 Date: Wednesday, June 17, 2020 Sheet 14 of 44