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PCI Express PHY PCB Layout Guideline

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Document information

Info	Content
Keywords	pcb, layout, symmetry, loss, jitter
Abstract	This document provides a practical guideline for incorporating the PCI Express PHY IC layout into the PCB design.

PHILIPS

Revision history

Rev	Date	Description
01	20050430	First release

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1. Introduction

This document provides a practical guideline for incorporating the Philips Peripheral Component Interconnect (PCI) Express Physical (PHY) IC layout into a Printed Circuit Board (PCB) design.

This document is composed of two main sections:

- Section 2 provides guidelines for PCI Express lane connection for the PCB traces, vias and AC coupling capacitors, as well as add-in card edge finger considerations. This section is based on Intel's guidelines [1], [2] and PCI-SIG recommendations [3].
- Section 3 describes the layout and termination of PXPIPE, which is Philips' proposed interface between the PHY and the Media Access Control (MAC).

2. PCI Express interconnection

PCI Express is a dual simplex point-to-point serial differential low-voltage interconnection. Each lane consists of two pairs of differential signals: transmit pair TXP/TXN, and receive pair RXP/RXN. The signals are 2.5 GHz with an embedded clock.

The embedded clock simplifies routing rules by removing the length matching requirements between the differential pairs.

The increased bit rate for PCI Express requires some specific design. Minimizing interconnect loss and jitter are the key requirements.

2.1 PCB stackup and reference planes

PCI Express requires no new technology. Generally desktop system boards are designed with 4-layer stackup, whereas server, workstation, and mobile system boards use 6-layer stackup or greater. Add-in cards may use either 4-layer or 6-layer stackup. ½ oz copper plated microstrip and 1 oz copper stripline are used.

An add-in card is required to have overall board thickness of 0.062 inches. A mobile platform can have a thickness of 0.062 inches or 0.050 inches.

To minimize loss and jitter, the most important considerations are to design to a target impedance and to keep tolerances small. Thicker dielectrics and wider traces will minimize loss. Microstrip differential traces produce greater impedance variation than stripline traces.

A signal pair should avoid discontinuities in the reference plane, such as splits and voids. When a signal changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split.

2.2 Traces

2.2.1 Impedance

PCI Express link traces must maintain 100 Ω differential / 60 Ω single-ended impedance for 4-layer or 6-layer boards; and 85 Ω differential / 55 Ω single-ended impedance for 8-layer or 10-layer boards.

2.2.2 Width and spacing

Coupling of the intra-pair differential signals and increased spacing to neighboring signals help to minimize harmful crosstalk impacts and Electro-Magnetic Interference

(EMI) effects. In the microstrip case, a differential trace should be 5 mils wide, with a 7 mil wide air gap spacing between the two traces of a pair. Any uncoupled sections whose intra-pair space exceeds 7 mils can be routed as a 7 mil wide trace, if the section is 100 mils or longer. In the stripline case, a differential trace should be 5 mils wide with a 5 mil wide gap between the two traces of a pair.

The spacing between pairs and to all non-PCI Express signals should be 20 mils or four times the dielectric height, whichever is greater. If the non-PCI Express signals have significantly higher voltage levels or edge rate than the PCI Express signal, the space should increase to 30 mils in order to avoid coupling.

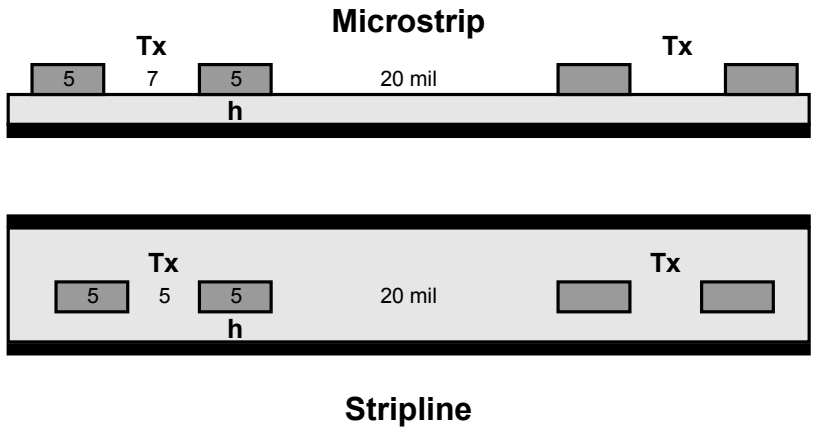

Fig 1. Trace width and spacing

2.2.3 Length and length matching

Trace length greatly affects the loss and jitter budgets of the interconnection. The PCB trace may introduce 1 ps to 5 ps of jitter and 0.35 dB to 0.50 dB of loss per inch.

For an add-in card, the trace length from the edge finger to the Philips PCI Express PHY pads should be limited to 4 inches. For the system board, the trace length is recommended to be less than 12 inches.

Long distance traces should be routed at an off-angle to the X-Y axis of a PCB layer, in order to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric.

The two traces of a pair should be symmetrically routed.

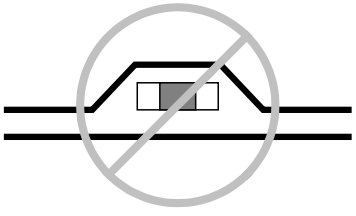

Fig 2. Nonsymmetrical routing should be avoided

The length difference between a differential pair should be limited to 5 mils maximum. Length matching is required per segment, and any length added (typically a “serpentine” section) for the sake of matching a pair should be added near the location where the mismatch occurs.

There is no length match requirement between transmit and receive pairs.

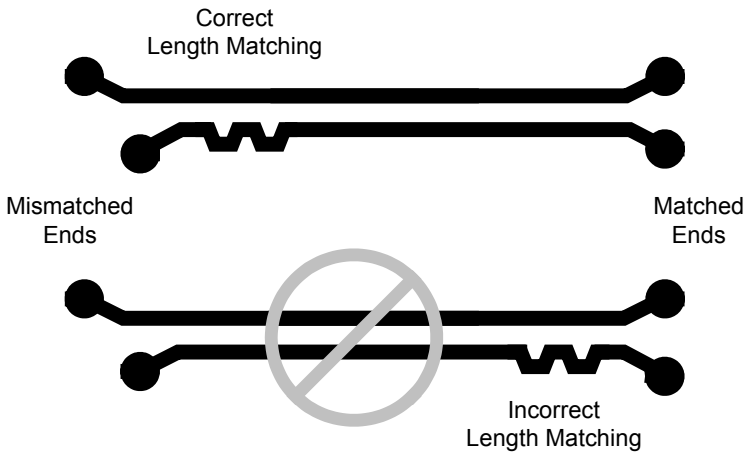

Fig 3. Length matching near location of mismatch

2.2.4 Bends

The use of bends should be kept to a minimum, since a bend can introduce common mode noise into the system, which will affect the signal integrity and EMI of the differential pair.

Bends on traces should be ≥ 135°. Tighter bends should be avoided because they impact the loss and jitter budgets.

If bends are used, the following guidelines are recommended to avoid tight bends. See Fig 4.

1. Keep all angles between traces (α) ≥ 135°.
2. Maintain an air gap (A) of ≥ 20 mils.
3. Segments such as B and C, which flank a bend, should have a length ≥ 1.5 times the width of the trace.

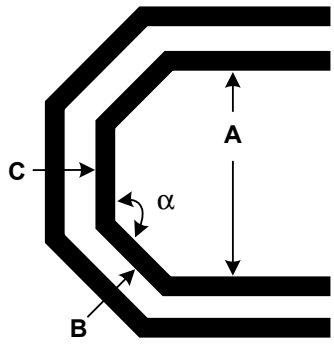

Fig 4. Trace bending guidelines

The number of left and right bends should be as close to equal as possible, to minimize the length mismatch.

When a serpentine section is used to match one length to another, as shown in Fig 5, the length of each jog must be at least 15 mils (three times the 5 mil trace width). The maximum distance between traces in a serpentine section should be less than two times the distance between traces in a non-serpentine section.

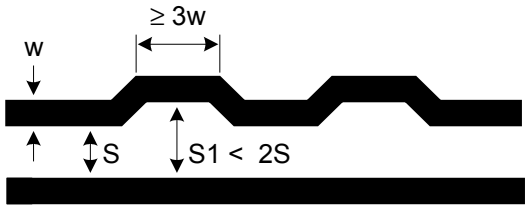

Fig 5. Serpentine section

An uncoupled section of trace routing into a pin or a ball should be ≤ 45 mils when using multiple bends, as shown in Fig 6.

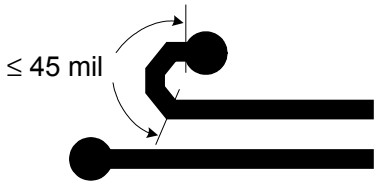

Fig 6. Uncoupled trace using multiple bends

2.3 Breakout areas

Within a breakout area (for example, Philips PCI Express PHY ball field, connector pins, or add-in card edge fingers), exceptions to the general trace routing guidelines may occur.

5 mils intra-pair space and 10 mils inter-pair space are allowed in the breakout region. A small section of trace, up to 50 mils, does not necessarily require a reference plane. Length matching should occur as close as possible to signal pins without introducing any tight bends.

Fig 7 shows some techniques used in breakout areas. Side-by-side placement is considered best. Adjacent with a small serpentine is acceptable. Diagonal routing and adjacent placement with a bend are acceptable but not as good as the other techniques.

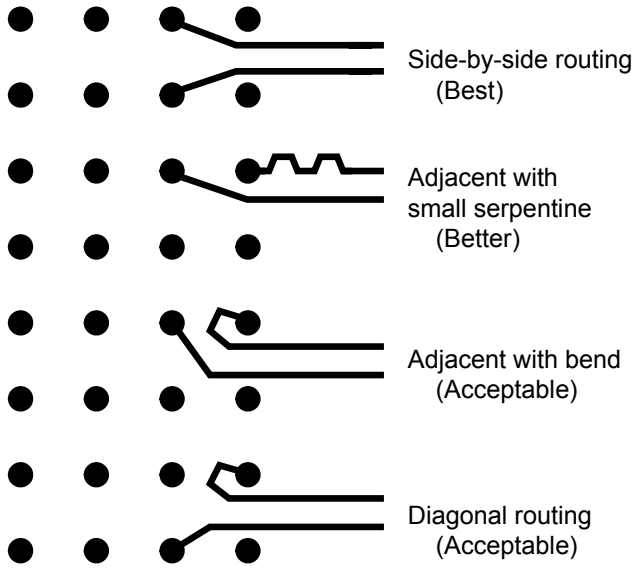

Fig 7. Breakout area layouts

2.4 Test points, vias and pads

Signal vias affect the overall loss and jitter budgets. Each via pair may contribute 0.25 dB of loss in some corner cases. Vias may limit the achievable maximum routing length.

A maximum of four via pairs can be used on a TX differential pair. A maximum of two via pairs can be used on an RX differential pair. Vias should have a pad size of 25 mils or less, and a finished hole size of 14 mils or less. Two vias must be placed as a symmetric pair in the same location.

Test points (which can be vias, pads or components) and probe pads should be placed symmetrically in series. Stubs should not be introduced on differential pairs. Refer to Fig 8 for illustrations of correct and incorrect placements.

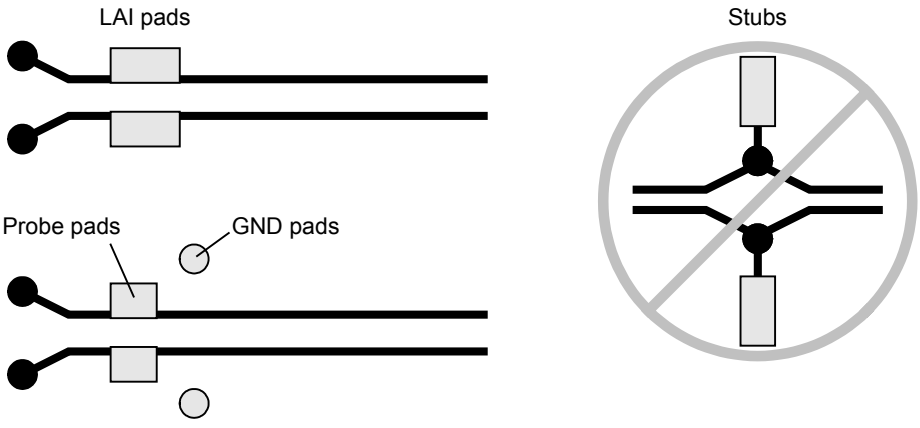

Fig 8. Test points and probe pads

2.5 AC coupling capacitors

PCI Express requires AC coupling between transmitter and receiver. The AC coupling capacitors for both differential pair signals must be the same value, same package size, and have symmetric placement. If possible, TX traces should route on the top layer.

The capacitor value must be in the range of 75 nF to 200 nF (100 nF is best). The 0402 package size is preferred, and 0603 is acceptable. C-pack is not allowed.

The breakout into and out of capacitors should be symmetrical for both signal lines in a differential pair. The trace separation for routing to pads must be minimized in order to optimize tight coupling between the signal pairs.

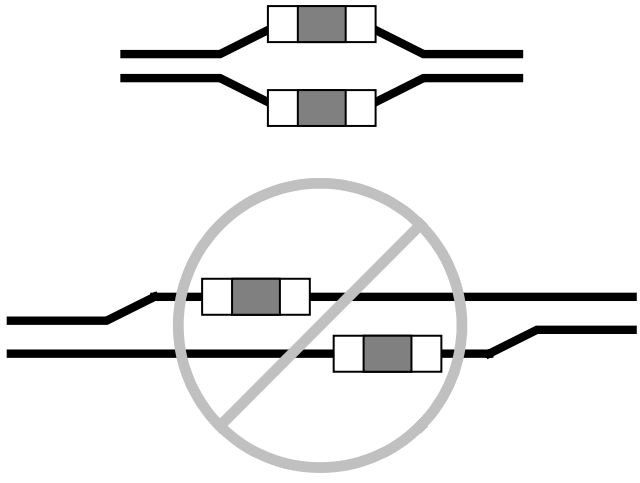

Fig 9. Placement of AC coupling capacitors

2.6 Edge fingers and connector

The reference planes under the edge finger pads should be removed to meet the impedance target. The planes should be removed along the entire length of the edge finger component. Both traces of a differential pair should route into a connector pin field from the same layer.

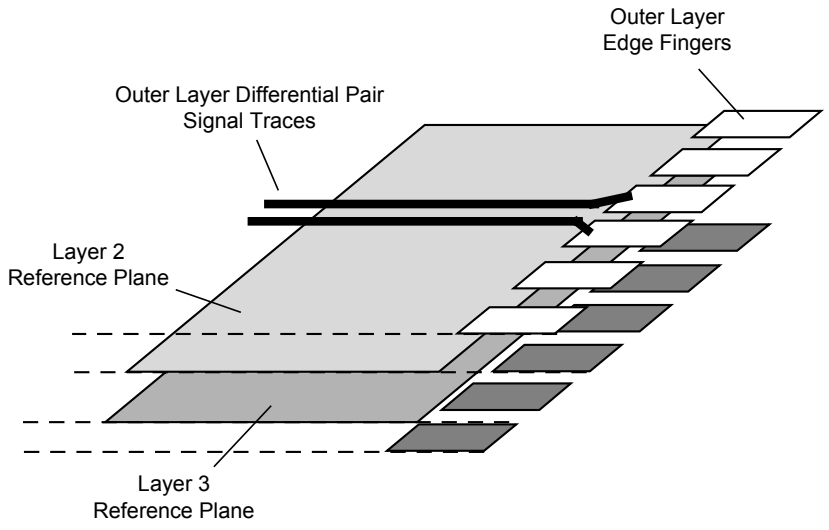

Fig 10. Add-in card edge fingers

2.7 Reference clock

The 100 MHz differential reference clock should use the same differential trace geometries as the high-speed serial data traces.

3. PXPIPE interface connection

The PXPIPE interface of the Philips PCI Express PHY consists of 8-bit input and 8-bit output words, each with control and status signals and source synchronous clocks. The data rate is 250 MB/s. The interface operates at the SSTL_2 (Stub Series Terminated Logic for 2.5 Volts) logic level.

3.1 SSTL_2 termination

The PXPIPE interface is an SSTL_2 Class I bus with:

VDD = VDDQ = 2.5 V

VTT = 1.2 V

A 25 Ω series resistor RS and a 50 Ω termination resistor RT are recommended for the PXPIPE interface termination, as shown in Fig 11.

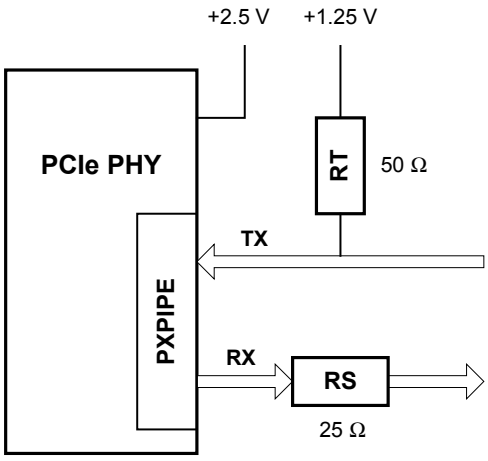

Fig 11. PXPIPE interface termination

3.2 Length matching of data bus route traces

Both TXDATA and RXDATA consist of 8-bit data. To minimize bit-to-bit skew, trace length matching is recommended among all PXPIPE outputs and among all PXPIPE inputs. Length matching between TXDATA and RXDATA is not required.

4. Summary

This document has provided practical layout guidelines for designing a PCB incorporating the Philips PCI Express PHY chip. The PCI Express interconnect is a point-to-point layout of the serial differential signal trace pairs. The most important considerations are to minimize loss and jitter, and to maintain symmetry for each differential trace pair. Loss and jitter are affected by trace length.

These are general guidelines only. Board designers should carefully weigh design tradeoffs and use simulation analysis to ensure a successful implementation.

5. References

- Board design guidelines for PCI Express interconnect, Intel
- PCI Express board design guidelines, Intel, June 2003
- Board design guidelines for PCI Express architecture, PCI-SIG, 2004

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8. Contents

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