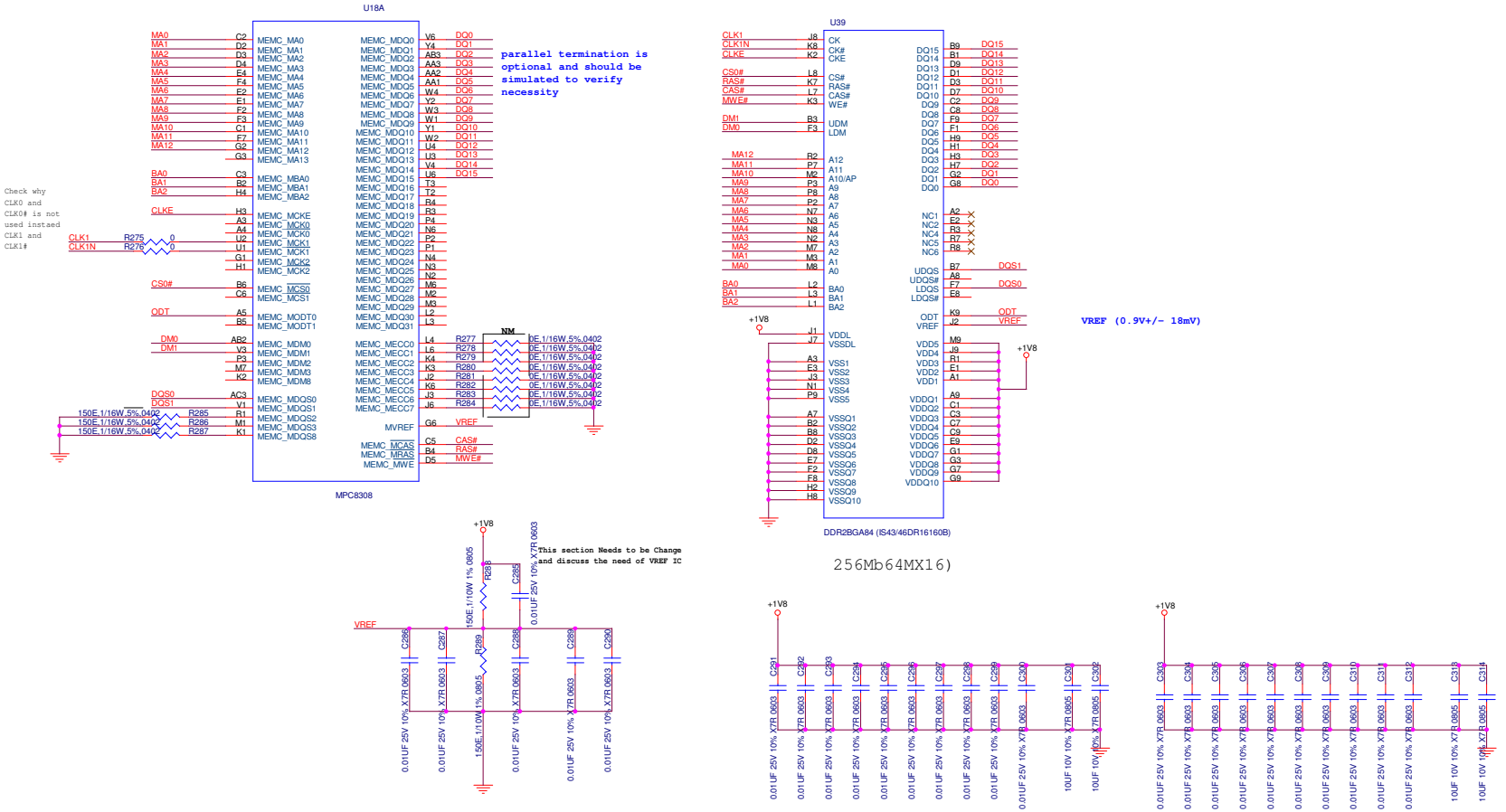
U18A
MPC8308
parallel termination is optional and should be simulated to verify necessity
Check why CLK0 and CLK0# is not used instead CLK1 and CLK1#
NM
U39
DDR2BGA84 (IS43/46DR16160B)
256Mb64MX16)
VREF (0.9V+/- 18mV)
This section Needs to be Change and discuss the need of VREF IC