FTF | FREESCALE TECHNOLOGY FORUM
POWERING INNOVATION

Simplified Industrial Safety Solutions

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Industrial Automation & Control Marketing

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Agenda

- IEC61508
  - Standard Explanation
  - How Freescale Addresses the Standard
    - SafeAssure
    - Product Offerings
    - Safety Process
    - Safety Hardware
    - Safety Software: Third-Party
    - Safety Support

- IEC60730
  - Standard Explanation
  - How Freescale Addresses the Standard
    - Software Coverage
    - Product Offerings

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Freescale and Safety

- Safety is difficult and you need a partner who understands safety and your needs.
- Freescale offers industrial solutions for many safety applications, including IEC 61508 functional safety and IEC 60730 safety for automation electronics for household appliances
- Unique IP and architectures — including safety checks, on-chip redundancy, watchdogs and more — are used to satisfy the safety requirements

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Industrial disasters happen have happened and *will* happen.
Robust safety systems are a key to **prevention**.

Deep Water Horizon Explosion

Air France Flight 447 Crash

Buncefield Fires

Qinghe Special Steel Corporation Disaster

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Safety Market Trends and Challenges

1 Trends

- Recent events (Japan tsunami, BP oil spill) have continued to reinforce the need for automated process safety systems
- Functional safety increasingly becoming part of system designs (operations) and at corporate level

2 Increasing integration and system complexity

- Increasingly complex electronic control is driving designs with safety requirements in non-traditional markets, e.g. solar energy
- Increase in use of high-performance sensor systems and complex control algorithms results in substantially higher MCU performance requirements

3 Functional safety & mounting cost pressures

- An increasing number of industrial control systems require IEC61508 (SIL3) system safety certification
- Applications typically need to duplicate system and/or have additional system level components in order for this to be to achieved
- Safety designs need to be designed from the ground up to ensure standards compliance
- Continuing pressure to reduce development cycle time and cost

4 Market trends outpacing customer experience levels

- Growing need for design-for-safety consultation and software support

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Functional Safety Defined

- Functional safety is the **absence of unreasonable risk** due to hazards caused by malfunctioning behavior of electrical/electronic systems
  - **Hazards**: potential source of harm
  - **Harm**: physical injury or damage to the health of people

- **Failures** are **main impairment** to safety:
  - **Systematic**: failures, related in a deterministic way to a certain cause, that can only be eliminated by a change of the design or manufacturing process, operational procedures, documentation or other relevant factors
  - **Random**: failures that can occur unpredictably during the lifetime of a hardware element and that follow a probability distribution

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What are Functional Safety Standards About?

- Functional safety standards impose a structured way for the industry to proceed
  - IEC61508 V1 published as international standard ~2000
  - IEC61508 V2 published as international standard 2010

- The standards address
  - Architectural & functional aspects
  - Procedural aspects (incl. safety lifecycle)
  - How to avoid faults and to control faults
  - Considering systematic faults and random hardware faults

- Rigorous documentation serves as evidence for complying to the safety standards

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Evolving Functional Safety Standards

	1980	1985	1990	1995	2000	2005	2010	2015
Aeronautic	DO 178 DO 178A		DO 178B ARP 4754	ARP 4761	DO 254		DO 178C ARP 4754A	
Rail Transport				EN 50155	IEC 61508 EN 5012X EN 50159			
Generic Standard IEC61508					IEC 61508		IEC 61508 Edition 2	
Industrial Automation					IEC 61508 IEC 61511 IEC 62061		IEC 61508 Edition 2	
Automotive					(IEC 61508)		ISO 26262	
Medical							IEC 60601 Edition 3	

□ Select Freescale products developed to target IEC 61508 and ISO 26262

freescale™

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Safety Integrity Levels (SIL)

- Safety standards defining five levels with
  - Availability, probabilities and consequences of failure
- Naming and definition vary by standard, e.g.:
  - Industry (IEC61508): SIL 0 – SIL 4
  - Automotive (ISO26262): ASIL A – ASIL D
  - Medical (IEC60601): Level 1 – Level 3

Safety Integrity Level	Demand Mode		Continuous Mode	Consequence of a failure
	Availability	Probability of a failure on demand	Probability of a dangerous failure per hour	
SIL 4	> 99.99%	>=10^{-5} to < 10^{-4}	>=10^{-9} to < 10^{-8}	Potential for fatalities in the community
SIL 3	99.9%	>=10^{-4} to < 10^{-3}	>=10^{-8} to < 10^{-7}	Potential for multiple fatalities
SIL 2	99% - 99.9%	>=10^{-3} to < 10^{-2}	>=10^{-7} to < 10^{-6}	Potential for major injuries or one fatality
SIL 1	90% - 99%	>=10^{-2} to < 10^{-1}	>=10^{-6} to < 10^{-5}	Potential for minor injuries
SIL 0	No requirements			n/a

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afety and Performance in Motion

Unmatched performance and ruggedized safety features for almost anything that moves

Unmatched MCU Performance

Get up to 600 DMIPS – the most powerful core for MCUs today – enabling single-chip design for complex algorithms

Assured Safety, Quality & Reliability

Meets industrial, medical, and transportation requirements to ease safety approvals and durability mandates

Market- Leading Integration

Get up to 4 MB embedded
flash and a rich set of analog, connectivity and timing peripherals to support complex real-time control

Easy Development

Make development a snap with run-time software, reference designs and tools for rapid prototyping, advanced debug and system modeling

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PX Series MCU Families for Industrial Applications

Safety and Performance in Motion

Performance

Performance-Leading MCU

PXR Family

Built for single-chip, high-performance real-time applications

- **Target Applications:**
  - Precision factory control
  - Industrial automation
  - Industrial transportation
  - Motor control/drives
  - Medical
  - Timing applications
- **Features:**
  - Up to 4MB Flash
  - 264MHz core frequency
  - 600DMIPS
  - 2x eTPU
  - 64ch Quad ADC

Functional Safety

Redundancy Reliability Quality

PXS Family

Simplifying safety certification while implementing zero defect methodologies

- **Target Applications:**
  - Industrial automation
  - Aerospace control
  - Motor control/drives
  - Industrial transportation
  - Power generation and management
  - Medical
  - Robotics
- **Features:**
  - Up to 2MB Flash
  - Dual Locking Core
  - Sphere of Replication
  - up to 600DMIPS
  - Fault Control & Collection Unit
  - Optional Ethernet

Connectivity

Connected Performance

PXN Family

Enabling data concentration and algorithm computation

- **Target Applications:**
  - Industrial gateways
  - Process measurement and control
  - Industrial hub
  - Input/output (I/O) control
  - Programmable logic control
- **Features:**
  - Up to 2MB Flash
  - 2nd core to offload communication processing
  - Up to 25 serial communication modules
  - Optional Ethernet

HMI/User Interface

Single-Chip Display Solution

PXD Family

Reduce footprint and cost for industrial display applications

- **Target Applications**:
  - Factory display units
  - Building control display units
  - Ruggedized displays
  - Industrial instrumentation
- **Features:**
  - Up to 2MB Flash
  - Display Control Unit driving up to WVGA
  - Optional Video Input
  - Stepper Motor Drivers
  - Quad SPI Interface

BUILT ON Power

PXS Family

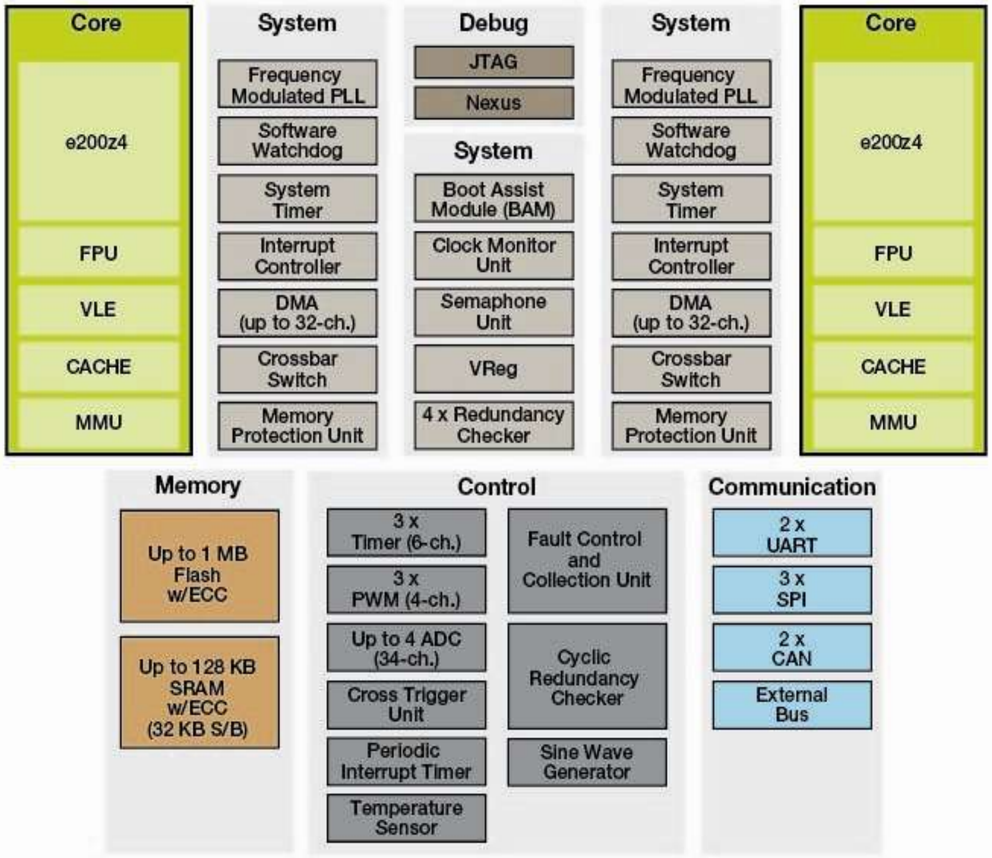
Functional safety & performance: Designed for IEC 61508 SIL 3. **Only** dual-core, dual-issue controller available that can switch between **lock-step mode and dual-parallel mode**

Sphere of Replication:
Typically only the actual cores in lock-step MCUs are replicated. PXS goes beyond this with duplication of **all** computational elements.

Over 600 DMIPS performance from dual-core, dual-issue e200 running at 120 MHz

Motor Control:
Fast 12-bit ADCs, PWM and the new CTU (cross triggering unit) enable control of up to two brushless DC motors with minimum interrupt load

PXS20 Block Diagram



Core
- e200z4
- FPU
- VLE
- CACHE
- MMU

System
- Frequency Modulated PLL
- Software Watchdog
- System Timer
- Interrupt Controller
- DMA (up to 32-ch.)
- Crossbar Switch
- Memory Protection Unit

Debug
- JTAG
- Nexus

System
- Boot Assist Module (BAM)
- Clock Monitor Unit
- Semaphone Unit
- VReg
- 4 x Redundancy Checker

System
- Frequency Modulated PLL
- Software Watchdog
- System Timer
- Interrupt Controller
- DMA (up to 32-ch.)
- Crossbar Switch
- Memory Protection Unit

Core
- e200z4
- FPU
- VLE
- CACHE
- MMU

Memory
- Up to 1 MB Flash w/ECC
- Up to 128 KB SRAM w/ECC (32 KB S/B)

Control
- 3 x Timer (6-ch.)
- 3 x PWM (4-ch.)
- Up to 4 ADC (34-ch.)
- Cross Trigger Unit
- Periodic Interrupt Timer
- Temperature Sensor
- Fault Control and Collection Unit
- Cyclic Redundancy Checker
- Sine Wave Generator

Communication
- 2 x UART
- 3 x SPI
- 2 x CAN
- External Bus

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SAFE
ASSURE™
by Freescale

Functional Safety. Simplified.

Simplifies the process of system compliance, with solutions designed to address the requirements of automotive and industrial functional safety standards

Reduces the time and complexity required to develop safety systems that comply with ISO 26262 and IEC 61508 standards

Supports the most stringent Safety Integrity Levels (SILs),enabling designers to build with confidence

Zero defect methodology from design to manufacturing to help ensure our products meet the stringent demands of safety applications

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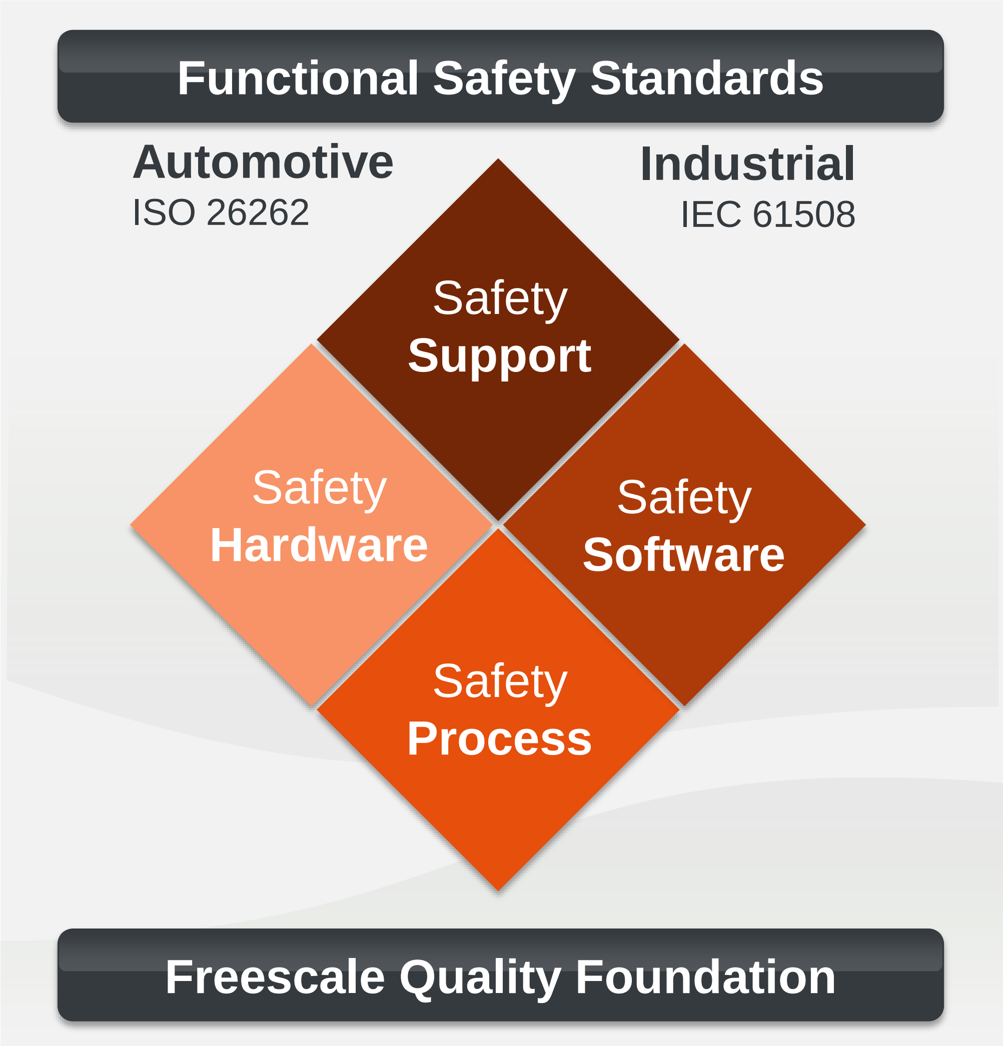
Freescale Approach to Functional Safety



Functional Safety Standards

Automotive
ISO 26262

Industrial
IEC 61508

Safety **Support**

Safety **Hardware**

Safety **Software**

Safety **Process**

Freescale Quality Foundation

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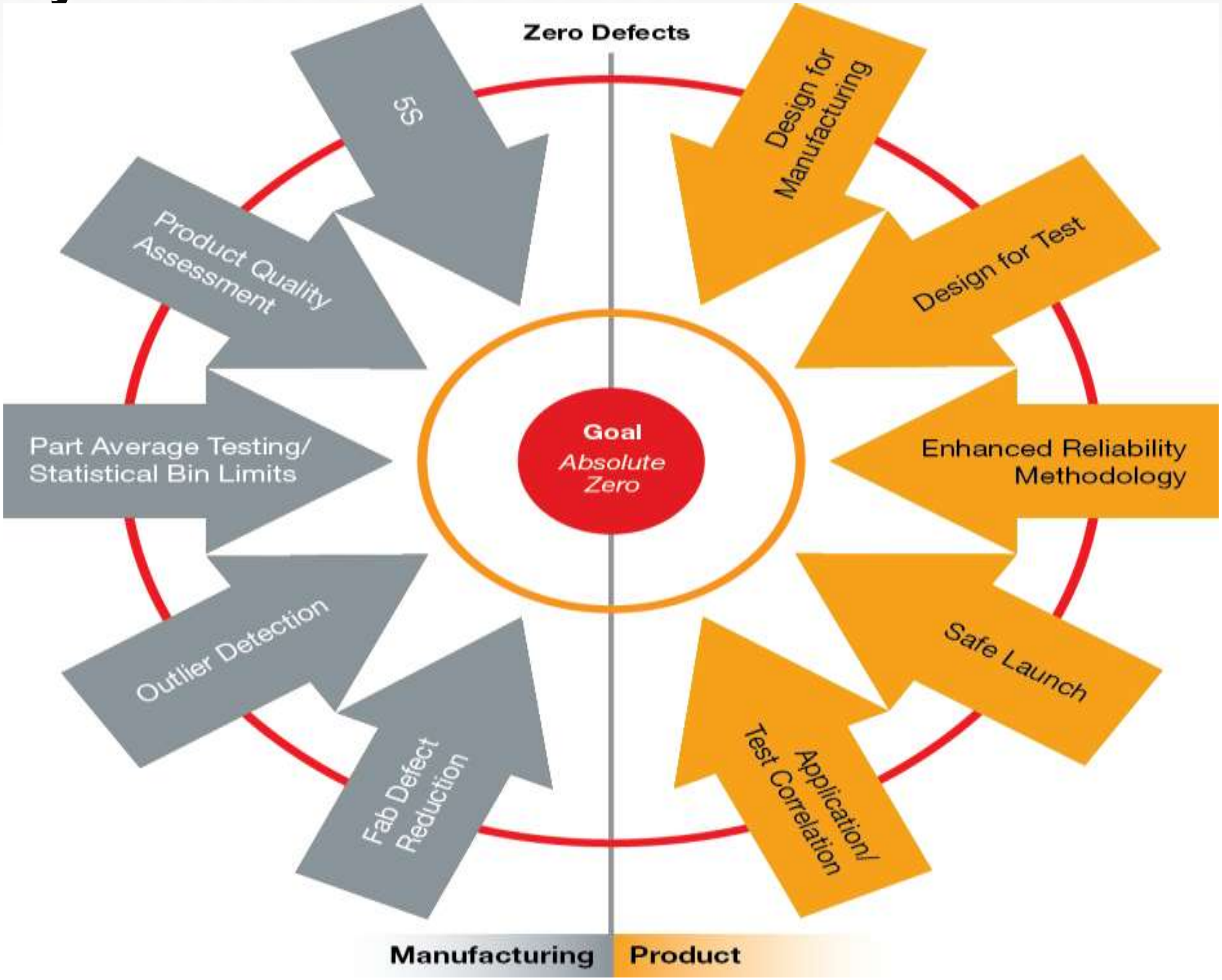
Safety Process: Zero Defect



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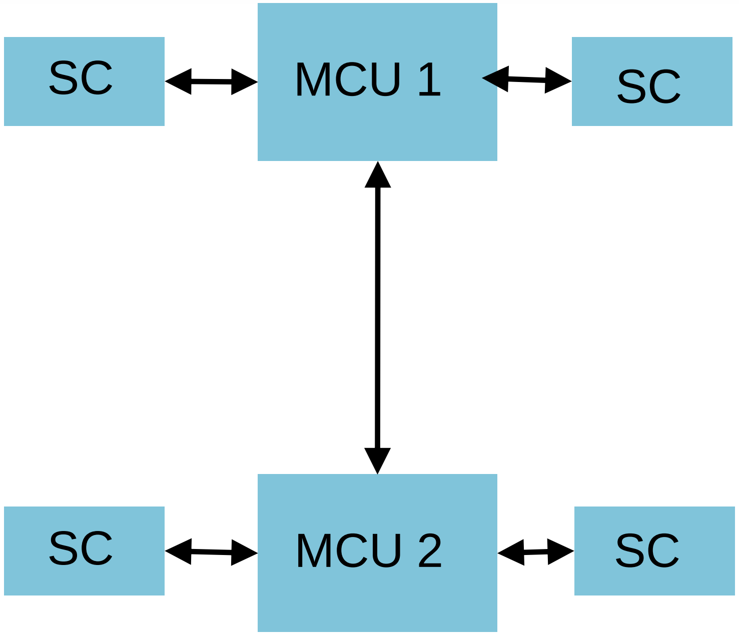
Safety Hardware: Traditional Safety Approach

Multi-chip, single-core systems

Redundancy is created by using multiple chips and external safety components



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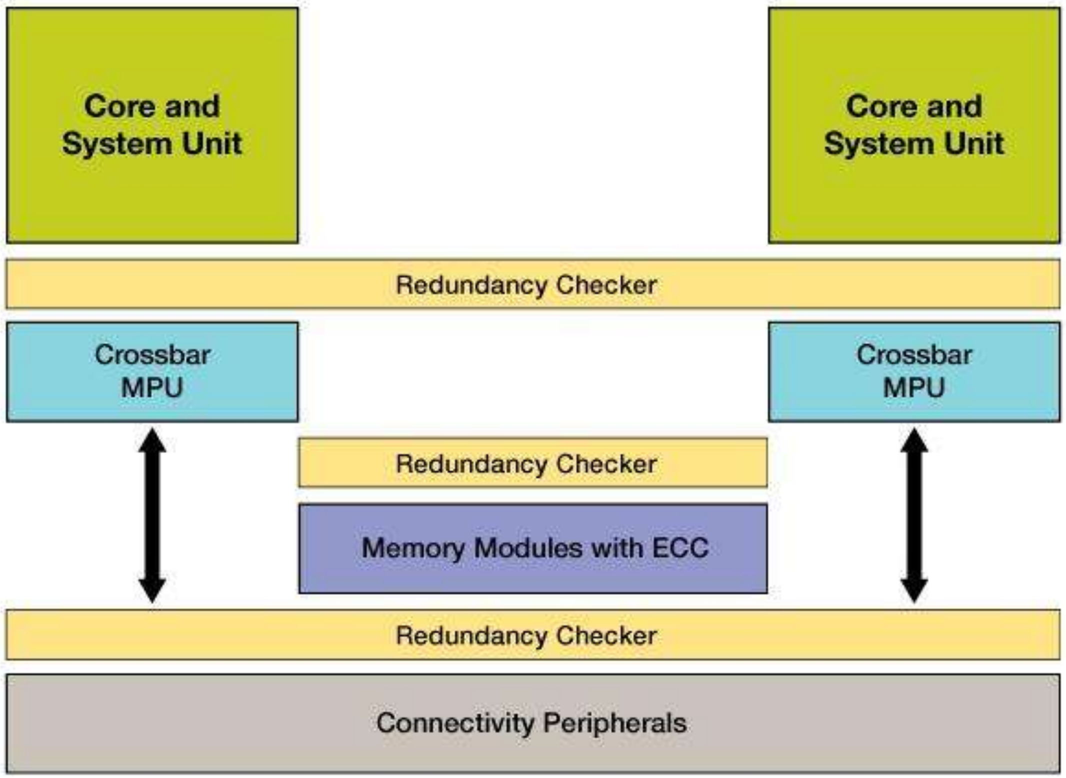
New Safety System

Single-chip, dual-core solution

One chip with replicated dual cores and integrated safety features



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XS20 Safety Measures at Module Level

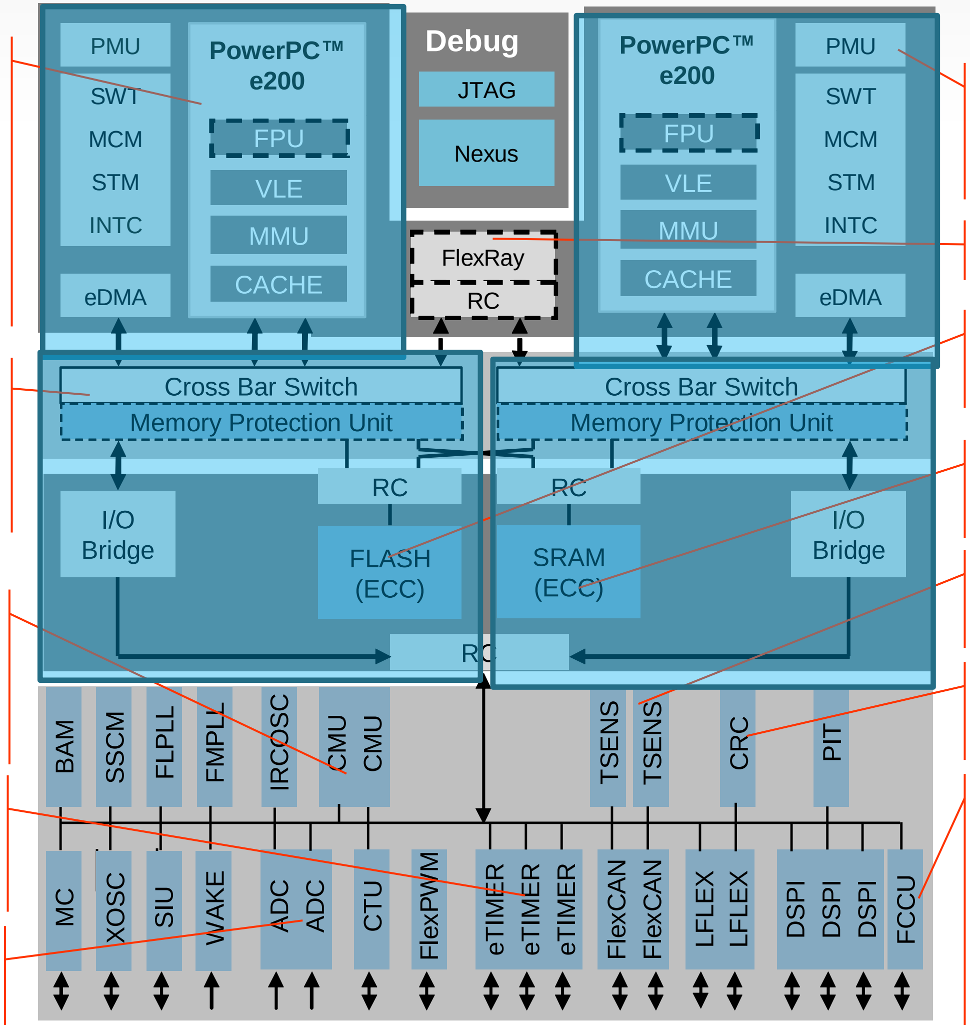
Sphere of Replication:
- *Replicated e200Core*
- *Replicated eDMA*
- *Redundant INTC, SWT, etc*
- *Redundant MMU*
- *RC units at gates to non redundant sphere*

XBAR + MPU:
- *Redundant*
- *RC units at gates to non redundant sphere*

Clock Monitoring
- *Detects and mitigates clock disturbances*
- PLL

Timer
- *eTimer0 channels "isolated"*

ADC
- *On line assisted hardware BIST*



PMU
- *Internal Vreg*
- *Redundant Vmonitor*

Flexray

Flash
- *ECC*

RAM
- *ECC*

Temp Sensor
- *Redundant*

CRC Unit
- *Application signature*

Fault Collection Unit
- *Detects when errors have occurred*
- *Indicates error to external*
- *Independent of software operation*

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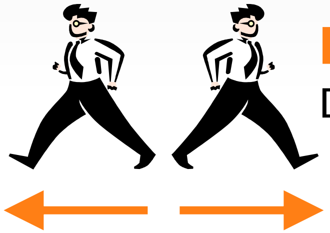
Dual-Core Modes of Operation

LSM

Lock Step Mode

- 1x performance
- MCU mode which allows SIL3 with minimal software overhead
- Formal check of outputs for replicated IP modules
- Checker (RC) guarantee detection of non-common cause faults when redundant channels are merged



DPM

Decoupled Parallel Mode

- Up to 2x performance
- MCU mode which allows SIL3 with algorithm diversity
- CPU cores and subsystems run independently
- Checker units (RC) are disabled in this mode

- Device concept supports static configuration of the operating mode during Reset
- Selection between the two modes is done by programming a user option bit stored in the shadow sector of the flash array

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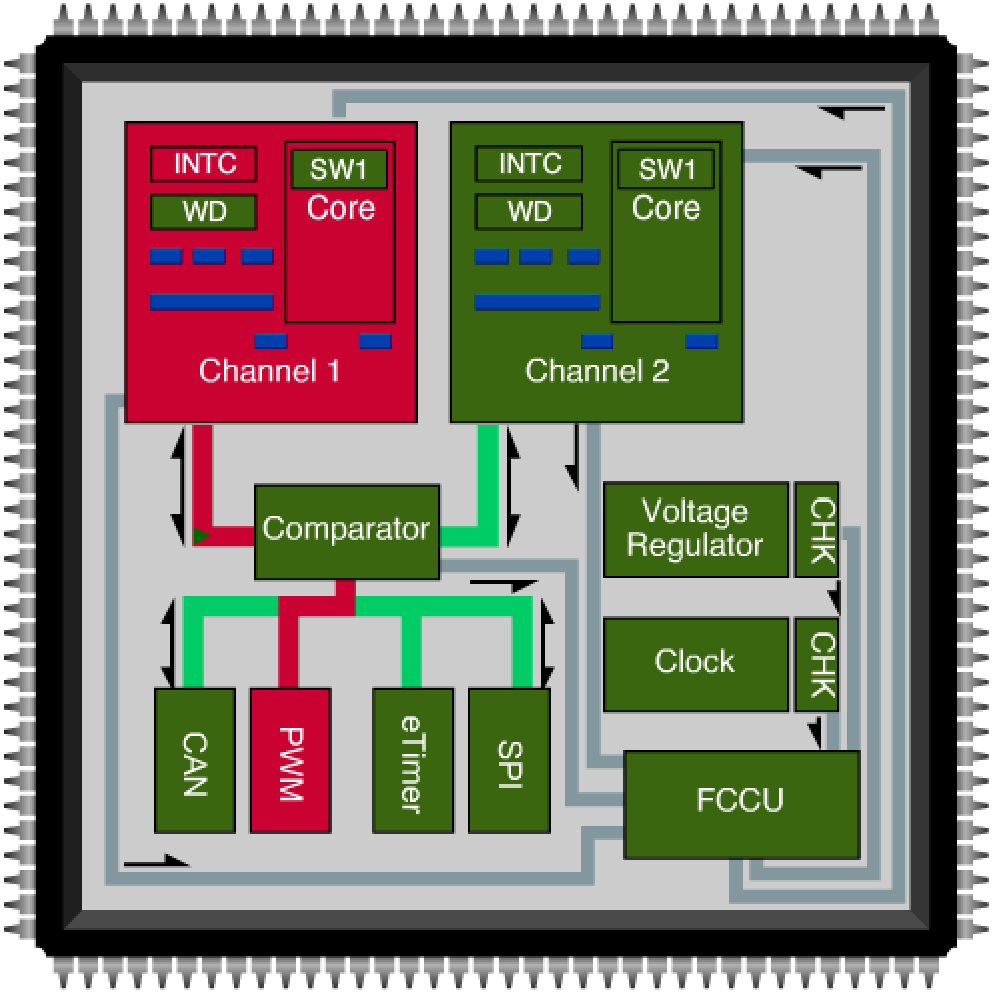
Single-Chip Dual Core Fault Handling

- Fault constantly raises an interrupt at Core 1
- Core 1 can no longer execute safety-relevant application
- Core 1 does not issue expected commands to the PWM
- PWM considered failed



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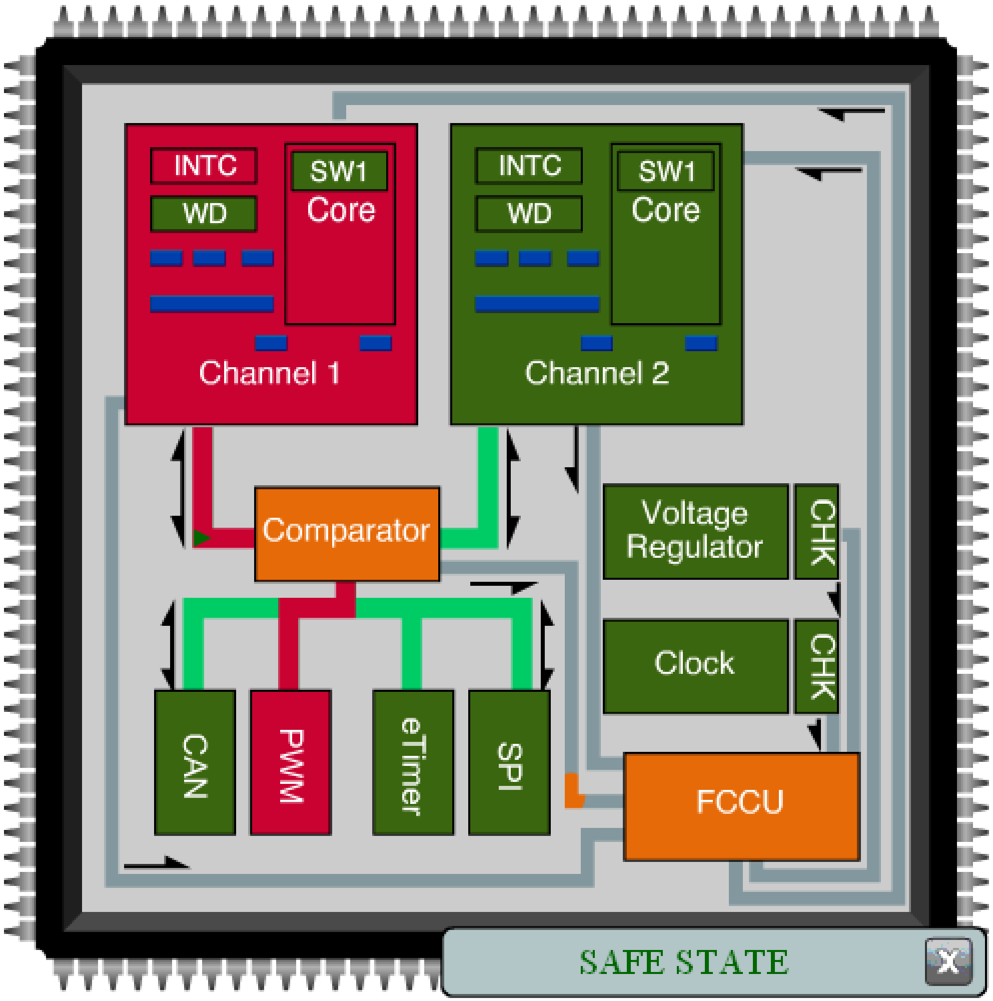
Single-Chip Dual Core Fault Handling

- The comparator detects that both channels show different behaviors: Core 1 does not write to PWM where Core 2 does
- Comparator signals deviation to Fault Collection & Control Unit
- FCCU determines the fault is critical
- Triggers external system
- System moves itself into a safe state



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Safety Software:

Green Hills SOFTWARE

IEC 61508

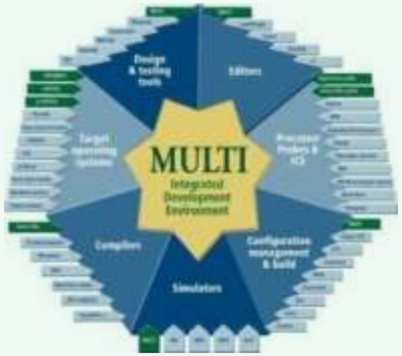
Safety BSP & Test,
Best Practices Training,
Cert Documentation

ISO 26262 EN 50128

INTEGRITY- IEC µ-velOSity

Safety Certified Real Time Operating Systems, and Middleware

QorIQ,
Qorivva,
PX



Safety qualified development tools and optimizing compilers

TimeMachine

Trace-powered analysis and backward execution to FIND EVERY BUG

Green Hills Probe

SuperTrace PROBE

JTAG and Trace Probes

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INTEGRITY Real-Time Operating System

- Unique real-time operating system architecture
- Separation kernel architecture
- Partition scheduling / resource guarantees
- Advanced multicore/multiprocessor support
  - Single-Core, AMP, SMP
- Safely consolidate software on same processor
- The most highly certified RTOS in embedded industry
- Common Criteria EAL 6+, highest software security certification in world
- IEC-61508 SIL3 for industrial
- CENELEC EN50128 for railway
- DO-178B Level A for avionics
- FDA Class II, III approvals for medical
- Extensive middleware and ecosystem
- Networking, routing, graphics and much more
- Open platform support
- POSIX conformant, BSD sockets, upgradeable and flexible

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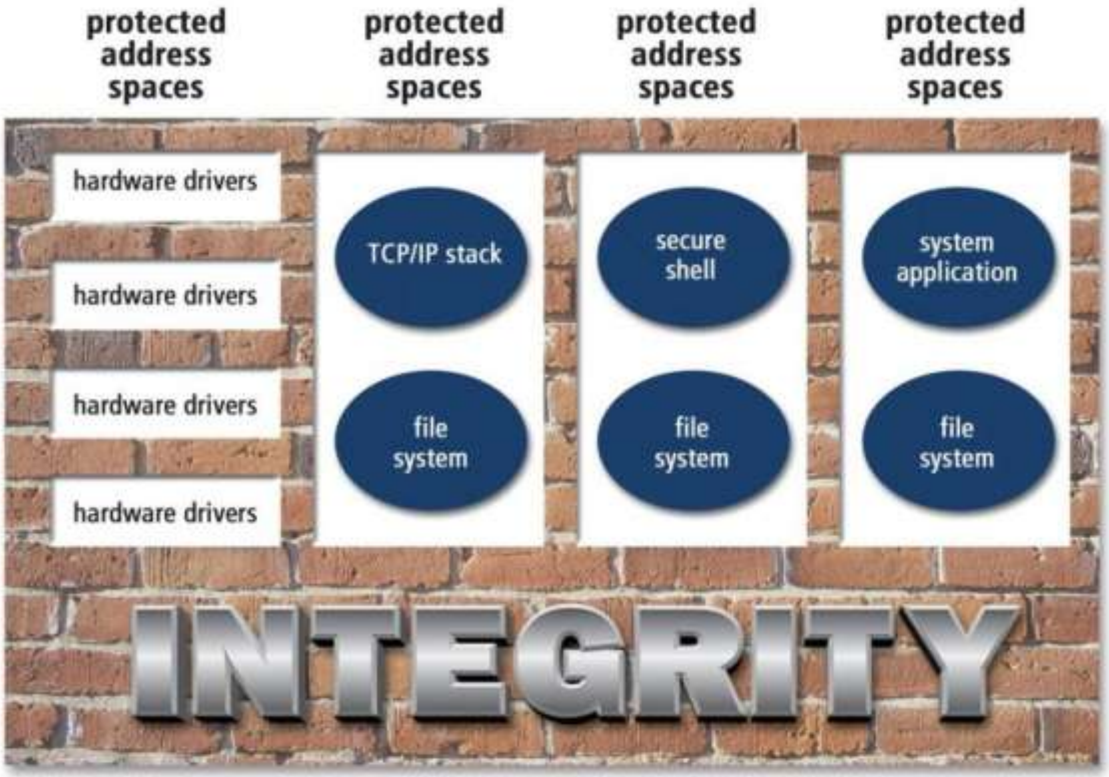
INTEGRITY Unique Architecture

Separation Kernel Architecture

- Separation kernel technology
- User-defined brick wall partitioning
- Contains errors & attacks
- Isolates stack and application
- Guaranteed resource allocation
- Access control between partitions



Key Point

Separation kernel enables far-reaching benefits for customer's functional safety software

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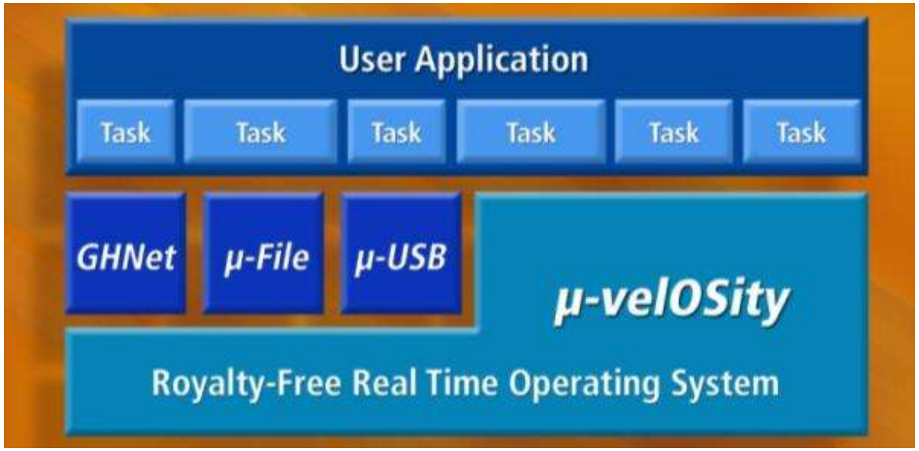
µ-velOSity RTOS Highlights

- Royalty-free
- Delivered in source code
- Simple native API
- Fits in under 5 KB of ROM
- Boots in less than 1,500 instructions

- Integrated middleware support
  - Full TCP/IPv4/v6 with IP Apps
  - MS/DOS file system with FLASH wear leveling
  - USB device with Mass Storage Class
  - PEG Embedded graphics

- Upward compatible API with INTEGRITY
- Integration with Green Hills best-in-class MULTI Tools



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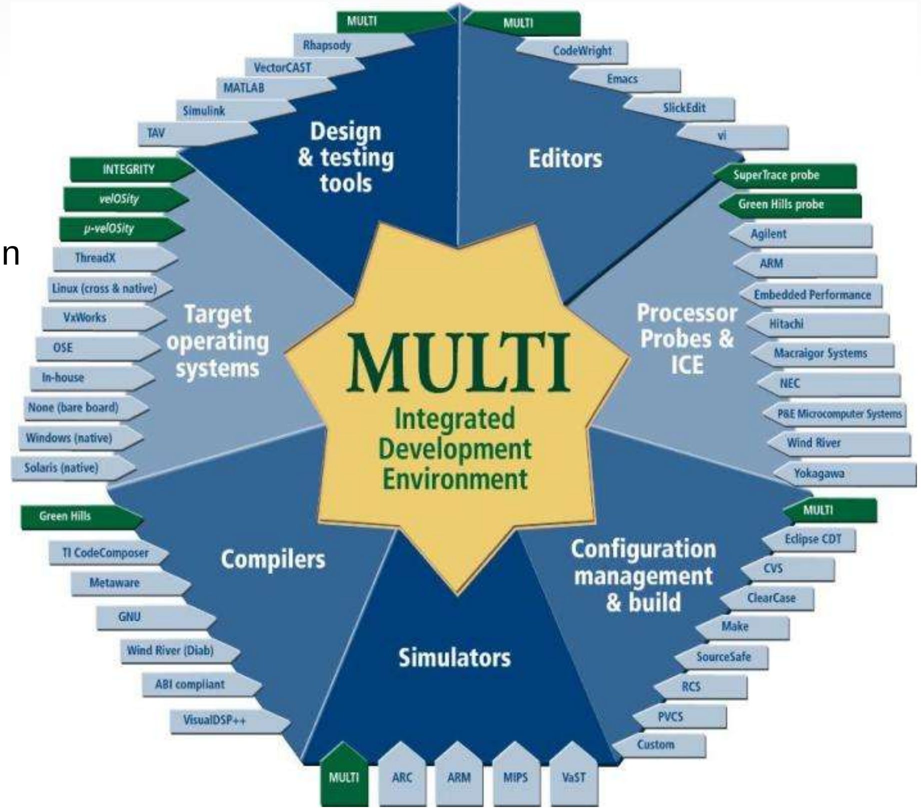
MULTI Integrated Development Environment

Debug, Analyze and Optimize Embedded Projects

- Optimizing C/C++ /EC++ cross compiler and toolchain
- Multicore, multithread source level debugger
- OS-Aware, Run-Mode, Stop-Mode Debugging
- Run-time Error Detection & Memory Leak Detection
- Instruction Set Simulator
- Trace-assisted TimeMachine & Path Analyzer
- Code Coverage Analysis
- Performance Profiler
- Flash programming
- DoubleCheck® Source Code Analyzer
- The MathWorks™ Link MU Integration
- Debug 3rd Party RTOS (VxWorks, Linux, home-grown)



Better Managed Embedded Projects

- Project Builder
- Source Code Editor
- MISRA C Checker – safe code checker

Safety Qualified version of MULTI in Q3

- **ISO 26262**
- **IEC 61508**
- **EN 50128**

TÜV CERT

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Flexible Solutions For PX Customer Requirements

General Purpose Platform	**IEC**
INTEGRITY RTOS or u-velOSity RTOS	**Pre-certified INTEGRITY RTOS for IEC 61508 SIL3 (Industrial) and CENELEC EN 50128 SWIL4 (Railway)**
Extensive middleware including flash programming, USB, and more	
MULTI multicore debugging, MISRA C Wizard, source code analysis tools	
	Certified code generation tools
Record-breaking optimizing compilers	
TimeMachine reverse execution debugging and profiling	
Green Hills Probe and SuperTrace Probe	
Training and services	**Certification services for design, safety BSP development, and certification strategies**

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Flexible Solutions For PX Customer Requirements

General Purpose Platform	Industrial Safety Platform
INTEGRITY RTOS or u-velOSity RTOS	Pre-certified INTEGRITY RTOS or Certifiable u-velOSity
Extensive middleware including flash programming, USB, and more	
MULTI multicore debugging, MISRA C Wizard, source code analysis tools	
	Safety Qualified tool chain
Record-breaking optimizing compilers	
TimeMachine reverse execution debugging and profiling	
Green Hills Probe and SuperTrace Probe	
Training and services	Certification services for design, safety BSP development, certification documentation

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PX Solutions from Green Hills

Product Family	MULTI Toolchain + TimeMachine + Probes	RTOS	Functional Safety Solution		
			Qualified* MULTI Toolchain IEC61508 & ISO 26262	Preferred RTOS	Safety BSP, Best Practices Training, Life Cycle Data, Risk Management Report
PXR40	✔	u-velOSity	✔	u-velOSity	✔
PXN20	✔	u-velOSity INTEGRITY	✔	INTEGRITY-IEC	✔
PXD10	✔	u-velOSity	✔	u-velOSity	✔
PXD20	✔	u-velOSity INTEGRITY[1]	✔	INTEGRITY-IEC	✔
PXS20	✔	u-velOSity	✔	u-velOSity	✔
PXS30	✔	u-velOSity INTEGRITY	✔	INTEGRITY-IEC	✔

(1) Port to INTEGRITY per customer demand

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Green Hills Platform for Industrial Safety for PX

Platform Overview

Green Hills Platform for Industrial Safety is a complete solution for creating safe, reliable, secure industrial embedded systems.

1. For industrial control & automation, automotive, rail and nuclear industries
2. Pre-certified partition architecture RTOS for highest safety levels
   1. IEC 61508 SIL3 (Industrial)
   2. CENELEC EN 50128 SWIL4 (Railway)
3. Certifiable lightweight and simple u-velOSity RTOS
4. Extensive middleware
5. Integrated development tools for the complete lifecycle
6. Certified code generation tools
7. Consulting for Safety BSP, Best Practices Training, Life Cycle Data, Risk Management Report

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Safety Software

- **Sciopta: Safe RTOS**
- Multi tasking, high-performance real time safety kernel
- TÜV certified IEC61508 at Safety Integrity Level 3
- High-value diagnostic test functions for all kernel internal data
- Direct Message Transferring for increased safety

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Safety Support: Safety Manual

- Functional safety concept
  - Description of safety offering of the device
- Functional Safety Requirements on system level
  - Description of software mechanisms
  - Description of required functions by external hardware
  - Basic interaction with complementary Freescale products
- Failure rates and FMEDA
  - Introduction to FMEDA and presentation of key values
- Provisions against dependent failures
- Code examples / pseudo-code
  - Exemplification of selected software interactions through code fragments

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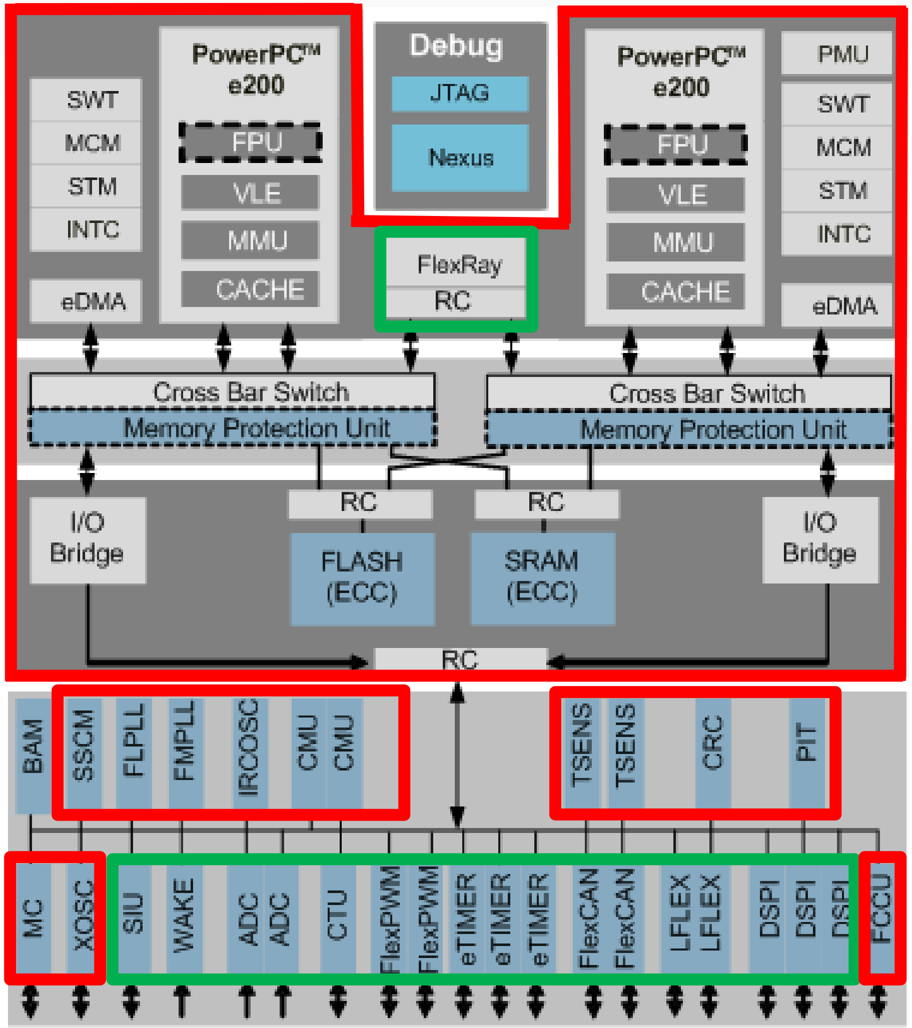
Failure Mode, Effect and Diagnostic Analysis

- FMEDA
  - Processing units
  - Power supply
  - Clock
  - Non-volatile memory
  - Volatile memory
- Raw failure rates
  - Digital I/O
  - Analogue I/O
  - External communication

=> for system level analysis



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Freescale Product Longevity Program

Freescale formally offers many devices for a minimum of 10 or 15 years from the time of launch

Participating Freescale products and program terms are listed at

www.freescale.com/productlongevity

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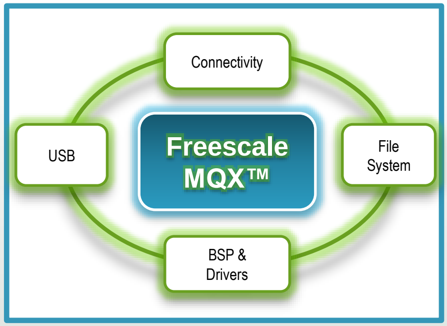
PXS Software and Tools

Modular, expandable and cost-effective development platform



Full-featured, scalable, proven RTOS and middleware

Green Hills SOFTWARE

MULTI IDE: Multicore development & verification, optimized compilers, MISRA C error checking

SCIOPTA

Safe RTOS: IEC 61508 SIL 3 Certified

RAppID

Toolbox w/Simulink

PinWizard

Init Tool

- Model-based design
- Configuring function assignment to pins
- Initialization setup

FreeMASTER

Real-time debugging tool

CodeWarrior

- Build, debug and flash tools
- Software analysis
- Kernel-aware debug

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PX Series Tower Boards

TWR-PXS20

MSRP: $139
Available: Now

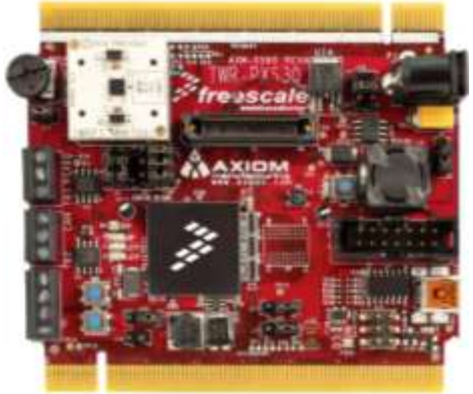
TWR-PXD10

MSRP: $139
Available: Now

TWR-PXR40

MSRP: $249
Available: Now

TWR-PXS30



MSRP: $219
Available: Now

TWR-PXD20

MSRP: $169
Available: Now

TWR-PXN20

MSRP: $219
Available: Now

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IEC 60730 Explained

- The Underwriters Laboratory (UL) has adopted IEC 60730 for certifying consumer devices and industrial products with automatic controls, e.g. appliances or HVAC systems. UL1998, Software in Programmable Components, specifies “detection of all single bit errors.” This means microcontrollers must detect faults and force motors and systems to a safe state if the fault is not corrected.
- This session will explain the IEC 60730 standard, how it can impact your next design, and how Freescale can help you quickly gain 60730 compliance.

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IEC 60335-1 (IEC 60730-1)

- IEC 60335-1 Household and similar electrical appliances – Safety-Part 1. General Requirements.
  - Compliance safety requirements for large appliance manufacturers.

- IEC 60335-1 Annex R – Software Evaluation
  - Software shall be evaluated in accordance with the following clauses of Annex H of IEC 60730-1, as modified below …

- IEC 60730-1 Annex H – Requirements for electronic controls.
  - This chapter centres around Table H.11.12.7

- IEC 60730-1 Annex H Table H.11.12.7
  - Discusses the various embedded “components” that have to be tested to comply for class B and class C electronic controls.
  - Provides optional “measures” that are required to ensure reliable and safe operation of the embedded “component”.

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IEC 60730 Classification of Appliances

- Class A are products with no feature/function that can harm a human being.
- Class B
  - IEC 60730-1: Control functions intended to prevent unsafe operation of the controlled equipment. Examples are: thermal cut-offs and door locks for laundry equipment.
  - IEC 60335-1: Software that includes code intended to prevent hazards if a fault, other than a software fault, occurs in the appliance
- Class C
  - IEC 60730-1: Control functions which are intended to prevent special hazards (e.g. explosion of the controlled equipment). Examples are: automatic burner controls and thermal cut-outs for closed water heater systems (unvented).
  - IEC 60335-1: Software that includes code intended to prevent hazards without the use of other protective devices.

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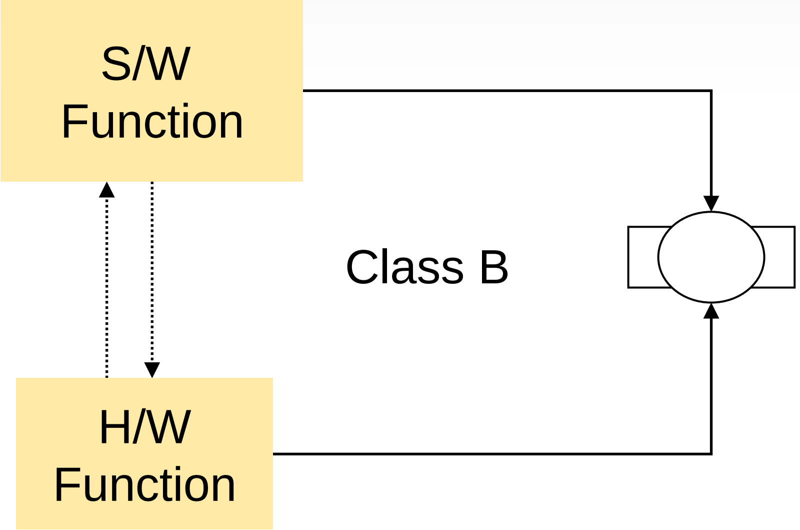
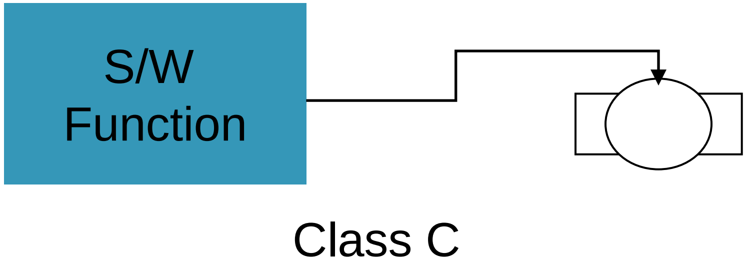
Example Hazard: Overheating of Motor



Hardware PTC monitor temp
Software also monitors motor current.
If one function fails, the other ensures safe operation

Class B – A fault occurring in a safety-critical software routine will not result in a hazard due to another software routine or redundant hardware intervening.



Software only monitors motor current.
If function fails, then hazard will occur.
Need more thorough diagnostics to ensure the software function is working reliably

Class C – A fault occurring in a safety-critical software routine will result in a hazard.

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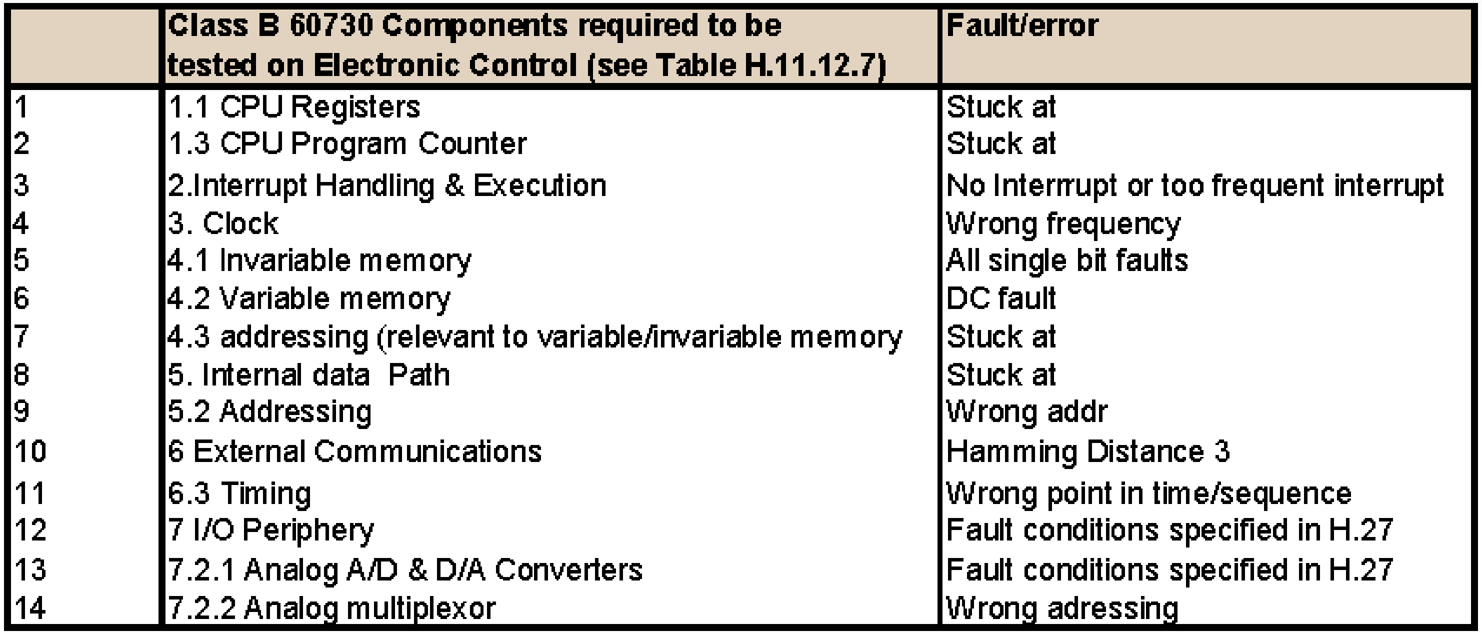
60730 Class B Components



	Class B 60730 Components required to be tested on Electronic Control (see Table H.11.12.7)	Fault/error
1	1.1 CPU Registers	Stuck at
2	1.3 CPU Program Counter	Stuck at
3	2.Interrupt Handling & Execution	No Interrrupt or too frequent interrupt
4	3. Clock	Wrong frequency
5	4.1 Invariable memory	All single bit faults
6	4.2 Variable memory	DC fault
7	4.3 addressing (relevant to variable/invariable memory	Stuck at
8	5. Internal data Path	Stuck at
9	5.2 Addressing	Wrong addr
10	6 External Communications	Hamming Distance 3
11	6.3 Timing	Wrong point in time/sequence
12	7 I/O Periphery	Fault conditions specified in H.27
13	7.2.1 Analog A/D & D/A Converters	Fault conditions specified in H.27
14	7.2.2 Analog multiplexor	Wrong adressing

Appliance manufacturers are required to implement “measures” to ensure that the above components are working reliably.

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Class B Test Matrix

IEC 60730 CLASS B	Components	Registers Stuck at:	Program Counter stuck at	Interrupt handling and execution	clock	Invaraible Memory	Varaible memory	addressing Stuck at	Internal data path Stuck at	Addressing Wrong address	Hamming Distance 3	Timing	Wrong sequence	Input/Output Periphery
Acceptable measures	**Defininitions**													
Comparison of redundant CPUs be either														
reciprocal comparison,	**H.2.18.15**							X				X		
independent hardware comparator,	**H.2.18.3**							X				X		
full bus redundancy.	**H.2.18.1.1**							X						
Word protection with single bit redundancy	**H.2.19.8.2**	X	X			X	X	X	X	X				
Word protection with multi-bit redundancy including address	**H.2.19.8.1**								X		X			
Frequency monitoring	**H.2.18.10.1**				X									
Time-slot and logical monitoring,	**H.2.18.10.3**											X		
Independent time-slot monitoring or	**H.2.18.10.4**		X	X	X							X	X	
Logical monitoring of the program sequence.	**H.2.18.10.2**		X										X	
Transfer redundancy	**H.2.18.2.2**										X			
Protocol test	**H.2.18.14**													
Scheduled transmission.	**H.2.18.18**											X	X	
Periodic self-test	**H.2.16.6**													
Static memory test	**H.2.19.6**	X	X				X							
Periodic modified checksum;	**H.2.19.3.1**					X								
Multiple checksum,	**H.2.19.3.2**					X								
Periodic CRC-single word,	**H.2.19.4.1**							X	X		X			
Periodic CRC double word	**H.2.19.4.2**							X	X					
testing pattern	**H.2.18.22**							X	X	X				
Functional test	**H.2.16.5**	X	X	X										
Plausibility check	**H.2.18.13**													X

Dual MCU/CPU

ECC type

Indep. WDOG

S/W Design

Periodic
Self checks

Pre-application code

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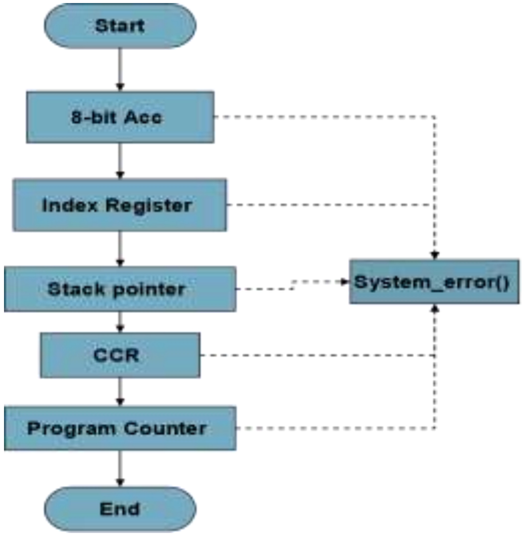
CPU Registers Stuck At

- Functional test H.2.16.5: A single channel structure in which test data is introduced to the functional unit prior to its operation.
- Periodic self-test H.2.16.6: A single channel structure in which components of the control are periodically tested during operation.
  using either:
  - Static memory test H.2.19.6: A fault/error control technique which is intended to detect only static errors.
  - Word protection with single bit redundancy H.2.19.8.2: A fault/error control technique in which a single bit is added to each word in the memory area under test and saved, creating either even or odd parity. As each word is read, a parity check is conducted.



Using #0x55 and #0xAA data
Check each CPU register for “stuck at”

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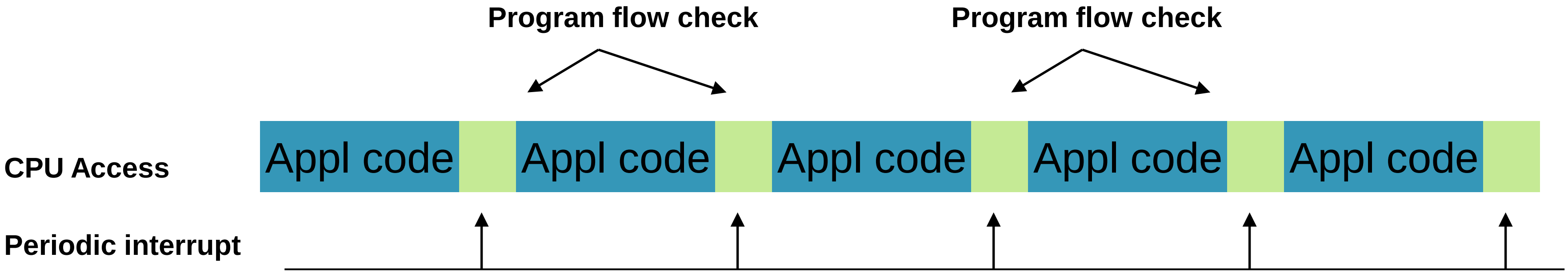
Time Slot Monitoring

- Time-slot monitoring for H.2.18.10.4: A fault/error control technique in which timing devices with an independent time base are periodically triggered in order to monitor the program function and sequence. An example is a watchdog timer.
- Covers checking and verifying of the following components:
  - CPU program counter
  - Interrupt handling
  - Clock
  - External communications
  - Timing



🟩 Time-slot monitoring; a periodic check on program code flow

A periodic interrupt, e.g. timer overflow, interrupts the application periodically, and within the ISR some checks are made.

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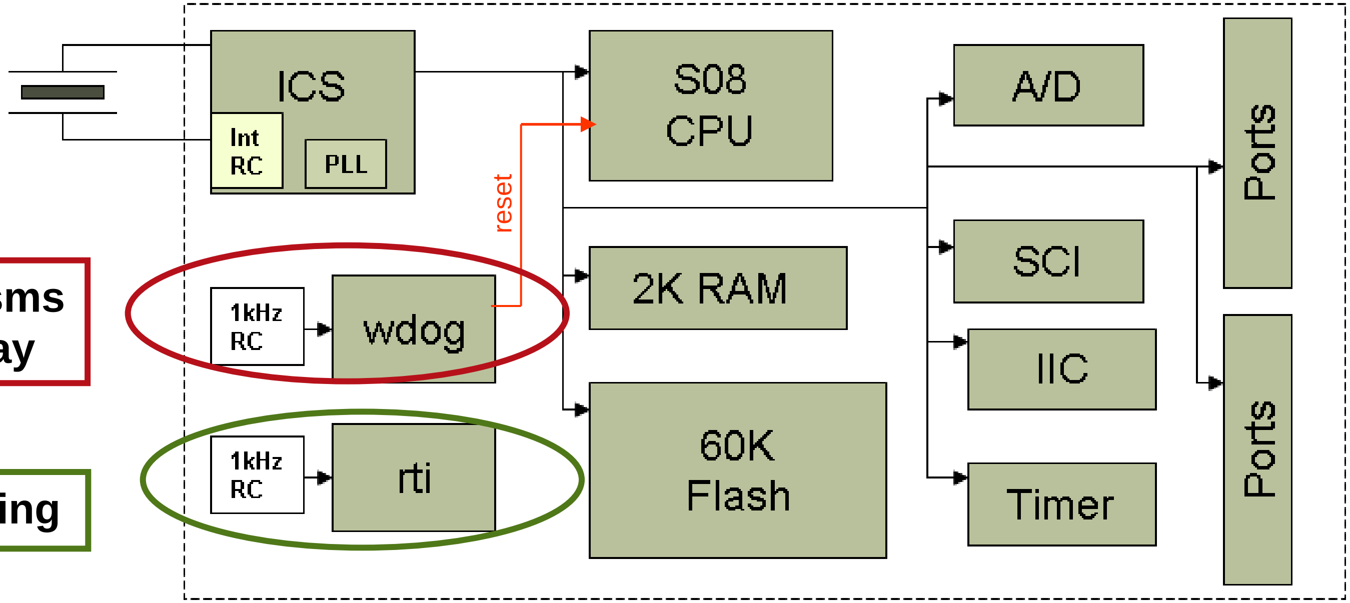
Time Slot Monitoring

- Watchdogs should and must be deployed as the backup if all other safety mechanisms fail and/or there is code runaway.
- Not really designed for periodic interrupts to execute time slot monitoring.
- A better feature is an “independently clock” timer module, e.g. S08AC60 RTI.

If all other mechanisms fail or code runaway

Time-slot monitoring



Block diagram of Freescale MC9S08AC60 microcontroller

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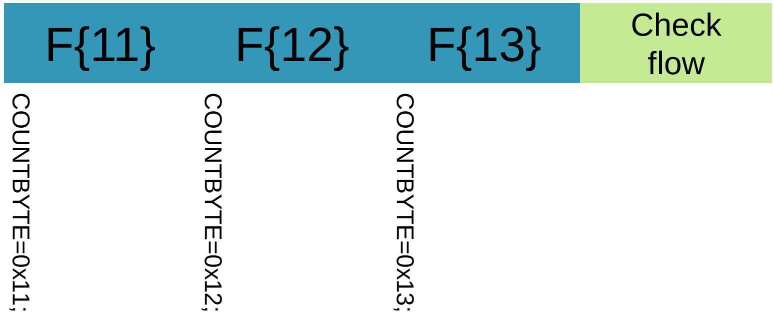
Token Passing: Program Flow

- A simple form of token passing is that you deploy a variable in RAM called COUNTBYTE and for each significant function you increment this COUNTBYTE by 1.
- On the knowledge of how long the program takes to execute these various functions, then the COUNTBYTE can be read within the ISR and compared to previous captured values.
- Caution: Within each software function it is not recommended that you increment the COUNTBYTE by a certain value, but actually set the COUNTBYTE to a fixed value.
- On real time embedded systems interrupts can occur at any random time and therefore are more difficult to monitor along with the program flow as described above. Therefore only the frequency of interrupts can be monitored then checked within the same periodic ISR routine.



```
….
If (COUNTBYTE < (previousCOUNTBYTE+2)) Error;
If (COUNTBYTE > (previousCOUNTBYTE+6)) Error;
/* program flow OK */
previousCOUNTBYTE = COUNTBYTE;
…..
```

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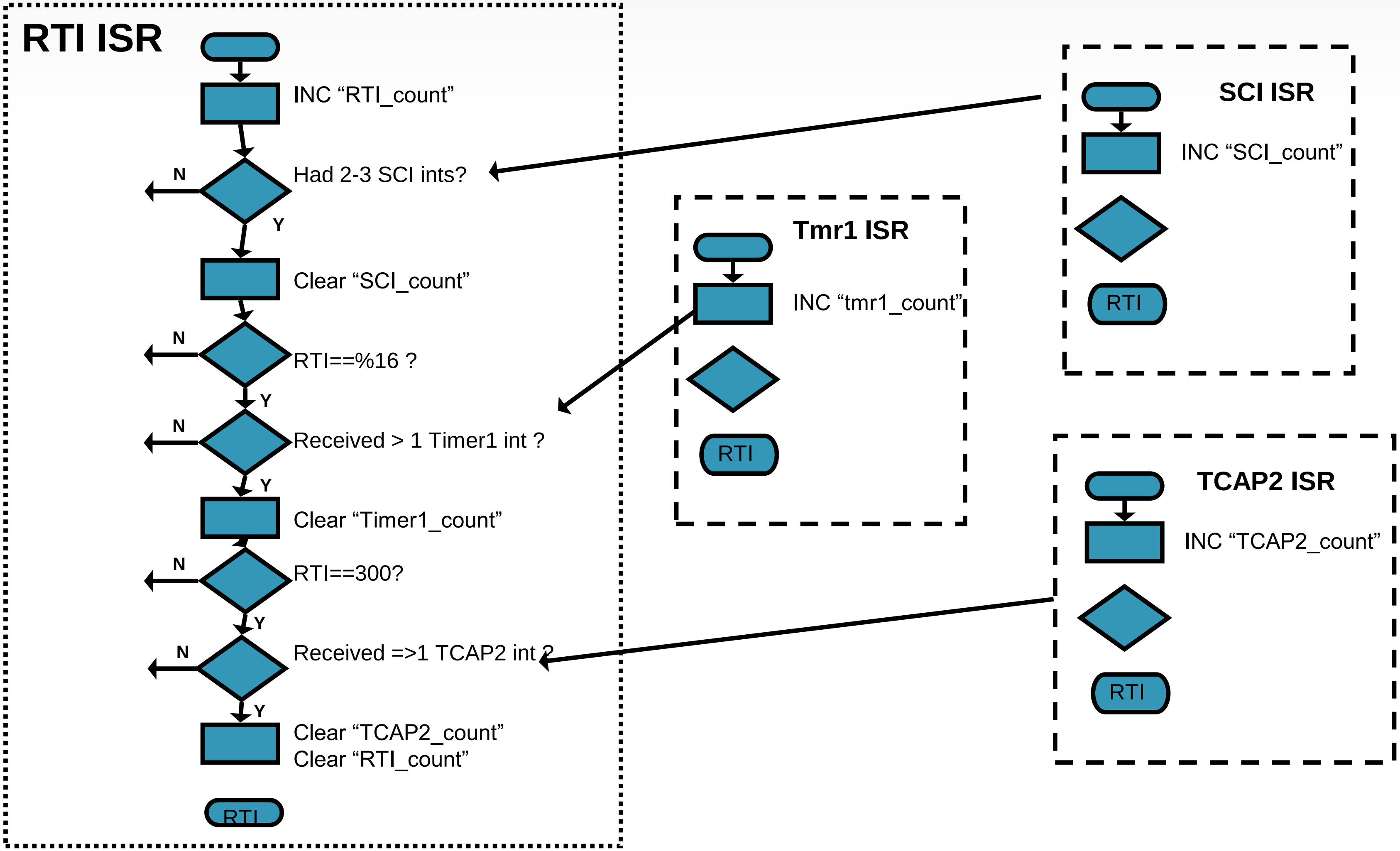
Token Passing on Interrupts



RTI ISR

INC “RTI_count”

Had 2-3 SCI ints?

Clear “SCI_count”

RTI==%16 ?

Received > 1 Timer1 int ?

Clear “Timer1_count”

RTI==300?

Received =>1 TCAP2 int ?

Clear “TCAP2_count”
Clear “RTI_count”

Tmr1 ISR

INC “tmr1_count”

SCI ISR

INC “SCI_count”

TCAP2 ISR

INC “TCAP2_count”

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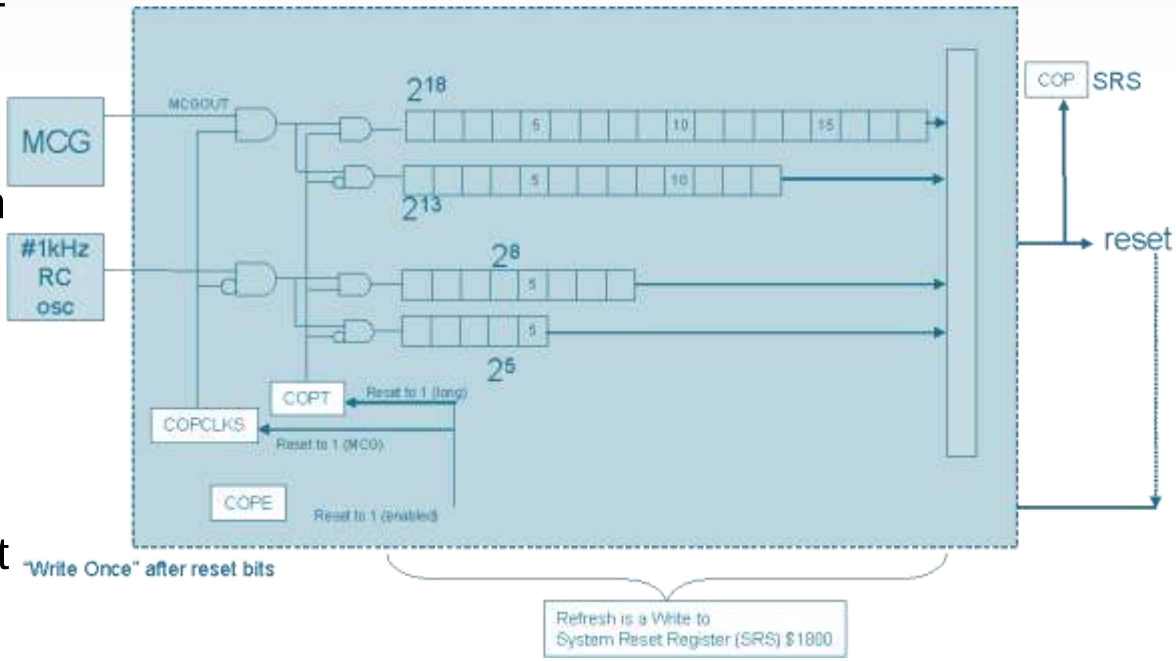
Independent Clocked Watchdog

- S08AC60 watchdog using 1 Khz RC oscillator is independent of CPU clock source
- Providing reliable protection against clock faults (too fast/slow, stuck clock) and code runaway
- Watchdog must provide a asynchronous reset to all peripherals and input/output ports
- A timeout test should be initiated after power on reset, prior to running application code



"Write Once" after reset bits

Refresh is a Write to System Reset Register (SRS) $1800

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Invariable Memory: All Single Bits Faults

- Periodic modified checksum, H.2.19.3.1: A fault/error control technique in which a single word representing the contents of all words in memory is generated and saved. During self test, a checksum is formed from the same algorithm and compared with the saved checksum. This technique recognizes all the odd errors and some of the even errors.

Or

- Multiple checksum, H.2.19.3.2: A fault/error control technique in which separate words representing the contents of the memory areas to be tested are generated and tested. During self test, a checksum is formed from the same algorithm and compared with the saved checksum for that area. This technique recognizes all odd errors and some of the even errors.

Or

- Word protection with single bit redundancy H.2.19.8.2

A CRC (16-bit) signature of the invariable memory is the preferred method of ensuring there are no single faults.

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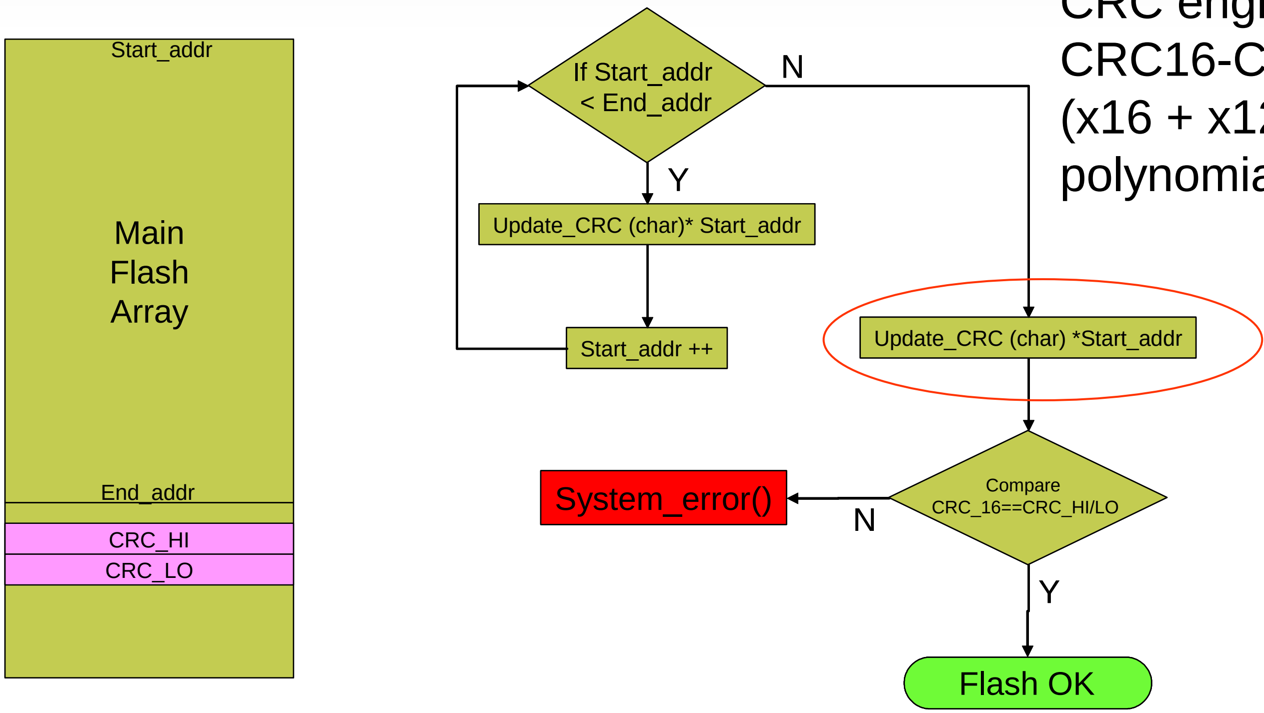
Flash CRC Test



CRC engine complying to CRC16-CCITT specification. (x16 + x12 + x5 + 1 polynomial)

>64 k H/W CRC recommended

Note:
It is recommended that one CRC 16-bit signature is reliable for detecting single bit faults flash blocks < 48 Kbytes. Large flash arrays will require multiple CRC signatures.

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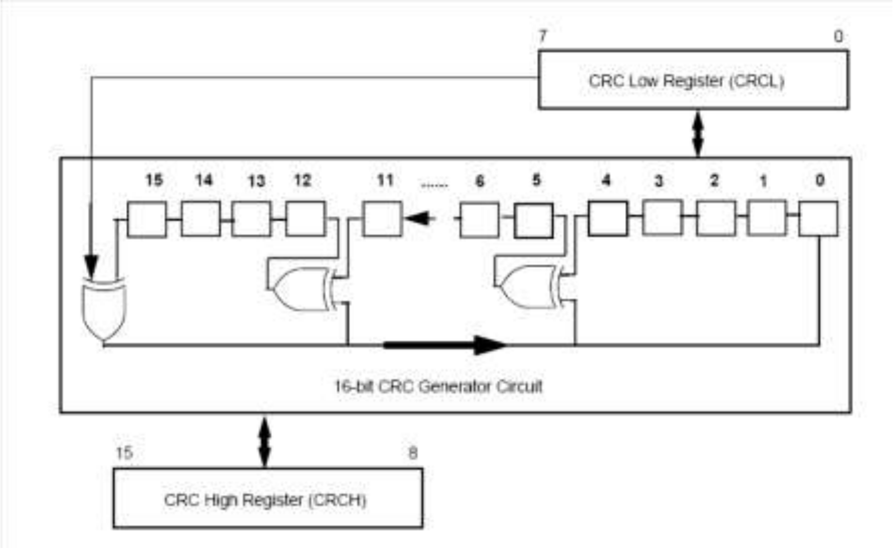
Flash CRC Test: Hardware Implementation



CRC engine complying to CRC16-CCITT specification. (x16 + x12 + x5 + 1 polynomial).

One byte shifted through CRC in 1-CPU cycles.

~ 15x faster than software implementation on an 8-bit core.

Deployed on HCS08ACxx and MCF51ACxx devices.

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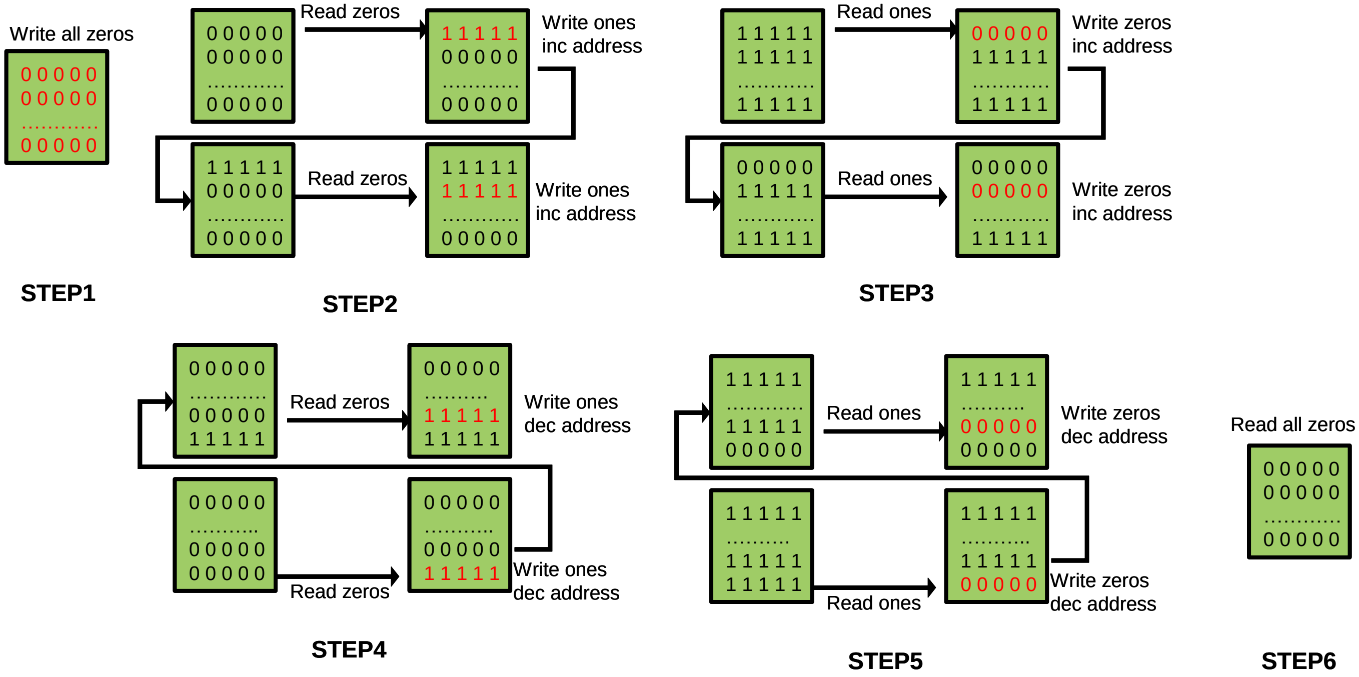
Variable Memory: DC fault

- **Periodic static memory test H.2.19.6**: A fault/error control technique which is intended to detect only static errors



or

March C (van der Goor, 1991)

- **Word protection with single bit redundancy H.2.19.8.2** (hardware error code correction)

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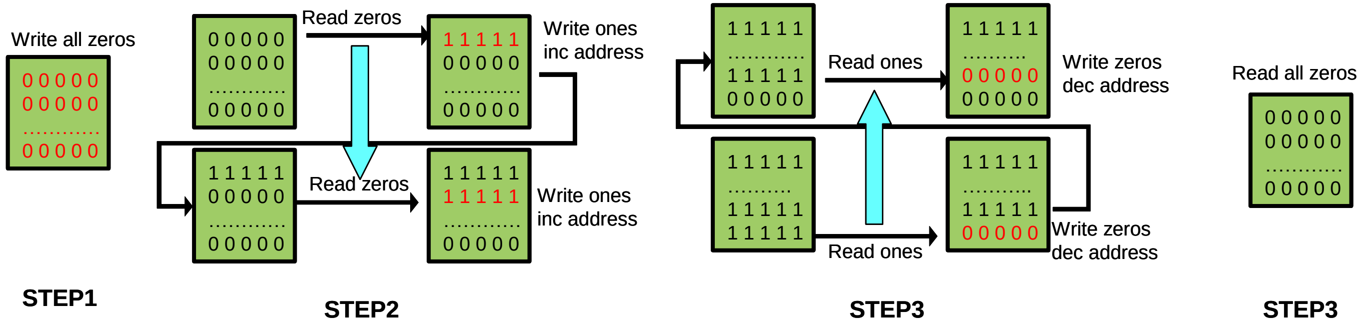
March X Pattern



Write all zeros

00000
00000
....
00000

STEP1

00000
00000
....
00000

Read zeros

11111
00000
....
00000

Write ones inc address

11111
00000
....
00000

Read zeros

11111
11111
....
00000

Write ones inc address

STEP2

11111
....
11111
00000

Read ones

11111
....
00000
00000

Write zeros dec address

11111
....
11111
11111

Read ones

11111
....
11111
00000

Write zeros dec address

STEP3

Read all zeros

00000
00000
....
00000

STEP3

March X pattern is a subset of the March C pattern, which detects the majority of failure mechanisms of the March C but with a faster execution time.

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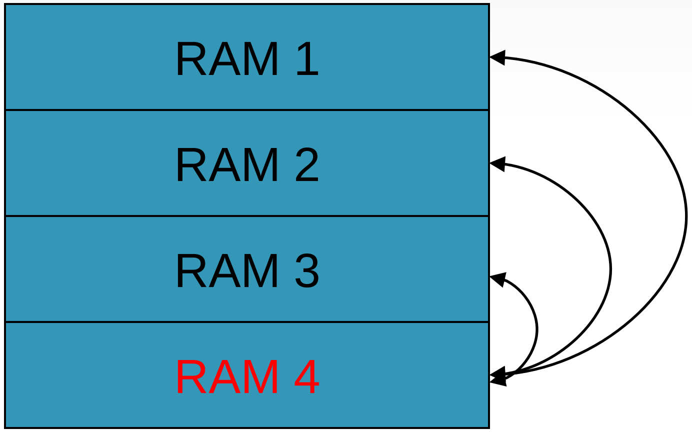
Transparent March

- Split RAM into four segments
- Fourth segment is “shadow” RAM used to temporarily store other segments variables until March test completed.
- At a convenient time, complete the following:
  - RAM 1 copy to RAM 4
  - Verify copy is successful
  - Deploy MARCH test on RAM 1
  - Copy RAM 4 to RAM 1
  - Verify copy is successful
  - Deploy normal application code



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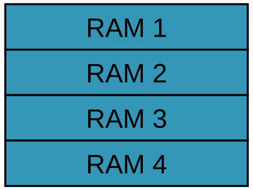
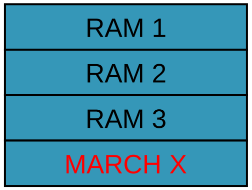
Making “Destructive” into “Transparent”



RAM 1
RAM 2
RAM 3
RAM 4

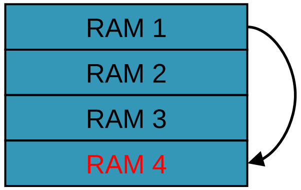
Segment RAM

Redundant RAM segment



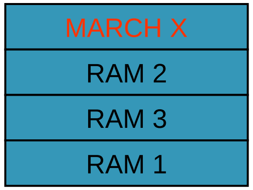
RAM 1
RAM 2
RAM 3
MARCH X

March X on RAM4



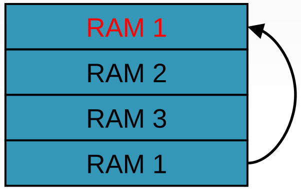
RAM 1
RAM 2
RAM 3
RAM 4

Copy RAM1 to RAM4.
Verify data copied.



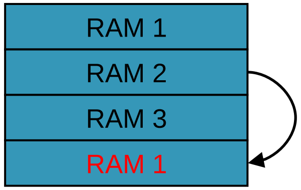
MARCH X
RAM 2
RAM 3
RAM 1

March X on RAM1



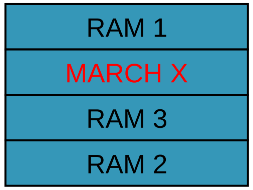
RAM 1
RAM 2
RAM 3
RAM 1

Copy RAM4 to RAM1.
Verify data copied.



RAM 1
RAM 2
RAM 3
RAM 1

Copy RAM2 to RAM4.
Verify data copied.



RAM 1
MARCH X
RAM 3
RAM 2

March X on RAM2

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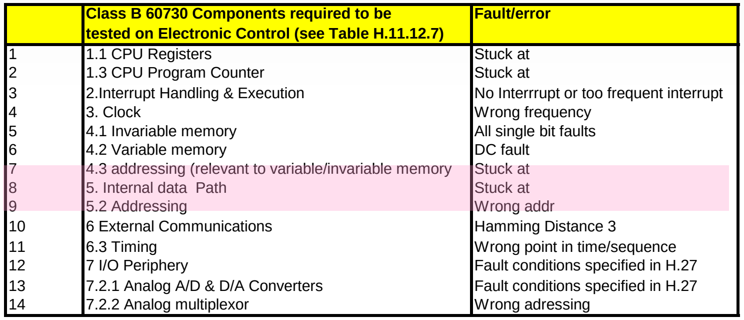
Class B Memory Address and Data Path



	Class B 60730 Components required to be tested on Electronic Control (see Table H.11.12.7)	Fault/error
1	1.1 CPU Registers	Stuck at
2	1.3 CPU Program Counter	Stuck at
3	2.Interrupt Handling & Execution	No Interrrupt or too frequent interrupt
4	3. Clock	Wrong frequency
5	4.1 Invariable memory	All single bit faults
6	4.2 Variable memory	DC fault
7	4.3 addressing (relevant to variable/invariable memory	Stuck at
8	5. Internal data Path	Stuck at
9	5.2 Addressing	Wrong addr
10	6 External Communications	Hamming Distance 3
11	6.3 Timing	Wrong point in time/sequence
12	7 I/O Periphery	Fault conditions specified in H.27
13	7.2.1 Analog A/D & D/A Converters	Fault conditions specified in H.27
14	7.2.2 Analog multiplexor	Wrong adressing

- 4.3 Addressing

(relevant to variable and invariable memory) stuck at

- 5. Internal data path stuck at
- 5.2 Addressing: Wrong address

These components intended for external memory microprocessor based designs. These components are tested by other measures on single chip microcontrollers.

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External Communications

Hamming Distance 3

- **Word protection with multi-bit redundancy including address H.2.19.8.1.**

Or

- **CRC-single word, H.2.19.4.1**: A fault/error control technique in which a single word is generated to represent the contents of memory. During self test the same algorithm is used to generate another signature word which is compared with the saved word. The technique recognizes all one-bit, and a high percentage of multi-bit, errors.

Or

- **Transfer redundancy H.2.18.2.2**: A form of code safety in which data is transferred at least twice in succession and then compared. This technique will recognize intermittent errors.

Or

- **Protocol test H.2.18.14**: A fault/error control technique in which data is transferred to and from computer components to detect errors in the internal communications protocol.

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Plausibility Check

- 7. I/O Periphery: Fault conditions specified in H.27
- 7.2.1 A/D & D/A converters: Fault conditions specified in H.27
- 7.2.2 Analog Multiplexer: Wrong addressing

Plausibility check H.2.18.13: A fault/error control technique in which program execution, inputs or outputs are checked for inadmissible program sequence, timing or data. Examples are the introduction of an additional interrupt after the completion of a certain number of cycles or checks for division by zero.

I/O Periphery: For digital outputs, checks can be made to verify no short circuits or open circuits between adjacent signals and power supply. Manufacturers will utilize redundant input pins on MCUs to check on key signal pins that a short or open-circuit would lead to a hazard.
For analogue signals A/D and D/A checks on the boundary limits of the absolute value should be made.
For example, an input A/D pin should only see a small range of values with the full voltage conversion range, any value outside would be ignored in software.
Analogue multiplexers: Today most manufacturers will need to have the capability to provide a known d.c. value to all input A/P pins. This allows test software to check the multiplexer is working. Future analogue multiplexers should provide additional redundant channels on each pin so that a comparison between two channels can be made to verify that the multiplexer is working as expected.

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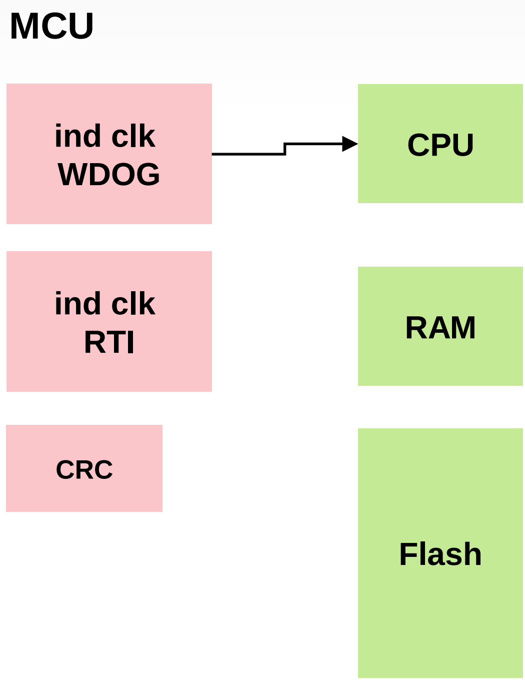
Class B Generic MCU Requirements Summary



MCU

ind clk WDOG

ind clk RTI

CRC

CPU

RAM

Flash

Software

- CPU register “SA faults” test
- March C and MARCH X (transparent) RAM test
- Modified checksum or CRC flash test
- Independent WDOG test
- Plausibility tests for key digital and analogue I/O signals
- Time slot monitoring of program flow and interrupt behavior
  - Token passing
  - Independent RTI

Hardware

- Independent clocked WDOG
- Independent real time interrupt
- Nice to have
- CRC engine for 64K+ memory devices
- Loss of clock/lock reset

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60730 Class C: Components to Be Tested

	Class C 60730 Components required to be tested on Electronic Control (see Table H.11.12.7)	Fault/error
1	1.1 CPU Registers	DC fault
2	1.3 CPU Program Counter	Stuck at
3	1.2 CPU Instruction Decoding & Execution	Wrong decoding or execution
4	2. Interrupt Handling & Execution	No Interrupt or too frequent interrupt
5	3. Clock	Wrong frequency
6	4.1 Invariable Memory	99.6% coverage of all info errors
7	4.2 Variable Memory	DC fault & dynamic cross links
8	4.3 Addressing (relevant to variable/invariable memory	Stuck at
9	5. Internal Data Path	Stuck at
10	5.2 Addressing	Wrong addr
11	6 External Communications	Hamming distance 4
12	6.3 Timing	Wrong point in time/sequence
13	7 I/O Periphery	Fault conditions specified in H.27
14	7.2.1 Analog A/D & D/A Converters	Fault conditions specified in H.27
15	7.2.2 Analog Multiplexer	Wrong addressing

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Class C Test Matrix

Components →

Optional Measures ↓

Acceptable measures	Defininitions	1.1 Registers:DC fault	1.2Wrong decoding & execution	1.3 Program Counter Stuck at	1.4 Addressing: DC Fault	1.5 Data paths instr. Decodeing: DC fault & execution	2. Interrupt handling &execution	3.Clock	4.1 Invariable memory:99.6% of all infor errors	Variable memory: DC fault dynamic cross links	4.3 addressing oboth variable & invariabl:dc fault	5.Internal Data path: DC fault	5.2 Wrong address	6. External Comms: hamming dist 4	6.2 Addressing	6.4 Timing	7.I/O Periphery	7.2 Analog
Comparison of redundant CPUs by either			1		1													
-reciprocal comparison	H.2.18.15	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
-independent hardware comparator,	H.2.18.3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
input comparison	H.2.18.8																X	X
multiple parallel outputs	H.2.18.11																X	X
output verification	H.2.18.12																X	X
testing pattern	H.2.18.22																X	X
code safety	H.2.18.2																X	
Internal error detection,	H.2.18.9	X	X			X												
redundant memory with comparison,	H.2.19.5	X							X	X								
Periodic self-test using either																		
- walkpat memory test	H.2.19.7	X								X								
- Abraham test	H.2.19.1	X								X								
- transparent GALPAT test	H.2.19.2.1	X								X								
word protection with multi-bit redundancy	H.2.19.8.1	X							X	X	X	X	X		X			
including the address, or data redundancy,	H.2.18.2.1											X	X	X				
static memory test and word protection	H.2.19.6	X																
with single bit redundancy	H.2.20.8.2	X																
Periodic self-test using equivalence class test	H.2.18.5		X															
Periodic self-test and monitoring using either	H.2.16.7			X	X	X												
-independent time-slot and logical monitoring	H.2.18.10.3			X			X									X		
- internal error detection	H.2.18.9			X														
the address lines	H.2.18.22				X	X					X	X	X					
full bit bus parity including the address	H.2.18.1.1				X						X				X			
Periodic self-test using a testing pattern of:multibit parity	H.2.18.1.2					X												
Frequency monitoring	H.2.18.10.1							X										
time-slot monitoring	H.2.18.10.4							X								X		
crc -single word	H.2.19.4.1								X		X				X			
crc -double word	H.2.19.4.2								X		X			X	X			
protocol test	H.2.18.14											X			X			
transfer redundancy	H.2.18.2.2														X			
scheduled transmission	H.2.18.18															X		
Logical monitoring	H.2.18.10.2															X		

Dual MCU/CPU/channel

ECC type

Periodic
Self checks

S/W Design

Indep. WDOG

S/W Design

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1.2 Instruction Decoding And Execution

Acceptable measures are:

1.2 Instruction decoding and execution	Wrong decoding and execution	rq	Comparison of redundant CPUs by either • Reciprocal comparison • Independent hardware comparator • Internal error detection • Periodic self-test using equivalence class test	Or	H.2.18.15 H.2.18.3 H.2.18.9 H.2.18.5

IEC 60730 Class C Requirement to test Instruction Decoding & Execution.

Acceptable measure to test is:

Periodic self-test using equivalence class test

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H.2.18.5 Equivalence Class Test

A systematic test intended to determine whether the instruction decoding and execution are performed correctly. The test data is derived from the CPU instruction specification.

Similar instructions are grouped and the input data set is subdivided into specific data intervals (equivalence classes) Each instruction within a group processes at least one set of test data, so that the entire group processes the entire test data set. The test can be formed from the following:

- Data from a valid range

- Data from invalid range

- Data from the bounds

- Extreme values and their combinations

The tests within a group are run with different addressing modes, so that the entire group executes all addressing modes.

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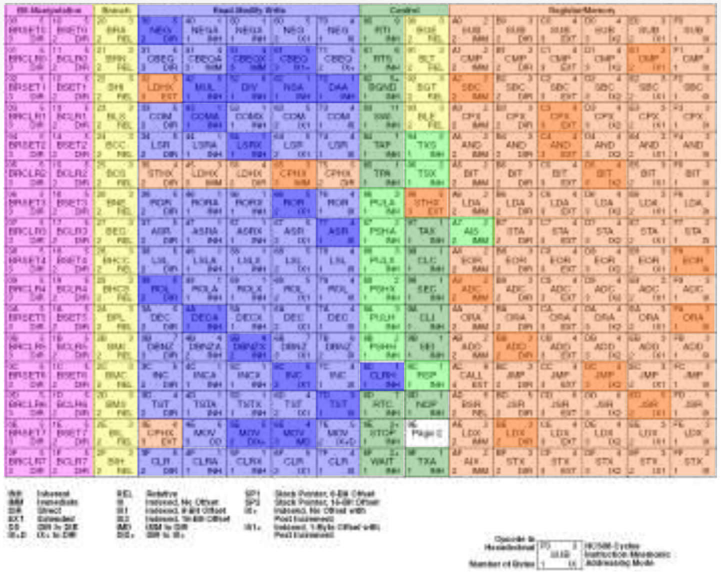
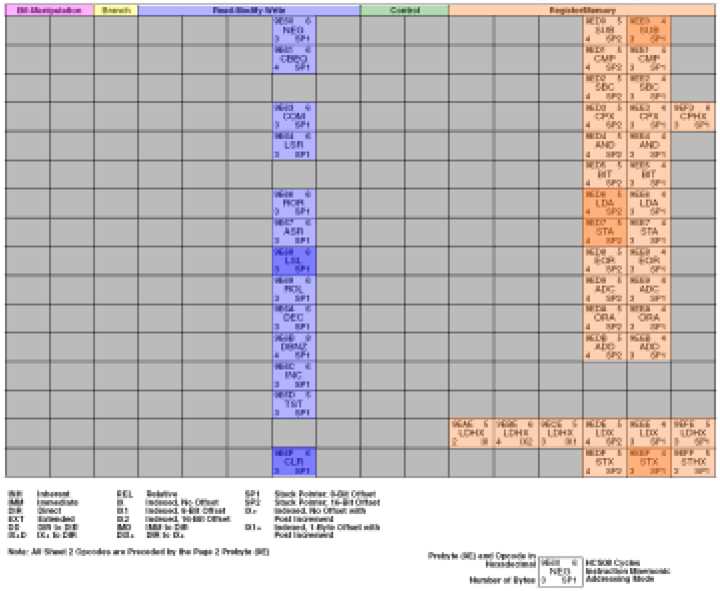
S08 CPU Instruction Grouping

The S08 instructions were analysed and placed into the 6 different groups (as shown in Instruction map diagrams below):

1. Register/Memory Tests
2. Control
3. Read Modify Write
4. Branch
5. Bit Manipulation
6. Stack Pointer


Bit Manipulation
Branch
Read Modify Write
Control
Register/Memory


Bit Manipulation
Branch
Read Modify Write
Control
Register/Memory

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S08 CPU Instruction Test

- Memory Footprint: 2148 bytes (this can be reduced if instructions are not utilised in application code)
- Execution Time: 3666 CPU BUS cycles (183.3 µs at 20 MHz)
- Reviewed, tested and certified by Tuev-Sued GmbH

- Instructions not tested (as they require hardware considerations):
  - STOP WAIT BGND BIH BIL RSP SWI

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4.2 Variable Memory

Acceptable measures for class C systems are:

4.2 Variable memory	DC fault and dynamic cross links	rq	Comparison of redundant CPUs by either		
			• Reciprocal comparison	Or	H.2.18.15
			• Independent hardware comparator,	Or	H.2.18.3
			Redundant memory with comparison	Or	H.2.19.5
			Periodic self-test using either		
			• Walkpat memory test		H.2.19.7
			• Abraham test		H.2.19.1
			• Transparent GALPAT test	Or	H.2.19.2.1
			Word protection with multi-bit redundancy	Or	H.2.19.8.1

- IEC 60730 Class C Requirement to test variable memory(RAM) for DC faults
- Acceptable measure to test is:
  - Periodic self-test using “walkpat memory test”

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H.2.19.7 Equivalence Class Test

H.2.19.7 walkpat memory test

A fault/error control technique in which a standard data pattern is written to the memory area under test as in normal operation. A bit inversion is performed on the first cell and the remaining memory area is inspected. Then the first cell is again inverted and the memory inspected. This process is repeated for all memory cells under test. A second test is conducted by performing a bit inversion of all cells in memory under test and proceeding as above.

This technique recognises all static bit errors as well as errors in interfaces between memory cells.

A walking 1s pattern followed by a walking 0s pattern

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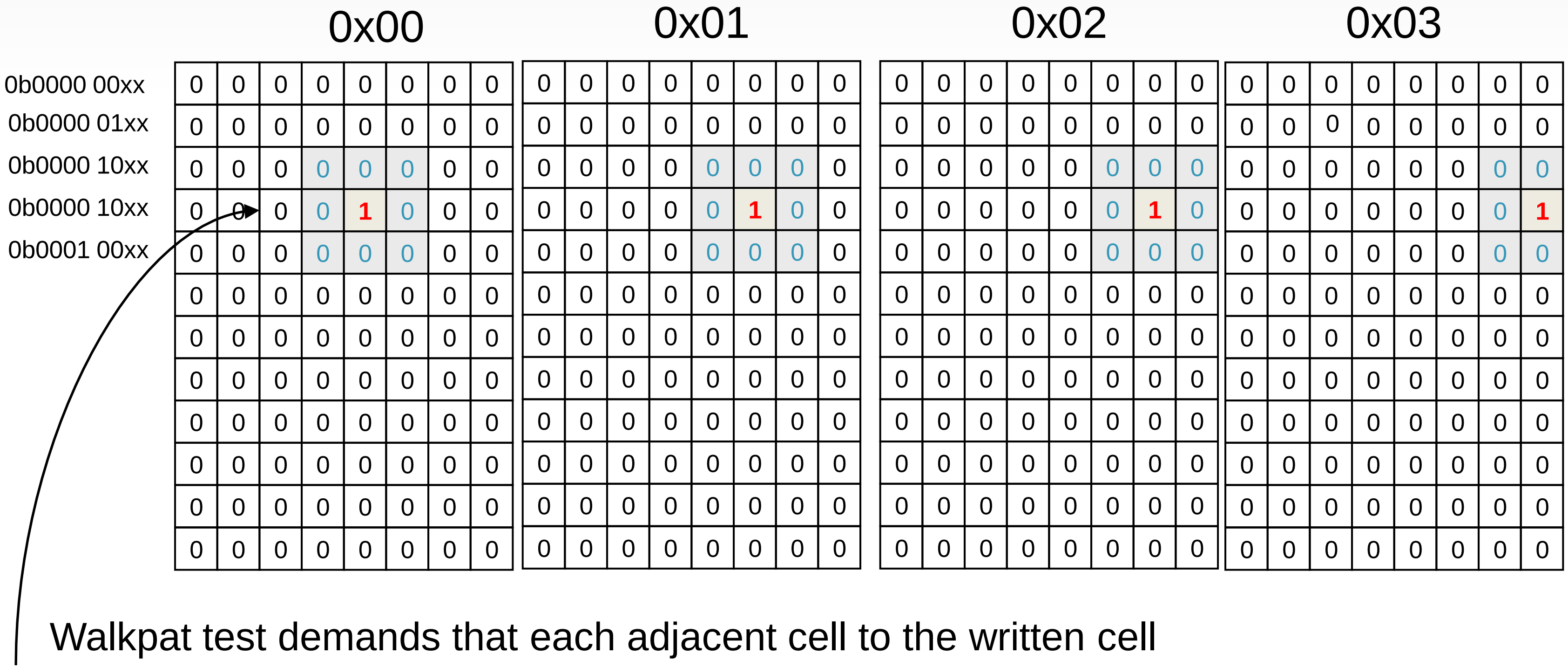
Walkpat RAM Test



0x00

0b0000 00xx	0	0	0	0	0	0	0	0
0b0000 01xx	0	0	0	0	0	0	0	0
0b0000 10xx	0	0	0	0	0	0	0	0
0b0000 10xx	0	0	0	0	1	0	0	0
0b0001 00xx	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0

0x01

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

0x02

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

0x03

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Walkpat test demands that each adjacent cell to the written cell
Is checked to have the opposite state.

Two things are required to ensure speedy execution times in application:
1) RAM split into sizeable segments
2) Need to understand the RAM topology to ensure that the walking 1s pattern is testing the adjacent cells as intended.

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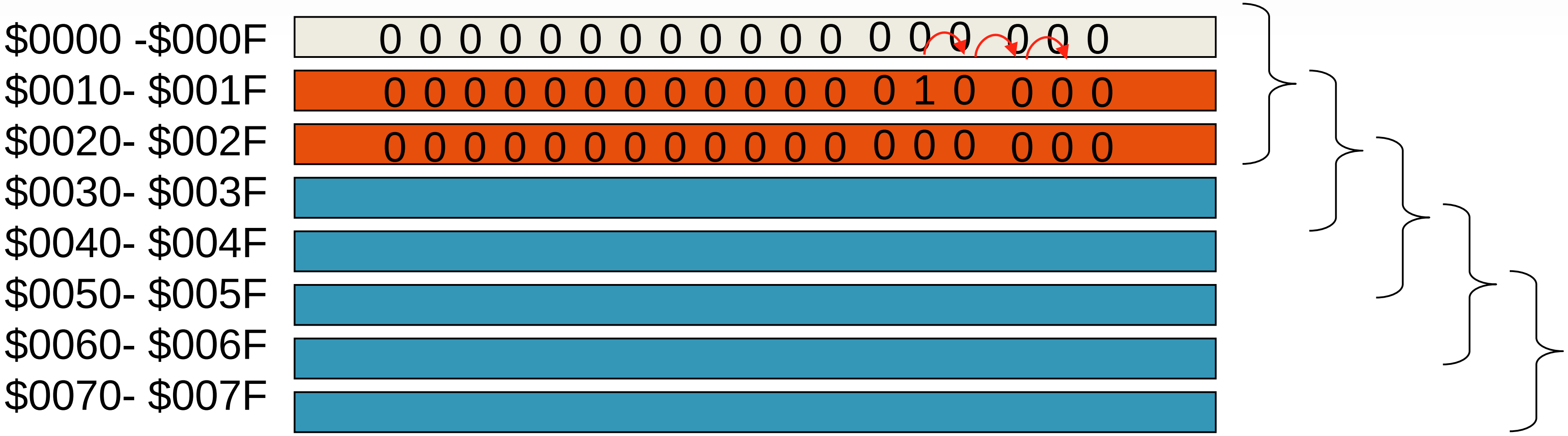
Walking 1s



$0000 -$000F 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

$0010- $001F 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0

$0020- $002F 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

$0030- $003F

$0040- $004F

$0050- $005F

$0060- $006F

$0070- $007F

0 0 0
0 1 0
0 0 0

When cell set to 1
the 8 adjacent cells to the
test cell are verified to be 0.

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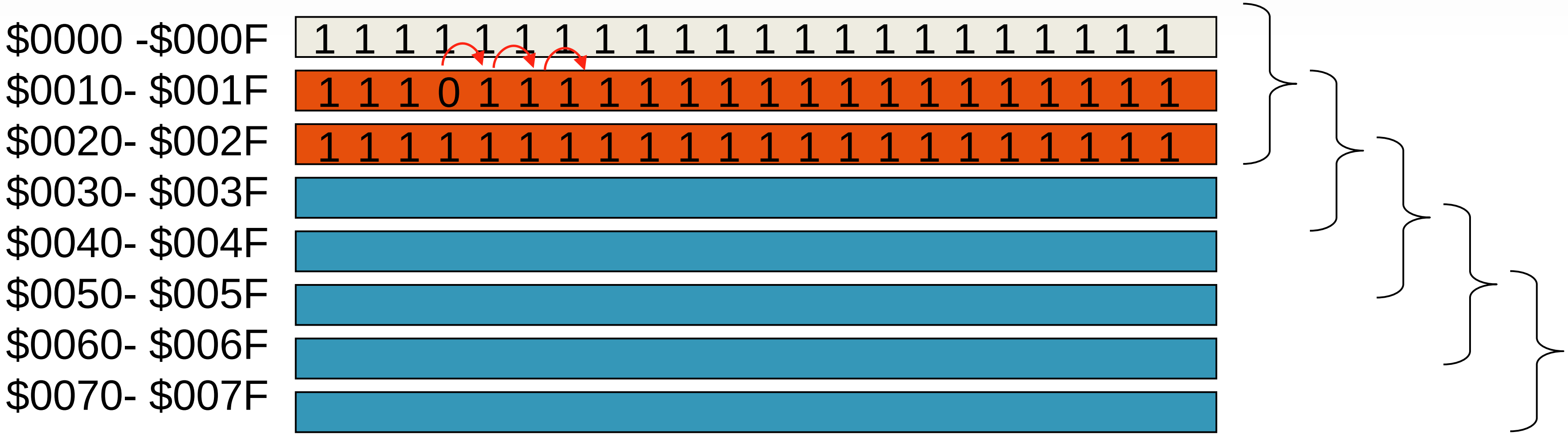
Walking 0s



$0000 -$000F 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$0010- $001F 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$0020- $002F 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$0030- $003F
$0040- $004F
$0050- $005F
$0060- $006F
$0070- $007F

```
1 1 1
1 0 1
1 1 1
```

When cell set to 0
the 8 adjacent cells to the
test cell are verified to be 1.

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Walking 1s RAM Test

- Memory footprint: Walking 1s only: 1245 bytes
  Walking1s and 0s: 2174 bytes

- Execution time for 16 byte row:
- Walking1s 12544 CPU cycles (627uS @20 Mhz)
- Walking1s+0s 27016 CPU cycles (1.35ms @20 Mhz)

- Execution time for 2048 bytes (16 bytes at a time)
- Walking 1s+0s 2.765 seconds @20 Mhz

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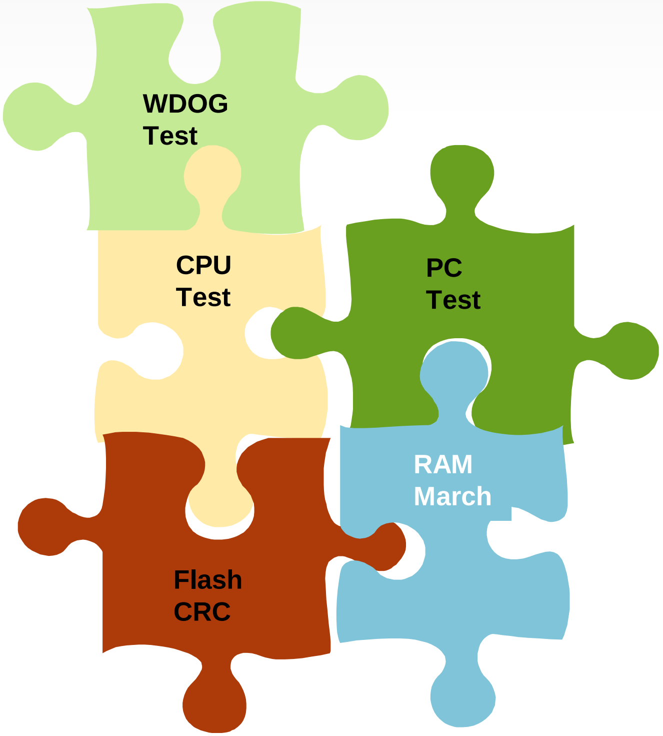
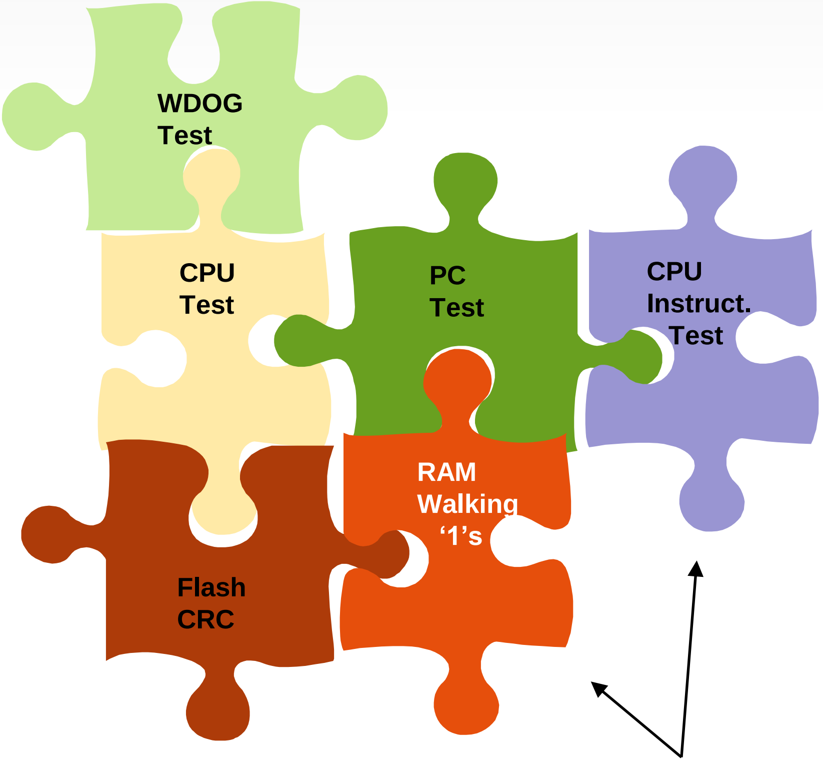
Freescale Will Provide Pieces of the 60730 Jigsaw



Class B Routines



Class C Routines

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Example Roadmap: Legend Horizontal

Features	Class B	Class C
32-bit	Kinetis 2013 ColdFireV1	ColdFireV1
16-bit	DSC	DSC
8-bit	S08AC > SO8P	S08AC > SO8P

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Generic MCU Requirements for IEC/UL 60730

Class B

Hardware

Independent clocked WDOG
Independent real time interrupt

Software

CPU register "SA faults" test

March C and MARCH X (transparent) RAM test

Modified checksum or CRC flash test

Independent WDOG / RTI test

Plausibility tests

Time slot monitoring of program flow and interrupt behavior

Class C

Hardware

Independent clocked WDOG

Independent real time interrupt

2nd CPU or RAM error correction coding

CRC engine

Software

CPU register "walkpat" test

CPU instruction set test

GALPAT/walking 1's RAM test

CRC flash test

Independent WDOG / RTI test

Plausibility tests

Time slot monitoring of program flow and interrupt behavior

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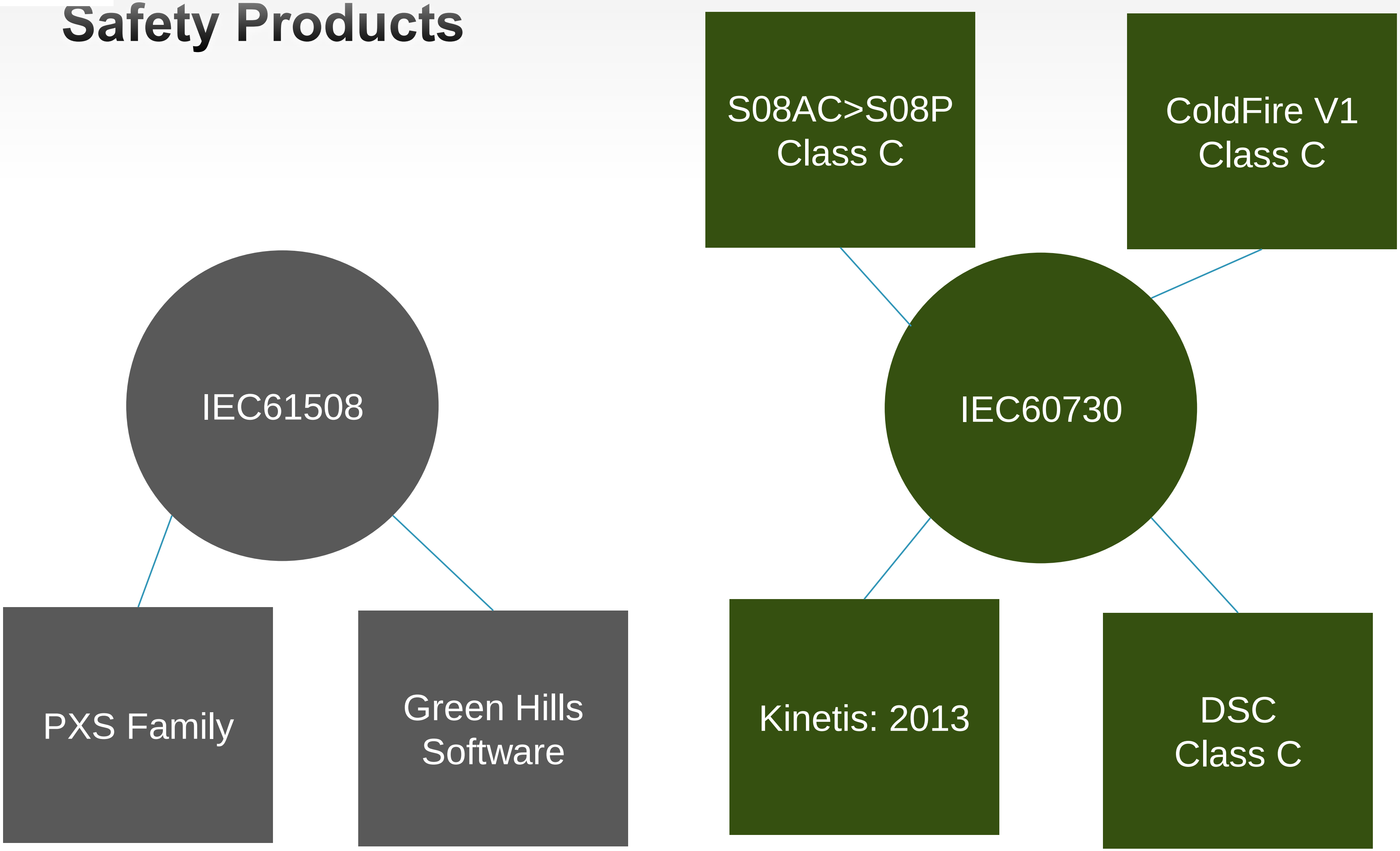
Safety Products



IEC61508

PXS Family

Green Hills Software

IEC60730

S08AC>S08P Class C

ColdFire V1 Class C

Kinetis: 2013

DSC Class C

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Q&A

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