KUGA7048N

Hardware Design
Engineering Specification

12/09, 2013

Editor: Matt Kuo

KUGA7048N-R
Hardware Design Engineering Specification

Table of Contents

Revision History

Rev	Date	Description		Editor
0.1	10/03/2013	Initial draft		Matt.Kuo
		5.2 CPLD of Main Board via IIC2:	Not-reliable	
0.2	10/25/2013	Add I2C Registers		Matt.Kuo
0.3	12/01/2013	Uniform the register for series projects		Matt.Kuo
	1.	Rename “Main board” to “Switch Board”		
	2.	Rename “MainCPLD” to “SWPLD”		
	3.	3.5 CPU IRQ definition		
	4.	5.2. CPLD of CPU Board via local bus		

Reference Documents

1. BCM56844Advance Data Sheet, 640 Gbps Ethernet Multilayer Swtich, Rev. 01, Aug. 21, 2009, Broadcom Corporation

2. BCM5461S Preliminary Data Sheet, Single-Chip 10/100/1000Base-T Gigabit Ethernet Transceiver, Rev.2 03, May 12, 2009, Broadcom Corporation

3. P2020- Freescale Semiconductor P2010QorIQ Integrated Processor Hardware Specifications Rev.0 04/2011,

4. Hot Swap controller LTC4125 datasheet
http://www.linear.com/pc/productDetail.jsp?navId=H0,C1,C1003,C1006,C1163,P17572

5. NOR Flash S29GL01GP12TFI010 Spansion Inc.

6. ALTERA EPM1270F256 design guideline
http://www.altera.com/literature/an/an428.pdf

7. ALTERA MAX V 5M1270ZF324 JTAG and In-System Programmability
http://www.altera.com/literature/hb/max2/max2_mii51003.pdf

8. TI TMP75 thermal sensor
http://focus.ti.com/lit/ds/symlink/tmp175.pdf

9. FAN Controller MAXIM MAX6620
http://datasheets.maxim-ic.com/en/ds/MAX6650-MAX6651.pdf

10. BCM84328 Dual 40G channels with two XLPPI-to-XLAUI/KR4 ports supporting SR4/LR4/CR4 QSFP+Retimer/Equalization applications
The document connect please contact with Broadcom CORP

1. Rerview

The KUGA7048N platform has 640Gbps switching bandwidth. It supports forty-eight 10GbE SFP+ ports.

Feature

- Forty-eight 10Gbps ports for 1G/10G transceiver.
- 2 PSU.
- 2 FAN Sets.
- LED display for System, FAN and power status indicates.
- On board high performance CPU system with large memory.
- Software readable thermal monitor.

KUGA7048N	
CPU	P2020
MAC	BCM56844
PHY (Management Port)	BCM5461S

There are 3 boards in KUGA7048N. One is CPU Board (CPU BD), one is Switch Board (Main BD), the other FAN Board (FAN BD).

- CPU Board (CPU BD) has P2020 as CPU and a CPLD (EPM1270F256) to handle some interrupts and enable some devices, and a RTC circuit. P2020 use PCIe interface to communication with MAC (BCM56844), and use SGMII to communication with BCM5461S, one UART interface as a console port, IIC interface to control other devices.
- Switch Board (Main BD) has a MAC (BCM56844), and a CLPD (5M1270ZF324) as control LED and SFP port control signals.
- FAN Board (FAN BD) has 2 FAN Speed-controller (MAX6620).

2. Functionality

2.1. System Blockdiagram

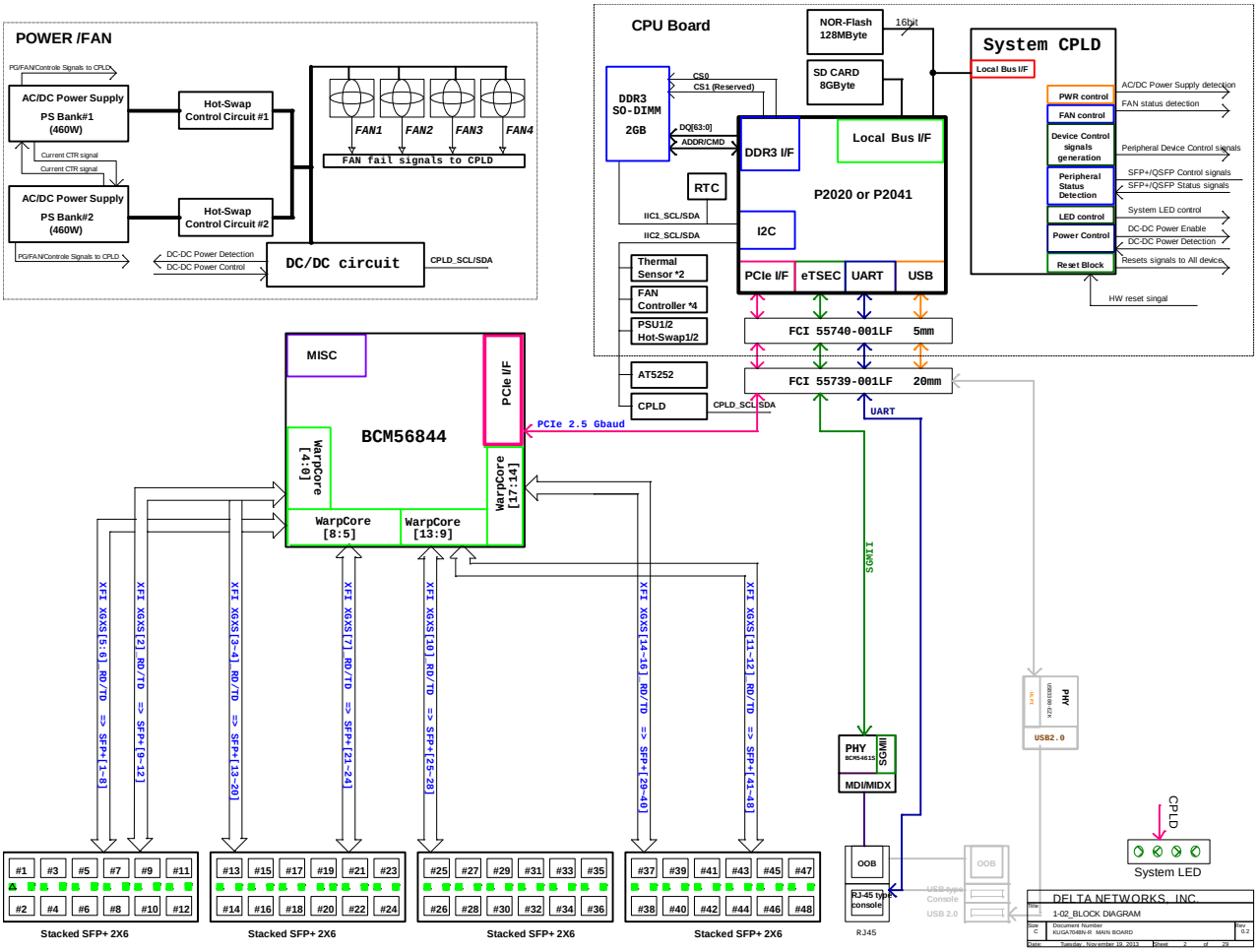


Figure 1: System blockdiagram

In KUGA7048N, there are several subsystem topics to discuss: CPU subsystem including Flash and DDR, Switching Subsystem, CPLD Subsystem, Power Subsystem, Reset Subsystem, Clock system, SFP+ port, I2C,LED, Thermal, HOT-SWAP, RTC, and Serial Console.

3. CPU Subsystem

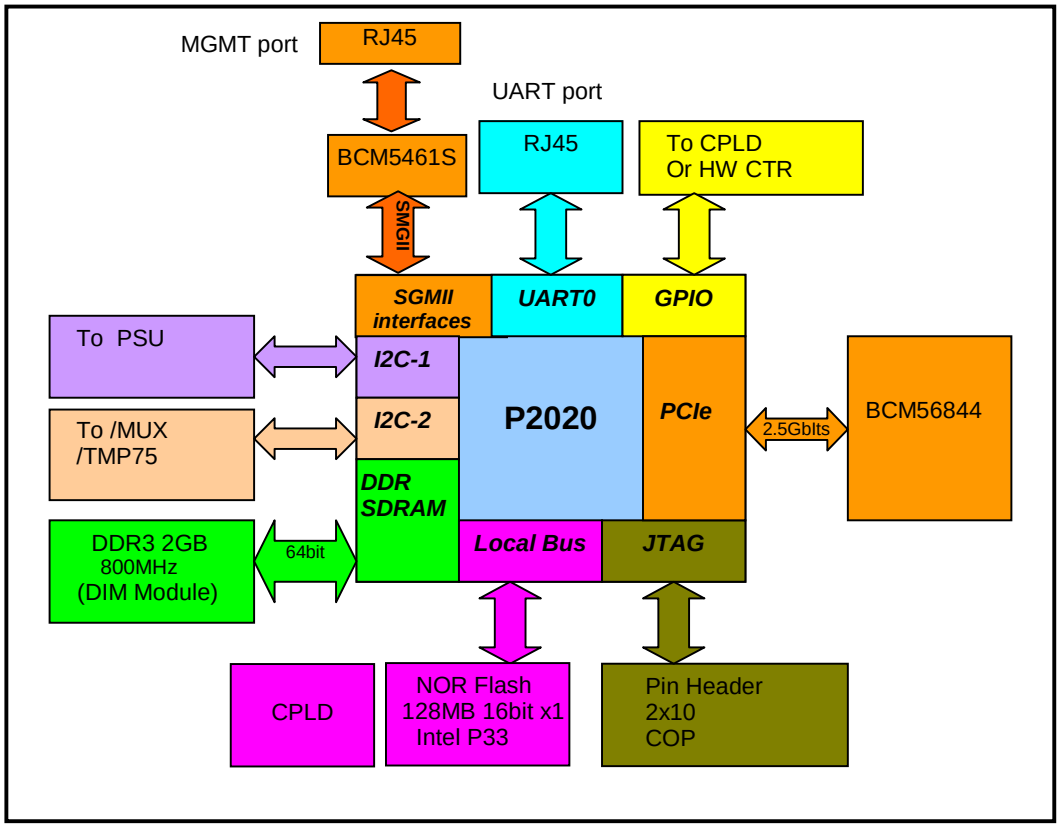


Figure 2: CPU board

3.1. CPU, P2020

The KUGA7048N is design with Freescale *P2020* chipset. The P2020 combines dual Power Architecture™ e500v2 processor cores with system logic required for networking, wireless infrastructure, and telecommunications applications. The P2020 offers an excellent combination of protocol and interface support including dual high-performance CPU cores, a large L2 cache, a DDR2/DDR3 memory controller, three enhanced three-speed Ethernet controllers with SGMII support, two Serial RapidIO® interfaces with a messaging unit, a secure digital interface, a USB 2.0 interface, and three PCI Express® controllers. The device also supports the IEEE 1588™ precision time protocol for network synchronization over Ethernet.

P2020 TePBGA Major Feature

- *Dual* Core high-performance Power Architecture e500 cores.
- 36-bit physical addressing.
- 512 Kbyte L2 cache with ECC. Also configurable as SRAM and stashing memory.
- High-speed interfaces supporting various multiplexing options
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Three PCI Express interfaces
  - Two Serial RapidIO interfaces
  - Two SGMII interfaces

- Enhanced secure digital host controller (SD/MMC)
- RSA/ECC, RNG, single-pass SSL/TLS, Kasumi
- 64-bit DDR2/DDR3 SDRAM memory
- ECC support
- Programmable interrupt controller (PIC)
- OpenPIC standard
- Two four-channel DMA controllers
- Two I2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals

Functions Diagram

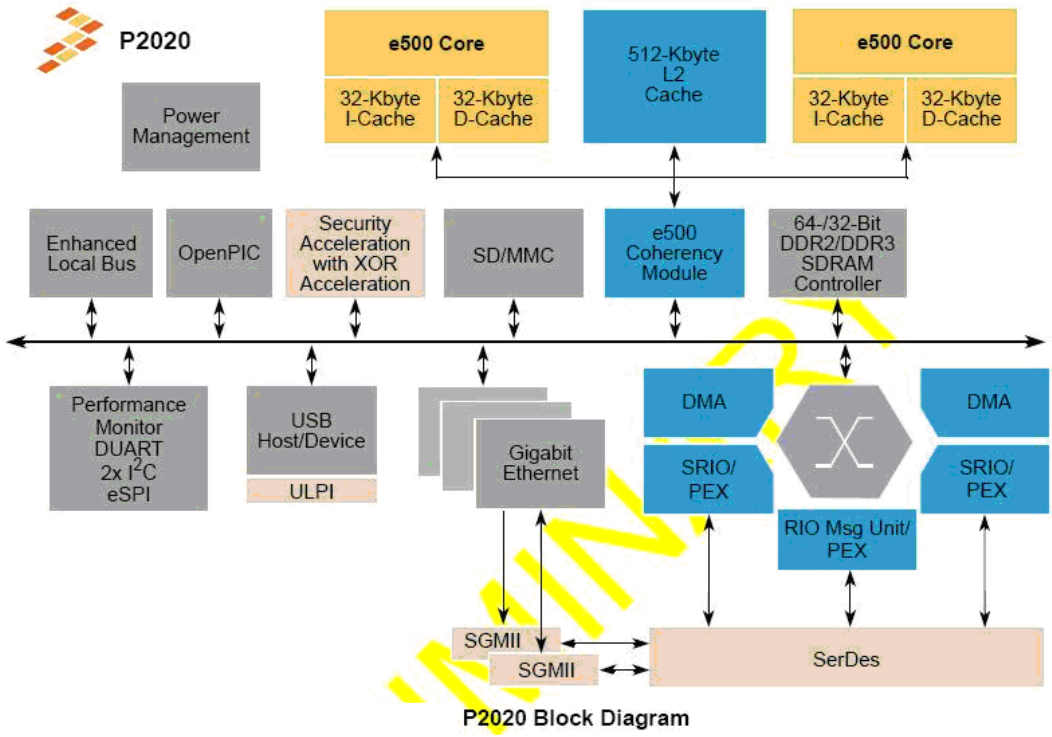


Figure 3: P2020 internal blockdigram

CPU clock configuration

Items	*Rates*	*Refer chapter*	*Remarks*
SYSCLK input	100 MHz		
CCB clock	600MHz	4.4.3.1 System PLL Ratio	6 : 1 SYSCLK
e500 Core0 Clock	1200 MHz	4.4.3.3 e500 Core PLL Ratios	2 : 1 CCB CLK
e500 Core1 Clock	1200 MHz	4.4.3.3 e500 Core PLL Ratios	2 : 1 CCB CLK
DDRCLK input	66.66MHz		

DDR Data Rate	800 Mbps	4.4.3.2 DDR PLL Ratio	12 : 1 DDRCLK
SD1_REF_CLKp/n	100MHz Diff	4.4.3.10 SerDes Reference Clock Configuration	cfg_srds_refclk=1b
Boot ROM Location		4.4.3.4 Boot ROM Location	cfg_rom_loc[0:3] = 1110b
Host/Agent Configuration		4.4.3.5 Host/Agent Configuration	cfg_host_agt[0:2] = 111b
I/O Port Selection		4.4.3.6 I/O Port Selection	cfg_io_ports[0:3] = 1111b
CPU Boot Configuration		4.4.3.7 CPU Boot Configuration	cfg_cpu0_boot[0:1]= 10b
Boot Sequencer Configuration		4.4.3.8 Boot Sequencer Configuration	cfg_boot_seq[0:1]= 11b
DDR SDRAM Type		4.4.3.9 DDR SDRAM Type	cfg_dram_type = 1b
Platform Speed setting		4.4.3.19 Platform Speed	cfg_plat_speed = 1b

3.2. Memory

The KUGA7048N model defined the 2GB memory size. There use DDR 3 DIMM module on system design.

- RAM size = 2GB, SO-DIMM.
- Data bus width = 64 bits.
- DDR-SDRAM working frequency = 800 Mbps.
- ECC

3.3. Flash

This family of devices provides high performance at low voltage on a 16-bit data bus. Individually erasable memory blocks are sized for optimum code and data storage. Upon initial power-up or return from reset, the device defaults to asynchronous page mode read. Configuring the RCR enables synchronous burst-mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides an easy CPU-to-flash memory synchronization

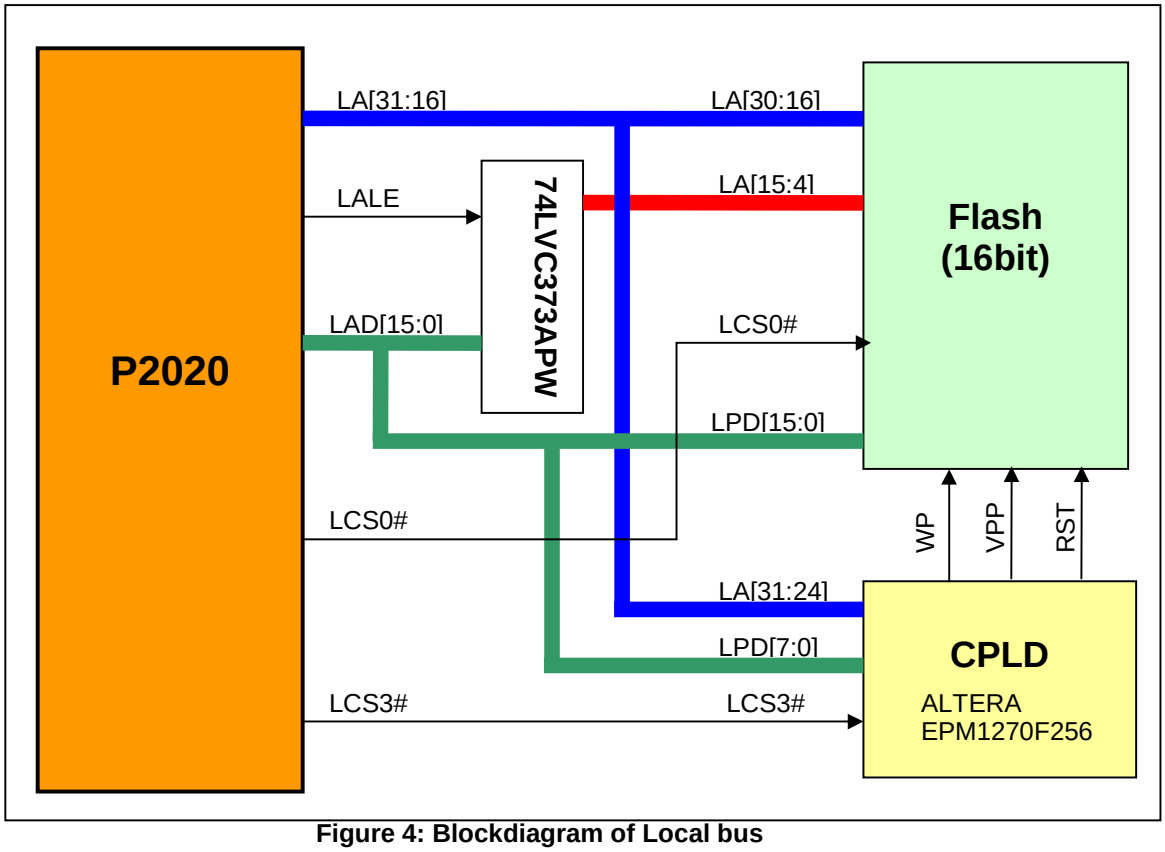


Figure 4: Blockdiagram of Local bus

Protection: Xref to CPLD register " Flash write protect Register (Base: LCS3, Offset+0009)" . There are two bits that can control flash Vpp and Wp# pin by CPU.

Feature

Function	Features
Performance	— 105ns initial access time(512-Mbit, 1-Gbit) Easy BGA and TSOP: —Buffered Enhanced Factory Programming at 2.0MByte/s (typ) using 512-word buffer — 3.0V buffered programming at 1.46MByte/s (Typ) using 512-word buffer

Architecture	— Multi-Level Cell Technology: Highest Density at Lowest Cost — Symmetrically-blocked architecture (512-Mbit, 1-Gbit, 2-Gbit) — Asymmetrically-blocked architecture, Four 32-KByte parameter blocks: Top or Bottom configuration (512-Mbit, 1-Gbit) — 128-KByte array blocks — Blank Check to verify an erased block
Security	— Absolute write protection: VPP = VSS — Power-transition erase/program lockout — Individual zero-latency block locking — Individual block lock-down capability — Password Access feature — One-Time Programmable Register: — 64 OTP bits, programmed with unique information by Numonyx — 2112 OTP bits, available for customer programming
Software	— 25µ s (Typ) program suspend — 30µ s (Typ) erase suspend — Numonyx® Flash Data Integrator optimized — Basic Command Set and Extended Function Interface (EFI) Command Set compatible — Common Flash Interface capable
Density and Packaging	— 56-Lead TSOP(512-Mbit, 1-Gbit) — 64-Ball Easy BGA(512-Mbit, 1-Gbit, 2-Gbit) — 16-bit wide data bus
Quality and Reliability	— Operating temperature: – 40°C to +85°C — Minimum 100,000 erase cycles — 65nm process technology

Configuration

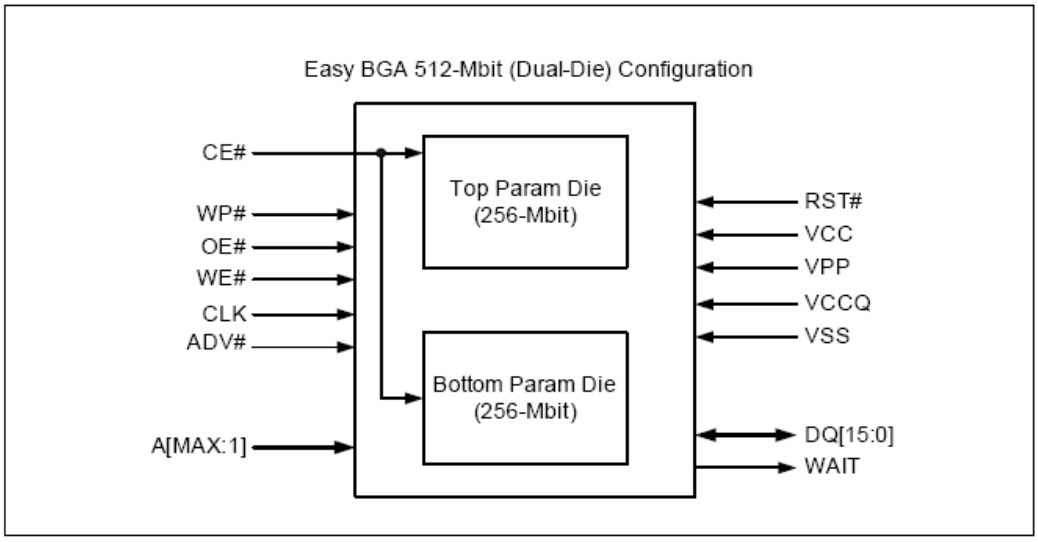
Pin Assignment

Pin name	Connection	Name and Function
RST#	Connect to CPLD with RST sequence	**RESET:** Active low input. RST# resets internal automation and inhibits write operations. This provides data protection during power transitions. RST# high enables normal operation. Exit from Reset places the device in asynchronous read array mode.
CLK	Not used, tie to VSS	**CLOCK:** Synchronizes the device with the system' s bus frequency in synchronous-read mode. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. WARNING: Designs not using CLK for synchronous read mode must tie it to VCCQ or VSS.

ADV#	Not used, tie to VSS	**ADDRESS VALID:** Active low input. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. In asynchronous mode, the address is latched when ADV# going high or continuously flows through if ADV# is held low. WARNING: Designs not using ADV# must tie it to VSS to allow addresses to flow through.
VPP	Connect to CPLD by CPU software control	**ERASE AND PROGRAM POWER:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when VPP ≤ V_{PPLK}. Block erase and program at invalid VPP voltages should not be attempted. Set VPP = V_{PPL} for in-system program and erase operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of VPP can be as low as V_{PPL} min. VPP must remain above V_{PPL} min to perform in-system flash modification. VPP may be 0 V during read operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. VPP can be connected to 9 V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9 V may reduce block cycling capability.
WP#	Connect to CPLD by CPU software control	**WRITE PROTECT:** Active low input. WP# low enables the lock-down mechanism. Blocks in lockdown cannot be unlocked with the Unlock command. WP# high overrides the lock-down function enabling blocks to be erased or programmed using software commands.
WAIT	Not connect	**WAIT:** Indicates data valid in synchronous array or non-array burst reads. RCR [10], (WT) determines its polarity when asserted. Wait's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is high-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, WAIT indicates invalid data when asserted and valid data when disserted. • In asynchronous page mode, and all write modes, WAIT is disserted.
WE#	Connect to CPU LWE0# pin	**WRITE ENABLE:** Active low input. WE# controls writes to the device. Address and data are latched on the rising edge of WE#.
OE#	Connect to CPU LGPL2 pin	**OUTPUT ENABLE:** Active low input. OE# low enables the device's output data buffers during read cycles. OE# high places the data outputs and WAIT in High-Z. **RESET:** Active low input. RST# resets internal automation and inhibits write operations. This provides data protection during power transitions. RST# high enables normal operation. Exit from reset places the device in asynchronous read array mode.
CE#	Connect to CPU LCS0# pin	**CHIP ENABLE:** Active low input. CE# low selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When disserted, the associated flash die is deselected, power is reduced to standby levels, data and WAIT outputs are placed in high-Z state. WARNING: All chip enables must be high when device is not in use.

Functional overview

Figure 6: 512-Mbit Easy BGA Block Diagram



Note: $A_{max} = V_{IH}$ selects the Top parameter Die; $A_{max} = V_{IL}$ selects the Bottom Parameter Die.

Figure 5: Blockdiagram of Flash internal

3.4. Memory Map

Device	Chip Select	R/W	Start Address	End Address	Size	Bus Width	Note
SDRAM	**CS0#/CS1#**	R/W	0x00000000	0x7FFFFFFF	2GB	64 Bits	
NOR Flash Memory	**LCS0#**	R/W	0xE8000000	0xEFFFFFFF	128MB	16 Bits	1,2
CPLD	**LCS3#**	R/W	0xA0000000	0xA00FFFFF	256MB	8 Bits	1,2

Table 1: Memory Map

Note:

1. Read control: There is one /LOE (CLGPL2#) signal (P2020. A20) will used for read signal.
2. Write control: There is one /WE0 signal (P2020. F12) will used for write signal.

3.5. CPU IRQ definition

P2020 supports 12 external interrupts. The KUGA7048N uses 9 of them in the system. The configuration of interrupts is shown below.

IRQ					
PIN# of P2020	Signal Name	I/O	Remark	Output source	Read Status
L24	IRQ0#	INPUT	PS_POWER_INTn	CPLD	
K26	IRQ1#	INPUT	SFP_INTn	CPLD	
K29	IRQ2#	INPUT	Reserved	CPLD	
N25	IRQ3#	INPUT	PCI Express_INTn	CPU	R only
L26	IRQ4#	INPUT	HOT_SWAP_INTn	CPLD	R only
L29	IRQ5#	INPUT	Thermal_INTn	CPLD	R only
K27	IRQ6#	INPUT	FAN_INTn	CPLD	R only
R28	GPIO0	INPUT	RTC_INTn	RTC	R only

Table 2: Interrupt allocation

** The detail discussion for IRQ function, please see "* *chapter 5 CPLD Register"* .

** Read* Status: **R=> Read; COR => Clear Of Read**

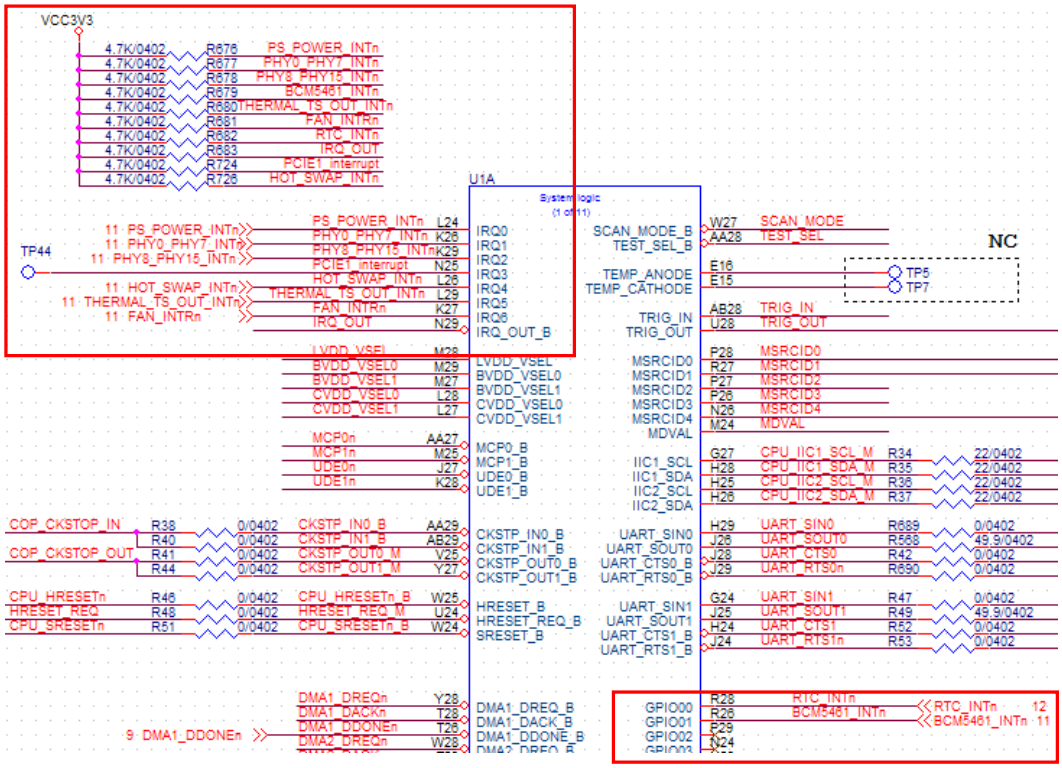


Figure 6: schematic of interrupt

Assignments

Following interrupt request signal were connected to CPU interrupt input.

- ***IRQ 0 for Power Supply status changes***

CPU Interrupt Request Input: IRQ0, *PS_POWER_INTn*
Interrupt Source: PSU1/2_SMB_ALERT of CPLD on CPU Board.

Power Supply Status Register (Base: LCS3, Offset: 0x0A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	HOT_SWAP_INT1	HOT_SWAP_INT2	PSU2_SMB_ALERT	PSU1_SMB_ALERT

Any fault status in Power Status Register (offset+0x0020) will driven this signal to LOW. When there is any status change then CPLD will output this interrupt signal LOW. Notice once interrupt generated will not resume to normal condition, output HIGH, unless hardware fault condition removed.

- *IRQ 1 for SFP status changes*

CPU Interrupt Request Input: IRQ1, SFP_INTn
Interrupt Source: CPLD on Switch Board => CPLD on CPU Board.

SFP INT Register (IIC2 Offset: 0X1D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SFP42-48_INTn	SFP36-41_INTn	SFP30-35_INTn	SFP24-29_INTn	SFP18-23_INTn	SFP12-17_INTn	SFP6-11_INTn	SFP0-5_INTn

Any fault status in SFP INT Register (offset+0x00D0) will driven this signal to LOW. When there is any status change then CPLD will output this interrupt signal LOW. Notice once interrupt generated will not resume to normal condition, output HIGH, unless hardware fault condition removed.

- *IRQ2 for PHY status changes*

CPU Interrupt Request Input: IRQ1, Retimer PHY_INT
Interrupt Source: CPLD on Switch Board => CPLD on CPU Board.

Retimer PHY_INT Register (IIC2 Offset: 0X1E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SFP42-48_INTn	SFP36-41_INTn	SFP30-35_INTn	SFP24-29_INTn	SFP18-23_INTn	SFP12-17_INTn	SFP6-11_INTn	SFP0-5_INTn

Any fault status in PHY_INTn Register (offset+0x00E0) will driven this signal to LOW. When there is any status change then CPLD will output this interrupt signal LOW. Notice once interrupt generated will not resume to normal condition, output HIGH, unless hardware fault condition removed.

- *IRQ 3 for PCIe Interface*

Reserve

- *IRQ 4 for* HOT_SWAP *controller*

CPU Interrupt Request Input: IRQ4, HOT_SWAP_INTn
Interrupt Source: HOT_SWAP_INT1/2 of CPLD on CPU Board.

HOT_SWAP Register (Base: LCS3, Offset: 0x0A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	HOT_SWAP_INT1	HOT_SWAP_INT2	PSU2_SMB_ALERT	PSU1_SMB_ALERT

SWHOT_SWAP 1/2 in **HOT_SWAP** Register will driven this signal to LOW. When there is any status change then CPLD will output this interrupt signal LOW. Notice once interrupt generated will not resume to normal condition, output HIGH, unless hardware fault condition removed.

- ***IRQ 5 for Temperature sensor***

  CPU Interrupt Request Input: IRQ5, ***THERMAL_TS_OUT_INTn***
  Interrupt Source: TS_OUT(CPU board) and THERMAL_OUT (Switch board)

Temperature Sensor Register (Base: LCS3, Offset: 0x19)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TS_OUT	THERMAL_OUT	-	-	-	-	-	

When temperature exceeds programmable limit, thermal sensor will output LOW on this output signal. For proper operation please refer to National Semiconductor TPM75 Data sheet.

- ***IRQ 6 for system FAN status changes***

  CPU Interrupt Request Input: IRQ6, ***FAN_INTRn***
  Interrupt Source: FAN_ALERTn of CPLD on CPU board.

FAN Status Register (Base: LCS3, Offset: 0x0B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	FAN_ALERTn

Any fault status in FAN Status Register will driven this signal to LOW. Notice once interrupt generated will not resume to normal condition, output HIGH, unless hardware fault condition removed.

3.6. GPIO

P2020 GPIO	I/O	Description	Note
GPIO0	Input	RTC_INTn	RTC interrupt
GPIO1	Input	BCM5461_INTn	BCM5461 interrupt
GPIO2	NA	NA	
GPIO3	NA	NA	
GPIO4	NA	NA	
GPIO5	Output	CPLD_WE	For CPLD programming
GPIO6	NA	NA	
GPIO7	NA	NA	
GPIO8	Input	SDHC_CD, eSDHC command	For SD Flash Card
GPIO9	Input	SDHC_WP, eSDHC write protect	For SD Flash Card
GPIO10	NA	NA	
GPIO11	NA	NA	
GPIO12	Output	CPU_CPLD_TCK	For CPLD programming
GPIO13	Input	CPU_CPLD_TDO	For CPLD programming
GPIO14	Output	CPU_CPLD_TMS	For CPLD programming
GPIO15	Output	CPU_CPLD_TDI	For CPLD programming

Table 3: GPIO allocation

Note:

- GPIO 1: This pin is driven low when the RTC timer IC has fault happen.
- GPIO 2: This pin is driven low when the BCM5461 PHY has fault happen.
- GPIO 8: SD card detection pin. ‘ Low’ - Card present, ‘ High’ – No card present
- GPIO 9: SD card write protect detect. ‘ Low’ - Write protected, ‘ High’ – Write enabled
- GPIO [15...12] and GPIO5 are used for CPLD code reprogramming. The detail

control setting please refer *Chapter 5.3.3 CPU on line upgrade CPLD*

3.7. PCIe

P2020 device features one SerDes interface to be used for high-speed serial interconnection applications. The SerDes interface can be used for PCI Express, SGMII and/or Serial RapidIO data transfers. Here, P2020 use 2 PCIE interfaces to link with MAC BCM56844.

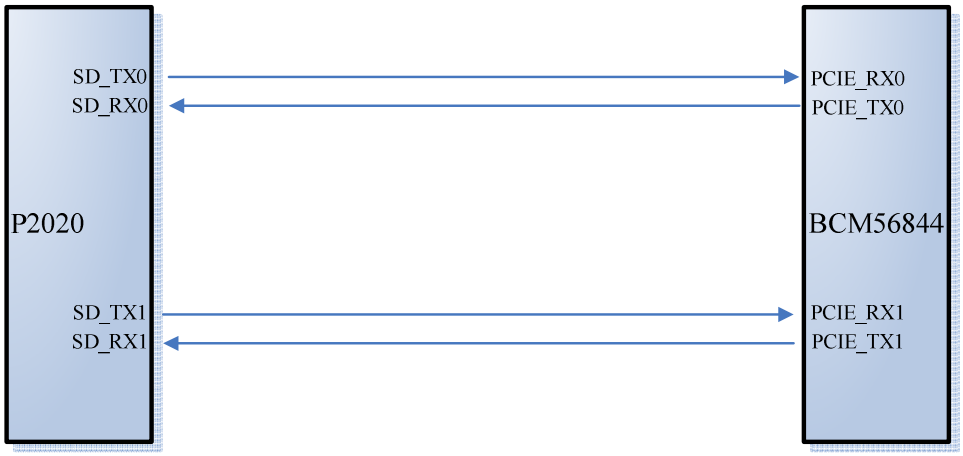


Figure 7: PCIe between CPU and BCM

Table 76. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Comments
Differential Peak-to-Peak Output Voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized Differential Output Voltage (Ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC impedance during all states

Note:

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive Tx UIs.

Table 78 defines the PCI Express (2.5 Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Comments
Differential Input Peak-to-Peak Voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC Differential Input Impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2
DC Input Impedance	Z_{RX-DC}	40	50	60	Ω	Required RX D+ as well as D– DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered Down DC Input Impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3.
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**	**Comments**
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the Receiver

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 must be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

3.8. UART

P2020 have two UART interfaces. One is connect to Switch Board as USB console. The other is hold on CPU Board for debug console used.

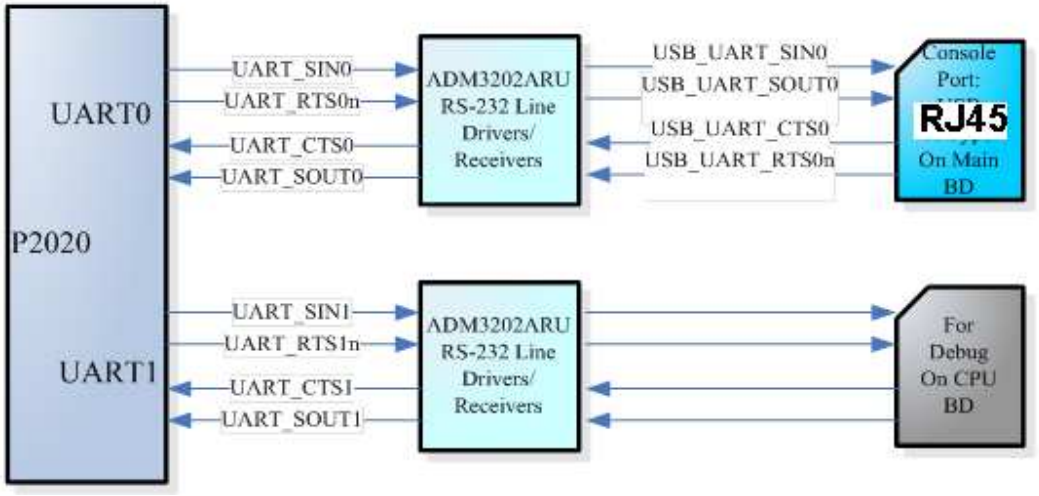


Figure 8: Blockdiagram of UART

Table 29. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = GND or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Note**
Low-level output voltage (OV_{DD} = min, I_{OL} = 2mA)	V_{OL}	—	0.4	V	

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 2 and Table 3.

3.9. I2C

P2020 have 2 IIC interface. IIC1 is used to communication with DDR. The other is used to communication with all IIC devices.

** The detail discussion for IIC subsystem, please see " chapter 10. IIC System"*

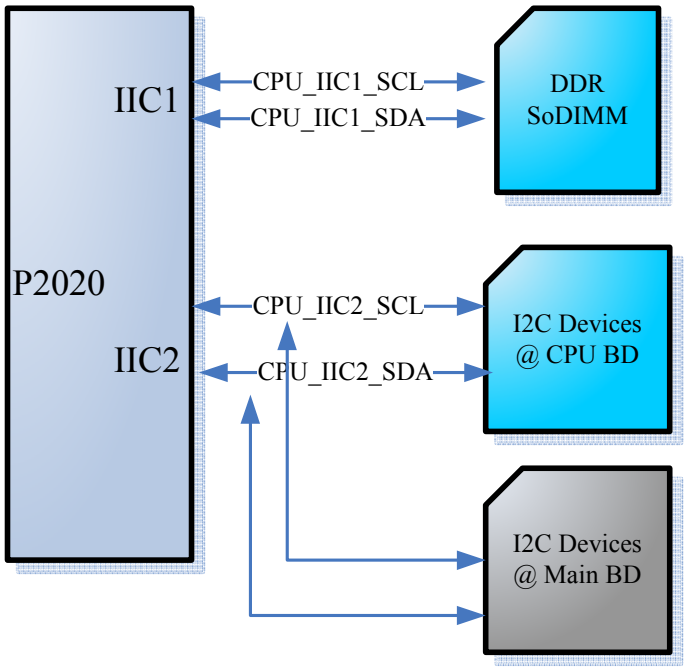


Figure 9: Blockdigram of I2C

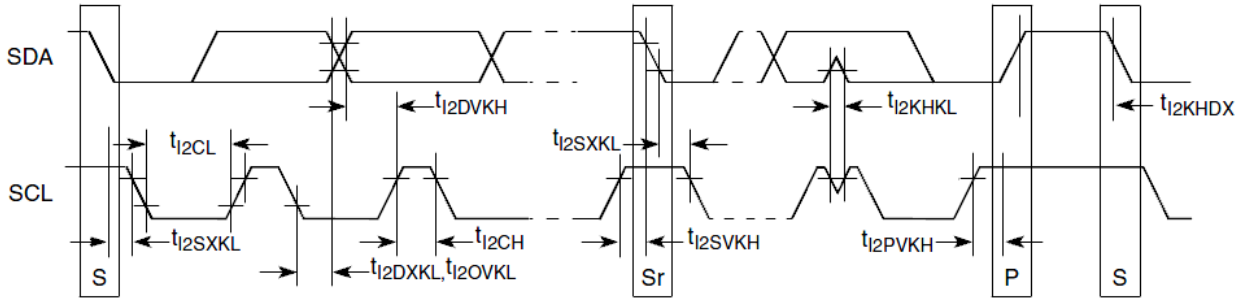


Figure 48. I²C Bus AC Timing Diagram

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz[4]	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

3.10. JTAG

CPU JTAG connector (ICE conector), Dual in line pin header (P1 on CPU BD)

Description	pin
TDO	1
KEY1	2
TDI	3
TRST#	4
QREQ#	5

VDD_SENSE	6
TCK	7
CHKSTP_IN	8
TMS	9
NC	10
SRESET#	11
GND	12
HRESET#	13
KEY2	14
CHKSTP_OUT#	15
GND	16

CPLD JTAG connector (CON1 on CPU BD)

Description	pin
TCK	1
GND	2
TDO	3
VCC	4
TMS	5
NC	6
NC	7
NC	8
TDI	9
GND	10

CPLD JTAG connector (CON4 on Main BD)

Description	pin
TCK	1
GND	2
TDO	3
VCC	4
TMS	5
NC	6
NC	7
NC	8

TDI	9
GND	10

CPLD JTAG Chain is designed on Main BD and CPU BD, so it can easier to programm both at the same time. If only re-program CPLD on Main BD, jump-wire have to be put on CON5 on Main BD.

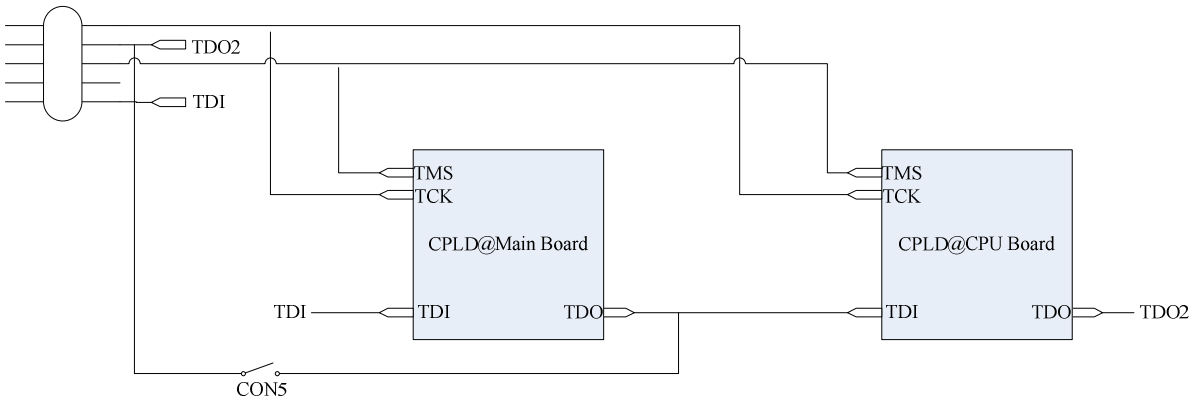


Figure 10: CPLD JTAG chain

3.11. SGMII

Bus description

- IEEE 802.3u-compliant MIIM interface for communication with external PHY devices

Speeds

- 2.5-MHz operation

Devices

BCM5641S

MIIM INTERFACE TIMING

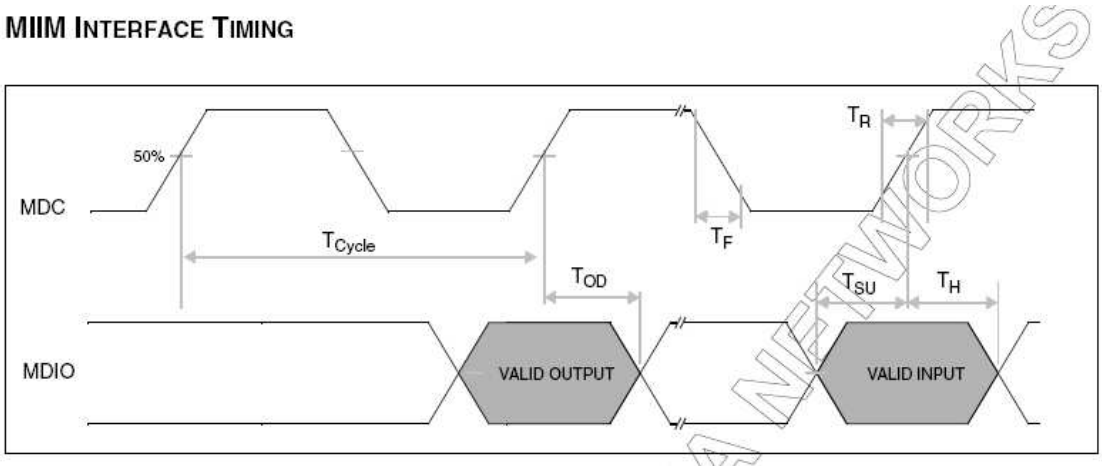


Table 9: MDC/MDIO Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
MDC cycle time	T_{CYCLE}	400	–	–	ns
MDC rise/fall time	T_R, T_F	–	–	10	ns
MDIO input setup	T_{SU}	30	–	–	ns
MDIO input hold time	T_{HO}	0	–	–	ns
MDIO output delay	T_{OD}	10	–	20	ns

3.12. SD Flash Card

The enhanced secure digital host controller (eSDHC) provides an interface between the host system and SD/MMC cards. The eSDHC acts as a bridge, passing host bus transactions to SD/MMC cards by sending commands and performing data accesses to or from the cards. Under SD protocol, it can be categorized as a memory card, I/O card, or combo card. The memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard.

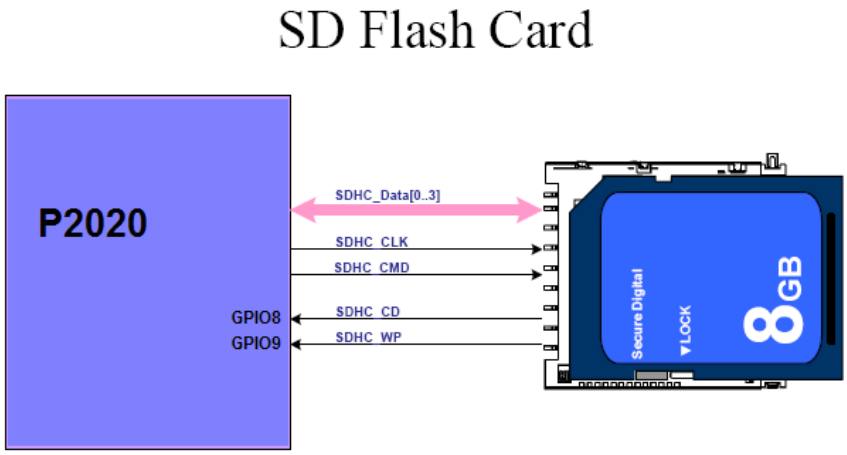


Figure 11: Blockdigram of SD flash card

4. CPLD Subsystem

In CPLD Subsystem is describing to how to light LED, how to collect interruptions from the relative devices, and how get the status of devices from SPF EEPROM. There are two CPLD in KUGA7048N, one is EPM1270F256 on CPU BD, and the other is 5M1270ZF324C5N on Main BD. The below figure shows their role in KUGA7048N

4.1. EPM1270F256 on CPU BD:

ALTERA EPM1270F256 - The MAX® II family of instant-on, non-volatile CPLD is based on a 0.18-µ m, 6-layermetal-flash process, with densities from 240 to 2,210 logic elements (LEDs) (128 to 2,210 equivalent macro cells) and non-volatile storage of 8 Kbits. MAX II devices offer high I/O counts, fast performance, and reliable fitting versus other CPLD architectures. Featuring Multi-Volt core, a user flash memory (UFM) block, and enhanced in-system programmability (ISP), MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.

Features

- Low-cost, low-power CPLD
- Instant-on, non-volatile architecture
- Standby current as low as 25 µ A
- Provides fast propagation delay and clock-to-output times
- UFM block up to 8 Kbits for non-volatile storage
- Multi-Volt core enabling external supply voltages to the device of 3.3 V/2.5 V or 1.8 V
- Multi-Volt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
- I/Os are fully compliant with the Peripheral Component Interconnect Special Interest Group (PCI SIG) PCI Local Bus Specification, Revision 2.2 for 3.3-V operation at 66 MHz
- Supports hot-socketing
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry Compliant with IEEE Std. 1149.1-1990
- ISP circuitry compliant with IEEE Std. 1532

Functional overview, Function Diagram

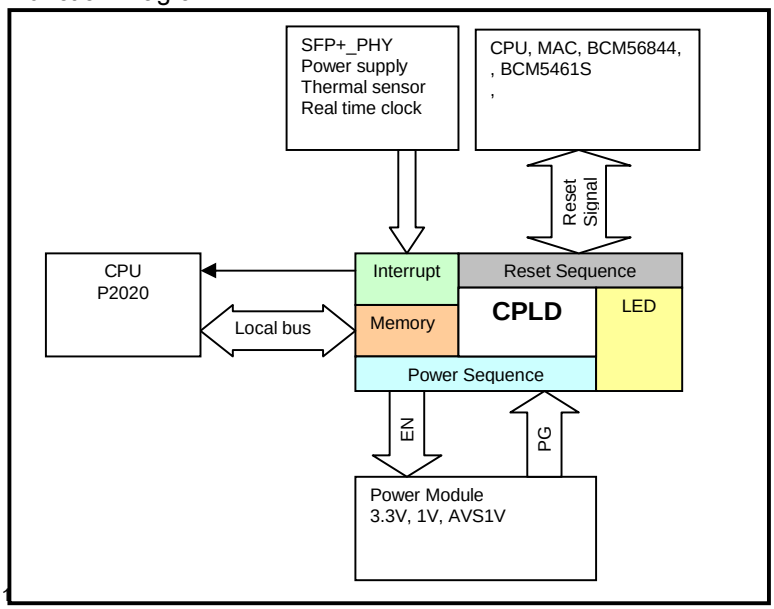


Figure 12: Blockdiagram of CPLD on CPU board

4.2. 5M1270ZF324C5N on MAIN BD:

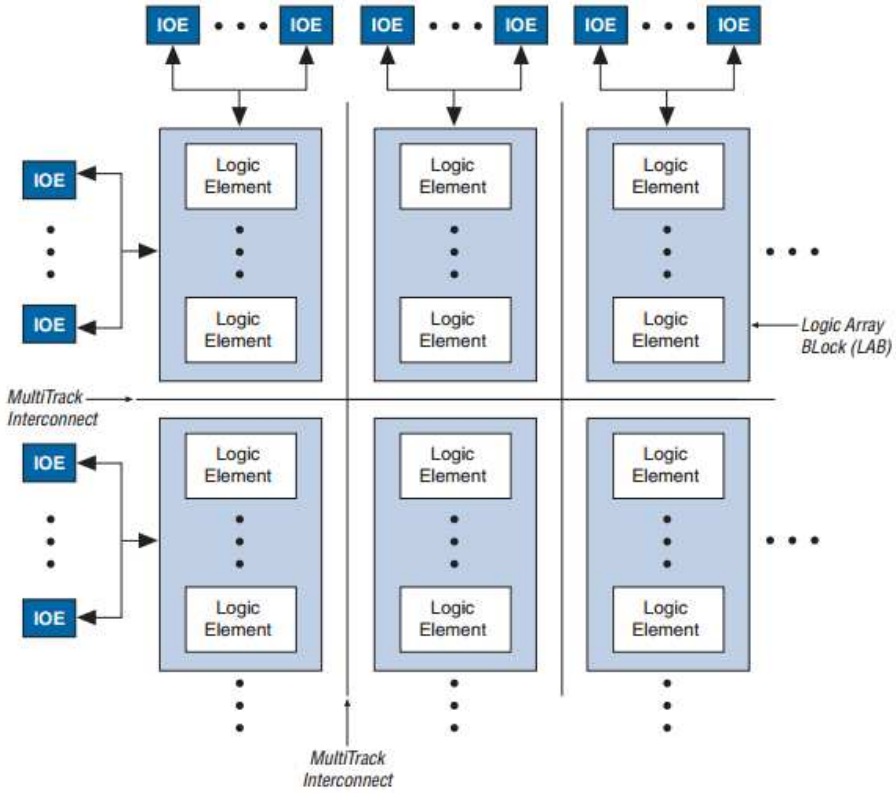
The MAX® V family of low cost and low power CPLDs offer more density and I/Os per footprint versus other CPLDs. Ranging in density from 40 to 2,210 logic elements (LEs) (32 to 1,700 equivalent macrocells) and up to 271 I/Os, MAX V devices provide programmable solutions for applications such as I/O expansion, bus and protocol bridging, power monitoring and control, FPGA configuration, and analog IC interface.

MAX V devices contain a two-dimensional row- and column-based architecture to implement custom logic. Row and column interconnects provide signal interconnects between the logic array blocks (LABs). Each LAB in the logic array contains 10 logic elements (LEs). An LE is a small unit of logic that provides efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The MultiTrack interconnect provides fast granular timing delays between LABs. The fast routing between LEs provides minimum timing delay for added levels of logic versus globally routed interconnect structures.

The I/O elements (IOEs) located after the LAB rows and columns around the periphery of the MAX V device feeds the I/O pins. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt trigger inputs and various single-ended standards, such as 33-MHz, 32-bit PCI™, and LVTTL.MAX V devices provide a global clock network. The global clock network consists of four global clock lines that drive

throughout the entire device, providing clocks for all resources within the device. You can also use the global clock lines for control signals such as clear, preset, or output enable.

Figure 2–1. Device Block Diagram



Features

- Low-cost, low-power, and non-volatile CPLD architecture
- Instant-on (0.5 ms or less) configuration time
- Standby current as low as 25 µA and fast power-down/reset operation
- Fast propagation delay and clock-to-output times
- Internal oscillator
- Emulated RSDS output support with a data rate of up to 200 Mbps
- Emulated LVDS output support with a data rate of up to 304 Mbps
- Four global clocks with two clocks available per logic array block (LAB)
- User flash memory block up to 8 Kbits for non-volatile storage with up to 1000 read/write cycles
- Single 1.8-V external supply for device core
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors

- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
- I/Os are fully compliant with the PCI-SIG® PCI Local Bus Specification, revision 2.2 for 3.3-V operation
- Hot-socket compliant
- Built-in JTAG BST circuitry compliant with IEEE Std. 1149.1-1990

Functional overview,

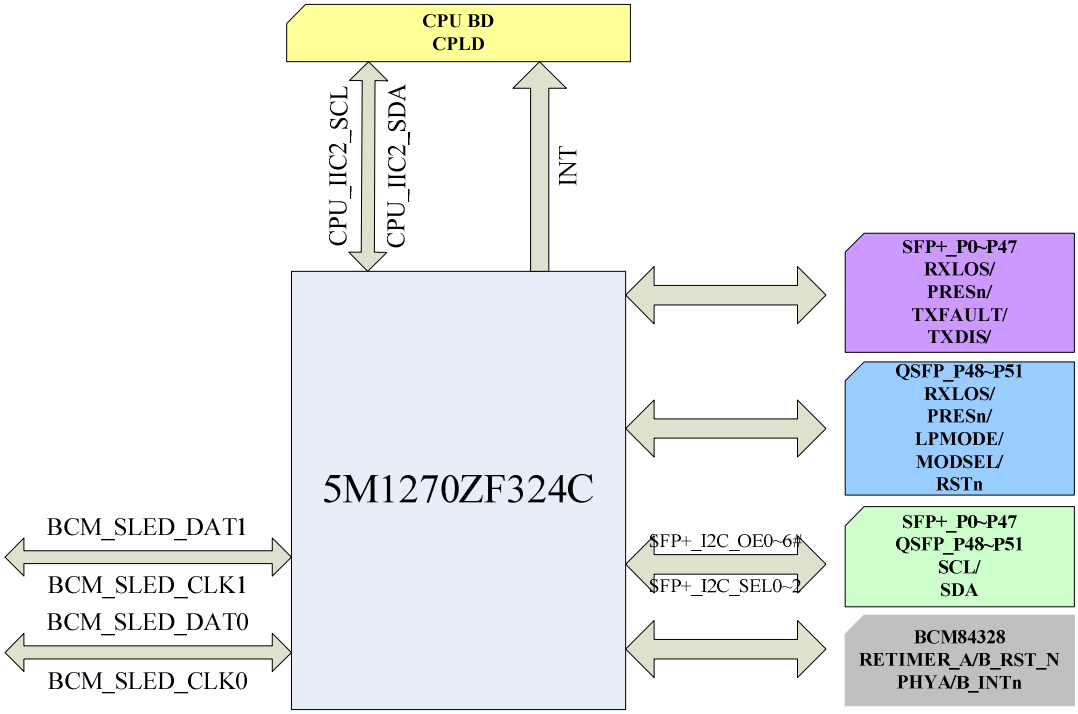


Figure 13: Blockdiagram of CPLD on Switch Board

4.3. CPLD communication between Switch Board and CPU Board

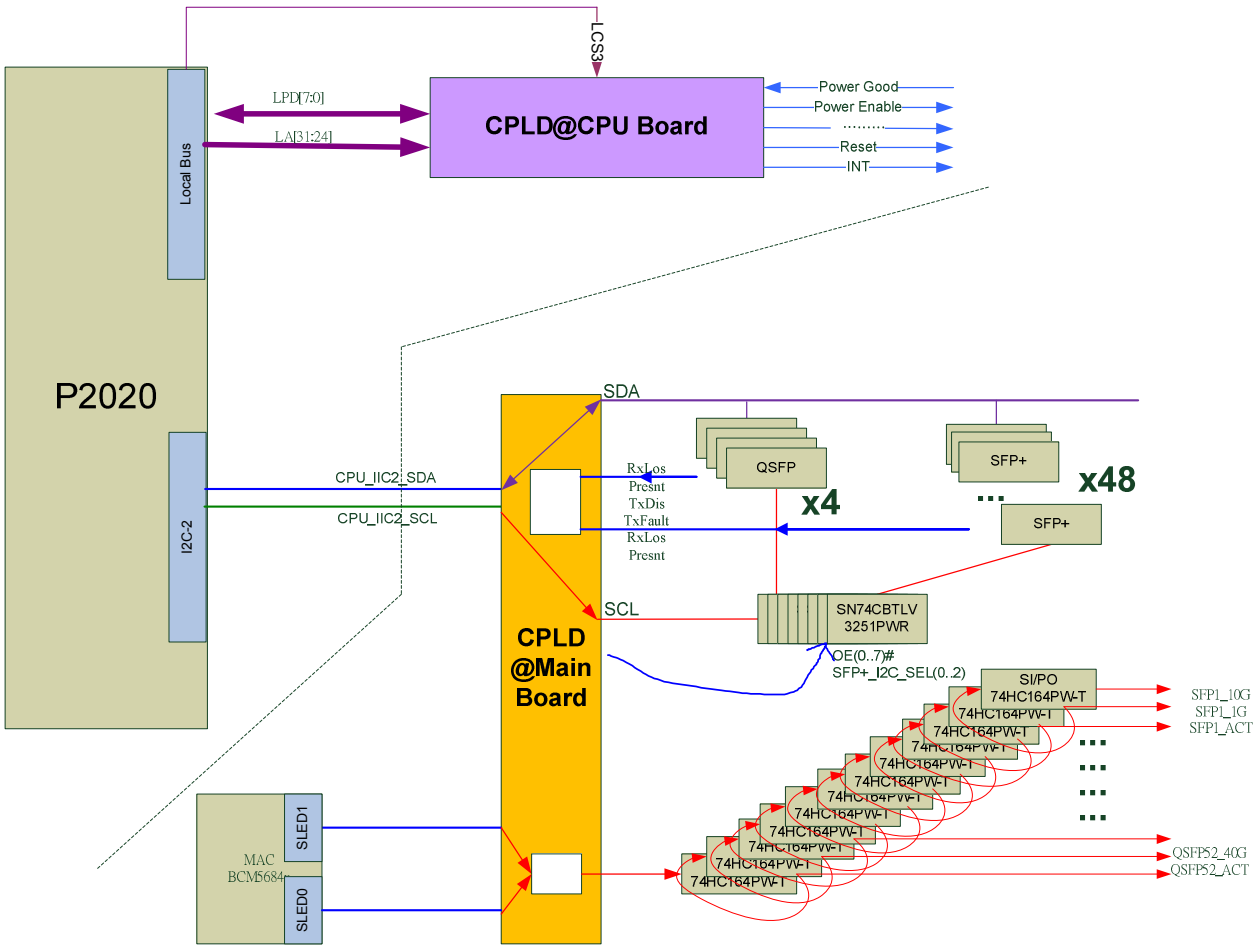


Figure 14: communication between CPLDs

CPLD communication between Switch Board and CPU Board use CPLD_RESEVED2/3 as I2C interface. Then some events on Switch Board can send to CPLD of CPU Board to handle.

4.4. CPLD JTAG Programming

For Altera MAX II CPLD we used Quartus II design software to program HDL. The Quartus II Assembler generates a device programming image, in the form of one or more of the following from a successful fit (that is, place-and-route).

- Programmer Object Files (.pof)
- SRAM Object Files (.sof)
- Hexadecimal (Intel-Format) Output Files (.hexout)
- Tabular Text Files (.ttf)
- Raw Binary Files (.rbf)

The .pof and .sof files are then processed by the Quartus II Programmer and downloaded to the device with the MasterBlaster TM or the ByteBlaster TM II download cable, or the Altera Programming Unit (APU). The Hexadecimal (Intel-Format) Output Files, Tabular Text Files, and Raw Binary Files can be used by other programming hardware manufacturers that provide support for Altera devices.

For CPLD program download, we using Byte Blaster TM II download cable through the JTAG interface to download programmer object files (.pof) into CPLD.

CPLD download connector, Single in line pin header

Description	pin
3.3V	1
TDO	2
TDI	3
NC	4
NC	5
TMS	6
GND	7
TCK	8

Table 4 CPLD Header, Single line.

4.4.1. CPU on line upgrade CPLD

The CPLD_WE signal level is low that programming bus is control by CPU. When CPLD_WE level is high, the CPLD is programmed by CPLD JTAG tools. The GPIO detail defined please refer *chapter 4.2.7 GPIO pin list*

The Altera EPM1270F256 support Real-Time ISP and ISP CLAMP State Editor for online programming. It can keep the pin status you set while there execute upgrade process. For the details of Altera CPLD re-programming by MCU, please contact with Altera FAE directly.

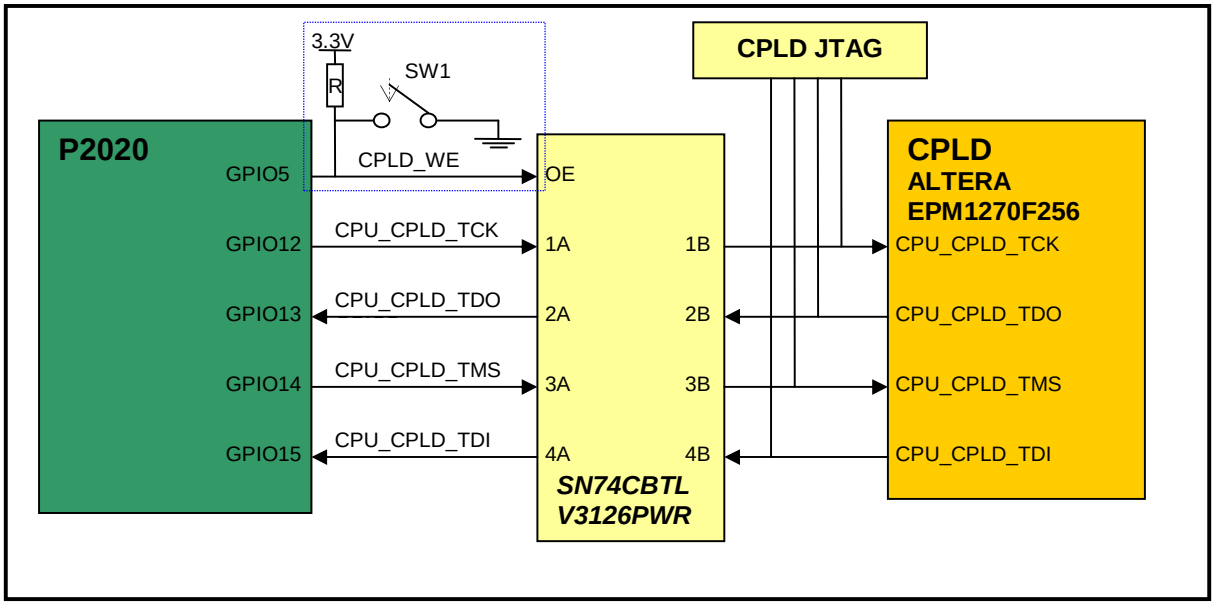


Figure 15: Blockdiagram of CPLD update circuit

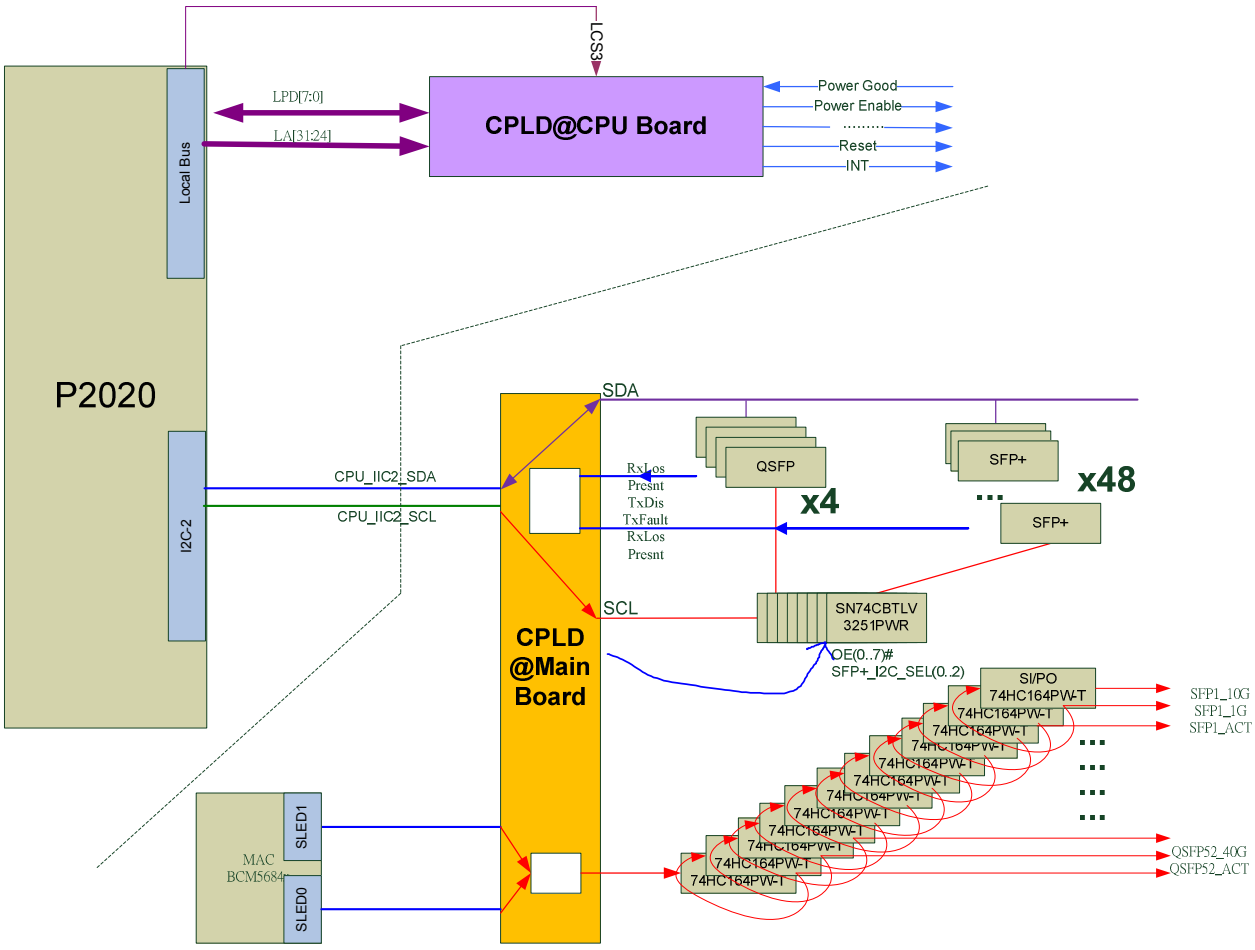
Note: There is reserved SW1 switch for first time production. When SW1 connect to GND, the CPLD can use Altera download tool to programming CPLD. After production this SW1 will be off.

5. CPLD Register

In KUGA7048N-R, there are three CPLDs on CPU Board and Switch Board. CPLD on CPU Board is charged of deal with system work, like interrupt, enable DC-DC power system, system LED, and FAN status. For two CPLDs on Switch Board, it is focused on deal with SFP control signals and Port LED.

They use different interfaces with CPU. CPU uses to local bus to control with CPLD on CPU Board. The other CPLDs on Switch Board, CPU uses IIC2 to deal with status of SFP ports.

The below will describe the definition of offset of REG of both CPLDs.



5.1. CPLD Register map

5.1.1. CPLD of CPU Board via local bus:

Device	Chip Select	R/W	Address	Bus Width	Note
CPUPLD	LCS3#	R	BASE+0x01	8 Bits	CPUPLD Revision Register
		R	BASE+0x02	8 Bits	CPU board Revision & board ID
		R/W	BASE+0x03	8 Bits	Software Reset Register 1/3
		R/W	BASE+0x04	8 Bits	Software Reset Register 2/3
		R/W	BASE+0x05	8 Bits	Software Reset Register 3/3
		R/W	BASE+0x06	8 Bits	POWER STATUS Control Register 1/4
		R/W	BASE+0x07	8 Bits	POWER STATUS Control Register 2/4
		R	BASE+0x08	8 Bits	POWER STATUS Control Register 3/4
		R	BASE+0x09	8 Bits	POWER STATUS Control Register 4/4
		R	BASE+0x0A	8 Bits	Interrupt Register 1/4
		R	BASE+0x0B	8 Bits	Interrupt Register 2/4
		R	BASE+0x0C	8 Bits	Interrupt Register 3/4
		R	BASE+0x0D	8 Bits	Interrupt Register 4/4
		R/W	BASE+0x0E	8 Bits	LED Control Register 1/3
		R	BASE+0x00F	8 Bits	Reserved
		R/W	BASE+0x10	8 Bits	LED Control Register 3/3
		R/W	BASE+0x11	8 Bits	FAN Status Register
		R	BASE+0x12	8 Bits	Reserved
		R	BASE+0x13	8 Bits	Reserved
		R	BASE+0x14	8 Bits	Reserved
		R	BASE+0x15	8 Bits	Reserved
		R	BASE+0x16	8 Bits	Reserved
		R/W	BASE+0x17	8 Bits	Flash Protection Register
		R/W	BASE+0x18	8 Bits	Watchdog Register
		R/W	BASE+0x19	8 Bits	Temperature Sensor and Alert Register

Table 5: CPLD Register mapping for Local bus

Note:

1. Read control: There is one /LOE (CLGPL2#) signal (P2020. A20) will used for read signal.
2. Write control: There is one /WE0 signal (P2020. F12) will used for write signal.

It is not necessary program CPLD registers after power up. System can work without programming them. However for proper panel display and access some peripheral info like I2C bus, some registers must be filled with correct data. Please refer to CPLD registers section in hardware specification.

5.1.2. CPLD of Switch Board via IIC2:

Device	IIC2 Address	R/W	Offset Address	Bus Width	Note
		R	0x00	8 Bits	Switch Board ID and Revision Register
		R	0x01	8 Bits	Switch CPLD code Revision Register
		R/W	0x02	8 Bits	Selection of SFP and I2C device Register
		R/W	0x03	8 Bits	Reserved
		R	0x04	8 Bits	Reserved
		R/W	0x05	8 Bits	Tx Disable 1 of SFP transceiver
		R/W	0x06	8 Bits	Tx Disable 2 of SFP transceiver
		R/W	0x07	8 Bits	Tx Disable 3 of SFP transceiver
		R/W	0x08	8 Bits	Tx Disable 4 of SFP transceiver
		R/W	0x09	8 Bits	Tx Disable 5 of SFP transceiver
		R/W	0x0A	8 Bits	Tx Disable 6 of SFP transceiver
		R	0x0B	8 Bits	RXLos 1 of SFP transceiver
		R	0x0C	8 Bits	RXLos 2 of SFP transceiver
		R	0x0D	8 Bits	RXLos 3 of SFP transceiver
		R	0x0E	8 Bits	RXLos 4 of SFP transceiver
		R	0x0F	8 Bits	RXLos 5 of SFP transceiver
		R	0x10	8 Bits	RXLos 6 of SFP transceiver
		R	0x11	8 Bits	Present 1 of SFP transceiver
		R	0x12	8 Bits	Present 2 of SFP transceiver
		R	0x13	8 Bits	Present 3 of SFP transceiver
		R	0x14	8 Bits	Present 4 of SFP transceiver
		R	0x15	8 Bits	Present 5 of SFP transceiver
		R	0x16	8 Bits	Present 6 of SFP transceiver
		R/W	0x17	8 Bits	TX Fault 1 of SFP transceiver
		R/W	0x18	8 Bits	TX Fault 2 of SFP transceiver
		R/W	0x19	8 Bits	TX Fault 3 of SFP transceiver

		R/W	0x1A	8 Bits	TX Fault 4 of SFP transceiver
		R/W	0x1B	8 Bits	TX Fault 5 of SFP transceiver
		R/W	0x1C	8 Bits	TX Fault 6 of SFP transceiver
		R	0x1D	8 Bits	SFP INT
		R	0x1E	8 Bits	Retimer PHY_INT
		R	0x1F	8 Bits	QSFP Reset and Modsel
		R	0x20	8 Bits	Retimer reset
		R	0x21	8 Bits	Reserved

5.2. CPLD of CPU Board via local bus

5.2.1. CPUPLD, CPUPLD_Rev Register (Base: LCS3#, Offset: 0x01) – Read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUPLD Revision[7:0]							

Bit	Name	R/W	Description	Default
7:0	CPUPLD_Rev	R	Rev	0002b

5.2.2. CPUPLD, CPUBRD_ID_Rev Register (Base: LCS3#, Offset: 0x02) – Read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID				Revision			

Bit	Name	R/W	Description	Default
7:4	ID	R	CPU board ID “0000”: P2020 non-ECC “0001”: P2020 ECC “0010”: P2041	“0001”
3:0	Revision	R	CPU board Revision “0000”: proto-A “0001”: proto-B	“0001”

5.2.3. CPUPLD, Software Reset Register 1/3 (Base: LCS3#, Offset: 0x03) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FORCE_RESETn	CPU_HRESETn	--	--	FLASH_RSTn	BCM56846_RESn	Rstn_SWPLD	BCM5461S_MB_RSTN

Bit	Name	R/W	Description	Default
7	FORCE_RESETn	**R/W**	Software reset the whole system “1” = Normal operation “0” = Reset	**1b**
6	CPU_HRESETn_Rq	**R/W**	Reset the CPU Hardware. “1” = Normal operation “0” = Reset	**1b**
5	Reserve	**--**	--	**--**
4	Reserve	**--**	--	**--**
3	FLASH_RSTn	R/W	Software reset the FLASH “1” = Normal operation “0” = Reset	1b
2	BCM56846_RESn	**R/W**	Reset the MAC. “1” = Normal operation “0” = Reset	**1b**

1	Rstn_SWPLD	R/W	Software reset Switch Board CPLD “1” = Normal operation “0” = Reset	**1b**
0	BCM5461S_MB_RSTN	R/W	Software reset the management PHY device “1” = Normal operation “0” = Reset	**1b**

5.2.4. CPUPLD, Software Reset Register 2/3 (Base: LCS3#, Offset: 0x04) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
~~RETIMER_A_RST_N~~	~~RETIMER_B_RST_N~~	~~USB_RESET~~	74HC164_RST_N			--	--

Bit	Name	R/W	Description	Default
7	~~RETIMER_A_RST_N~~	~~**R/W**~~	~~Software reset RETIMER_A only.~~ ~~“1” = Normal operation~~ ~~“0” = Reset~~	~~**1b**~~
6	~~RETIMER_B_RST_N~~	~~**R/W**~~	~~Software reset RETIMER_B only.~~ ~~“1” = Normal operation~~ ~~“0” = Reset~~	~~**1b**~~
5	~~USB_RESET~~	~~**R/W**~~	~~Optional active high transceiver reset.~~ ~~“1” = Reset~~ ~~“0” = Normal operation~~	~~**1b**~~
4	74HC164_RST_N	**R/W**	Software reset 74HC164 for LEDs of SFP and QSFP. “1” = Normal operation “0” = Reset	**1b**
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.5. CPUPLD, Software Reset Register 3/3 (Base: LCS3#, Offset: 0x05) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.6. CPUPLD, POWER STATUS Control Register 1/4 (Base: LCS3#, Offset: 0x06) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN_MAC1V	EN_AVS1V

Bit	Name	R/W	Description	Default
7	Reserved			
6	Reserved			
5	Reserved			
4	Reserved			
3	Reserved			
2	Reserved			
1	EN_MAC1V	**R/W**	EN_MAC1V "1" = Voltage enable is ON. "0" = Voltage enable is OFF.	**1b**
0	EN_AVS1V	**R/W**	EN_AVS1V "1" = Voltage enable is ON. "0" = Voltage enable is OFF.	**1b**

5.2.7. CPUPLD, POWER STATUS Control Register 2/4 (Base: LCS3#, Offset: 0x07) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Reserve	EN_CPU_1V	Reserve	DDR_POWER_EN	Reserve	RETIMER_1V_EN	PWM_EN5V	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	EN_CPU_1V	**R/W**	EN_CPU_1V "1" = Voltage enable is ON. "0" = Voltage enable is OFF.	**1b**
5	Reserve	--	--	--
4	DDR_POWER_EN	**R/W**	DDR_POWER_EN "1" = Voltage enable is ON. "0" = Voltage enable is OFF.	**1b**
3	Reserve	--	--	--
2	~~RETIMER_1V_EN~~	~~**R/W**~~	~~RETIMER_1V_EN~~ ~~"1" = Voltage enable is ON.~~ ~~"0" = Voltage enable is OFF.~~	~~**1b**~~
1	~~PWM_EN5V~~	~~**R/W**~~	~~PWM_EN5V~~ ~~"1" = Voltage enable is ON.~~ ~~"0" = Voltage enable is OFF.~~	~~**1b**~~
0	Reserve	--	--	--

5.2.8. CPUPLD, POWER STATUS Control Register 3/4 (Base: LCS3#, Offset: 0x08) – R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSU1_PWOK	PSU2_PWOK	HOT_SWAP_PG1	HOT_SWAP_PG2	Reserved	VCC3V3_PG	MAC1V_PG	AVS_1V_PG

Bit	Name	R/W	Description	Default
7	PSU1_PWOK	**R**	PSU1_PWOK "1" = Power is good. "0" = Power fail.	
6	PSU2_PWOK	**R**	PSU2_PWOK "1" = Power is good. "0" = Power fail.	
5	HOT_SWAP_PG1	**R**	HOT_SWAP1 POWER "1" = power good "0" = Power fail	
4	HOT_SWAP_PG2	**R**	HOT_SWAP2 POWER "1" = Power is good. "0" = Power fail	
3	Reserved			
2	VCC3V3_PG	**R**	VCC3V3_PG "1" = Power is good. "0" = Power fail	

1	MAC1V_PG	**R**	MAC1V_PG "1" = Power is good. "0" = Power fail.	
0	AVS_1V_PG	**R**	AVS_1V_PG "1" = Power is good. "0" = Power fail.	

5.2.9. CPUPLD, POWER STATUS Control Register 4/4 (Base: LCS3#, Offset: 0x09) – R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	CPU_1V_PG	Reserve	DDR_POWER_PG	Reserve	Reserve	RETIMER_1V_PG	PWM_PG5V

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	CPU_1V_PG	**R**	CPU_1V_PG "1" = Power is good. "0" = Power is failed.	**1b**
5	Reserve	--	--	--
4	DDR_POWER_PG	**R**	DDR_POWER_PG "1" = Power is good. "0" = Power is failed.	**1b**
3	Reserve	--	--	--
2	Reserve	--	--	--
1	~~RETIMER_1V_PG~~	~~**R**~~	~~RETIMER_1V_PG~~ ~~"1" = Power is failed.~~ ~~"0" = Power is good.~~	~~**1b**~~
0	~~PWM_PG5V~~	~~**R**~~	~~PWM_PG5V~~ ~~"1" = Power is failed.~~ ~~"0" = Power is good.~~	~~**0b**~~

5.2.10. CPUPLD, Interrupt Register 1/4 (Base: LCS3#, Offset: 0x0A) – Read Clear

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	HOT_SWAP_INT1	HOT_SWAP_INT2	PSU2_SMB_ALERT	PSU1_SMB_ALERT

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--

5	Reserve	--	--	--
4	Reserve	--	--	--
3	HOT_SWAP_INT1	**R**	HOT_SWAP_INT1 “1” = No Interrupt “0” = Interrupt	
2	HOT_SWAP_INT2	**R**	HOT_SWAP_INT2 “1” = No Interrupt “0” = Interrupt	
1	PSU2_SMB_ALERT	**R**	PSU2_SMB_ALERT is indicate temperature warming, over-current, over-voltage, and fan fail situation. “1” = PS2 is not alert “0” = PS2 is alert.	
0	PSU1_SMB_ALERT	**R**	PSU1_SMB_ALERT is indicate temperature warming, over-current, over-voltage, and fan fail situation. “1” = PS2 is not alert “0” = PS2 is alert.	

5.2.11. CPUPLD, Interrupt Register 2/4 (Base: LCS3#, Offset: 0x0B) – Read Clear

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	FAN_ALERTn

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	FAN_ALERTn	**R**	FAN sets operate “1” = FAN is operating good “0” = Fan is failed	

5.2.12. CPUPLD, Interrupt Register 3/4 (Base: LCS3#, Offset: 0x0C) – Read Clear

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	BCM5461S_MB_IRQ	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	BCM5461S_MB_IRQ	**R**	Indicate the BCM5461_INTn “1” = Interrupt isn't required “0” = Interrupt is required	
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.13. CPUPLD, Interrupt Register 4/4 (Base: LCS3#, Offset: 0x0D) – R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.14. CPUPLD, FAN LED Control Register 1/3 (Base: LCS3#, Offset: 0x0E) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	FANBD2_LED_G	FANBD2_LED_Y	FANBD1_LED_G	FANBD1_LED_Y

Bit	Name	R/W	Description	Default
7				
6				
5				
4				
3	FANBD2_LED_Y	**RW**	Indicate the Yellow LED of FAN Tray2 status '1': LED off. '0': LED on	1b
2	FANBD2_LED_G	**RW**	Indicate the Green LED of FAN Tray2 status '1': LED off. '0': LED on	1b
1	FANBD1_LED_Y	**RW**	Indicate the Yellow LED of FAN Tray1 status '1': LED off. '0': LED on	1b
0	FANBD1_LED_G	**RW**	Indicate the Green LED of FAN Tray1 status '1': LED off. '0': LED on	0b

5.2.15. CPUPLD, LED Control Register 2/3 (Base: LCS3#, Offset: 0x0F) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.16. CPUPLD, System LED Control Register 3/3 (Base: LCS3#, Offset: 0x10) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POWER1_LED_G	POWER1_LED_Y	POWER2_LED_G	POWER2_LED_Y	SYSTEM_LED_G	SYSTEM_LED_R	FAN_LED_G	FAN_LED_Y

Bit	Name	R/W	Description	Default
7:6	POWER1_LED_G/ POWER1_LED_Y	R/W	Indicate the Power supply 1 LED status '01': Green LED on. '10': Yellow LED on.	00b
5:4	POWER2_LED_G/ POWER2_LED_Y	R/W	Indicate the Power supply 2 LED status '01': Green LED on. '10': Yellow LED on	00b
3:2	SYSTEM_LED_G/ SYSTEM_LED_R	R/W	Indicate the SYSTEM LED status '01': Green LED on. '10': Red LED on	00b
1:0	FAN_LED_G/ FAN_LED_Y	R/W	Indicate the FAN LED status '01': Green LED on '10': Yellow LED on.	00b

5.2.17. CPUPLD, FAN Status Register (Base: LCS3#, Offset: 0x11) – R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	FAN2_EEPROM_WP	FAN1_EEPROM_WP	Reserve	FAN_M_PRESENT1	FAN_M_PRESENT2	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
	Reserve			
5	FAN2_EEPROM_WP	R/W	Fan2 EEPROM "1" = Write operating is disabled. "0" = Write operating is enabled.	1b
4	FAN1_EEPROM_WP	R/W	Fan1 EEPROM "1" = Write operating is disabled. "0" = Write operating is enabled..	1b
3	Reserve	--	--	--
2	FAN_M_PRESENT1	R	Indicate the FAN Board1 is present or not "1" = Fan Board1 isn't present "0" = Fan board1 is present	0b
1	FAN_M_PRESENT2	R	Indicate the FAN Board2 is present or not "1" = Fan Board2 isn't present "0" = Fan board2 is present	0b
0	Reserve			

5.2.18. CPUPLD, Reserve Register (Base: LCS3#, Offset: 0x12) – R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.19. CPUPLD, Reserve Register (Base: LCS3#, Offset: 0x13) – R

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	**Name**	**R/W**	**Description**	**Default**
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.20. CPUPLD, Reserve Register (Base: LCS3#, Offset: 0x14) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.21. CPUPLD Register (Base: LCS3#, Offset: 0x15) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.22. CPUPLD Register (Base: LCS3#, Offset: 0x16) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.2.23. CPUPLD, Flash Protection Register (Base: LCS3#, Offset: 0x17) – R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	FLASH_WP#	FLASH_VPP#

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	FLASH_WP#	R/W	Flash Write Protect※ “0” = enables the lock-down mechanism. “1” = overrides the lock-down function enabling blocks to be erased or programmed using software commands.	0b
0	FLASH_VPP#	R/W	Erase and Program Power “0” = block erase and program should not be attempted. “1” = for in-system program and erase operations.	0b

※Flash Write Protect: Active Low. WP# Low enables the lock-down mechanism. Blocks in lock down cannot be unlocked with Unlock command. WP# high overrides the lock-down function enabling blocks to be earsed or programmed using software commands.

5.2.24. CPUPLD, Watchdog Register (Base: LCS3#, Offset: 0x18) – R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	Reserve	Reserve	RTC_WDI	RTC_RST_OUT

Bit	Name	R/W	Description	Default
7	Reserve	--	--	--
6	Reserve	--	--	--
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	RTC_WDI	**R/W**	Watchdog timer clear flag bit 1= flag not clear 0= flag clear	**1b**
0	RTC_RST_OUT	**R**	RTC output the reset to CPLD “1” = Normal operation “0” = Reset	

5.2.25. CPUPLD, Temperature Sensor and Alert Register (Base: LCS3, Offset: 0x19) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TS_OUT	THERMAL_OUT	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Bit	Name	R/W	Description	Default
7	TS_OUT	**R**	Indicate the TS_OUT of CPU board require to interrupt or not “1” = Interrupt isn't required “0” = Interrupt is required	
6	THERMAL_OUT	**R**	Indicate TMP75s of Switch board alert to interrupt or not “1” = Interrupt isn't required “0” = Interrupt is required	
5	Reserve	--	--	--
4	Reserve	--	--	--
3	Reserve	--	--	--
2	Reserve	--	--	--
1	Reserve	--	--	--
0	Reserve	--	--	--

5.3. CPLD of Switch Board via IIC2:

5.3.1. SWPLD, SWBRD_ID_Revision Register (Offset: 0x00) – Read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Switch Board ID				Switch Board Version			

Bit	Name	R/W	Description	Default
7-4	ID	R	SWBRD_ID “0000”: FS-1024D “0001”: FS-1048D “0010”: L7048 “0011”: L3032 “0100”: L76416 “0101”: L74812	“0010”
3-0	Version	R	SWBRD_Revision “0000”: proto-A “0001”: proto-B	“0001”

Switch Board ID: Identify the product. L7048 is 0010

5.3.2. SWPLD, Switch CPLD code Revision Register (Offset: 0x01) – Read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Code Version							

Bit	Name	R/W	Description	Default
7-0	Switch CPLD Code Version	R	Switch Code Version in Hex Numbering	0x02

Code Revision: Indicate the code board revision. The released revision is starting from 0x01. For testing, it will be 0xff.

5.3.3. SWPLD, Selection of SFP and I2C device Register (Offset: 0x02) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Selection of SFP and I2C device							

Bit	Name	R/W	Description	Default
7:0	--	R/W	Selection of SFP and I2C device: SFP1 = 0x01; SFP2 = 0x02; SFP3 = 0x03; SFP4 = 0x04; SFP5 = 0x05; SFP6 = 0x06; SFP7 = 0x07; SFP8 = 0x08; SFP9 = 0x09; SFP10 = 0x0a; SFP11 = 0x0b; SFP12 = 0x0c; SFP13 = 0x0d; SFP14 = 0x0e; SFP15 = 0x0f; SFP16 = 0x10; SFP17 = 0x11; SFP18 = 0x12; SFP19 = 0x13; SFP20 = 0x14; SFP21 = 0x15; SFP22 = 0x16; SFP23 = 0x17; SFP24 = 0x18; SFP25 = 0x19; SFP26 = 0x1a	-

Bit	Name	R/W	Description			Default
7:0	--	--	SFP27	0x1b		-
			SFP28	0x1c		
			SFP29	0x1d		
			SFP30	0x1e		
			SFP31	0x1f		
			SFP32	0x20		
			SFP33	0x21		
			SFP34	0x22		
			SFP35	0x23		
			SFP36	0x24		
			SFP37	0x25		
			SFP38	0x26		
			SFP39	0x27		
			SFP40	0x28		
			SFP41	0x29		
			SFP42	0x2a		
			SFP43	0x2b		
			SFP44	0x2c		
			SFP45	0x2d		
			SFP46	0x2e		
			SFP47	0x2f		
			SFP48	0x30		
			L6718	0x61	0x46, 0x66	
			TPS40422	0x62	0x09	
			Reserved	0x63		
			FAN board	0x64	0x29	
			PSU1	0x65	0x50, 0x58	
			Reserved	0x66		
			PSU2	0x67	0x51, 0x59	
			Reserved	0x68		

※ This REG (0x02) has integrated the relative pins (mux_oe and mux_sel) and just entering the assigned port is done.

5.3.4. SWPLD, Reserved Register (Offset: 0x03) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Name	R/W	Description	Default
7-0	Reserved	--	--	-

5.3.5. SWPLD, Reserved Register (Offset: 0x04) – Read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Name	R/W	Description	Default
7-0	Reserved	--	--	-

5.4.5 SWPLD, Tx Disable 1 of SFP transceiver Register (Offset: 0x05) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxDis_8	TxDis_7	TxDis_6	TxDis_5	TxDis_4	TxDis_3	TxDis_2	TxDis_1

Bit	Name	R/W	Description	Default
7	TxDis_8	R/W	Transceiver TX enable for SFP8 "1" = Transceiver turn off "0" = Transceiver turn on	0
6	TxDis_7	R/W	Transceiver TX enable for SFP7 "1" = Transceiver turn off "0" = Transceiver turn on	0
5	TxDis_6	R/W	Transceiver TX enable for SFP6 "1" = Transceiver turn off "0" = Transceiver turn on	0
4	TxDis_5	R/W	Transceiver TX enable for SFP5 "1" = Transceiver turn off "0" = Transceiver turn on	0
3	TxDis_4	R/W	Transceiver TX enable for SFP4 "1" = Transceiver turn off "0" = Transceiver turn on	0
2	TxDis_3	R/W	Transceiver TX enable for SFP3 "1" = Transceiver turn off "0" = Transceiver turn on	0
1	TxDis_2	R/W	Transceiver TX enable for SFP2 "1" = Transceiver turn off "0" = Transceiver turn on	0
0	TxDis_1	R/W	Transceiver TX enable for SFP1 "1" = Transceiver turn off "0" = Transceiver turn on	0

5.4.6 SWPLD, Tx Disable 2 of SFP transceiver Register (Offset: 0x06) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxDis_16	TxDis_15	TxDis_14	TxDis_13	TxDis_12	TxDis_11	TxDis_10	TxDis_9

Bit	Name	R/W	Description	Default
7	TxDis_16	R/W	Transceiver TX enable for SFP16 "1" = Transceiver turn off "0" = Transceiver turn on	0
6	TxDis_15	R/W	Transceiver TX enable for SFP15 "1" = Transceiver turn off "0" = Transceiver turn on	0
5	TxDis_14	R/W	Transceiver TX enable for SFP14 "1" = Transceiver turn off "0" = Transceiver turn on	0
4	TxDis_13	R/W	Transceiver TX enable for SFP13 "1" = Transceiver turn off "0" = Transceiver turn on	0
3	TxDis_12	R/W	Transceiver TX enable for SFP12 "1" = Transceiver turn off "0" = Transceiver turn on	0
2	TxDis_11	R/W	Transceiver TX enable for SFP11 "1" = Transceiver turn off "0" = Transceiver turn on	0
1	TxDis_10	R/W	Transceiver TX enable for SFP10 "1" = Transceiver turn off "0" = Transceiver turn on	0
0	TxDis_9	R/W	Transceiver TX enable for SFP9 "1" = Transceiver turn off "0" = Transceiver turn on	0

5.4.7 SWPLD, Tx Disable 3 of SFP transceiver Register (Offset: 0x07) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxDis_24	TxDis_23	TxDis_22	TxDis_21	TxDis_20	TxDis_19	TxDis_18	TxDis_17

Bit	Name	R/W	Description	Default
7	TxDis_24	R/W	Transceiver TX enable for SFP24 "1" = Transceiver turn off "0" = Transceiver turn on	0
6	TxDis_23	R/W	Transceiver TX enable for SFP23 "1" = Transceiver turn off "0" = Transceiver turn on	0
5	TxDis_22	R/W	Transceiver TX enable for SFP22 "1" = Transceiver turn off "0" = Transceiver turn on	0
4	TxDis_21	R/W	Transceiver TX enable for SFP21 "1" = Transceiver turn off "0" = Transceiver turn on	0
3	TxDis_20	R/W	Transceiver TX enable for SFP20 "1" = Transceiver turn off "0" = Transceiver turn on	0
2	TxDis_19	R/W	Transceiver TX enable for SFP19 "1" = Transceiver turn off "0" = Transceiver turn on	0
1	TxDis_18	R/W	Transceiver TX enable for SFP18 "1" = Transceiver turn off "0" = Transceiver turn on	0
0	TxDis_17	R/W	Transceiver TX enable for SFP17 "1" = Transceiver turn off "0" = Transceiver turn on	0

5.4.8 SWPLD, Tx Disable 4 of SFP transceiver Register (Offset: 0x08) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxDis_32	TxDis_31	TxDis_30	TxDis_29	TxDis_28	TxDis_27	TxDis_26	TxDis_25

Bit	Name	R/W	Description	Default
7	TxDis_32	R/W	Transceiver TX enable for SFP32 "1" = Transceiver turn off "0" = Transceiver turn on	0
6	TxDis_31	R/W	Transceiver TX enable for SFP31 "1" = Transceiver turn off "0" = Transceiver turn on	0
5	TxDis_30	R/W	Transceiver TX enable for SFP30 "1" = Transceiver turn off "0" = Transceiver turn on	0
4	TxDis_29	R/W	Transceiver TX enable for SFP29 "1" = Transceiver turn off "0" = Transceiver turn on	0
3	TxDis_28	R/W	Transceiver TX enable for SFP28 "1" = Transceiver turn off "0" = Transceiver turn on	0
2	TxDis_27	R/W	Transceiver TX enable for SFP27 "1" = Transceiver turn off "0" = Transceiver turn on	0
1	TxDis_26	R/W	Transceiver TX enable for SFP26 "1" = Transceiver turn off "0" = Transceiver turn on	0
0	TxDis_25	R/W	Transceiver TX enable for SFP25 "1" = Transceiver turn off "0" = Transceiver turn on	0

5.4.9 SWPLD, Tx Disable 5 of SFP transceiver Register (Offset: 0x09) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxDis_40	TxDis_39	TxDis_38	TxDis_37	TxDis_36	TxDis_35	TxDis_34	TxDis_33

Bit	Name	R/W	Description	Default
7	TxDis_40	R/W	Transceiver TX enable for SFP40 "1" = Transceiver turn off "0" = Transceiver turn on	0
6	TxDis_39	R/W	Transceiver TX enable for SFP39 "1" = Transceiver turn off "0" = Transceiver turn on	0
5	TxDis_38	R/W	Transceiver TX enable for SFP38 "1" = Transceiver turn off "0" = Transceiver turn on	0
4	TxDis_37	R/W	Transceiver TX enable for SFP37 "1" = Transceiver turn off "0" = Transceiver turn on	0
3	TxDis_36	R/W	Transceiver TX enable for SFP36 "1" = Transceiver turn off "0" = Transceiver turn on	0
2	TxDis_35	R/W	Transceiver TX enable for SFP35 "1" = Transceiver turn off "0" = Transceiver turn on	0
1	TxDis_34	R/W	Transceiver TX enable for SFP34 "1" = Transceiver turn off "0" = Transceiver turn on	0
0	TxDis_33	R/W	Transceiver TX enable for SFP33 "1" = Transceiver turn off "0" = Transceiver turn on	0

5.4.10 SWPLD, Tx Disable 6 of SFP transceiver Register (Offset: 0x0a) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxDis_48	TxDis_47	TxDis_46	TxDis_45	TxDis_44	TxDis_43	TxDis_42	TxDis_41

Bit	Name	R/W	Description	Default
7	TxDis_48	R/W	Transceiver TX enable for SFP48 "1" = Transceiver turn off "0" = Transceiver turn on	0
6	TxDis_47	R/W	Transceiver TX enable for SFP47 "1" = Transceiver turn off "0" = Transceiver turn on	0
5	TxDis_46	R/W	Transceiver TX enable for SFP46 "1" = Transceiver turn off "0" = Transceiver turn on	0
4	TxDis_45	R/W	Transceiver TX enable for SFP45 "1" = Transceiver turn off "0" = Transceiver turn on	0
3	TxDis_44	R/W	Transceiver TX enable for SFP44 "1" = Transceiver turn off "0" = Transceiver turn on	0
2	TxDis_43	R/W	Transceiver TX enable for SFP43 "1" = Transceiver turn off "0" = Transceiver turn on	0
1	TxDis_42	R/W	Transceiver TX enable for SFP42 "1" = Transceiver turn off "0" = Transceiver turn on	0
0	TxDis_41	R/W	Transceiver TX enable for SFP41 "1" = Transceiver turn off "0" = Transceiver turn on	0

5.4.11 SWPLD, RxLos 1 of SFP transceiver Register (Offset: 0x0b) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLos_8	RxLos_7	RxLos_6	RxLos_5	RxLos_4	RxLos_3	RxLos_2	RxLos_1

Bit	Name	R/W	Description	Default
7	RxLos_8	R	Transceiver RxLos for SFP8 “1” = optical signal level below that specified “0” = Optical signal level is normal	1
6	RxLos_7	R	Transceiver RxLos for SFP7 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
5	RxLos_6	R	Transceiver RxLos for SFP6 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
4	RxLos_5	R	Transceiver RxLos for SFP5 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
3	RxLos_4	R	Transceiver RxLos for SFP4 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
2	RxLos_3	R	Transceiver RxLos for SFP3 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
1	RxLos_2	R	Transceiver RxLos for SFP2 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
0	RxLos_1	R	Transceiver RxLos for SFP1 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1

5.4.12 SWPLD, RxLos 2 of SFP transceiver Register (Offset: 0x0c) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLos_16	RxLos_15	RxLos_14	RxLos_13	RxLos_12	RxLos_11	RxLos_10	RxLos_9

Bit	Name	R/W	Description	Default
7	RxLos_16	R	Transceiver RxLos for SFP16 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
6	RxLos_15	R	Transceiver RxLos for SFP15 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
5	RxLos_14	R	Transceiver RxLos for SFP14 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
4	RxLos_13	R	Transceiver RxLos for SFP13 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
3	RxLos_12	R	Transceiver RxLos for SFP12 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
2	RxLos_11	R	Transceiver RxLos for SFP11 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
1	RxLos_10	R	Transceiver RxLos for SFP10 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
0	RxLos_9	R	Transceiver RxLos for SFP9 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1

5.4.13 SWPLD, RxLos 3 of SFP transceiver Register (Offset: 0x0d) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLos_24	RxLos_23	RxLos_22	RxLos_21	RxLos_20	RxLos_19	RxLos_18	RxLos_17

Bit	Name	R/W	Description	Default
7	RxLos_24	R	Transceiver RxLos for SFP24 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
6	RxLos_23	R	Transceiver RxLos for SFP23 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
5	RxLos_22	R	Transceiver RxLos for SFP22 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
4	RxLos_21	R	Transceiver RxLos for SFP21 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
3	RxLos_20	R	Transceiver RxLos for SFP20 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
2	RxLos_19	R	Transceiver RxLos for SFP19 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
1	RxLos_18	R	Transceiver RxLos for SFP18 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
0	RxLos_17	R	Transceiver RxLos for SFP17 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1

5.4.14 SWPLD, RxLos 4 of SFP transceiver Register (Offset: 0x0e) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLos_32	RxLos_31	RxLos_30	RxLos_29	RxLos_28	RxLos_27	RxLos_26	RxLos_25

Bit	Name	R/W	Description	Default
7	RxLos_32	R	Transceiver RxLos for SFP32 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
6	RxLos_31	R	Transceiver RxLos for SFP31 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
5	RxLos_30	R	Transceiver RxLos for SFP30 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
4	RxLos_29	R	Transceiver RxLos for SFP29 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
3	RxLos_28	R	Transceiver RxLos for SFP28 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
2	RxLos_27	R	Transceiver RxLos for SFP27 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
1	RxLos_26	R	Transceiver RxLos for SFP26 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1
0	RxLos_25	R	Transceiver RxLos for SFP25 "1" = Optical signal level below that specified "0" = Optical signal level is normal	1

5.4.15 SWPLD, RxLos 5 of SFP transceiver Register (Offset: 0x0f) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLos_40	RxLos_39	RxLos_38	RxLos_37	RxLos_36	RxLos_35	RxLos_34	RxLos_33

Bit	Name	R/W	Description	Default
7	RxLos_40	R	Transceiver RxLos for SFP40 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
6	RxLos_39	R	Transceiver RxLos for SFP39 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
5	RxLos_38	R	Transceiver RxLos for SFP38 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
4	RxLos_37	R	Transceiver RxLos for SFP37 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
3	RxLos_36	R	Transceiver RxLos for SFP36 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
2	RxLos_35	R	Transceiver RxLos for SFP35 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
1	RxLos_34	R	Transceiver RxLos for SFP34 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
0	RxLos_33	R	Transceiver RxLos for SFP33 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1

5.4.16 SWPLD, RxLos 6 of SFP transceiver Register (Offset: 0x10) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLos_48	RxLos_47	RxLos_46	RxLos_45	RxLos_44	RxLos_43	RxLos_42	RxLos_41

Bit	Name	R/W	Description	Default
7	RxLos_48	R	Transceiver RxLos for SFP48 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
6	RxLos_47	R	Transceiver RxLos for SFP47 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
5	RxLos_46	R	Transceiver RxLos for SFP46 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
4	RxLos_45	R	Transceiver RxLos for SFP45 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
3	RxLos_44	R	Transceiver RxLos for SFP44 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
2	RxLos_43	R	Transceiver RxLos for SFP43 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
1	RxLos_42	R	Transceiver RxLos for SFP42 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1
0	RxLos_41	R	Transceiver RxLos for SFP41 “1” = Optical signal level below that specified “0” = Optical signal level is normal	1

5.4.17 SWPLD, Present 1 of SFP transceiver Register (Offset: 0x11) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Present_8	Present_7	Present_6	Present_5	Present_4	Present_3	Present_2	Present_1

Bit	Name	R/W	Description	Default
7	Present_8	R	Transceiver Present for SFP8 “1” = Absent “0” = Present	1
6	Present_7	R	Transceiver Present for SFP7 “1” = Absent “0” = Present	1
5	Present_6	R	Transceiver Present for SFP6 “1” = Absent “0” = Present	1
4	Present_5	R	Transceiver Present for SFP5 “1” = Absent “0” = Present	1
3	Present_4	R	Transceiver Present for SFP4 “1” = Absent “0” = Present	1
2	Present_3	R	Transceiver Present for SFP3 “1” = Absent “0” = Present	1
1	Present_2	R	Transceiver Present for SFP2 “1” = Absent “0” = Present	1
0	Present_1	R	Transceiver Present for SFP1 “1” = Absent “0” = Present	1

5.4.18 SWPLD, Present 2 of SFP transceiver Register (Offset: 0x12) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Present_16	Present_15	Present_14	Present_13	Present_12	Present_11	Present_10	Present_9

Bit	Name	R/W	Description	Default
7	Present_16	R	Transceiver Present for SFP16 "1" = Absent "0" = Present	1
6	Present_15	R	Transceiver Present for SFP15 "1" = Absent "0" = Present	1
5	Present_14	R	Transceiver Present for SFP14 "1" = Absent "0" = Present	1
4	Present_13	R	Transceiver Present for SFP13 "1" = Absent "0" = Present	1
3	Present_12	R	Transceiver Present for SFP12 "1" = Absent "0" = Present	1
2	Present_11	R	Transceiver Present for SFP11 "1" = Absent "0" = Present	1
1	Present_10	R	Transceiver Present for SFP10 "1" = Absent "0" = Present	1
0	Present_9	R	Transceiver Present for SFP9 "1" = Absent "0" = Present	1

5.4.19 SWPLD, Present 3 of SFP transceiver Register (Offset: 0x13) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Present_24	Present_23	Present_22	Present_21	Present_20	Present_19	Present_18	Present_17

Bit	Name	R/W	Description	Default
7	Present_24	R	Transceiver Present for SFP24 “1” = Absent “0” = Present	1
6	Present_23	R	Transceiver Present for SFP23 “1” = Absent “0” = Present	1
5	Present_22	R	Transceiver Present for SFP22 “1” = Absent “0” = Present	1
4	Present_21	R	Transceiver Present for SFP21 “1” = Absent “0” = Present	1
3	Present_20	R	Transceiver Present for SFP20 “1” = Absent “0” = Present	1
2	Present_19	R	Transceiver Present for SFP19 “1” = Absent “0” = Present	1
1	Present_18	R	Transceiver Present for SFP18 “1” = Absent “0” = Present	1
0	Present_17	R	Transceiver Present for SFP17 “1” = Absent “0” = Present	1

5.4.20 SWPLD, Present 4 of SFP transceiver Register (Offset: 0x14) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Present_32	Present_31	Present_30	Present_29	Present_28	Present_27	Present_26	Present_25

Bit	Name	R/W	Description	Default
7	Present_32	R	Transceiver Present for SFP32 "1" = Absent "0" = Present	1
6	Present_31	R	Transceiver Present for SFP31 "1" = Absent "0" = Present	1
5	Present_30	R	Transceiver Present for SFP30 "1" = Absent "0" = Present	1
4	Present_29	R	Transceiver Present for SFP29 "1" = Absent "0" = Present	1
3	Present_28	R	Transceiver Present for SFP28 "1" = Absent "0" = Present	1
2	Present_27	R	Transceiver Present for SFP27 "1" = Absent "0" = Present	1
1	Present_26	R	Transceiver Present for SFP26 "1" = Absent "0" = Present	1
0	Present_25	R	Transceiver Present for SFP25 "1" = Absent "0" = Present	1

5.4.21 SWPLD, Present 5 of SFP transceiver Register (Offset: 0x15) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Present_40	Present_39	Present_38	Present_37	Present_36	Present_35	Present_34	Present_33

Bit	Name	R/W	Description	Default
7	Present_40	R	Transceiver Present for SFP40 “1” = Absent “0” = Present	1
6	Present_39	R	Transceiver Present for SFP39 “1” = Absent “0” = Present	1
5	Present_38	R	Transceiver Present for SFP38 “1” = Absent “0” = Present	1
4	Present_37	R	Transceiver Present for SFP37 “1” = Absent “0” = Present	1
3	Present_36	R	Transceiver Present for SFP36 “1” = Absent “0” = Present	1
2	Present_35	R	Transceiver Present for SFP35 “1” = Absent “0” = Present	1
1	Present_34	R	Transceiver Present for SFP34 “1” = Absent “0” = Present	1
0	Present_33	R	Transceiver Present for SFP33 “1” = Absent “0” = Present	1

5.4.22 SWPLD, Present 6 of SFP transceiver Register (Offset: 0x16) – Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Present_48	Present_47	Present_46	Present_45	Present_44	Present_43	Present_42	Present_41

Bit	Name	R/W	Description	Default
7	Present_48	R	Transceiver Present for SFP48 “1” = Absent “0” = Present	1
6	Present_47	R	Transceiver Present for SFP47 “1” = Absent “0” = Present	1
5	Present_46	R	Transceiver Present for SFP46 “1” = Absent “0” = Present	1
4	Present_45	R	Transceiver Present for SFP45 “1” = Absent “0” = Present	1
3	Present_44	R	Transceiver Present for SFP44 “1” = Absent “0” = Present	1
2	Present_43	R	Transceiver Present for SFP43 “1” = Absent “0” = Present	1
1	Present_42	R	Transceiver Present for SFP42 “1” = Absent “0” = Present	1
0	Present_41	R	Transceiver Present for SFP41 “1” = Absent “0” = Present	1

5.4.23 SWPLD, Tx_fault 1 of SFP transceiver Register (Offset: 0x17) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_fault_8	Tx_fault_7	Tx_fault_6	Tx_fault_5	Tx_fault_4	Tx_fault_3	Tx_fault_2	Tx_fault_1

Bit	Name	R/W	Description	Default
7	Tx_fault_8	R	Transceiver Tx_fault for SFP8 “1” = detected Tx_fault “0” = normal	1
6	Tx_fault_7	R	Transceiver Tx_fault for SFP7 “1” = detected Tx_fault “0” = normal	1
5	Tx_fault_6	R	Transceiver Tx_fault for SFP6 “1” = detected Tx_fault “0” = normal	1
4	Tx_fault_5	R	Transceiver Tx_fault for SFP5 “1” = detected Tx_fault “0” = normal	1
3	Tx_fault_4	R	Transceiver Tx_fault for SFP4 “1” = detected Tx_fault “0” = normal	1
2	Tx_fault_3	R	Transceiver Tx_fault for SFP3 “1” = detected Tx_fault “0” = normal	1
1	Tx_fault_2	R	Transceiver Tx_fault for SFP2 “1” = detected Tx_fault “0” = normal	1
0	Tx_fault_1	R	Transceiver Tx_fault for SFP1 “1” = detected Tx_fault “0” = normal	1

5.4.24 SWPLD, Tx_fault 2 of SFP transceiver Register (Offset: 0x18) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_fault_16	Tx_fault_15	Tx_fault_14	Tx_fault_13	Tx_fault_12	Tx_fault_11	Tx_fault_10	Tx_fault_9

Bit	Name	R/W	Description	Default
7	Tx_fault_16	R	Transceiver Tx_fault for SFP16 “1” = detected Tx_fault “0” = normal	1
6	Tx_fault_15	R	Transceiver Tx_fault for SFP15 “1” = detected Tx_fault “0” = normal	1
5	Tx_fault_14	R	Transceiver Tx_fault for SFP14 “1” = detected Tx_fault “0” = normal	1
4	Tx_fault_13	R	Transceiver Tx_fault for SFP13 “1” = detected Tx_fault “0” = normal	1
3	Tx_fault_12	R	Transceiver Tx_fault for SFP12 “1” = detected Tx_fault “0” = normal	1
2	Tx_fault_11	R	Transceiver Tx_fault for SFP11 “1” = detected Tx_fault “0” = normal	1
1	Tx_fault_10	R	Transceiver Tx_fault for SFP10 “1” = detected Tx_fault “0” = normal	1
0	Tx_fault_9	R	Transceiver Tx_fault for SFP9 “1” = detected Tx_fault “0” = normal	1

5.4.25 SWPLD, Tx_fault 3 of SFP transceiver Register (Offset: 0x19) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_fault_24	Tx_fault_23	Tx_fault_22	Tx_fault_21	Tx_fault_20	Tx_fault_19	Tx_fault_18	Tx_fault_17

Bit	Name	R/W	Description	Default
7	Tx_fault_24	R	Transceiver Tx_fault for SFP24 "1" = detected Tx_fault "0" = normal	1
6	Tx_fault_23	R	Transceiver Tx_fault for SFP23 "1" = detected Tx_fault "0" = normal	1
5	Tx_fault_22	R	Transceiver Tx_fault for SFP22 "1" = detected Tx_fault "0" = normal	1
4	Tx_fault_21	R	Transceiver Tx_fault for SFP21 "1" = detected Tx_fault "0" = normal	1
3	Tx_fault_20	R	Transceiver Tx_fault for SFP20 "1" = detected Tx_fault "0" = normal	1
2	Tx_fault_19	R	Transceiver Tx_fault for SFP19 "1" = detected Tx_fault "0" = normal	1
1	Tx_fault_18	R	Transceiver Tx_fault for SFP18 "1" = detected Tx_fault "0" = normal	1
0	Tx_fault_17	R	Transceiver Tx_fault for SFP17 "1" = detected Tx_fault "0" = normal	1

5.4.26 SWPLD, Tx_fault 4 of SFP transceiver Register (Offset: 0x1a) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_fault_32	Tx_fault_31	Tx_fault_30	Tx_fault_29	Tx_fault_28	Tx_fault_27	Tx_fault_26	Tx_fault_25

Bit	Name	R/W	Description	Default
7	Tx_fault_32	R	Transceiver Tx_fault for SFP32 “1” = detected Tx_fault “0” = normal	1
6	Tx_fault_31	R	Transceiver Tx_fault for SFP31 “1” = detected Tx_fault “0” = normal	1
5	Tx_fault_30	R	Transceiver Tx_fault for SFP30 “1” = detected Tx_fault “0” = normal	1
4	Tx_fault_29	R	Transceiver Tx_fault for SFP29 “1” = detected Tx_fault “0” = normal	1
3	Tx_fault_28	R	Transceiver Tx_fault for SFP28 “1” = detected Tx_fault “0” = normal	1
2	Tx_fault_27	R	Transceiver Tx_fault for SFP27 “1” = detected Tx_fault “0” = normal	1
1	Tx_fault_26	R	Transceiver Tx_fault for SFP26 “1” = detected Tx_fault “0” = normal	1
0	Tx_fault_25	R	Transceiver Tx_fault for SFP25 “1” = detected Tx_fault “0” = normal	1

5.4.27 SWPLD, Tx_fault 5 of SFP transceiver Register (Offset: 0x1b) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_fault_40	Tx_fault_39	Tx_fault_38	Tx_fault_37	Tx_fault_36	Tx_fault_35	Tx_fault_34	Tx_fault_33

Bit	Name	R/W	Description	Default
7	Tx_fault_40	R	Transceiver Tx_fault for SFP40 “1” = detected Tx_fault “0” = normal	1
6	Tx_fault_39	R	Transceiver Tx_fault for SFP39 “1” = detected Tx_fault “0” = normal	1
5	Tx_fault_38	R	Transceiver Tx_fault for SFP38 “1” = detected Tx_fault “0” = normal	1
4	Tx_fault_37	R	Transceiver Tx_fault for SFP37 “1” = detected Tx_fault “0” = normal	1
3	Tx_fault_36	R	Transceiver Tx_fault for SFP36 “1” = detected Tx_fault “0” = normal	1
2	Tx_fault_35	R	Transceiver Tx_fault for SFP35 “1” = detected Tx_fault “0” = normal	1
1	Tx_fault_34	R	Transceiver Tx_fault for SFP34 “1” = detected Tx_fault “0” = normal	1
0	Tx_fault_33	R	Transceiver Tx_fault for SFP33 “1” = detected Tx_fault “0” = normal	1

5.4.28 SWPLD, Tx_fault 6 of SFP transceiver Register (Offset: 0x1c) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tx_fault_48	Tx_fault_47	Tx_fault_46	Tx_fault_45	Tx_fault_44	Tx_fault_43	Tx_fault_42	Tx_fault_41

Bit	Name	R/W	Description	Default
7	Tx_fault_48	R	Transceiver Tx_fault for SFP48 “1” = detected Tx_fault “0” = normal	1
6	Tx_fault_47	R	Transceiver Tx_fault for SFP47 “1” = detected Tx_fault “0” = normal	1
5	Tx_fault_46	R	Transceiver Tx_fault for SFP46 “1” = detected Tx_fault “0” = normal	1
4	Tx_fault_45	R	Transceiver Tx_fault for SFP45 “1” = detected Tx_fault “0” = normal	1
3	Tx_fault_44	R	Transceiver Tx_fault for SFP44 “1” = detected Tx_fault “0” = normal	1
2	Tx_fault_43	R	Transceiver Tx_fault for SFP43 “1” = detected Tx_fault “0” = normal	1
1	Tx_fault_42	R	Transceiver Tx_fault for SFP42 “1” = detected Tx_fault “0” = normal	1
0	Tx_fault_41	R	Transceiver Tx fault for SFP41 “1” = detected Tx_fault “0” = normal	1

5.4.29 SWPLD, SFP INT Register (Offset: 0x1d) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SFP43-48_INT	SFP37-42_INT	SFP31-36_INT	SFP25-30_INT	SFP19-24_INT	SFP13-18_INT	SFP7-12_INT	SFP1-6_INT

Bit	Name	R/W	Description	Default
7	SFP43-48_INT	R/W	SFP43-48 issue INT. When status of SFP43-48 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
6	SFP37-42_INT	R/W	SFP37-42 issue INT. When status of SFP37-42 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
5	SFP31-36_INT	R/W	SFP31-36 issue INT. When status of SFP31-36 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
4	SFP25-30_INT	R/W	SFP25-30 issue INT. When status of SFP25-30 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
3	SFP19-24_INT	R/W	SFP19-24 issue INT. When status of SFP19-24 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
2	SFP13-18_INT	R/W	SFP13-18 issue INT. When status of SFP13-18 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
1	SFP7-12_INT	R/W	SFP7-12 issue INT. When status of SFP7-12 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1
0	SFP1-6_INT	R/W	SFP1-6 issue INT. When status of SFP1-6 (TX_Dis, RXLos, Present, TX_Fault) change, this bit will be '0'. "1" = nothing "0" = INT.	1

5.4.30 SWPLD, Retimer PHY_INT Register (Offset: 0x1e) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PHYB_INT	PHYA_INT

Bit	Name	R/W	Description	Default
7-0	Reserved	--	--	-
1	PHYB_INT	R/W	Retimer PHYB_INT "1" = nothing "0" = INT.	1
0	PHYA_INT	R/W	Retimer PHYA_INT "1" = nothing "0" = INT.	1

5.4.31 SWPLD, QSFP Rsent/Mosel Register (Offset: 0x1f) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Modsel3	Modsel2	Modsel1	Modsel0	QSFPRes3	QSFPRes2	QSFPRes1	QSFPRes0

Bit	Name	R/W	Description	Default
7	Modsel3	R/W	Modsel for QSFP3: cable select "1" = can not use i2c bus "0" = can use i2c bus	1
6	Modsel2	R/W	Modsel for QSFP2: cable select "1" = can not use i2c bus "0" = can use i2c bus	1
5	Modsel1	R/W	Modsel for QSFP1 : cable select "1" = can not use i2c bus "0" = can use i2c bus	1
4	Modsel0	R/W	Modsel for QSFP0: cable select "1" = can not use i2c bus "0" = can use i2c bus	1
3	QSFPRes3	R/W	Reset for QSFP3 "1" = normal "0" = reset	1
2	QSFPRes2	R/W	Reset for QSFP2 "1" = normal "0" = reset	1
1	QSFPRes1	R/W	Reset for QSFP1 "1" = normal "0" = reset	1
0	QSFPRes0	R/W	Reset for QSFP0 "1" = normal "0" = reset	1

※ RXLos/Present/LPmode of QSFP are connect to BCM84328.

5.4.32 SWPLD, Retimer Rsest Register (Offset: 0x20) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Retimer B Rsest	Retimer A Rsest

Bit	Name	R/W	Description	Default
7-2	Reserved	--	--	-
1	Retimer B Rsest	R/W	Retimer PHY_B Rsest "1" = normal "0" = Reset	0
0	Retimer A Rsest	R/W	Retimer PHY_A Rsest "1" = normal "0" = Reset	0

5.4.33 SWPLD, Reserved Register (Offset: 0x21) – Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Name	R/W	Description	Default
7-4	Reserved	--	--	-

6. I2C Subsystem

6.1. I2C tree

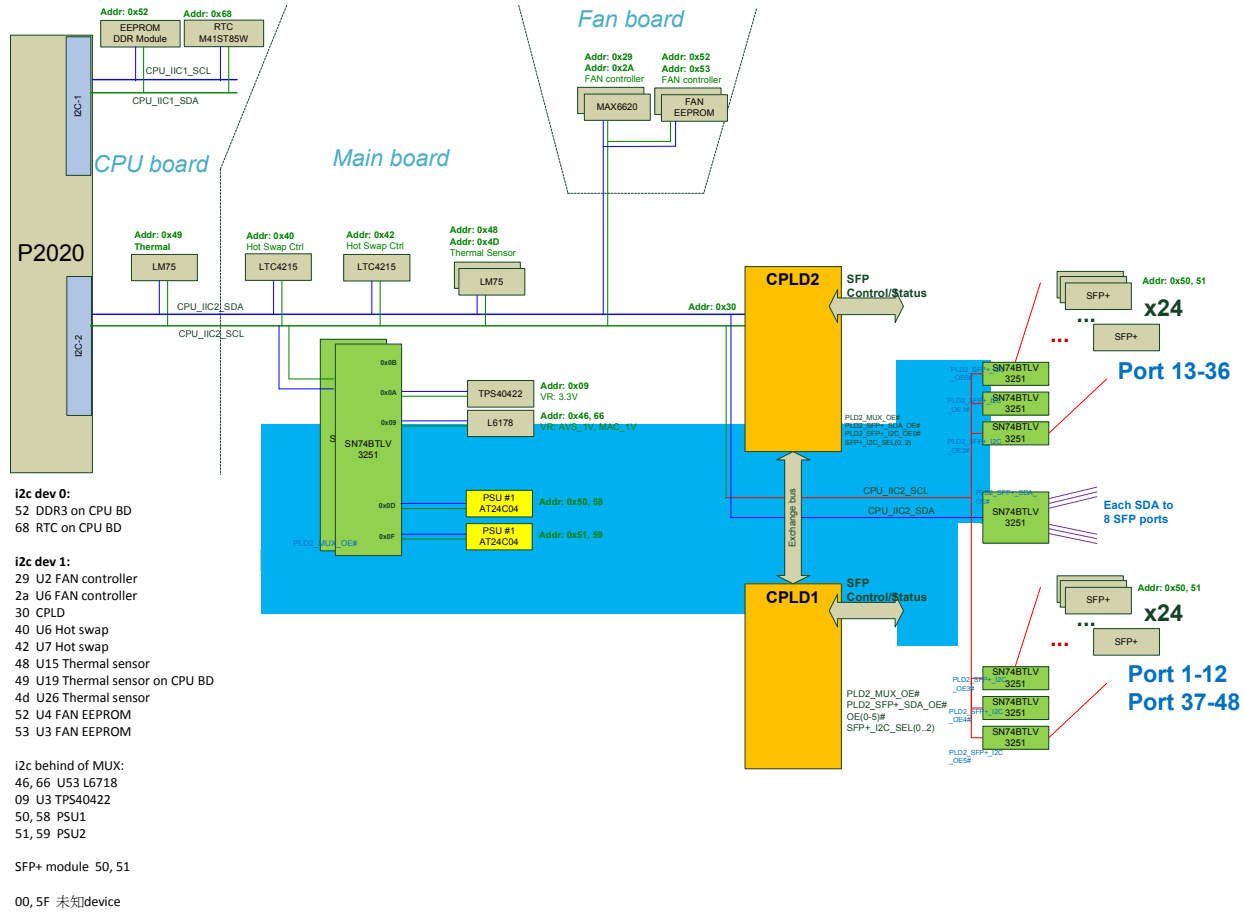
Bus description

I2C Bus used for access/program thermal sensor, power supply, FAN controller and RTC timer. The I2C channel-1 will be support to DDR2 module and RTC device and the I2C channel-2 will have TMP75, FAN controller, PSU and Hot Swap IC.

Speeds

To supports a maximum clock rate of 2080 KHz

I2C of Kuga7048



i2c dev 0:
52 DDR3 on CPU BD
68 RTC on CPU BD

i2c dev 1:
29 U2 FAN controller
2a U6 FAN controller
30 CPLD
40 U6 Hot swap
42 U7 Hot swap
48 U15 Thermal sensor
49 U19 Thermal sensor on CPU BD
4d U26 Thermal sensor
52 U4 FAN EEPROM
53 U3 FAN EEPROM

i2c behind of MUX:
46, 66 U53 L6718
09 U3 TPS40422
50, 58 PSU1
51, 59 PSU2

SFP+ module 50, 51

00, 5F 未知device

Figure 16: I2C blockdiagram

6.2. I2C device addressing

I2C channel-1 address table

Device Name	Description	ID#	Remark
DDR3 module	DDR3 SDRAM	0xA4	
RTC	Real time clock w/ X' TAL and Battery	0xD0	

I2C channel-2 address table

Device	Description	ID#	Remark
Power controller #1	Hot Swap/Current monitoring	0x80	
Power controller #2	Hot Swap/Current monitoring	0x84	
TPM75 #A	Thermal sensor on CPU BD	0x92	
TPM75 #B	Thermal sensor on Main BD	0x90	
TPM75 #C	Thermal sensor on Main BD	0x9A	
Device behind of MUX	Description	ID#	Remark
DCDC_	ST L6718	0x 8C, CC	MUX_A. B1
DCDC_	TPS40422	0x18	MUX_A. B2
FAN controller#A	FAN speed controller	0x52	MUX_A. B4
FAN Tray 1	FAN set 1	0xA6	MUX_A. B4
FAN Tray 2	FAN set 2	0xA4	MUX_A. B4
PSU #1	DPS-460KBB	0xA0, B0	MUX_A. B5
PSU #2	DPS-460KBB	0xA2, B2	MUX_A. B7
SFP Transceiver		0xA0, A2	MUX_B for 48 port SFP

I2C channel of SFP+ address table

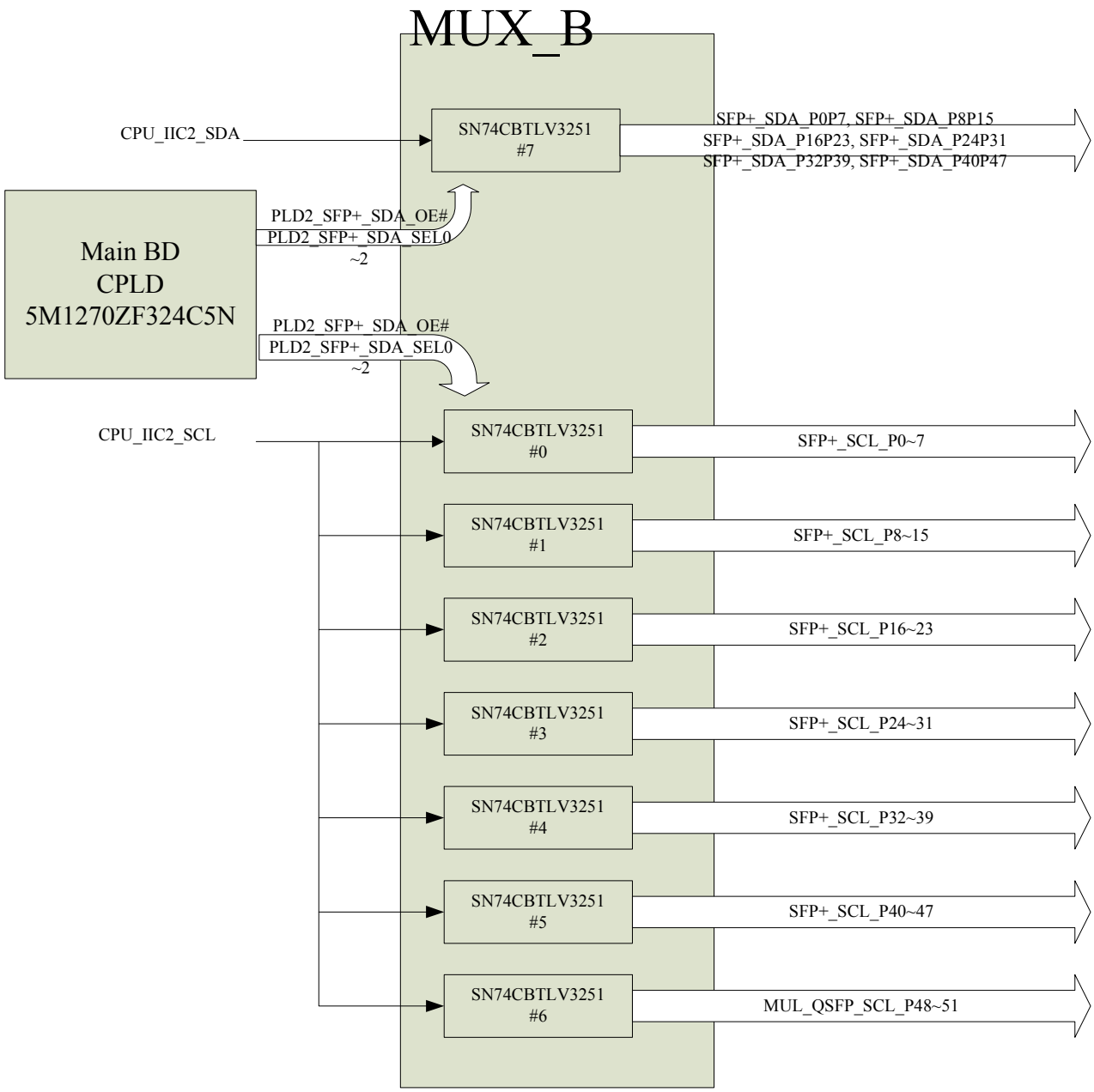


Figure 17: I2C to SFP+ ports

7. RTC

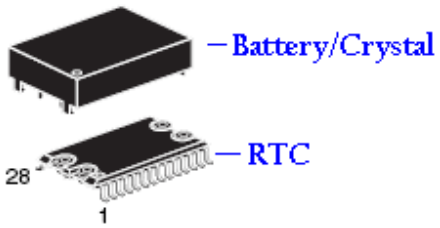
The M41ST85W is a combination Serial Real-Time Clock, Microprocessor Supervisor, and NVRAM Supervisor. It is built in a low power CMOS SRAM process and has a 64-byte memory space with 44 bytes of NVRAM and 20 memory-mapped RTC registers (see *Table 2 on page 20*). The RTC registers are configured in binary coded decimal (BCD) format.

The M41ST85W combines a 400kHz I^2C Serial RTC with an Automatic Back-up Battery Switchover circuit for powering an external LPSRAM as well as the internal RTC. When power begins to fail, the switchover automatically connects to the back-up battery to keep the RTC and external LPSRAM alive in the absence of system power. Access to the LPSRAM is also cut off via a chip-enable gate function, thereby write-protecting the memory. A programmable Watchdog and Power-on Reset/Low Voltage Detect function are the key elements in the Microprocessor Supervisor section.

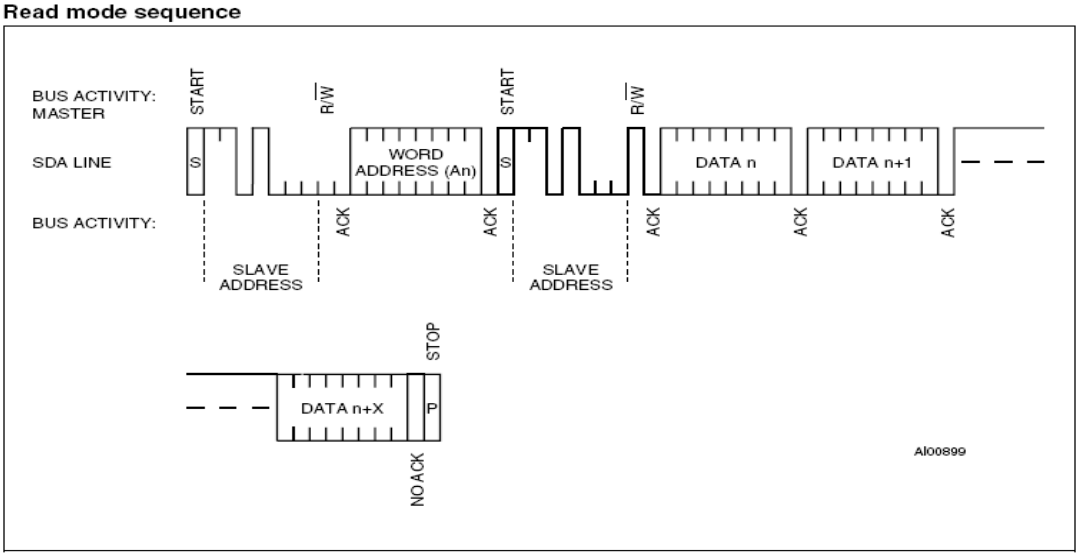
The Real-Time Clock includes a built-in 32.768kHz oscillator (crystal-controlled), which provides the time base for the timekeeping and calendar functions. Eight of the 20 clock registers provide the basic clock/calendar functions while the other 12 bytes provide status/control for the Alarm, Watchdog, and Squarewave functions.

Serial RTC features

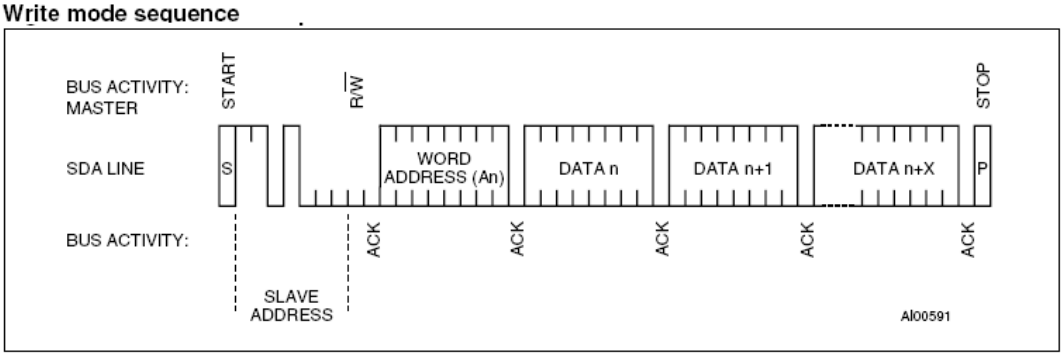
- 400kHz I^2C
- 44 bytes of general purpose NVRAM
- Counters for:
  - Seconds, minutes, hours, day, date, month, and year
  - Century
  - 10ths/100ths of seconds
  - Clock calibration register allows compensation for crystal variations over temperature
- Programmable alarm with repeat modes
  - Functions in battery back-up mode
- Power-down timestamp (HT Bit)
- 2.5 to 5.5V oscillator operating voltage



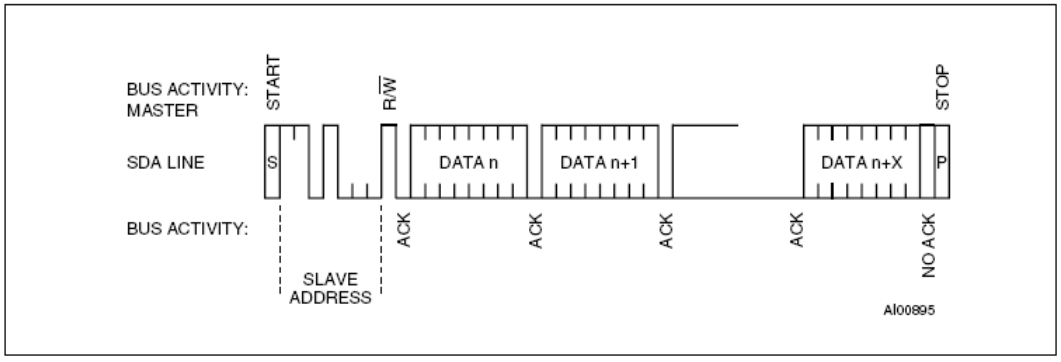
Read mode sequence



Write mode sequence



Alternate read mode sequence

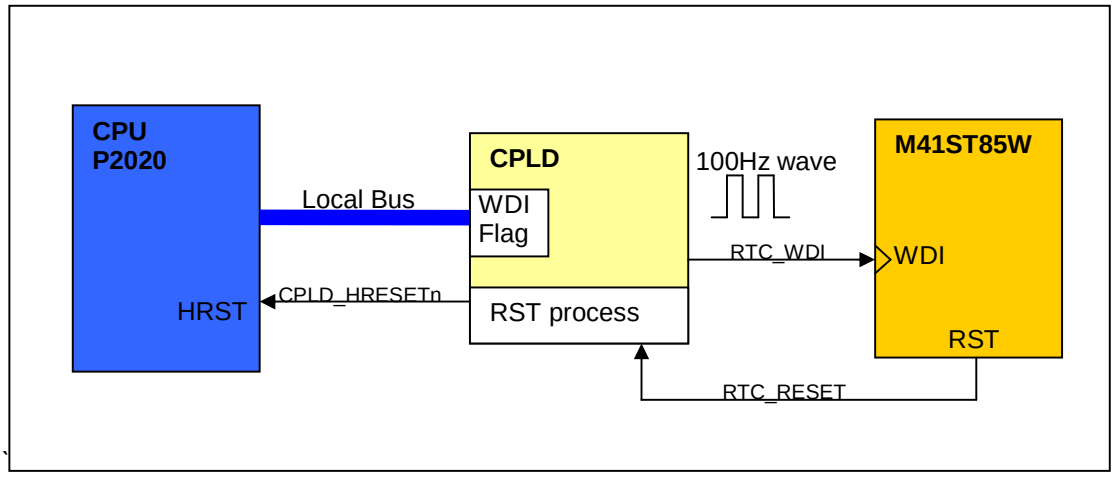


TIMEKEEPER® register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 Seconds				0.01 Seconds				Seconds	00-99
01h	ST	10 Seconds			Seconds				Seconds	00-59
02h	0	10 Minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 Hours		Hours (24 Hour Format)				Century/Hours	0-1/00-23
04h	TR	0	0	0	0	Day of Week			Day	01-7
05h	0	0	10 Date		Date: Day of Month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	Al 10M	Alarm Month				Al Month	01-12
0Bh	RPT4	RPT5	Al 10 Date		Alarm Date				Al Date	01-31
0Ch	RPT3	HT	Al 10 Hour		Alarm Hour				Al Hour	00-23
0Dh	RPT2	Alarm 10 Minutes			Alarm Minutes				Al Min	00-59
0Eh	RPT1	Alarm 10 Seconds			Alarm Seconds				Al Sec	00-59
0Fh	WDF	AF	0	BL	0	0	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

KEYS: S = Sign Bit
FT = Frequency Test Bit
ST = Stop Bit
0 = Must be set to zero
BL = Battery Low Flag (Read only)
BMB0-BMB4 = Watchdog Multiplier Bits
CEB = Century Enable Bit
CB = Century Bit
OUT = Output level
AFE = Alarm Flag Enable Flag
RB0-RB1 = Watchdog Resolution Bits
WDS = Watchdog Steering Bit
ABE = Alarm in Battery Back-Up Mode Enable Bit
RPT1-RPT5 = Alarm Repeat Mode Bits
WDF = Watchdog flag (Read only)
AF = Alarm flag (Read only)
SQWE = Square Wave Enable
RS0-RS3 = SQW Frequency
HT = Halt Update Bit
TR = t_{rec} Bit

7.1. Watchdog operation black diagram



- Please refer the M41ST85W datasheet as watchdog register setting. The watchdog timer by

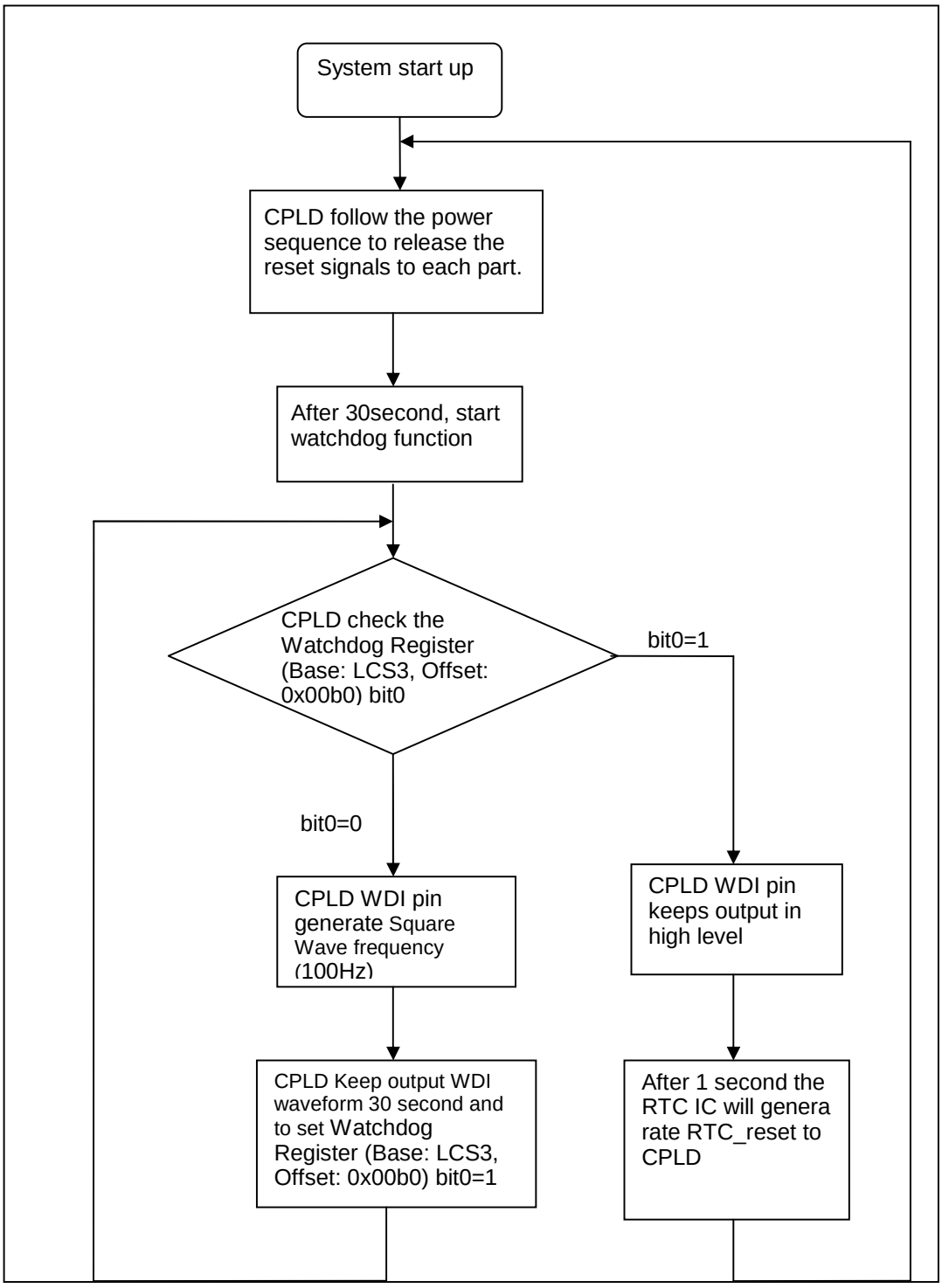
setting the desired amount of time-out into the Watchdog Register, address 09h.

- The RB [1:0] should be " 10" =1 seconds. And RMB [4:0] should be " 0011" =3. The Watchdog Register = 3*1 or 3 seconds.

09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	

- The CPU need to check and set the Watchdog Register (Base: LCS3, Offset: 0x00b0) bit0 per 10 second one time.

7.2. Watchdog timer working flow



8. Switching Subsystem

8.1. Switch Engine BCM56844

The Broadcom® BCM56844 family is a high performance 640Gbps network switch with 18 integrated Warp Cores. Each Warp Core has four integrated 10G SerDes for native support of 40 GbE, 10 GbE, HiGig+™, and HiGig2™ as well as XFI, XAUI™, 10GBASE-KR, 40GBASE-KR4, and XLAUI.

BCM56844 features

- Hardware-based encapsulations, including MPLS, VPLS, GRE, ISATAP, and MAC in MAC
- TRILL for hardware-based layer 2 multi pathing
- Congestion management capabilities including Priority Flow Control, Destination Module Flow Control, QCN, and Dynamic HiGig Load balancing
- Hardware-based storage virtualization
- Robust, proven architecture based upon StrataXGS
- Stacking ports can operate from 10G up to 40G using the HiGig or HiGig2 protocols
- Port trunking and remote mirroring support
- On-chip packet buffer memory with dynamic buffer management for maximum burst absorption
- Full IPv4 and IPv6 routing support
- Low latency
- Enhanced security and management capabilities
- Scheduling algorithms

- Strict Priority
- Round Robin
- Weighted Round Robin (WRR)
- Weighted Elastic Round Robin (WERR)

- Congestion control

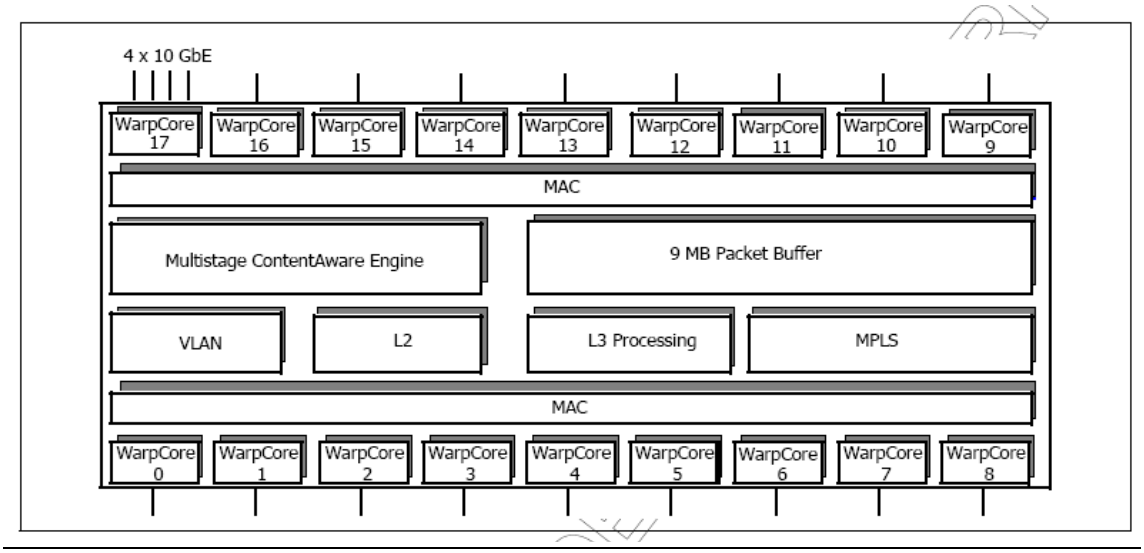
- HOL prevention
- Ingress back pressure (flow control)

- Three-stage ContentAware™ Processing
- Full Quality of Service (QoS) support

- Service Aware Flow Control (SAFC)
- Weighted RED
- srTCM and trTCM color marking and metering

- Extensive double tagging support
- Support for jumbo frames, up to 12K
- x2 PCIe™ Gen 2.0 interface to support a local CPU
- Storm control for broadcast, multicast, unknown unicast packets
- Scalable architecture supporting high performance switch designs of 5 Tbps and beyond
- Power and footprint optimized design with integrated 10G SerDes and Energy Efficient Ethernet principles maximizing port density per RU
- Interface flexibility coupled with hardware based features and Broadcom software enable common solutions across multiple form factors including blade, top of rack, and chassis

Functional overview



Interfaces

Interface	Description
10 GbE	• Integrated Quad 10G SerDes core • 10 GbE: XFI, KR • 40 GbE: XLAUI • Supports speeds ranging from 1G to 40G • Can operate in HiGig2 or HiGig+™ mode ranging from 10G to 40G • Full-duplex operation is supported (Half duplex is not supported at any speeds)
GE SerDes	• GE port full- and half-duplex mode of operation, compliant to IEEE 802.3. • 1000 Mbps using auto-negotiation (SGMII) • Integrated SerDes • SGMII • Jumbo frames, up to 12 KB
CPU (PCI, PCIe)	• PCI rev 2.2-compliant interface—32 bit, 66 MHz • PCIe v1.1a-compliant interface • Scatter-Gather DMA for packet transfer to CPU

	• Table DMA: For copying any switch table into system memory • Statistics DMA: For gathering on-chip statistics counters • Packet DMA: For transferring packets from/to the CPU • Master and Slave PCI mode
LED	• Control of up to 512 system LEDs at a 30 Hz refresh rate • Simple microcontroller with instructions optimized for LED control • Low-cost two-wire interface to system LEDs • 512 bytes of program RAM • 512 bytes of data RAM • Direct access to per-port speed, duplex state, flow control state, link state, transmit and receive activity, and collision activity
MIIM	• IEEE 802.3u-compliant MIIM interface for communication with external PHY devices • 2.5-MHz operation
BSC	• BSC-compliant interface • Supports slave mode, allowing an external microcontroller to configure the BCM56844 device • CPU controlled master mode to communicate with other BSC devices
JTAG	• JTAG-compliant interface used to support boundary scan operations • 20-MHz operation

8.2. BCM5461 Mgmt ports (10/100/1000 Mbps)

The P2020 have x4 SerDes channels for design. In the system, the SerDes 0/1 channels are for PCIe interfaces. The SerDes 2 is reserved. And SerDes 3 channel is for OOB port used. The software needs to set SGMII mode on SerDes 3 interface of PC2020. The OOB port has support 10/100/1000 Mpbs speeds.

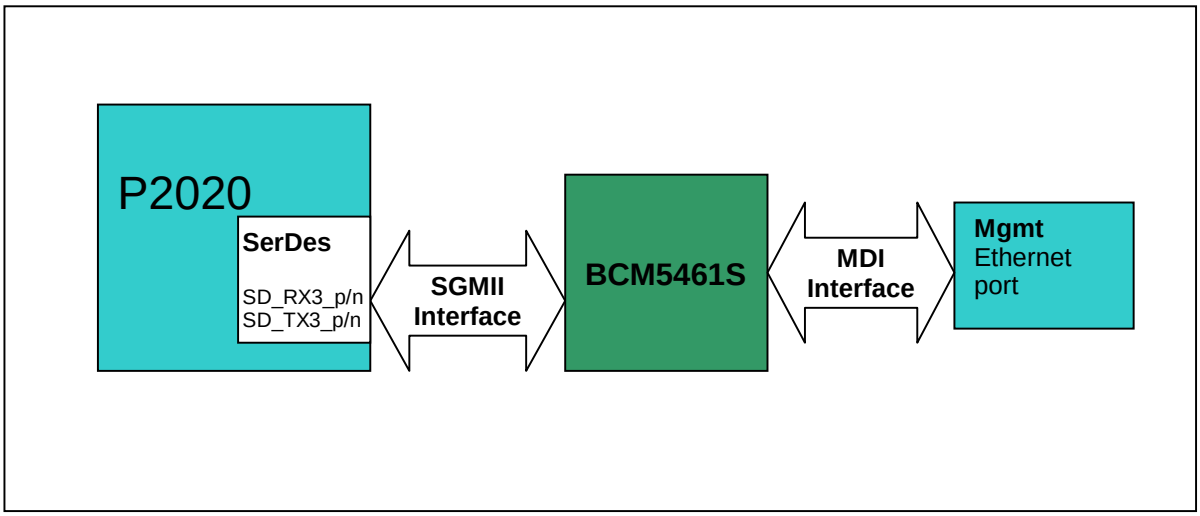


Figure 18: Block Diagram of Mgmt RJ45

Note:

1. The interface is SGMII interface between P2020 and BCM5461S.
2. The CPU can be access BCM5461S by SMI bus (MDC/MDIO) and the PHY address is 0x0001.

9. SFP+ Port Mapping

9.1. SFP port mapping to BCM56844

U65(MAC) BCM56844					
Warpcore	**Port**	**Lan**	**Swap**	**Port mapping**	**Interface**
Warpcore 5	XE0	XGXS0_Port_0		21	SGMII/KR
	XE1	XGXS0_Port_1		22	SGMII/KR
	XE2	XGXS0_Port_2	RX/NP	23	SGMII/KR
	XE3	XGXS0_Port_3	RX/NP	24	SGMII/KR
Warpcore 6	XE4	XGXS2_Port_0		25	SGMII/KR
	XE5	XGXS2_Port_1	RX/NP	26	SGMII/KR
	XE6	XGXS2_Port_2	RX/NP	27	SGMII/KR
	XE7	XGXS2_Port_3	RX/NP	28	SGMII/KR
Warpcore 2	XE8	XGXS3_Port_0	RX/NP	9	SGMII/KR
	XE9	XGXS3_Port_1	RX/NP	10	SGMII/KR
	XE10	XGXS3_Port_2		11	SGMII/KR
	XE11	XGXS3_Port_3		12	SGMII/KR
Warpcore 3	XE12	XGXS4_Port_1		13	SGMII/KR
	XE13	XGXS4_Port_0		14	SGMII/KR
	XE14	XGXS4_Port_2		15	SGMII/KR
	XE15	XGXS4_Port_3	RX/NP	16	SGMII/KR
Warpcore 4	XE16	XGXS5_Port_1		17	SGMII/KR
	XE17	XGXS5_Port_0		18	SGMII/KR
	XE18	XGXS5_Port_2	RX/NP	19	SGMII/KR
	XE19	XGXS5_Port_3		20	SGMII/KR
Warpcore 7	XE20	XGXS6_Port_1	RX/NP	29	SGMII/KR
	XE21	XGXS6_Port_0		30	SGMII/KR
	XE22	XGXS6_Port_2		31	SGMII/KR
	XE23	XGXS6_Port_3	RX/NP	32	SGMII/KR
Warpcore 10	XE24	XGXS7_Port_0		41	SGMII/KR
	XE25	XGXS7_Port_1	RX/NP	42	SGMII/KR
	XE26	XGXS7_Port_2		43	SGMII/KR
	XE27	XGXS7_Port_3	RX/NP	44	SGMII/KR

Warpcore 14	XE28	XGXS8_Port_0	RX/NP	57	SGMII/KR
	XE29	XGXS8_Port_1		58	SGMII/KR
	XE30	XGXS8_Port_2		59	SGMII/KR
	XE31	XGXS8_Port_3		60	SGMII/KR
Warpcore 15	XE32	XGXS9_Port_0		61	SGMII/KR
	XE33	XGXS9_Port_1		62	SGMII/KR
	XE34	XGXS9_Port_2	RX/NP	63	SGMII/KR
	XE35	XGXS9_Port_3		64	SGMII/KR
Warpcore 16	XE36	XGXS10_Port_3	TX/NP	65	SGMII/KR
	XE37	XGXS10_Port_1		66	SGMII/KR
	XE38	XGXS10_Port_0	RX/NP	67	SGMII/KR
	XE39	XGXS10_Port_2	RX/NP	68	SGMII/KR
Warpcore 11	XE40	XGXS11_Port_0	RX/NP	45	SGMII/KR
	XE41	XGXS11_Port_1		46	SGMII/KR
	XE42	XGXS11_Port_2		47	SGMII/KR
	XE43	XGXS11_Port_3	RX/NP	48	SGMII/KR
Warpcore 12	XE44	XGXS12_Port_0		49	SGMII/KR
	XE45	XGXS12_Port_1		50	SGMII/KR
	XE46	XGXS12_Port_3		51	SGMII/KR
	XE47	XGXS12_Port_2	RX/NP	52	SGMII/KR
Warpcore 0	NC			1	
				2	
				3	
				4	
Warpcore 1	NC			5	
				6	
				7	
				8	
Warpcore 8	NC			33	
				34	
				35	

				36	
Warpcore 9	NC			37	
				38	
				39	
				40	
Warpcore 13	NC			53	
				54	
				55	
				56	
Warpcore 17	NC			69	
				70	
				71	
				72	

10. LED Subsystem

10.1. LED Definition for System

System LEDs indications including System, RPS, and FAN Status

Feature	Detailed Description	Comment
System LED	**Off –** No Power **Blinking Green –** Booting, or System in Diagnostic mode **Solid Green –** Normal operation **Solid Red –** Critical Alarm **Blinking Red –** Non-critical alarm	At front side
Power 1 LED	**Solid Green** – Power Supplier 1 is supplied to the switch & operating normally **Solid Yellow** – POST in progress. **Blinking Yellow** – Power Supplier 1 is failed. **Off** – Power is Disconnected.	At front side
Power 2 LED	**Solid Green** – Power Supplier 2 is supplied to the switch & operating normally **Solid Yellow** – POST in progress. **Blinking Yellow** – Power Supplier 2 is failed. **Off** – Power is Disconnected.	At front side
FAN Status LED	**Green** – FAN operating normally. **Yellow** – A FAN is failed.	At front side
Management port (RJ-45) Two LEDs /port	**Link LED: (on the left side)** **Off** – No link is established on the port. **Solid Yellow** - A valid link at 10/100Mbps is established on the port. **Solid Green** – A valid link at 1000Mbps is established on the port. **Act LED: (on the right side)** **Off** – No link is established on the port. **Blinking green** – Activity, transmitting or receiving packet at this port.	

Note: The system temperature threshold is 75 centigrade when one of thermal sensors over temperature. And the TEMP LED will be lighted up to Amber.

10.2. SFP+ Port LEDs

Feature	Detailed Description	Comment
10G SFP+ slot *One LED per port*	**OFF** – No link is established on the port. **Solid Green** – A valid link is established on the port. **Blinking Green** – Packets transmission or reception is occurring on the port	

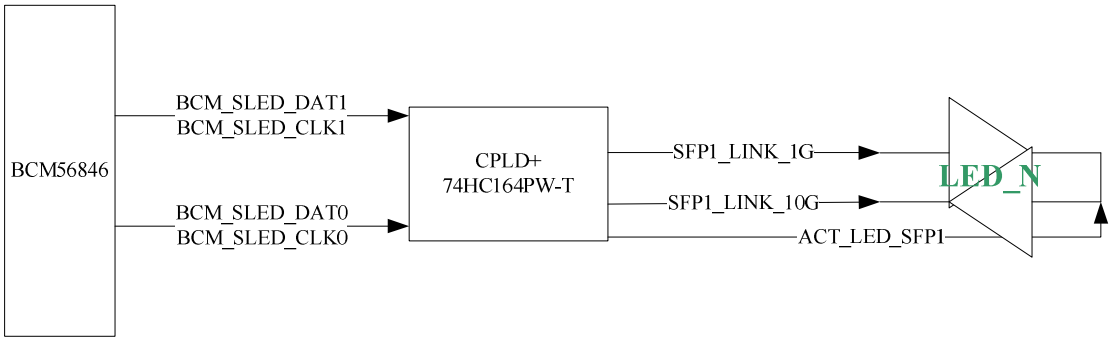
10.3. Fiber port LED programming

The Fiber port LEDs was decoding by BCM56844 LED interface for SFP+ ports. There are define Speed Speed 10G, Speed 1G and Link/Activity LED signals from BCM56844 LED shift out

BCM56844 provides two series LED interface for CPLD indicate.

BCM_SLED_DATA0/ CLK0: It is used to display port [35:0] status.

BCM_SLED_DATA1/ CLK1: It is used to display port [71:36] status.



LED

A two-wire (clock and data) LED interface is provided to control system LEDs. Both LED_CLK and LED_DATA are outputs. When active, LED_CLK is a 5 MHz clock. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED_DATA bits. The LED_DATA signal is pulsed high at the start of each LED refresh cycle. The LED refresh cycle is repeated approximately every 30 ms to refresh the LEDs. The timing diagrams are shown in Figure 6 and Figure 7.

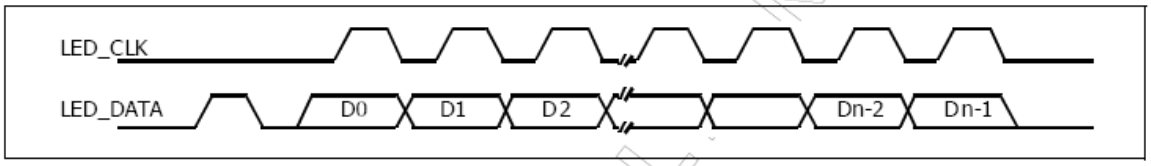


Figure 6: Single LED Refresh Cycle

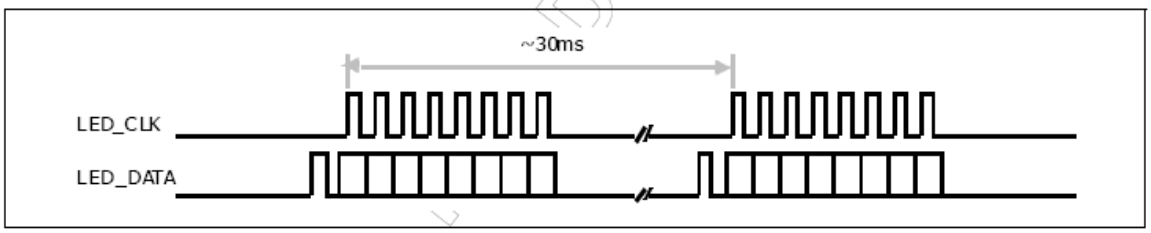


Figure 7: LED Refresh Timing

74HC164PW-T :

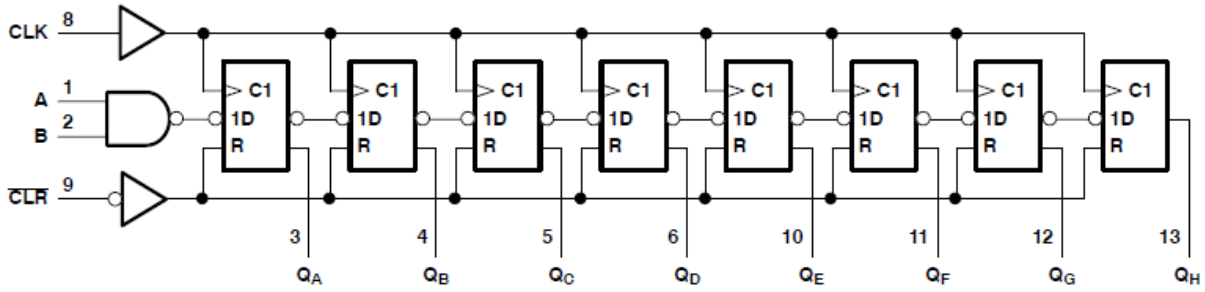
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	$Q_B \ldots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established

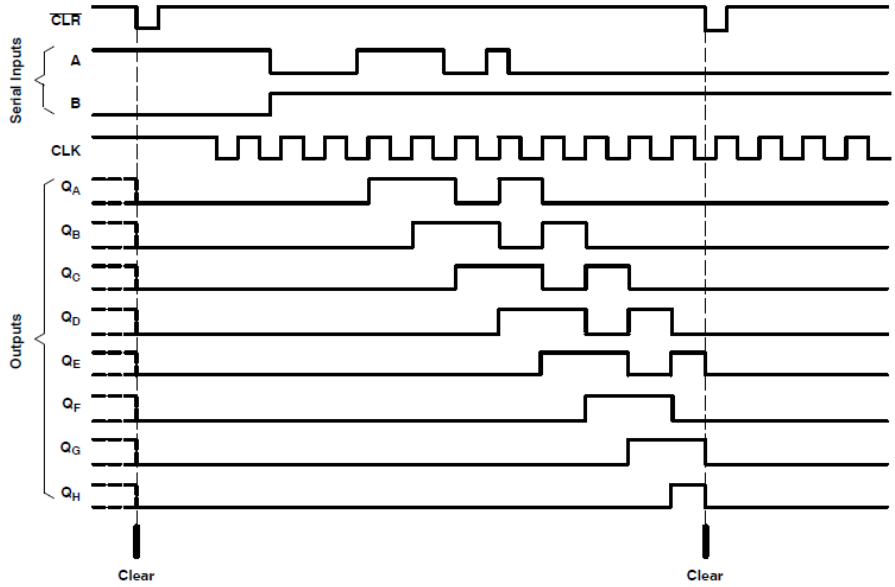
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of CLK: indicates a 1-bit shift

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

typical clear, shift, and clear sequence



LED Prossess		LED Prossess	
Port	**LED0 (D0~D47) 1G/10G link**	Port	**LED1 (D0~D47) 1G/10G link**
XE0	D0/ 1G link	XE24	D0/ 1G link
	D1/ 10G link		D1/ 10G link
XE1	D2/ 1G link	XE25	D2/ 1G link
	D3/ 10G link		D3/ 10G link
XE2	D4/ 1G link	XE26	D4/ 1G link
	D5/ 10G link		D5/ 10G link
XE3	D6/ 1G link	XE27	D6/ 1G link
	D7/ 10G link		D7/ 10G link
XE4	D8/ 1G link	XE28	D8/ 1G link
	D9/ 10G link		D9/ 10G link

XE5	D10/ 1G link	XE29	D10/ 1G link
	D11/ 10G link		D11/ 10G link
XE6	D12/ 1G link	XE30	D12/ 1G link
	D13/ 10G link		D13/ 10G link
XE7	D14/ 1G link	XE31	D14/ 1G link
	D15/ 10G link		D15/ 10G link
XE8	D16/ 1G link	XE32	D16/ 1G link
	D17/ 10G link		D17/ 10G link
XE9	D18/ 1G link	XE33	D18/ 1G link
	D19/ 10G link		D19/ 10G link
XE10	D20/ 1G link	XE34	D20/ 1G link
	D21/ 10G link		D21/ 10G link
XE11	D22/ 1G link	XE35	D22/ 1G link
	D23/ 10G link		D23/ 10G link
XE12	D24/ 1G link	XE36	D24/ 1G link
	D25/ 10G link		D25/ 10G link
XE13	D26/ 1G link	XE37	D26/ 1G link
	D27/ 10G link		D27/ 10G link
XE14	D28/ 1G link	XE38	D28/ 1G link
	D29/ 10G link		D29/ 10G link
XE15	D30/ 1G link	XE39	D30/ 1G link
	D31/ 10G link		D31/ 10G link
XE16	D32/ 1G link	XE40	D32/ 1G link
	D33/ 10G link		D33/ 10G link
XE17	D34/ 1G link	XE41	D34/ 1G link
	D35/ 10G link		D35/ 10G link
XE18	D36/ 1G link	XE42	D36/ 1G link
	D37/ 10G link		D37/ 10G link
XE19	D38/ 1G link	XE43	D38/ 1G link
	D39/ 10G link		D39/ 10G link
XE20	D40/ 1G link	XE44	D40/ 1G link
	D41/ 10G link		D41/ 10G link
XE21	D42/ 1G link	XE45	D42/ 1G link
	D43/ 10G link		D43/ 10G link
XE22	D44/ 1G link	XE46	D44/ 1G link
	D45/ 10G link		D45/ 10G link
XE23	D46/ 1G link	XE47	D46/ 1G link

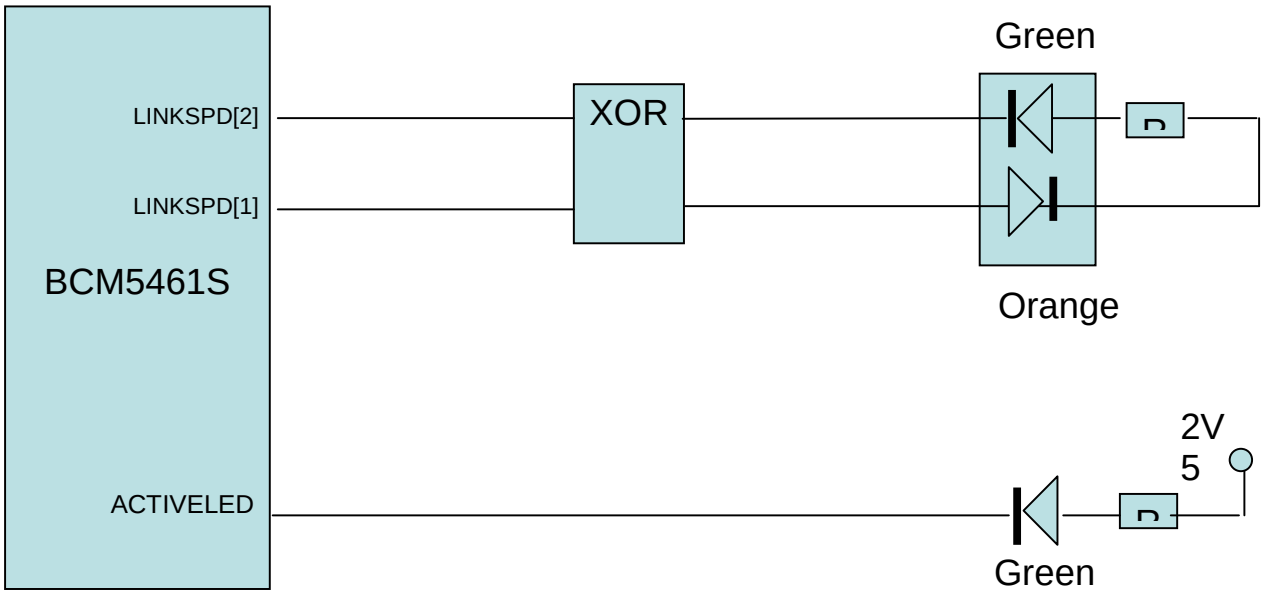
	D47/ 10G link		D47/ 10G link

10.4. PSU (DPS460KBB)

Feature	Detailed Description	Comment
AC LED	Solid green – AC input OK. OFF– NO AC input.	

10.5. Mgmt RJ45 port LED programming

LEDs of the RJ45 port on OOB were controlled by BCM5461s. LINKSPD[2/1] are link status of LED indicated. There are define speed of 1000M is Green, and 100M/10M Speed is Orange.



Speed of Link status	LINKSPD[2]	LINKSPD[1]	
1000M	0	0	Green
100M	0	1	Orange

10M	1	0	Orange
Off	1	1	Off

LINKSPD[1]/INTF_SEL[0] AND LINKSPD[2]/I²C_DISABLE

This pin has a dual input configuration/LED output function, which is described in "Dual Input Configuration/LED Output Function" on page 50. This is a general purpose LED. See "General Purpose LED Programmability" on page 51 for additional programmability. By default, the LED is configured by the hardware pin strappings shown in Table : "Overview," on page 1.

Copper or SGMII Mode

The LINKSPD[1]/INTF_SEL[0] and LINKSPD[2]/I²C_DISABLE LEDs indicate the link and speed status of the copper interface as shown in Table 17.

Table 17: LINKSPD[2:1] LED Function

LINKSPD[2]/I²C_DISABLE	*LINKSPD[1]/INTF_SEL[0]*	*Link/Speed*
0	0	Linked @ 1000BASE-T
0	1	Linked @ 100BASE-TX
1	0	Linked @ 10BASE-T
1	1	No link

ACTIVITYLED

This is a general purpose LED. See "General Purpose LED Programmability" on page 51 for additional programmability. By default, the LED is configured by the hardware pin strappings shown in Table 1: "Hardware Mode Selection," on page 3.

Copper or SGMII Mode

The Activity LED blinks whenever the device is receiving or transmitting packets on the copper interface. The LED is clocked at 167 ms and blinks with 50% duty cycle if activity occurs. This LED mode is active when register 1Ch, shadow 01001, bit 3 = 1.

10.6. System LED definition

POWER_LED1	H1	output	LED indicate	
POWER_LED2	H2	output	LED indicate	

11. Clock Subsystem

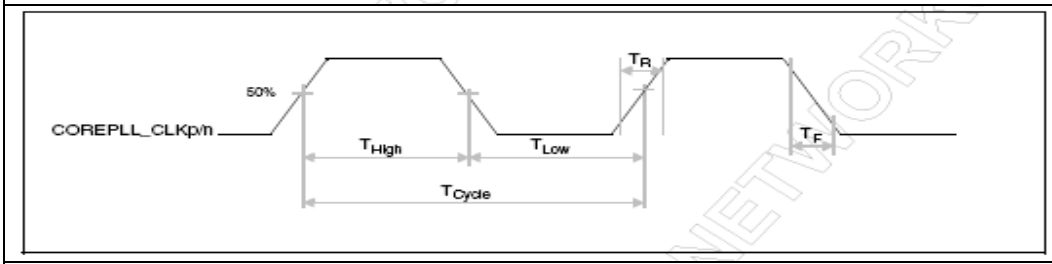
11.1. Clocks

Describe requirements

BCM56844

Core clock input

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Frequency	C_{freq}	–	25	–	MHz
Tolerance	–	-50	–	+50	ppm
Duty cycle distortion	–	40	–	60	%
Rise/fall time (20%–80%)	T_r/T_f	–	–	1	ns
RMS jitter (0–400 KHz)	–	–	–	2.0	ps-rms
Input voltage range	V_{IN}	0.5	–	1.5	Vp-p

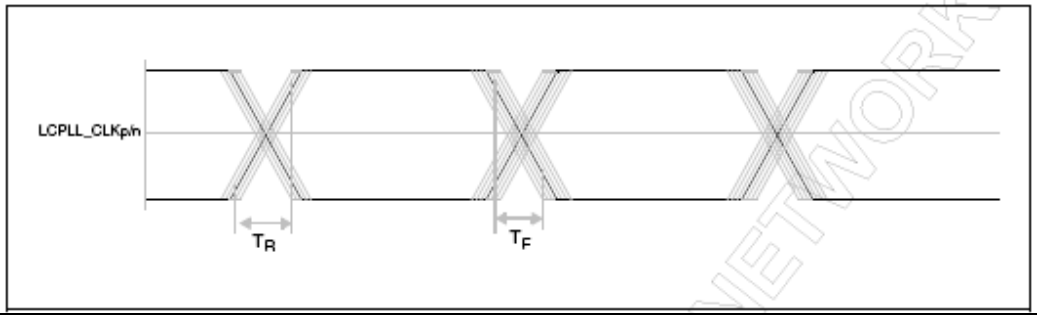


Clock source: 25Mhz_oscillator + Clock buffer

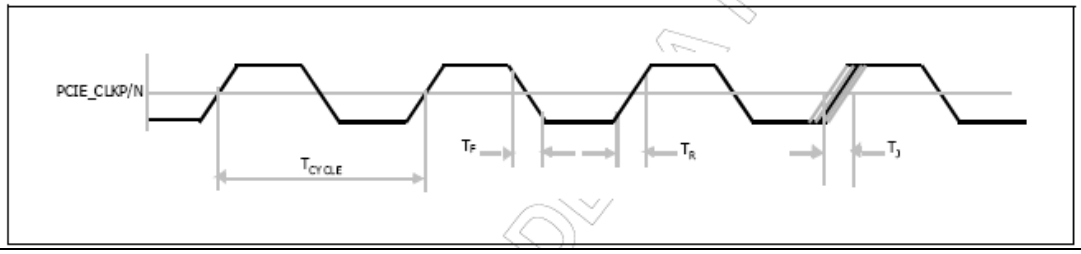
LCPLL clock input

Table 15: LCPLL_REFCLK Clock Input Timing

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Frequency (25 MHz)	C_{freq}	–	25	–	MHz
Frequency (156.25 MHz)	C_{freq}	–	156.25	–	MHz
Frequency Deviation	PPM	–50	–	+50	PPM
Duty Cycle	T_h/T_l	40	–	60	%
RMS Jitter maximum (10 kHz to 1 MHz)	–	–	–	0.3	ps-rms
Rise/Fall time (20% to 80%)	T_r/T_f	–	–	1	ns
Input Voltage Range	V_{IN}	600	–	2000	mVppd



Parameters	Symbol	Min	Typ	Max	Unit
Frequency	C_{freq}	–	100	–	MHz
Frequency Deviation	PPM	–300	–	+300	PPM
Duty Cycle	T_h/T_l	40	50	60	%
Cycle-to-Cycle Jitter	–	–	–	150	ps
Rise/Fall time (20% to 80%)	T_r/T_f	–	–	0.5	ns
Input Voltage Range	V_{IN}	500	–	1150	mVpp



Clock source:

25MHz_oscillator + Differential Clock buffer

156.25MHz_oscillator + Differential Clock buffer

100MHz_oscillator + Differential Clock buffer

P2020

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	—
SYSCLK jitter	—	—	—	±150	ps	3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. This represents the total input jitter—short- and long-term.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

Clock source: 66Mhz/100MHz/100MHz diff oscillator

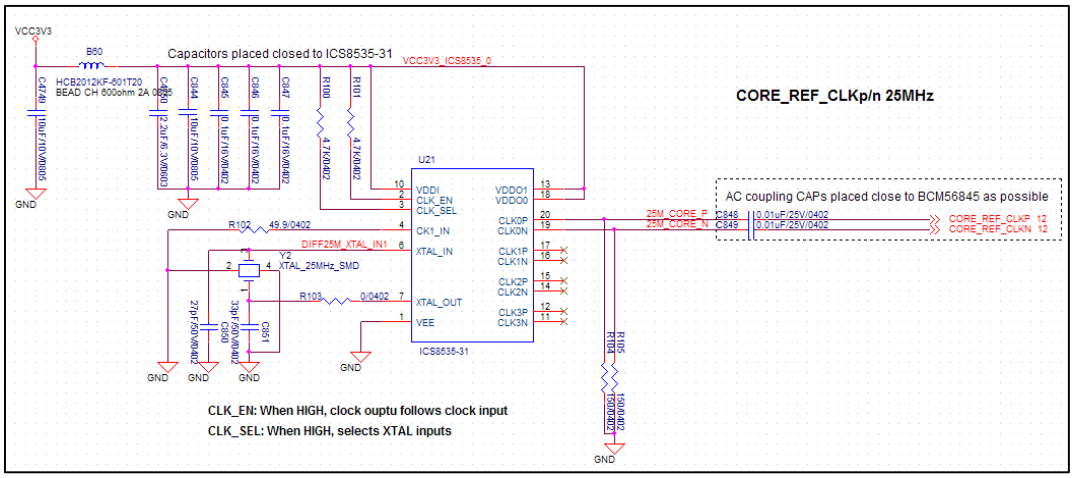
Power Supply: 3.3V

Notable components selections

25MHz Differential Clock for BCM56844

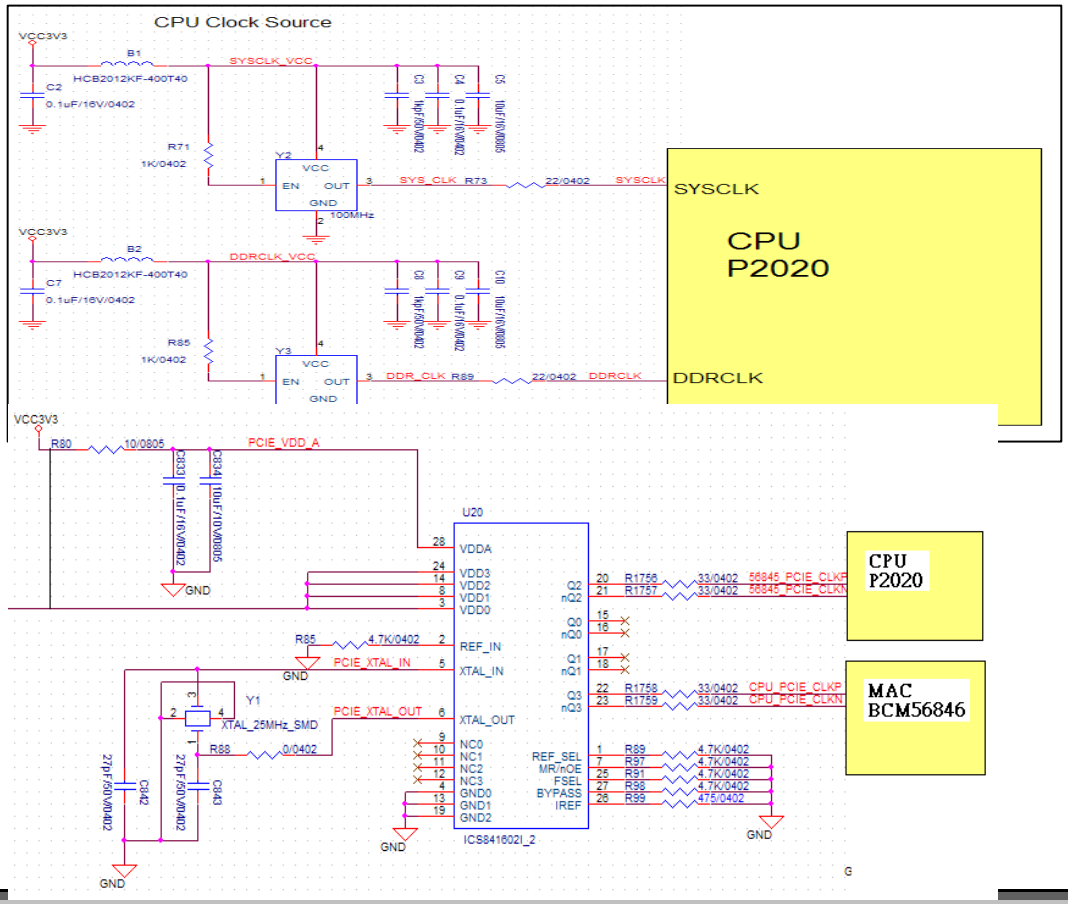
- Core PLL reference clock
  Provided by OSC_25Mhz with an ICS8535-31 clock buffers output.

- LCPLL reference clock
  Provided by OSC_25Mhz with an ICS8535-31 clock buffers output.



66MHz/100MHz Clock for P2020

- CPU P2020 SYSCLK: One external OSC_100Mhz for P2020
  OSC 100MHz 50PPM 15pF 3.3+/-10%V SMD-4P4P SMD
- CPU P2020 DDRCLK: One external OSC_66Mhz for P2020
  OSC 66MHz 50PPM 15pF 3.3V SMD-4P 4P SMD



100MHz Clock for P2020 and BCM56844

- CPU P2020 PCIe: Provided by OSC_25Mhz with an ICS841602I clock buffers output
- BCM56844_PCIe_clock: Provided by OSC_25Mhz with an ICS841602I clock buffers output

12. Reset Subsystem

12.1. Reset Overview:

- Global reset signal is comprised of several occurrences. The signal is activated if at least one of the following conditions occurs:
- The reset push button was pressed (On board for debug).
- Watchdog timer was expired.
- Power failure detected by CPLD, refer to PG signal of DC/DC convert
- Software-reset signals will be generated by the CPLD (Please refer to CPLD register section).
- Software-reset signals are:
  - Reset to Main_CPLD
  - Reset to CPU P2020
  - Reset to BCM56844
  - Reset to BCM5461s
- The Reset Control IC ：When power applied to system, Reset Control IC will generate reset signal with 200ms to 300ms periods.
- System CPLD monitor the PWM 3.3V power good signal PG_3.3V and reset all peripherals until the power good signal PG_3.3V active.

12.2. RESET FUNCTION BLOCK DIAGRAM

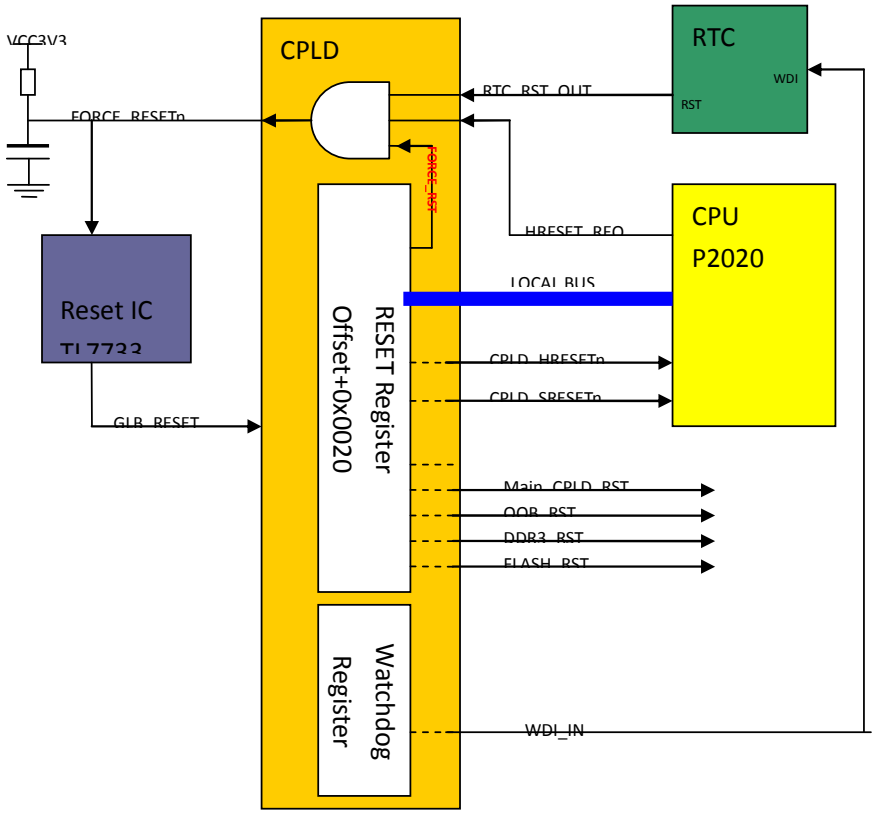
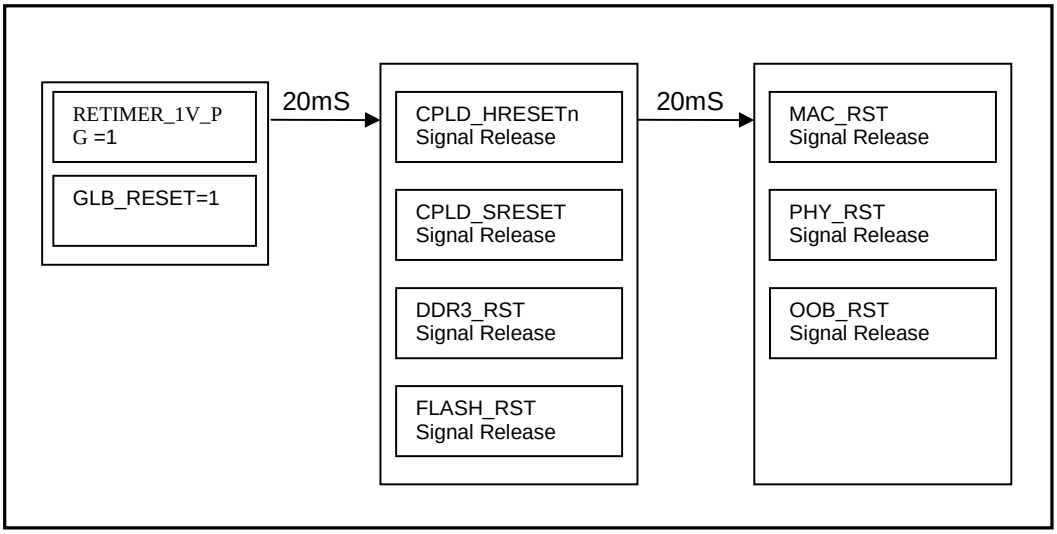


Figure 19: Reset blockdiagram

12.3. Power up reset sequence



Default states

Please refer to Software Reset Register (Base: LCS3#, Offset: 0x0020) – Read/Write

13. Power Subsystem

13.1. Power Tree

Describe distribution tree

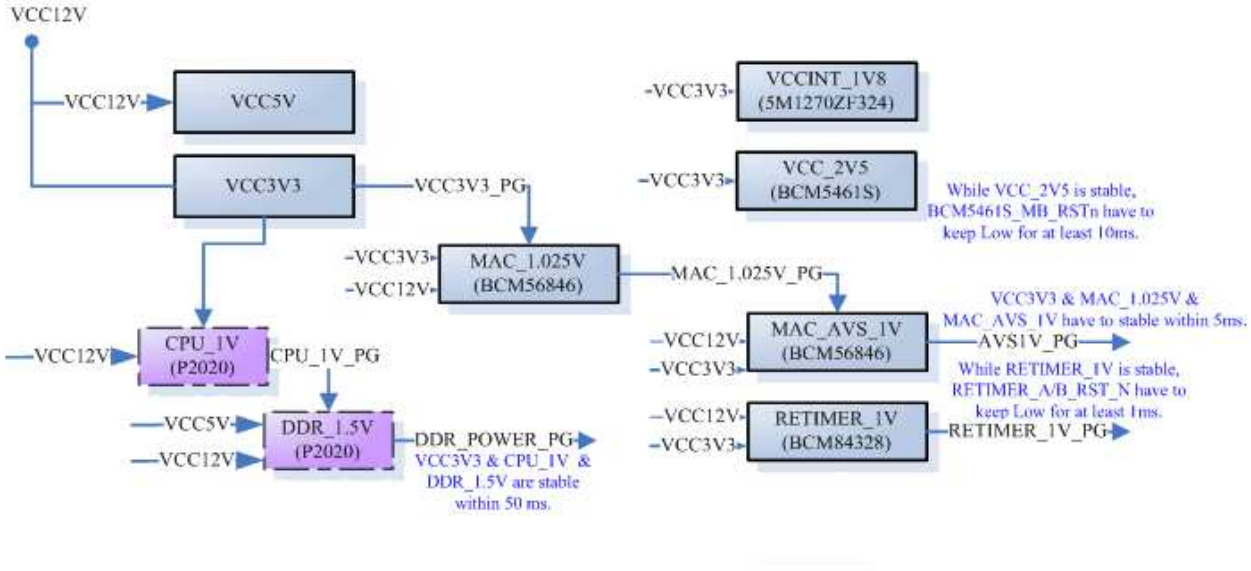


Figure 20: Power Tree

13.2. Sequencing, PowerGood logic

The CPLD program control the power sequence as VCC3V3=> VCCINT_1V8 => MAC_1.025V => MAC_AVS_1V =>CPU 1V=> DDR 1.5V/ VTT 0.75V=> RETIMER_1V=> VCC_2V5 as below diagram. The delay timing needs to meet the P2020 and BCM56844 spec as Power Sequence Requirement table. After the PHY 1V power good on that RST sequence has stared.

13.2.1. Power sequence diagram

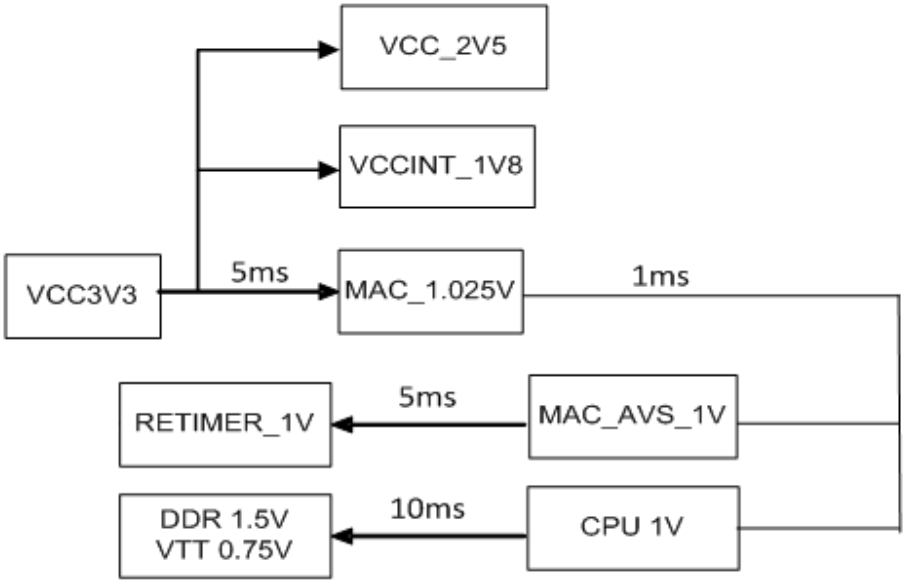


Figure 21: Power Sequence

13.2.2. Power Sequence Requirement

Main Chip	Power Sequence Requirement
P2020	The P2020 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up: 1. VDD, AVDD, BVDD, LVDD, CVDD, OVDD, SVDD_SRDS, and XVDD_SRDS 2. GVDD All supplies must be at their stable values within 50 ms.
BCM56844	1. All the power supplies **must** ramp up from 0V to their full voltages within 5 ms. 2. In addition, they **must** sequence from the highest supply (3.3V) to the lowest supply (1.0V). The 1.0V supply **must never** be at a level that is more than 0.2V higher than the 3.3V supply during ramp up.

13.2.3. VR component selections

Input Voltage	Output Voltage	Current	Component
12V	VCC5V	0.5A	MC7805BD2TR4G

12V	VCC3V3	33A	TPS40422_QFN
12V	MAC_1.025V	20A	ST L6718
12V	CPU_1V	8A	DNK12S0A0R30NFA
12V	MACAVS_1V	47A	ST L6718
12V	DDR_1.5V	3.12A	FAN2110EMPX
1.5V	DDR_VTT	0.6A	APL5336KAI
12V	RETIMER_1V	6.11A	NB6381DL
3V3	VCC_2V5	0.06A	MIC37152BR/1.5A

Table 6: Voltage Regulator list

13.3. Power Consumption table

FS-1048D (P2020 + Main + FAN)																
Device	Qty	Current per each Voltage Rate							Total per each voltage rail							Subtotal
		1.8V	Retimer 1V	AVS 1V	MAC 1V	2.5V	3.3V	12V	1.8	1	1	1	2.5	3.3	12	
CPU Board P2020	1						2,253	1,269	0		0	0	0	2,253	1,269	22.66
BCM56846	1			45,021	23,220		212		0		45,021	23,220	0	212	0	68.94
BCM84328	2		4,225				45		0	8,450	0	0	0	90	0	8.75
MAX V 5M1270ZF324	1	51					103		51		0	0	0	103	0	0.43
SFP+(1.5W)	48						455		0		0	0	0	21,840	0	72.07
QSFP+(1.5W/2W/2.5W/3.5W)	4						1,060		0		0	0	0	4,240	0	13.99
BCM5461S	1			310		240	4		0		310	0	240	4	0	0.92
LED	104						6		0		0	0	0	624	0	2.06
FAN (FFB03612EHN-9T13)	4							630	0		0	0	0	0	2,520	30.24
Other(ICs, OSCs,...)	1						400		0		0	0	0	400	0	1.32
Load Total Current per Voltage [A]:									0.05	8.45	45.33	23.22	0.24	29.77	3.79	
Load Power Dissipation per Voltage [W]:									0.09	8.45	45.33	23.22	0.60	98.23	45.47	221.39
DCDC Loss									0.02	1.49	8.00	4.10	0.11	17.33		39.07
PWM Input [W]									0.11	9.94	53.33	27.32	0.71	115.56	53.49	260.46
Total power comsuption (include efficiency of PWM) [W]:									260.46							

Table 7: Power consumption

13.4. HOTSWAP

The KUGA7048N system has two Hot-Swap controls IC LTC4215IUFD for PSU inserted or removed protection. It still has monitor board supply voltage and inrush current are ramped up at an adjustable rate. Also it can monitor current and power management. It support I2C bus and interrupt function. The detail control setting please refer to *chapter 4.2.2 CPU GPIO definition* and *chapter 4.4.4 I2C*. ***About the*** Current Monitoring of Power Management function please refer to *Chapter 5.9 Hot Swap Current Monitoring of Power Management*

13.4.1. LTC4215IUFD

Hot Swap 0: I2C ADDRESS: 0X84

Hot Swap 1: I2C ADDRESS: 0X80

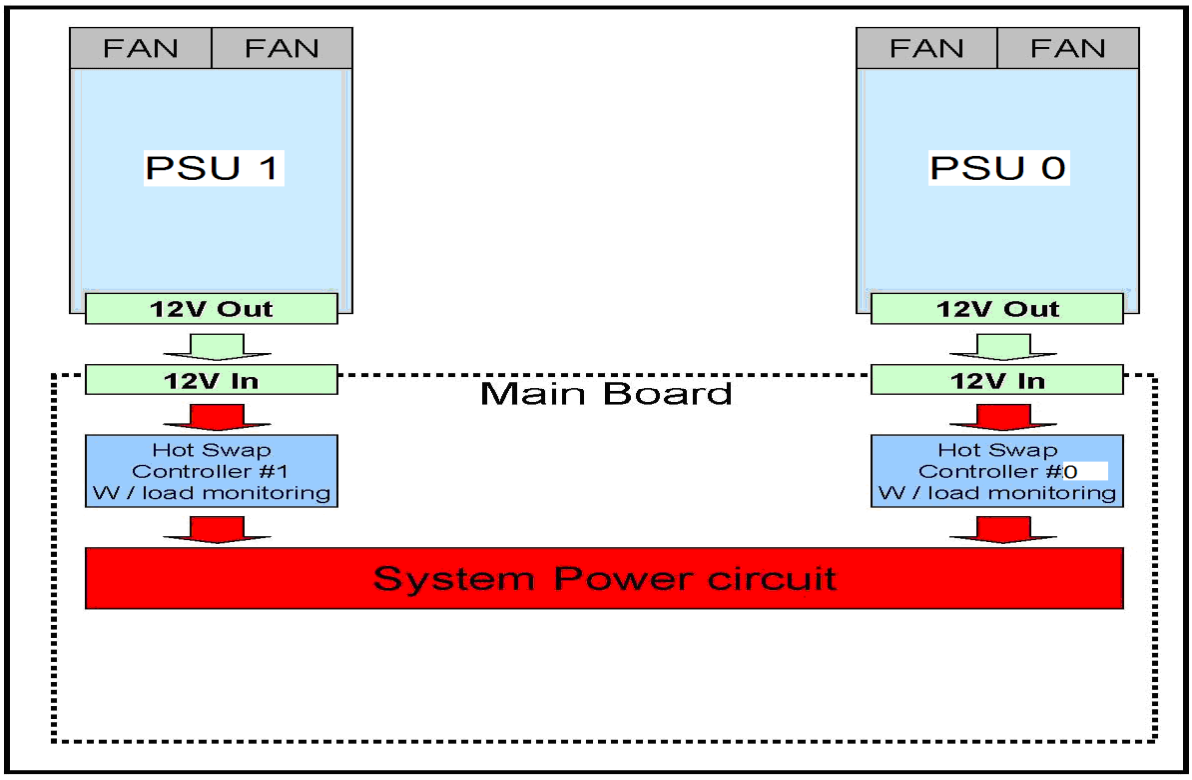


Figure 22: Blockdiagram of Hot Swap

13.4.2. Current Monitoring

The LTC4215 incorporates an 8-bit A/D converter that continuously monitors three different voltages. The SOURCE pin has a 1/12.5 resistive divider to monitor a full scale voltage of 15.4V with 60mV resolution. The ADIN pin is monitored with a 1.235V full scale and 4.82mV resolution, and the voltage between the VDD and SENSE pins is monitored with a 38.45mV full scale and 151μ V resolution. Results from each conversion are stored in registers E (Sense), F (Source) and G (ADIN), as seen in Tables 6, and are updated 10 times per second. It can calculate the current to get the power consumption.

For Example:

When we get the voltage value from 'SENSE Register E (04h)' of LTC4215, if V= 151uV.

We could divide Rsense value, R = 1mohm. The current should be, **I=V/R**=151u (V)/1m (ohm) =0.151A

Power consumption will be, **P=VI**=12V*0.151A=1.812W.

Table 6. SENSE Register E (04h)—Read/Write

BIT	NAME	OPERATION
E7:0	SENSE Voltage Measurement	Sense Voltage Data. 8-Bit Data with 151µV LSB and 38.45mV Full Scale.

14. FAN Control & Thermal Sensor

14.1. FAN Controll, MAX6620

Quad Linear Fan-Speed Controller

MAX6620

nominally 12V or 5V. The drive to the fans is proportional to V_{FAN}. See the *Fan_ Target Drive Voltage Registers* and the *Applications Information* sections for more details.

Fan-Speed Control

DAC (Voltage) Mode. In DAC mode, the MAX6620 simply sets the voltage that powers the fan. The fan's speed is related, but not precisely proportional to, the drive voltage. The drive voltage is set by the Fan_ Target Drive Voltage registers and may be read from the Fan_ Drive Voltage registers. Because the output voltage can ramp to new values at a controlled rate, the values in the two registers may be different. See the *Register Descriptions* and *Applications Information* sections for details.

RPM Mode. In RPM mode, the MAX6620 monitors tachometer output pulses from the fan and adjusts the fan drive voltage to force the fan's speed to the desired value. Fan speed is measured by counting the number of internal 8192Hz clock cycles that take place during a selectable number of tachometer periods. The number of clock cycles counted (11-bit value) is stored in the Fan_ TACH Count registers, and the desired number of cycles is stored in the Fan_ Target TACH Count registers. See the *Register Descriptions* and *Applications Information* sections for details.

Monitoring Tachometer Signals. The TACH_ inputs accept tachometer or "locked-rotor" output signals from 3- or 4-wire fans. When measuring fan speed, the MAX6620 counts the number of internal 8192Hz clock cycles that occur during 1, 2, 4, 8, 16, or 32 tachometer periods. The number of tachometer periods is selectable for each fan by using the appropriate Fan_ Dynamics register. Tachometer pulses <25µs in duration are ignored to minimize the effect of noise on the tachometer lines.

The TACH count for a given RPM can be obtained from the following equation:

$$\text{TACH count} = \frac{60}{NP \times RPM} \times SR \times 8192 = \frac{491520 \times SR}{NP \times RPM}$$

where:

NP = number of tachometer pulses per revolution. Most general-purpose brushless DC fans produce two tachometer pulses per revolution.

SR = 1, 2, 4, 8, 16, or 32. See the Fan_ Speed Range information in the *Fan_ Dynamics Registers (06h, 07h, 08h, 09h)—POR = 0100 1100* section.

The tachometer count consists of 11 bits in the Fan_ TACH Count registers and is available in RPM and DAC modes. In RPM mode, the desired fan count is written to the Fan_ Target TACH Count registers.

Fan Failure Detection

When enabled, the MAX6620 monitors the TACH_ inputs to determine when a fan has failed. For fans with tachometer outputs, failure is detected in various ways depending on the fan control mode. In every case, four consecutive fault detections are required to decide whether the fan has failed. In DAC mode, the Fan_ Target TACH Count registers hold the upper limit for Some fans have locked rotor outputs that produce a logic-level output to indicate that the fan has stopped spinning. These signals can be monitored by setting D2:D1 in the Fan_ Configuration registers. D2 selects locked rotor or tachometer monitoring and D1 selects the polarity of the locked rotor signal. A fan fault has occurred when a locked rotor signal has been present for 1s.

Fan failure is indicated in the Fan Fault register and also with the open-drain $\overline{FAN\_FAIL}$ output. The $\overline{FAN\_FAIL}$ output may be masked using the mask bits in the Fan Fault register. When a fan failure is detected, drive to the affected fan is removed. Drive may be restored by writing a new DAC or fan count target to the fan's control registers. The global configuration regis-

REGISTER SETTING

R/W	REGISTER NO./ADDRESS	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R/W	00h	0000 0XXX	Global Configuration	$\overline{\text{Run}}$: 0 = run 1 = standby	POR: 0 = normal 1 = reset	Bus Timeout (35ms): 0 = enabled 1 = disabled	Fans to 100% on failure: 0 = enabled 1 = disabled	OSC: 0 = internal 1 = XTAL	I^2C Watchdog: 00 = No watchdog 01 = 2s 10 = 6s 11 = 10s		I^2C Watchdog Status (read only): 1 = elapsed
R/W	01h	0000 1111	Fan Fault	Fan 4 Fault	Fan 3 Fault	Fan 2 Fault	Fan 1 Fault	Fan 4 Mask	Fan 3 Mask	Fan 2 Mask	Fan 1 Mask
R/W	02h	0XX0 0000	Fan 1 Configuration	Mode: 0 = DAC 1 = RPM	Spin-Up: 00 = No spin-up 01 = two TACH counts or 0.5s 10 = two TACH counts or 1s 11 = two TACH counts or 2s			TACH input enable	TACH/ Locked Rotor: 0 = TACH 1 = locked rotor	Locked Rotor Polarity: 0 = low 1 = high	
R/W	03h	0XX0 0000	Fan 2 Configuration	Same as Fan 1 Configuration							
R/W	04h	0XX0 0000	Fan 3 Configuration	Same as Fan 1 Configuration							
R/W	05h	0XX0 0000	Fan 4 Configuration	Same as Fan 1 Configuration							
R/W	06h	0100 1100	Fan 1 Dynamics	Speed Range (TACH periods): 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = 32 111 = 32			DAC Rate-of-Change: 000 = 0s per LSB (DAC mode) 0.0625s per LSB (RPM mode) 001 = 0.015625s per LSB 010 = 0.03125s per LSB 011 = 0.0625s per LSB 100 = 0.125s per LSB 101 = 0.25s per LSB 110 = 0.5s per LSB 111 = 1s per LSB				
R/W	07h	0100 1100	Fan 2 Dynamics	Same as Fan 1 Dynamics							
R/W	08h	0100 1100	Fan 3 Dynamics	Same as Fan 1 Dynamics							
R/W	09h	0100 1100	Fan 4 Dynamics	Same as Fan 1 Dynamics							

R/W	REGISTER NO./ADDRESS	POR STATE	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
R	10h	1111 1111	Fan 1 TACH Count	D10	D9	D8	D7	D6	D5	D4	D3
	11h	1110 0000		D2	D1	D0	—	—	—	—	—
R	12h	1111 1111	Fan 2 TACH Count	Same as Fan 1 TACH Count							
	13h	1110 0000									
R	14h	1111 1111	Fan 3 TACH Count	Same as Fan 1 TACH Count							
	15h	1110 0000									
R	16h	1111 1111	Fan 4 TACH Count	Same as Fan 1 TACH Count							
	17h	1110 0000									
R	18h	0000 0000	Fan 1 Drive Voltage	D8	D7	D6	D5	D4	D3	D2	D1
	19h	0000 0000		D0	—	—	—	—	—	—	Full
R	1Ah	0000 0000	Fan 2 Drive Voltage	Same as Fan 1 Drive Voltage							
	1Bh	0000 0000									
R	1Ch	0000 0000	Fan 3 Drive Voltage	Same as Fan 1 Drive Voltage							
	1Dh	0000 0000									
R	1Eh	0000 0000	Fan 4 Drive Voltage	Same as Fan 1 Drive Voltage							
	1Fh	0000 0000									
R/W	20h	0011 1100	Fan 1 Target TACH Count	D10	D9	D8	D7	D6	D5	D4	D3
	21h	0000 0000		D2	D1	D0	—	—	—	—	—
R/W	22h	0011 1100	Fan 2 Target TACH Count	Same as Fan 1 Target TACH Count							
	23h	0000 0000									
R/W	24h	0011 1100	Fan 3 Target TACH Count	Same as Fan 1 Target TACH Count							
	25h	0000 0000									
R/W	26h	0011 1100	Fan 4 Target TACH Count	Same as Fan 1 Target TACH Count							
	27h	0000 0000									
R/W	28h	XXXX XXXX	Fan 1 Target Drive Voltage	D8	D7	D6	D5	D4	D3	D2	D1
	29h	X000 0000		D0	—	—	—	—	—	—	—
R/W	2Ah	XXXX XXXX	Fan 2 Target Drive Voltage	Same as Fan 1 Target Drive Voltage							
	2Bh	X000 0000									
R/W	2Ch	XXXX XXXX	Fan 3 Target Drive Voltage	Same as Fan 1 Target Drive Voltage							
	2Dh	X000 0000									
R/W	2Eh	XXXX XXXX	Fan 4 Target Drive Voltage	Same as Fan 1 Target Drive Voltage							
	2Fh	X000 0000									

X = Depends on input states at power-up.

Fan_ Dynamics Registers (06h, 07h, 08h, 09h)—POR = 0100 1100

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>R/W</td><td rowspan="3">Fan_ Speed Range:
The MAX6620 determines fan speed by counting the number of internal 8192Hz clock cycles (using an 11-bit counter) during one or more fan tachometer periods. Three bits set the nominal RPM range for the fan, as shown in the table below. As an example, a setting of 010 causes the MAX6620 to count the number of 8192Hz clock cycles that occur during four complete tachometer periods. If the fan has a nominal speed of 2000RPM and two tachometer pulses per revolution, one tachometer period will be nominally 15ms, and four tachometer periods will be 60ms. With an 8192Hz clock, the TACH count will therefore be equal to 491. With a fan speed of 1/3 the nominal value, the count will be 1474. If the fan's nominal speed is 1000RPM, the full-speed TACH count will be 983. At 1/3 the nominal speed, there will be 2948 clock cycles in four tachometer periods. This is greater than the maximum 11-bit count of 2047, so four tachometer periods is too many for this fan; a setting of 001 (two clock cycles) is recommended instead.

The table below shows the full-speed tachometer counts for several combinations of nominal fan speeds and D7:D5 settings. The shaded combinations will provide the best results. When setting D7:D5, the goal is to obtain the highest tachometer count without exceeding the maximum count of 2047 when the fan is at the minimum speed of interest. For example, if the minimum speed of interest is 1/3 of full speed, the maximum tachometer count will be three times the value shown in the table below:

Tachometer Counts/(Counting Period) (8192Hz Clock Used):</td></tr>
<tr><td>6</td><td>R/W</td></tr>
<tr><td>5</td><td>R/W</td></tr>
</table>

D7:D5	NUMBER OF TACH PERIODS COUNTED	RPM					
		500	1000	2000	4000	8000	16000
000	1	**491** (60ms)	**245** (30ms)	**122** (15ms)	**61** (7.5ms)	**30** (3.75ms)	**15** (1.875ms)
001	2	**983** (120ms)	**491** (60ms)	**245** (30ms)	**122** (15ms)	**61** (7.5ms)	**30** (3.75ms)
010	4	**1966** (240ms)	**983** (120ms)	**491** (60ms)	**245** (30ms)	**122** (15ms)	**61** (7.5ms
011	8	**2047** (480ms)	**1966** (240ms)	**983** (120ms)	**491** (60ms)	**245** (30ms)	**122** (15ms)
100	18	**2047** (960ms)	**2047** (480ms)	**1966** (240ms)	**983** (120ms	**491** (60ms)	**245** (30ms
101, 110, 111	32	**2047** (1920ms)	**2047** (960ms)	**2047** (480ms)	**1966** (240ms)	**983** (120ms)	**491** (60ms)

Fan_ Dynamics Registers (06h, 07h, 08h, 09h)—POR = 0100 1100 (continued)

<table>
<tr><th>BIT</th><th>R/W</th><th>FUNCTION</th></tr>
<tr><td>4
3
2</td><td>R/W
R/W
R/W</td><td>
Fan_ DAC Rate-of-Change:
The fan drive voltage (at the DACFB_ inputs) varies from 0 to full scale in 512 increments. The rate-of-change bits determine the time interval between output voltage increments/decrements. In RPM mode, a setting of 0 would result in an unstable feedback loop, so a default value of 0.0625 is in effect when 0 is selected.

Regardless of the settings, there are a few cases for which the rate-of-change is always 0:
• When a target TACH count of 2047 (7FF) is selected, the fan drive voltage immediately goes to 0V. A full-scale target count is assumed to mean that the intent is to shut down the fan, and going directly to 0 drive avoids the possibility of loss of control-loop feedback at high TACH counts. If a slow- speed decrease toward 0 is desired, a target TACH count at the slowest practical value for the fan should be chosen. Once that count has been reached, selecting a count of 2047 (7FF) will then take the drive immediately to 0V.
• When a target fan drive voltage of 0V is selected, the drive voltage immediately goes to 0V. Again, it is assumed that the intent is to shut down the fan. If a slow-speed decrease toward 0 is desired, a target fan drive voltage of the slowest practical value for the fan in question should be chosen. Once that drive voltage has been reached, selecting a target value of 0 will then take the drive immediately to 0V.
• When the current drive level is 0 in DAC mode, selecting a new target fan drive voltage will immediately take the voltage to that value. The fan will spin-up first if spin-up is enabled.
• When the current drive level is 0 in RPM mode, selecting a new target TACH count that is less than 2047 (7FF) will immediately take the drive voltage to the value in the Fan_ Target Drive Voltage register. From this value, the drive voltage will increment as needed to achieve the desired TACH count. The fan will spin-up first if spin-up is enabled.
<table>
<tr><th rowspan="2">D4:D2</th><th colspan="2">TIME BETWEEN OUTPUT VOLTAGE INCREMENTS (s)</th><th rowspan="2">TIME FROM 33% TO 100% (s)</th></tr>
<tr><th>DAC MODE</th><th>RPM MODE</th></tr>
<tr><td>000</td><td>0</td><td>0.0625</td><td>0</td></tr>
<tr><td>001</td><td colspan="2">0.015625</td><td>10</td></tr>
<tr><td>010</td><td colspan="2">0.03125</td><td>20</td></tr>
<tr><td>011</td><td colspan="2">0.0625 (default)</td><td>40</td></tr>
<tr><td>100</td><td colspan="2">0.125</td><td>80</td></tr>
<tr><td>101</td><td colspan="2">0.25</td><td>160</td></tr>
<tr><td>110</td><td colspan="2">0.5</td><td>320</td></tr>
<tr><td>111</td><td colspan="2">1.0</td><td>640</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>—</td><td>Reserved</td></tr>
<tr><td>0</td><td>—</td><td>Reserved</td></tr>
</table>

Thermal threshold for Fan speed control table

SYSTEM	FAN Speed	REMARK
IDLE	6000PRM	No Ethernet ports is link or below 25C
Level 1	9000RPM	Temperature range from 31C to 50C
Level 2	11000RPM	Temperature range from 51C to 70C
Level 3	13000RPM	Temperature range from 71C to 80C
Level 4	14500RPM	Temperature range is 81C+

Note:

1) Threshold value will be define later

2) The temperature is read from thermal sensor (TMP75)

3) The Fan controller is MAX6620

4) Max Fan speed is 19000 r.p.m

5) The Fan speed trigger is according most high temperature while CPU read the thermal data form 4 thermal sensors.

14.2. Thermal sensor

P2020 build in thermal function. It needs extra thermal diode in SCH.

TMP421 sensor placement

Placement	Location	I2C address
U19	Close to CPU sensor (on CPU board)	0x92

TMP75 sensor placement

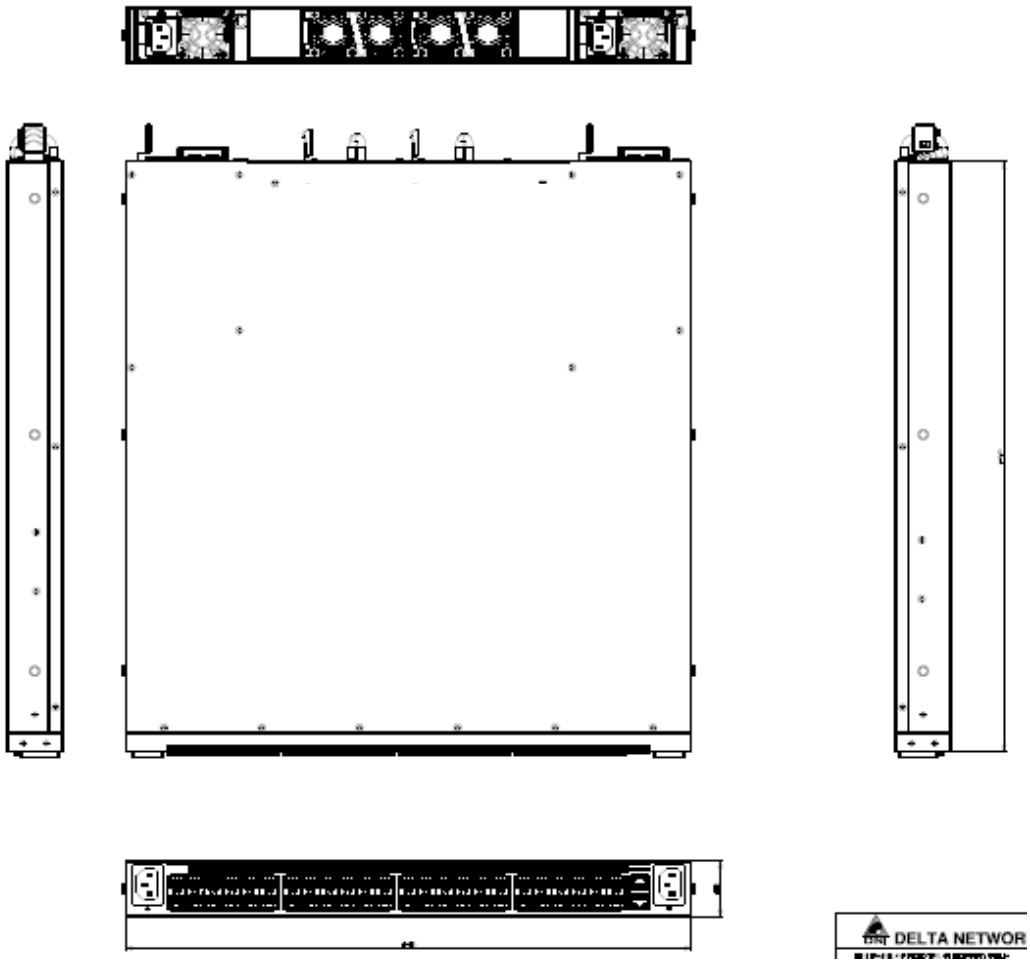
Placement	Location	I2C address
U26	On to Upper side of MAC	0x9A
U15	On to Down side of MAC	0x90

When TMP75 ALERT is assert, Thermal_out will be processed in CPLD and output to GPIO_7 of CPU.

15. Mechanical Subsystem

15.1. Pluggable Power Supply & Fan Tray

Power Supply & Fan Tray allocation



15.2. Pluggable Power Supply

This specification defines a 460W redundant power supply that supports server systems. The parameters of this power supply are defined in this specification. This specification defines a power supply with 2 outputs : 12V and 12VSB. The AC input shall be auto ranging and power factor corrected.

15.2.1. Mechanical defined:

The physical size of the power supply enclosure is 39/40mm x 74mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the following Figure 1. All dimensions are nominal.

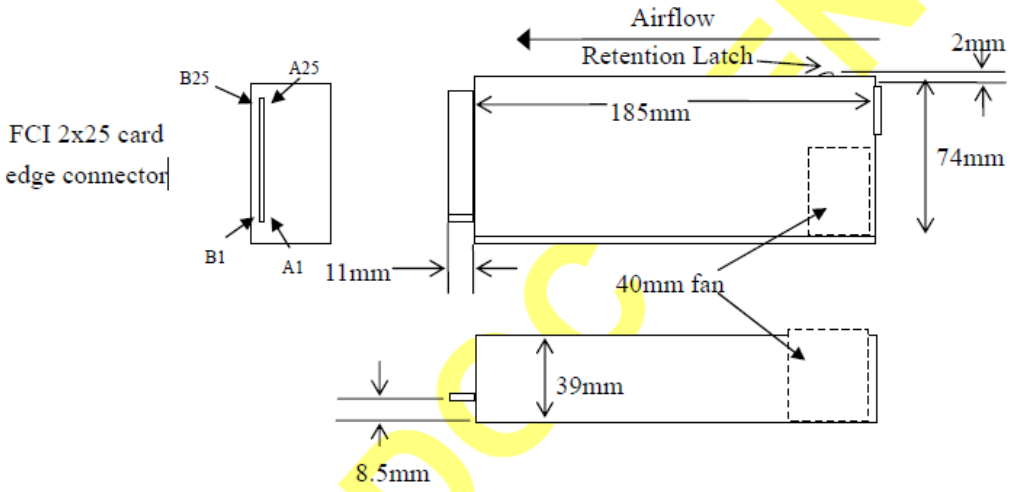


Figure 1 Power Supply Outline Drawing

15.2.2. LED Identification:

Table 1 LED Indicator States

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
AC present / Only 12VSB on (PS off) or PS in Smart on state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GRENN

15.2.3. AC input:

Table 2 AC Input Voltage Range

PARAMETER	MIN	RATED	V_{MAX}	Start up VAC	Power Off VAC
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	85VAC +/-4VAC	70VAC +/-5VAC
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}		
Frequency	47 Hz	50/60	63 Hz		

15.2.4. DC output:

Table 7 Load Ratings

Parameter	Min	Max.	Peak [1,2]	Unit
+12V	0.0	38.0	45.0	A
+12VSB	0.0	2.1		A

15.2.5. Protection Circuits:

- Current Limit (OCP)

Table 13 Over Current Protection

Output VOLTAGE	Input voltage range	OVER CURRENT LIMITS
+12V	90 – 264VAC	47A min; 55A max
12VSB	90 – 264VAC	2.5A min; 3.5A max

- Over Voltage Protection (OVP)

Table 14 over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.3	14.5
+12VSB	13.3	14.5

- Over Temperature Protection)OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4°C of ambient temperature margin.

Note: The power supply maximum output power is 400W when the power supply was protected by OTP function.

15.2.6. Pin Defined

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	N/A
A21	PSON	B21	12VSB
A22	SMBAlert#	B22	Smart_on
A23	Return Sense	B23	12VLS
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	N/A

15.3. Fan Tray with Normal Airflow

Normal Airflow: The Fan Tray ID is ‘ 1’ in CPLD Fan Tray Register (offset+0090), the airflow is from IO to PSU side.